THIS PRODUCT HAS REACHED END OF LIFE

Programmable Long-Delay Push-Button Reset Controller for Consumer Equipment

FEATURES & APPLICATIONS

- **De-Bounced Reset Input with up to 40 Second Programmable Delay Time**
- **External Push-Button Control Provides a Reliable End-User System Reset Function**
- **Reset Signal at 3.0V with a Programmable Timeout Period**
- **Brownout Warning Signal whenever the supply dips below 3.1V**
- **Programmable Glitch Filtering of Brownout Warning (BAD_PWR#) and Reset Function**
- **8 Pin SOIC Package**
- **6 ball *Ultra* CSP™ (Chip-Scale) Package**

Applications

- **Satellite and Cable-TV Set-top box**
- **Handheld PCs, Cameras, Camcorders, PDAs**
- **Security/Medical Alert Systems**

INTRODUCTION

The SMR100 programmable reset controller is designed for consumer applications specified by Satellite-TV set-top box standards. The SMR100 provides a satellite box controller solution during initial setup, changing programming cards and/or system reset needs without removing power. The part can accommodate a long-delay hold down of an external reset push-button using an internal programmable de-bounced timer. The part is factory programmed, however, multiplexed programming pins are also provided for in-system programming for prototype purposes.

The required hold down time is programmable from 0.325 to 40 Sec with an internal on-chip oscillator. Accurate warning of a 3.1V brownout condition (BAD_PWR#), and a programmable reset (RESET_OUT#) timeout period when the VDD supply pin reaches 3.0V are also provided. During a reset (RESET_OUT#), the part enables the "BAD_PWR#" or brownout warning output until the reset has cleared. A programmable glitch filter avoids nuisance tripping of the internal comparators.

SIMPLIFIED APPLICATIONS DRAWING

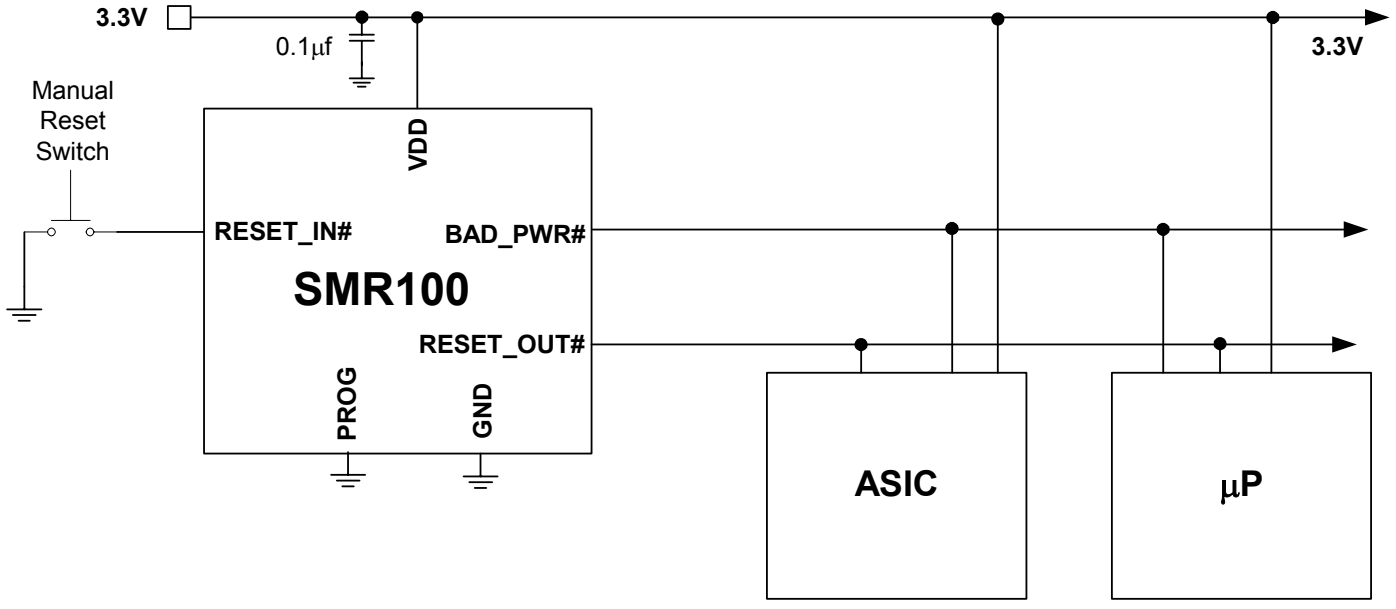


Figure 1 – Applications Schematic using the SMR100 to supervise the supply to digital components. As shown, the SMR100 is designed to use a minimum of external components.

GENERAL DESCRIPTION

The SMR100 is a programmable Reset Controller for Consumer Equipment used to monitor the power supply in µP and digital systems. It provides excellent circuit reliability and low cost by eliminating external components and adjustments when used with +3.3V powered circuits. The device performs several functions: it first asserts a 'bad power' signal and then a reset signal whenever the VDD supply voltage declines below two preset thresholds, keeping it asserted for a programmable time period after VDD has risen above the reset threshold. The part also provides a programmable delay push button input for manual system reset.

The open-drain RESET_OUT# and BAD_PWR# outputs have on-chip 100K pull-up resistors and do not require external pull-up resistors unless more drive current is needed (see figure 3). The RESET_OUT# and BAD_PWR# comparators are designed to ignore fast transients on VDD, and the outputs are guaranteed to be in the correct logic state for VDD down to 1V. Low supply current makes the SMR100 ideal for use in portable equipment. The RESET_IN# input includes a programmable hold-down delay timer for use with a push button switch for consumer equipment such as set-top boxes and PCs.

A microprocessor's (µP's) reset input starts the µP in a known state. The SMR100 asserts a reset to prevent code -execution errors during power-up, power-down, or UnderVoltage (UV) conditions. It asserts a RESET_OUT# signal whenever the VDD supply voltage declines below a 3.0V threshold, keeping it asserted for a programmable period after VDD has risen above the reset threshold. It also asserts a Bad Power signal to warn of an impending reset or brownout condition to allow time for the system to save data before a reset occurs. The BAD_PWR# signal is also asserted whenever RESET_OUT# is asserted to prevent erroneous or false Bad Power warnings during initial turn-on.

In addition to issuing a reset to the µP during power-up, power-down, and brownout conditions, the SMR100 is immune to short-duration VDD transients (glitches) due to a programmable glitch filter. Typically, a VDD transient of 100mV less than the reset threshold and lasting for a duration less than the programmed glitch filter setting will not cause a reset pulse. A 0.1µF bypass capacitor mounted as close as possible to the VDD pin provides additional transient immunity. Since the BAD_PWR# and RESET_OUT# outputs are open drain, the device interfaces easily with µPs that have bidirectional-reset pins. Connecting the RESET_OUT# output directly to the µP's RESET pin allows either the µP or the SMR100 to assert a reset.

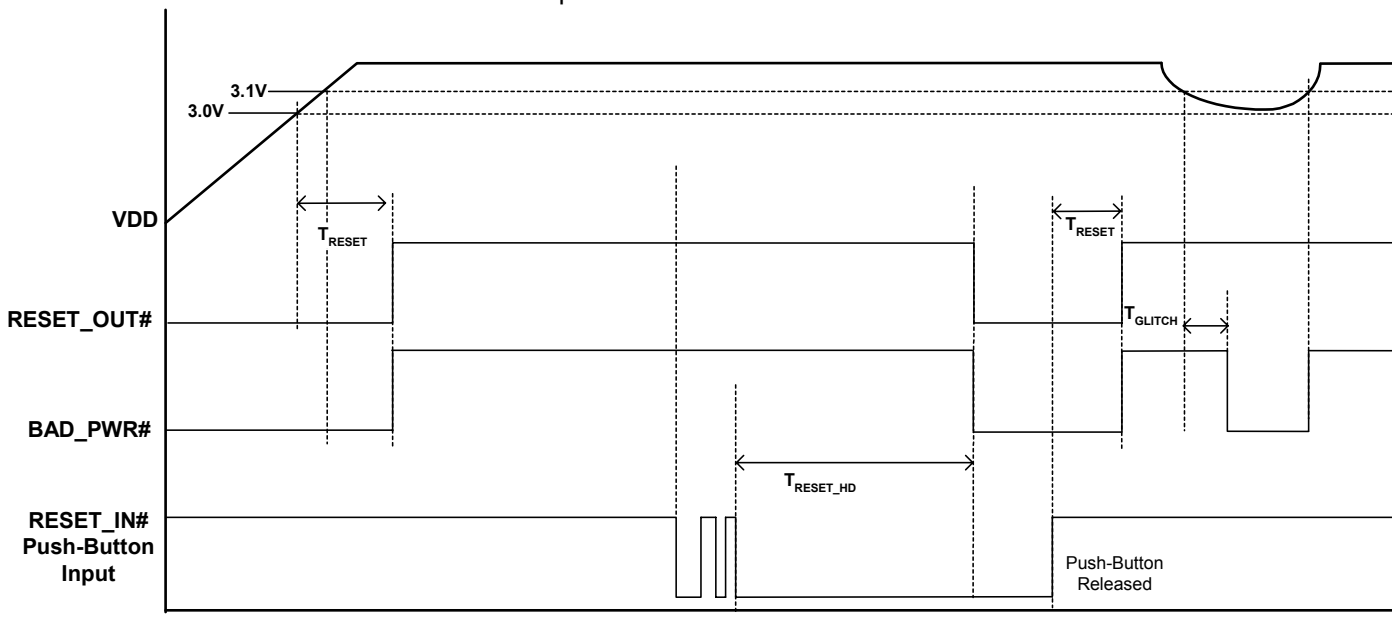


Figure 2 – SMR100 Operation and timing diagram

INTERNAL BLOCK DIAGRAM

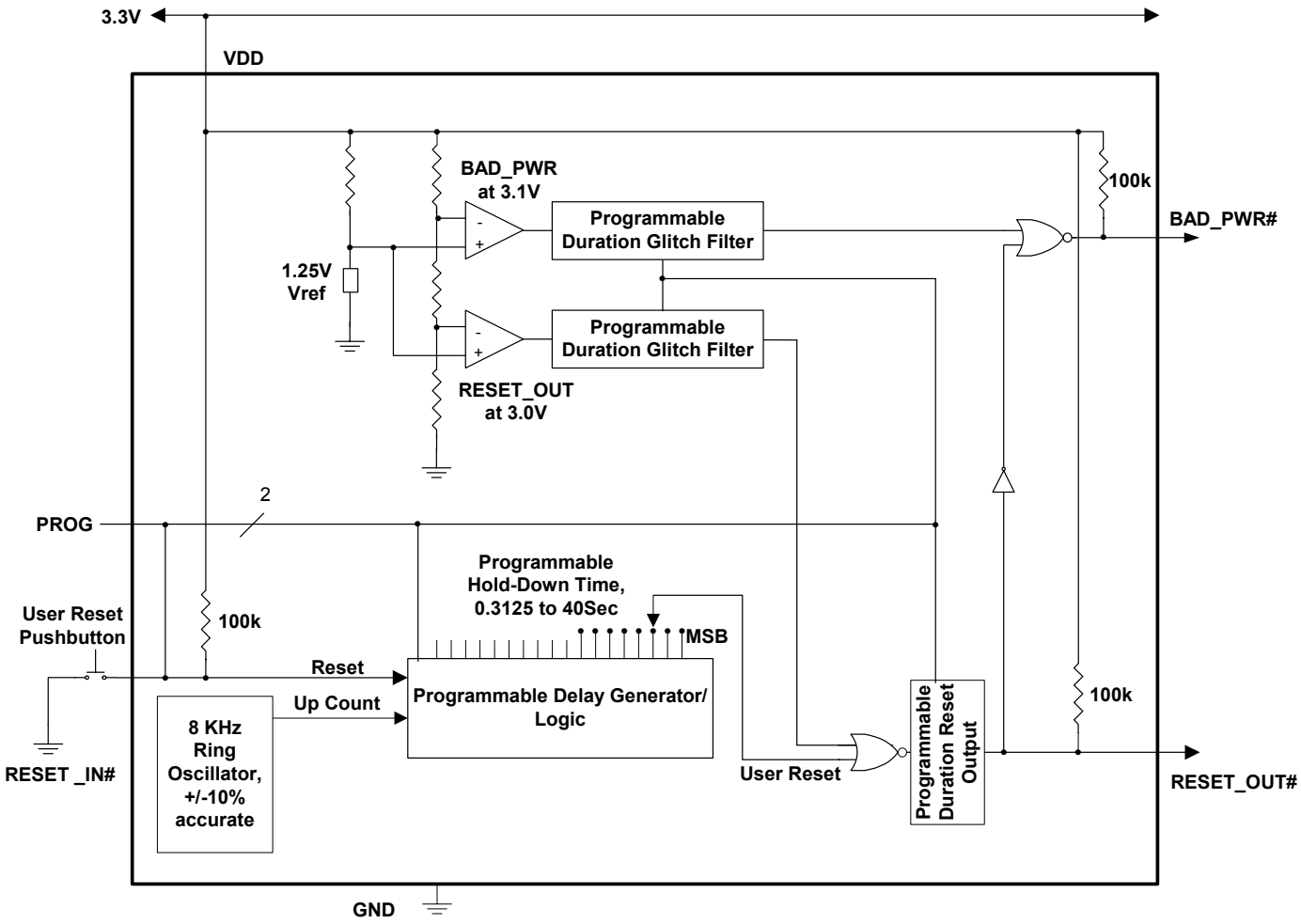
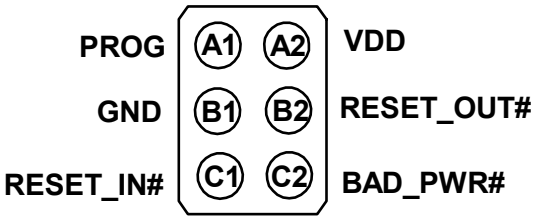


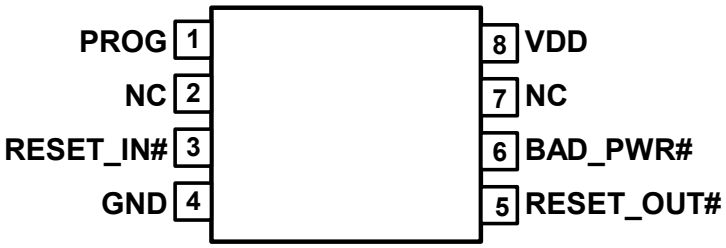
Figure 3 – SMR100 Controller Internal Block Diagram.

PACKAGE AND PIN CONFIGURATION

6 Ball *Ultra* CSP™
Bottom View



8 Pin SOIC
Top View



PIN DESCRIPTIONS

CSP Pin Number	SOIC Pin Number	Pin Type	Pin Name	Pin Description
A1	1	I	**PROG**	High voltage programming pin. Set to 12V in programming mode. Connected to ground if not used.
A2	8	PWR	**VDD**	Positive supply voltage.
B1	4	PWR	**GND**	Ground pin.
B2	5	O	**RESET_OUT#**	Open Drain active low Reset Out indicator. Internally connected to VDD through a 100KΩ resistor.
C1	3	I	**RESET_IN#**	De-bounced push button switch input. Internally connected to VDD through a 100KΩ resistor. Also used as the Data input programming pin when the PROG pin is set to 12V.
C2	6	O	**BAD_PWR#**	Open Drain active low Bad Power indicator. Internally connected to VDD through a 100KΩ resistor.
NA	2,7	NC	**NC**	No Connect

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias .....-55°C to 125°C
Storage Temperature.....-65°C to 125°C
Terminal Voltage with Respect to GND:
V_{DD}……..….-0.3V to 6.0V
PROG, RESET_IN#……..….-0.3V to 16.0V
All Others……..….VDD + 0.7V
Output Short Circuit Current 100mA
Reflow Solder Temperature (30 secs)..... 240°C
ESD Rating per JEDEC……..……..2000V
Latch-Up testing per JEDEC……..…±100mA

Note - The device is not guaranteed to function outside its operating rating. Stresses listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions outside those listed in the operational sections of the specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability. Devices are ESD sensitive. Handling precautions are recommended.

RECOMMENDED OPERATING CONDITIONS

Temperature Range (Commercial)…….–5°C to +70°C
Supply Voltage……..3.3V +/-10%[1]
Programming Supply Voltage……12.0V +/-10%

Note 1 – The device can operate over a supply range of 2.7V to 5.5V.

Package Thermal Resistance (θ_{JA})
8 Pin SOIC……..……23°C/W
6 Ball *Ultra* CSP™……..…TBD°C/W

Moisture Classification Level 1 (MSL 1) per J-STD- 020

RELIABILITY CHARACTERISTICS

Data Retention……..……..100 Years
Endurance……..…….100,000 Cycles

DC OPERATING CHARACTERISTICS

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Parameter	Notes	Min.	Typ.	Max	Unit
V_{DD}	Supply Voltage Range		2.7	3.3	5.5	V
V_{PROG}	Programming Supply Voltage Range		10.0	12.0	15.0	V
V_{RT}	Reset Threshold		2.95	3.0	3.05	V
V_{BPT}	Bad Power Warning Threshold		3.05	3.1	3.15	V
I_{DD}	Power Supply Current	VDD = 3.3V, no RESET_OUT# in progress		100	200	µA
V_{IH}	Input High Voltage	VDD = 3.3V	0.9xVDD		VDD	V
V_{IL}	Input Low Voltage	VDD = 3.3V			0.1xVDD	V
V_{OL}	Programmable Active High or Low Open Drain Outputs (RESET_OUT#, BAD_PWR#)	ISINK = 1mA	0		0.4	V
I_{OL}	Output Low Current		0		1.0	mA

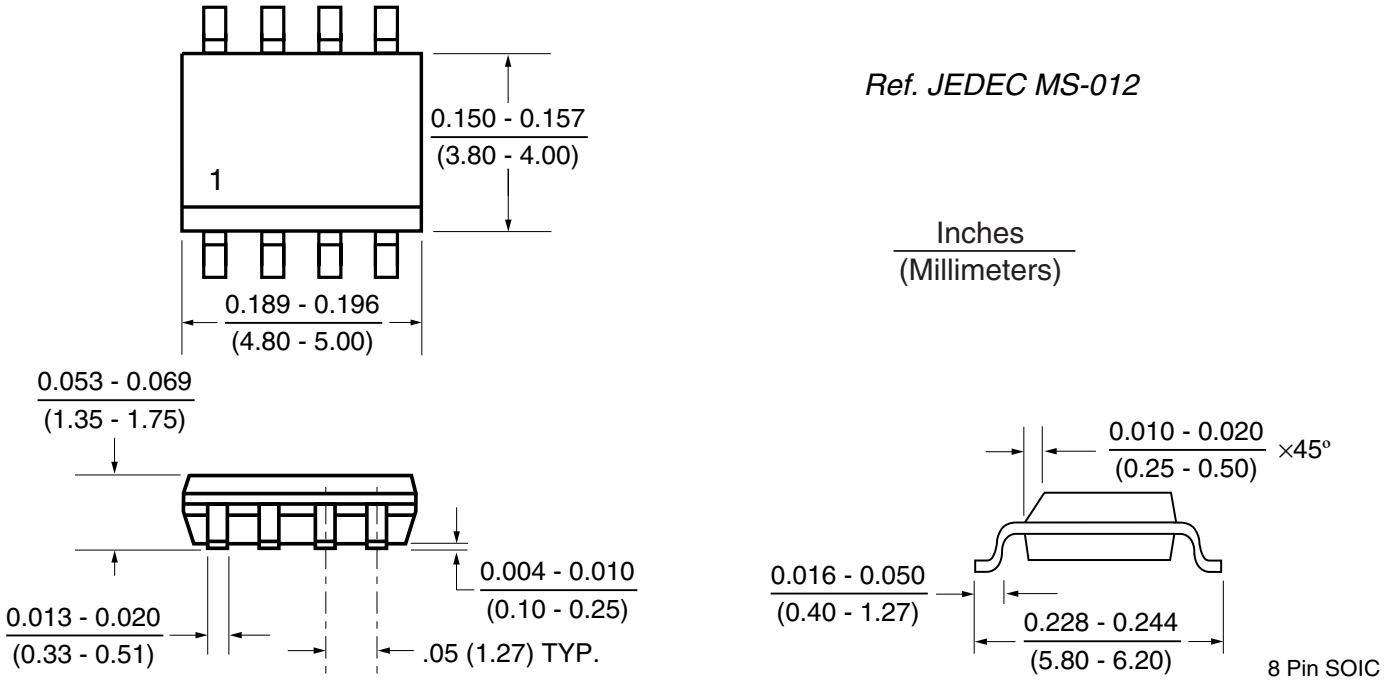
AC OPERATING CHARACTERISTICS

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Parameter	Notes	Min.	Typ.	Max	Unit
T_{RESET_OUT}	Reset Timeout period	Programmed Default = 25ms	0.8	1	1.2	ms
			20	25	30	ms
			80	100	120	ms
			160	200	240	ms
t_{GLITCH}	Programmable glitch filter times	Programmed Default = 4µs	3	4	5	µs
			4.5	6	7.5	µs
			7.5	10	12.5	µs
			13.5	18	22.5	µs
t_{RESET_HD}	Programmable Reset Hold-Down Delay times	Programmed Default = 10s	0.26	0.325	0.39	s
			0.5	0.625	0.75	s
			1	1.25	1.5	s
			2	2.5	3	s
			4	5	6	s
			8	10	12	s
			16	20	24	s
			32	40	48	s

PACKAGE OUTLINE

8 Pin SOIC Package



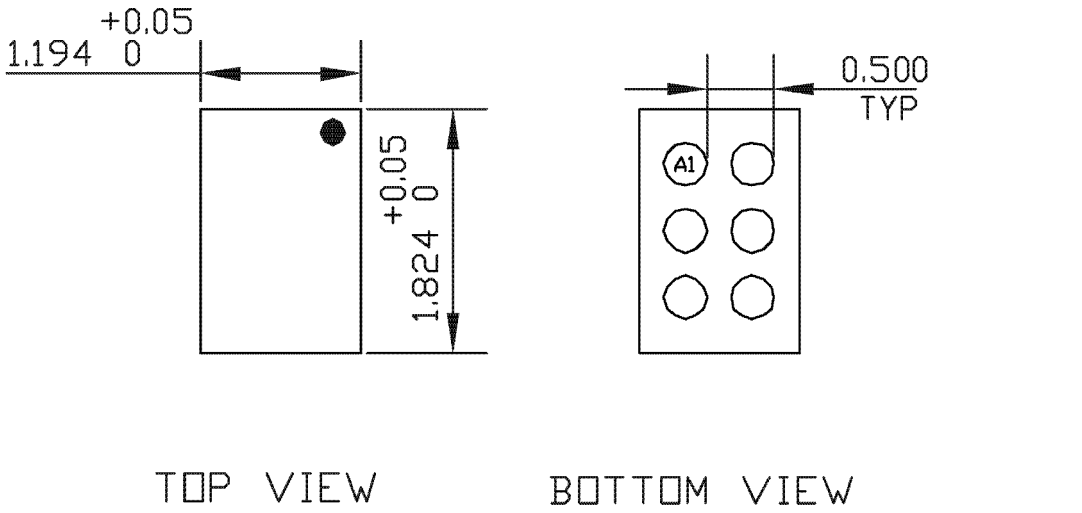
Ref. JEDEC MS-012

Inches
(Millimeters)

8 Pin SOIC

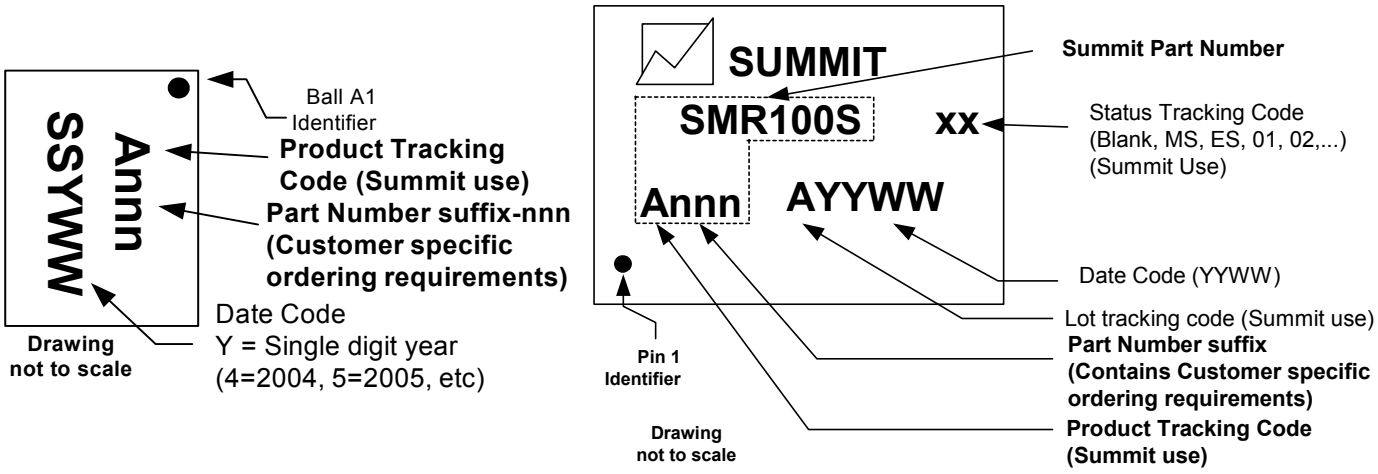
PACKAGE OUTLINE (CONTINUED)

6 Ball *Ultra* CSP™ – Chip Scale Package

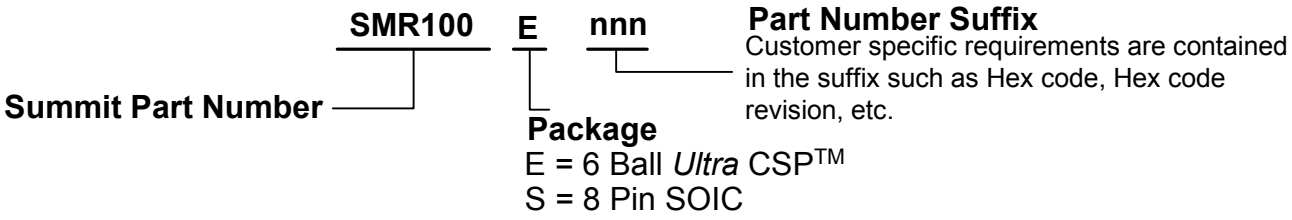


NOTES:
1. SOLDER COMPOSITION IS Sn 63% , Pb 37%
2. MELTING POINT IS 182°C ± 2°C
3. PART IS LASER MARKED 0.3mm FONT HEIGHT.
   0.2mm FONT PITCH.
   WHITE MARKING
   DEPTH: 3 TO 8um
4. ALL DIMENSIONS ARE IN MILLIMETERS [mm]

PART MARKING



ORDERING INFORMATION



The default device ordering number is SMR100E-100 and is programmed as described in the AC Operating Characteristics table on page 6 and tested over the commercial temperature range.

NOTICE

NOTE 1 - This is a ***Preliminary Information*** data sheet that describes a Summit product currently in pre-production with limited characterization.

Revision 1.6 - This document supersedes all previous versions. Data Sheet updates can be accessed by "right" or "left" mouse clicking on the link: http://www.summitmicro.com/

Device Errata sheets can be accessed by "right" or "left" mouse clicking on the link: http://www.summitmicro.com/errata/
