



LB1991V — Monolithic Digital IC For Fan Motor 3-phase Brushless Motor Driver

Overview

The LB1991V is a 3-phase brushless motor driver IC that is optimal for driving the DC fan motor.

Functions

- 3-phase full-wave voltage drive technique (120° voltage-linear technique)
- Torque ripple correction circuit (overlap correction)
- Speed control technique based on motor voltage and current control
- Built-in FG comparators
- Built-in thermal shutdown circuit

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{CC1} max		10	V
	V _{CC2} max		11	V
	V _S max		11	V
Applied output voltage	V _O max		V _S +2	V
Maximum output current	I _O max		1.0	A
Allowable power dissipation	P _d max	Independent IC	440	mW
Operating temperature	T _{opr}		-20 to +75	°C
Storage temperature	T _{stg}		-55 to +150	°C

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{CC1}	V _{CC1} ≤ V _{CC2}	2.7 to 6.0	V
	V _{CC2}		3.5 to 9.0	V
	V _S		Up to V _{CC2}	V
Hall input amplitude	V _{HALL}	Between Hall effect element inputs	±20 to ±80	mVp-p

■ Any and all SANYO Semiconductor Co.,Ltd. products described or contained herein are, with regard to "standard application", intended for the use as general electronics equipment (home appliances, AV equipment, communication device, office equipment, industrial equipment etc.). The products mentioned herein shall not be intended for use for any "special application" (medical equipment whose purpose is to sustain life, aerospace instrument, nuclear control device, burning appliances, transportation machine, traffic signal system, safety equipment etc.) that shall require extremely high level of reliability and can directly threaten human lives in case of failure or malfunction of the product or may cause harm to human bodies, nor shall they grant any guarantee thereof. If you should intend to use our products for applications outside the standard applications of our customer who is considering such use and/or outside the scope of our intended standard applications, please consult with us prior to the intended use. If there is no consultation or inquiry before the intended use, our customer shall be solely responsible for the use.

■ Specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.

LB1991V

Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC1} = 3\text{V}$, $V_{CC2} = 4.75\text{V}$, $V_S = 1.5\text{V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply Current						
V_{CC1} current drain	I_{CC1}	$I_{OUT} = 100\text{mA}$		3	5	mA
V_{CC2} current drain	I_{CC2}	$I_{OUT} = 100\text{mA}$		7.0	10.0	mA
V_{CC1} quiescent current	I_{CC1Q}	$V_{STBY} = 0\text{V}$		1.5	3.0	mA
V_{CC2} quiescent current	I_{CC2Q}	$V_{STBY} = 0\text{V}$			100	μA
V_S quiescent current	I_{SQ}	$V_{STBY} = 0\text{V}$		75	100	μA
VX1						
High side residual voltage	V_{XH1}	$I_{OUT} = 0.2\text{A}$	0.15	0.22	0.29	V
Low side residual voltage	V_{XL1}	$I_{OUT} = 0.2\text{A}$	0.15	0.20	0.25	V
VX2						
High side residual voltage	V_{XH2}	$I_{OUT} = 0.5\text{A}$		0.25	0.40	V
Low side residual voltage	V_{XL2}	$I_{OUT} = 0.5\text{A}$		0.25	0.40	V
Output saturation voltage	$V_{O(sat)}$	$I_{OUT} = 0.8\text{A}$, Sink + Source			1.4	V
Overlap	O.L	$R_L = 39\Omega \times 3$, Rangle = $20\text{k}\Omega$ *2	72	80	87	%
High/low overlap difference	$\Delta\text{O.L}$	(Average upper side overlap) – (Average lower side overlap) *2	-8		+8	%
Hall Amplifiers						
Input offset voltage	V_{HOFF}	Design target *1	-5		+5	mV
Common-mode input voltage range	V_{HCM}	Rangle = $20\text{k}\Omega$	0.95		2.1	V
I/O voltage gain	V_{GVH}	Rangle = $20\text{k}\Omega$	25.5	28.5	31.5	dB
Standby Pin						
High-level voltage	V_{STH}		2.5			V
Low-level voltage	V_{STL}				0.4	V
Input current	I_{STIN}	$V_{STBY} = 3\text{V}$		25	40	μA
Leakage current	I_{STLK}	$V_{STBY} = 0\text{V}$			-30	μA
FRC Pin						
High-level voltage	V_{FRCH}		2.5			V
Low-level voltage	V_{FRCL}				0.4	V
Input current	I_{FRCIN}	$V_{FRC} = 3\text{V}$		25	30	μA
Leakage current	I_{FRCLK}	$V_{FRC} = 0\text{V}$			-30	μA
VH						
Hall supply voltage	V_{HALL}	$I_H = 5\text{mA}$, $V_H(+)$ – $V_H(-)$	0.85	0.95	1.05	V
(-) pin voltage	$V_H(-)$	$I_H = 5\text{mA}$	0.81	0.88	0.95	V
FG Comparator						
Input offset voltage	V_{FGOFF}		-3		+3	mV
Input bias voltage	I_{bFG}	$V_{FGIN}^+ = V_{FGIN}^- = 1.5\text{V}$			500	nA
Input bias current offset	ΔI_{bFG}	$V_{FGIN}^+ = V_{FGIN}^- = 1.5\text{V}$	-100		+100	nA
Common-mode input voltage range	V_{FGCM}		1.2		2.5	V
Output high-level voltage	V_{FGOH}	At the internal pull-up resistors	2.8			V
Output low-level voltage	V_{FGOL}	At the internal pull-up resistors			0.2	V
Voltage gain	V_{GFG}	Design target *1		100		dB
Output current (sink)	I_{FGOS}	For the output pin low level			5	mA
Thermal shutdown						
Operating temperature	TSD	Design target *1		180		$^\circ\text{C}$
Temperature hysteresis	ΔTSD	Design target *1		20		$^\circ\text{C}$

*1: Design target values in the conditions column are not tested.

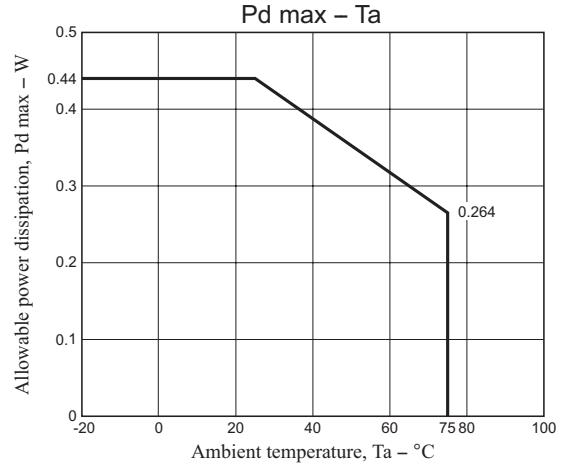
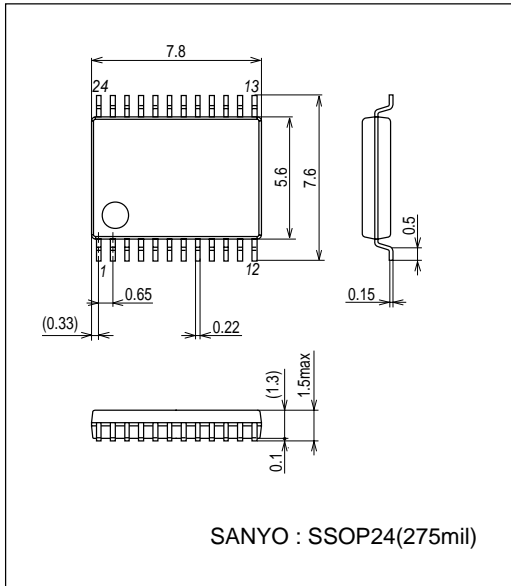
*2: The standard for overlap is the value as measured.

LB1991V

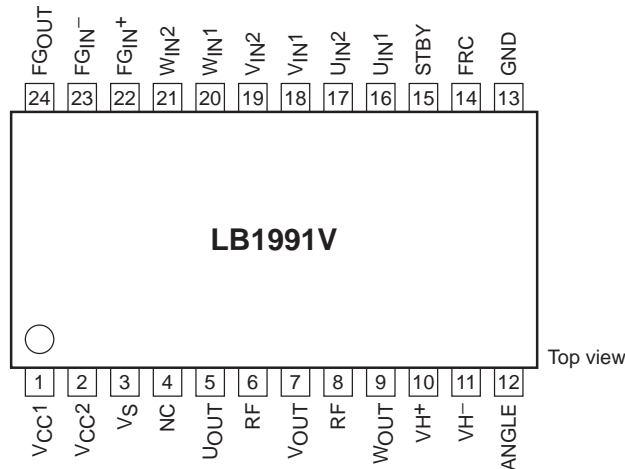
Package Dimensions

unit : mm (typ)

3175C



Pin Assignment



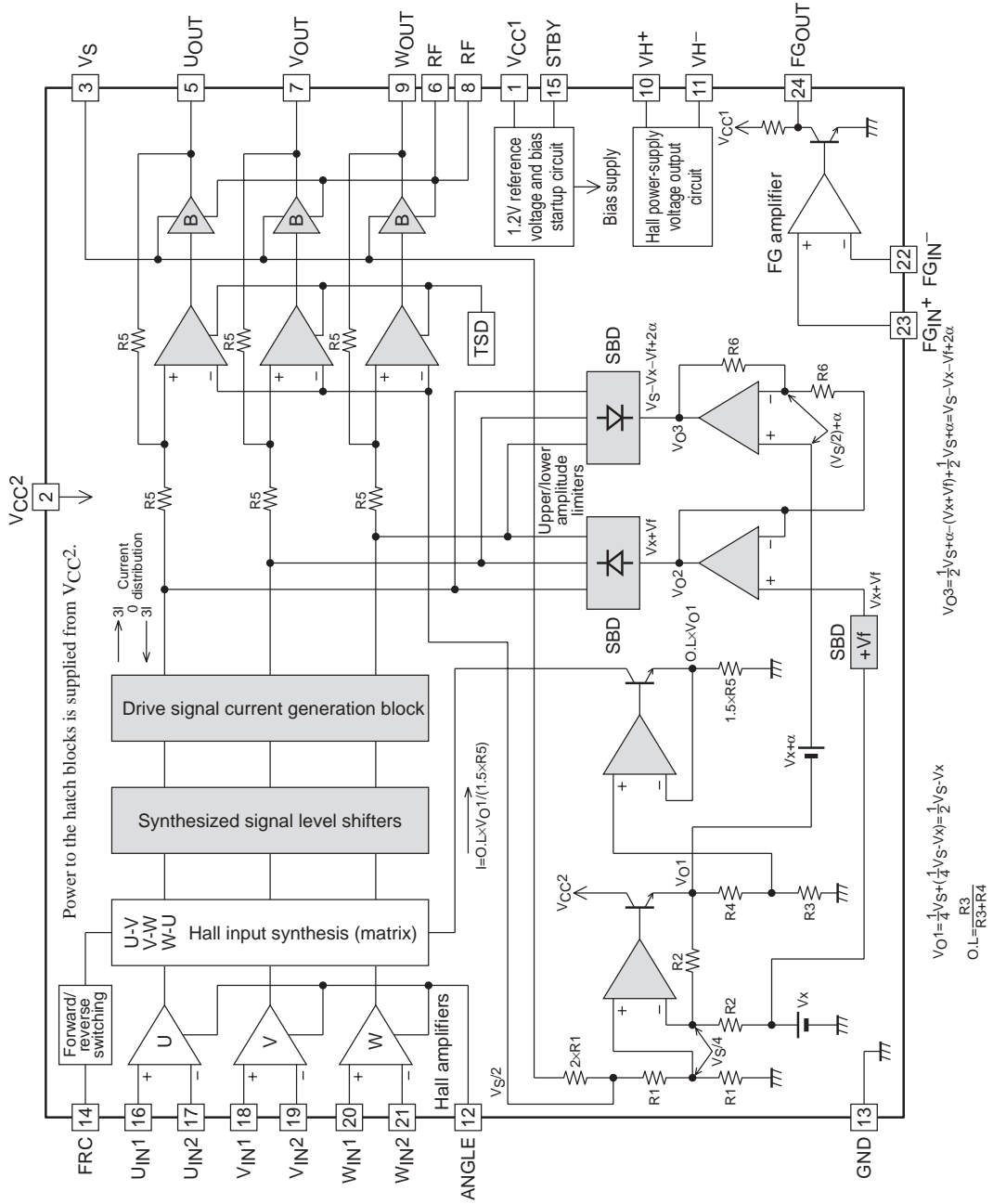
Truth Table

	Source phase → Sink phase	Hall input			FRC
		U	V	W	
1	V → W	H	H	L	H
	W → V	H	H	L	L
2	U → W	H	L	L	H
	W → U	H	L	L	L
3	U → V	H	L	H	H
	V → U	H	L	H	L
4	W → V	L	L	H	H
	V → W	L	L	H	L
5	W → U	L	H	H	H
	U → W	L	H	H	L
6	V → U	L	H	L	H
	U → V	L	H	L	L

Note: The "H" entries in the FRC column indicate a voltage of 2.50V or higher, and the "L" entries indicate a voltage of 0.4V or lower. (When V_{CC1} is 3V.)

At the Hall inputs, for each phase a high-level input is the state where the (+) input is 0.02V or higher than the (-) input. Similarly, a low-level input is the state where the (+) input is 0.02V or lower than the (-) input.

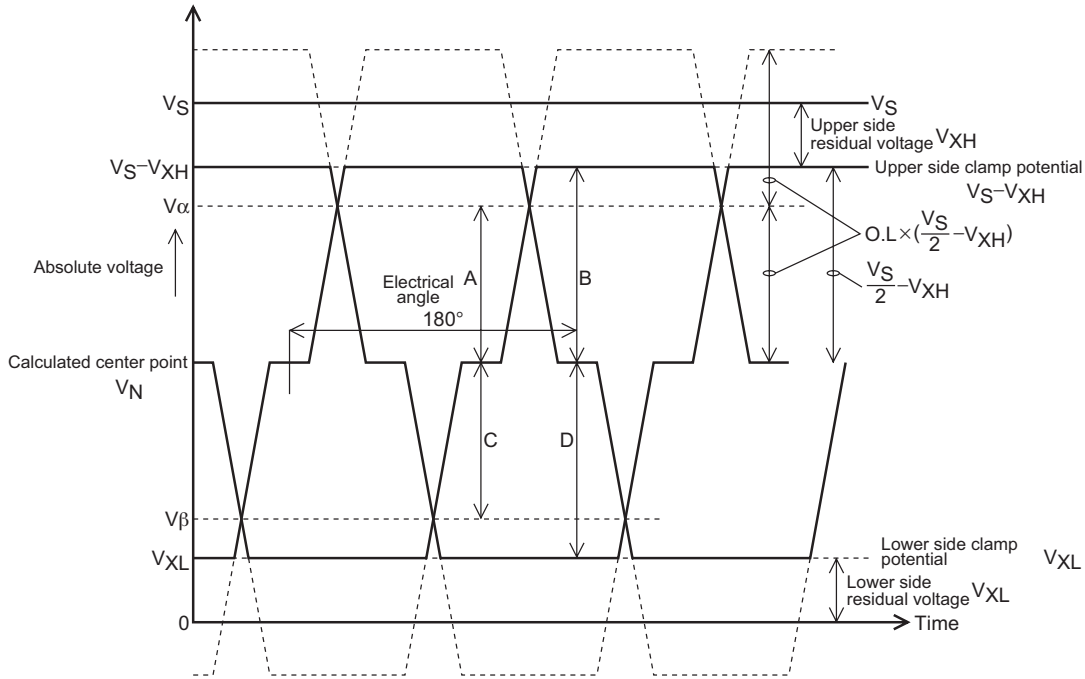
Block Diagram



Pin Function

Pin No.	Pin name	Pin function	Equivalent circuit
1	V _{CC1}	Supply voltage for all circuits other than the IC internal output block and the amplitude control block.	
2	V _{CC2}	Supply voltage for the IC internal output control block and the amplitude control block.	
3	V _S	Motor drive power supply. The voltage applied to this pin must not exceed V _{CC2} .	
5	U _{OUT}	U phase output.	
7	V _{OUT}	V phase output.	
9	W _{OUT}	W phase output. (These outputs include built-in spark killer diodes.)	
6,8	RF	Ground for the output power transistors.	
10	V _H ⁺	Hall element bias voltage supply. A voltage that is typically 0.95V is generated between the V _H ⁺ and V _H ⁻ pins (When I _H is 5mA).	
11	V _H ⁻		
13	GND	Ground for circuits other than the output transistor. The RF pin potential is the lowest output transistor potential.	
14	FRC	Forward/reverse selection. Applications can select motor forward or reverse direction rotation using this pin. (This pin has hysteresis characteristics.)	
15	STBY	Selects the bias supply for all circuits other than the FG comparators. The bias supply is cut when this pin is set to the low level.	
16	U _{IN1}	U phase Hall element input. The logic high level is the state where the IN ⁺ voltage is greater than the IN ⁻ voltage.	
17	U _{IN2}		
18	V _{IN1}	V phase Hall element input. The logic high level is the state where the IN ⁺ voltage is greater than the IN ⁻ voltage.	
19	V _{IN2}		
20	W _{IN1}	W phase Hall element input. The logic high level is the state where the IN ⁺ voltage is greater than the IN ⁻ voltage.	
21	W _{IN2}		
12	ANGLE	Hall input/output gain control. The gain is controlled by the resistor connected between this pin and ground.	
22	FG _{IN} ⁺	FG comparator non-inverting inputs. There is no internally applied bias.	
23	FG _{IN} ⁻	FG comparator inverting inputs. There is no internally applied bias.	
24	FG _{OUT}	FG comparator outputs. There is an internal 20kΩ resistor load.	

Overlap Generation and Calculation Method



Overlap Generation

Since the voltage generated in the amplitude control block is, taking the center point as the reference, $2 \times \langle \text{overlap} \rangle \times (1/2 V_S - V_X)$ on one side, the intersection point of the waveform will be $\langle \text{overlap} \rangle \times (1/2 V_S - V_X)$ from the center point.

To clamp that waveform at $(1/2 V_S - V_X)$ referenced to the center point the overlap must be:

$$A/B \times 100 = \langle \text{overlap} \rangle \times 100 (\%)$$

Overlap Calculation

- Upper side overlap

$$\text{Calculated center point: } V_N = \frac{(V_S - V_{XH} - V_{XL})}{2} + V_{XL} = \frac{(V_S - V_{XH} + V_{XL})}{2}$$

Since $A = V_\alpha - V_N$, $B = V_S - V_{XH} - V_N$, the upper side overlap will be:

$$\langle \text{overlap} \rangle = \frac{A}{B} = \frac{V_\alpha - ((V_S - V_{XH} + V_{XL})/2)}{V_S - V_{XH} - ((V_S - V_{XH} + V_{XL})/2)} \times 100$$

Which can be calculated as:

$$= \frac{2V_\alpha - (V_S - V_{XH}) - V_{XL}}{(V_S - V_{XH}) - V_{XL}} \times 100(\%)$$

- Lower side overlap

Since $C = V_N - V_\beta$, and $D = V_N - V_{XL}$, the lower side overlap will be:

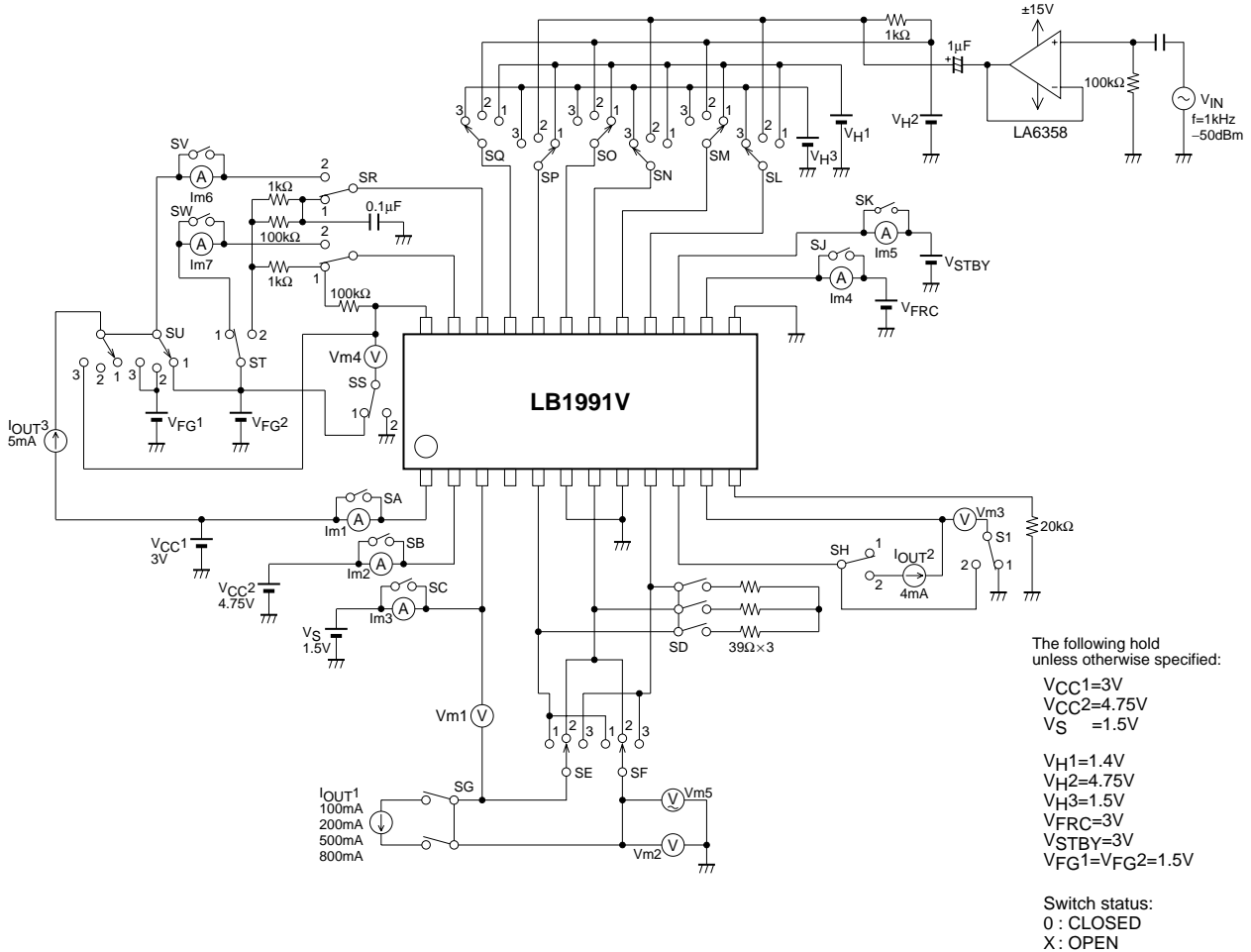
$$\langle \text{overlap} \rangle = \frac{C}{D} = \frac{((V_S - V_{XH} + V_{XL})/2) - V_\beta}{((V_S - V_{XH} + V_{XL})/2) - V_{XL}} \times 100$$

Which can be calculated as:

$$= \frac{(V_S - V_{XH}) + V_{XL} - 2V_\beta}{(V_S - V_{XH}) - V_{XL}} \times 100(\%)$$

LB1991V

Test Circuit



- SANYO Semiconductor Co.,Ltd. assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein.
- SANYO Semiconductor Co.,Ltd. strives to supply high-quality high-reliability products, however, any and all semiconductor products fail or malfunction with some probability. It is possible that these probabilistic failures or malfunction could give rise to accidents or events that could endanger human lives, trouble that could give rise to smoke or fire, or accidents that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO Semiconductor Co.,Ltd. products described or contained herein are controlled under any of applicable local export control laws and regulations, such products may require the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written consent of SANYO Semiconductor Co.,Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO Semiconductor Co.,Ltd. product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production.
- Upon using the technical information or products described herein, neither warranty nor license shall be granted with regard to intellectual property rights or any other rights of SANYO Semiconductor Co.,Ltd. or any third party. SANYO Semiconductor Co.,Ltd. shall not be liable for any claim or suits with regard to a third party's intellectual property rights which has resulted from the use of the technical information and products mentioned above.

This catalog provides information as of January, 2009. Specifications and information herein are subject to change without notice.