



LB1987, 1987D, 1987M, 1987H

Three-Phase Brushless Motor Driver for VCR Capstan Motors

Overview

The LB1987, LB1987D, LB1987M, and LB1987H are optimal capstan motor drivers for use in VCR sets.

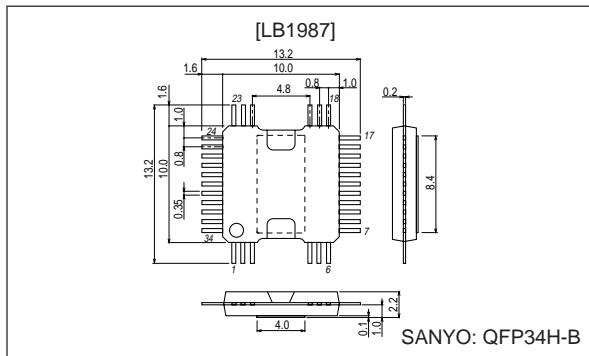
Functions

- Three-phase full-wave current-linear drive
- Torque ripple correction circuit (fixed correction ratio)
- Current limiter circuit with control characteristics gain switching
- Oversaturation prevention circuits for both the upper and lower sides of the output stage (No external capacitors are required.)
- FG amplifier
- Thermal shutdown circuit

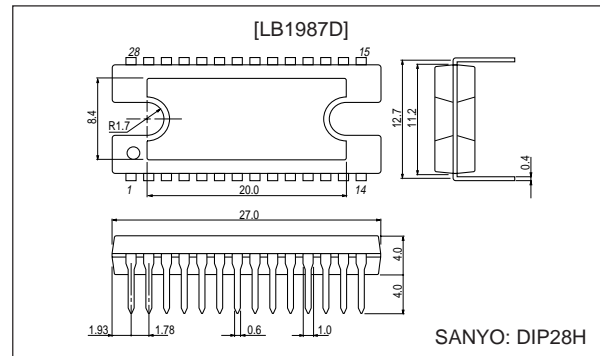
Package Dimensions

unit: mm

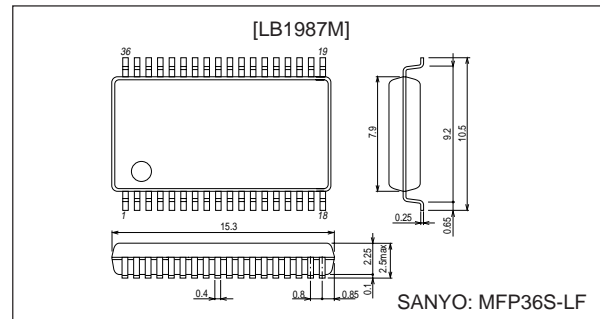
3240-QFP34H-B



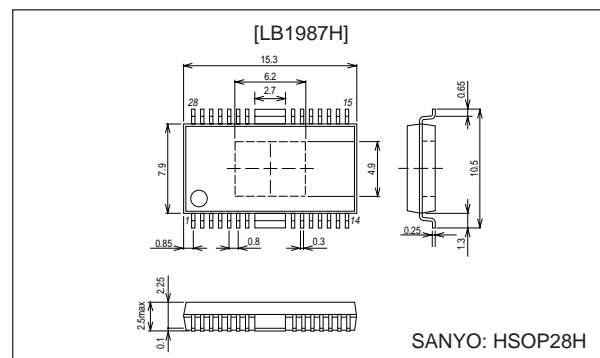
3147B-DIP28H



3129-MFP36S-LF



3233-HSOP28H



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81299RM (OT) No. 6109-1/17

LB1987, 1987D, 1987M, 1987H

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{CC} max		7	V
	V _S max		24	V
Maximum output current	I _O max		1.3	A
Allowable power dissipation	Pd max	(LB1987)	0.77	W
		(LB1987D)	3.0	W
		(LB1987M)	0.95	W
		(LB1987H)	0.77	W
Operating temperature	Topr		-20 to +75	°C
Storage temperature	Tstg		-55 to +150	°C

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _S		5 to 22	V
	V _{CC}		4.5 to 5.5	V
Hall input amplitude	V _{HALL}	Between Hall inputs	±30 to ±80	mV _{o-p}
GSENSE pin input range	V _{GSENSE}	Relative to the control system ground	-0.20 to +0.20	V

Electrical Characteristics at Ta = 25°C, V_{CC} = 5 V, V_S = 15 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
V _{CC} current drain	I _{CC}	RL = ∞, V _{CTL} = 0 V (Quiescent)		12	18	mA
[Outputs]						
Output saturation voltage	Vosat1	I _O = 500 mA, R _f = 0.5 Ω, Sink + Source, V _{CTL} = V _{LIM} = 5 V (With saturation prevention)		2.1	2.6	V
	Vosat2	I _O = 1.0 A, R _f = 0.5 Ω, Sink + Source, V _{CTL} = V _{LIM} = 5 V (With saturation prevention)		2.6	3.5	V
Output leakage current	I _{Oleak}				1.0	mA
[FR]						
FR pin input threshold voltage	V _{FSR}		2.25	2.50	2.75	V
FR pin input bias current	I _b (FSR)		-5.0			μA
[Control]						
CTLREF pin voltage	V _{CREF}		2.37	2.50	2.63	V
CTLREF pin input range	V _{CREFIN}		1.70		3.50	V
CTL pin input bias current	I _b (CTL)	V _{CTL} = 5 V, CTLREF: open			8.0	μA
CTL pin control start voltage	V _{CTL} (ST)	R _f = 0.5 Ω, V _{LIM} = 5 V, I _O ≥ 10 mA With the Hall input logic states fixed at (U, V, W = H, H, L)	2.20	2.35	2.50	V
CTL pin control switching voltage	V _{CTL} (ST2)	R _f = 0.5 Ω, V _{LIM} = 5 V	3.00	3.15	3.30	V
CTL pin control Gm1	Gm1(CTL)	R _f = 0.5 Ω, ΔI _O = 200 mA With the Hall input logic states fixed at (U, V, W = H, H, L)	0.52	0.65	0.78	A/V
CTL pin control Gm2	Gm2(CTL)	R _f = 0.5 Ω, ΔV _{CTL} = 200 mV With the Hall input logic states fixed at (U, V, W = H, H, L)	1.20	1.50	1.80	A/V
[Current Limiter]						
LIM current limiter offset voltage	V _{off} (LIM)	R _f = 0.5 Ω, V _{CTL} = 5 V, I _O ≥ 10 mA With the Hall input logic states fixed at (U, V, W = H, H, L)	140	200	260	mV
LIM pin input bias current	I _b (LIM)	V _{CTL} = 5 V, V _{CREF} : open, V _{LIM} = 0 V	-2.5			μA
LIM pin current limit level	I _{LIM}	R _f = 0.5 Ω, V _{CTL} = 5 V, V _{LIM} = 2.06 V With the Hall input logic states fixed at (U, V, W = H, H, L)	830	900	970	mA
[Hall Amplifiers]						
Input offset voltage	V _{off} (HALL)		-6		+6	mV
Input bias current	I _b (HALL)			1.0	3.0	μA
Common-mode input voltage	V _{cm} (HALL)		1.3		3.3	V
Torque ripple correction ratio	TRC	At the bottom and top of the R _f waveform when I _O = 200 mA. (R _f = 0.5 Ω) (Note 1)		9		%
[FG Amplifier]						
FG amplifier input offset voltage	V _{off} (FG)		-8		+8	mV
FG amplifier input bias current	I _b (FG)		-100			nA
FG amplifier output saturation voltage	Vosat(FG)	At the sink side internal pull-up resistor.			0.5	V
FG amplifier common-mode input voltage	V _{CM} (FG)		0.5		4.0	V

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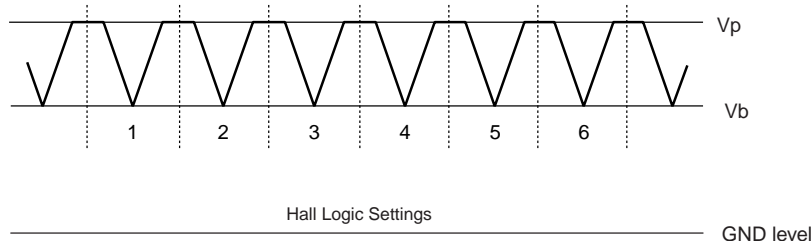
LB1987, 1987D, 1987M, 1987H

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Saturation Prevention]						
Saturation prevention circuit lower side voltage setting	Vosat(DET)	$I_O = 10 \text{ mA}$, $R_f = 0.5 \Omega$, $V_{CTL} = L_{VIM} = 5 \text{ V}$, The voltage between each OUT and Rf.	0.175	0.25	0.325	V
[Schmitt Amplifier]						
Duty ratio	DUTY	Under the specified conditions	47	50	53	%
Upper side output saturation voltage	Vsatu(SH)		4.8			V
Lower side output saturation voltage	Vsatd(SH)				0.2	V
Hysteresis	Vhys		32	50	60	mV
Thermal shutdown operating temperature	T-TSD	*		170		°C

Note: * Items marked with an asterisk are design target values and are not measured.

Note: 1. The torque ripple correction ratio is determined from the Rf voltage waveform as shown below.



$$\text{Correction ratio} = \frac{2 \cdot (V_p - V_b)}{V_p + V_b} \cdot 100 \cdot (\%)$$

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Truth Table and Control Functions

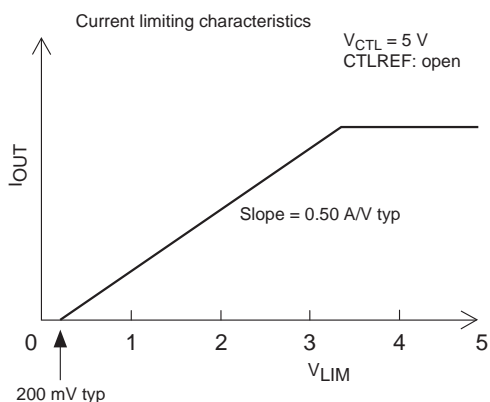
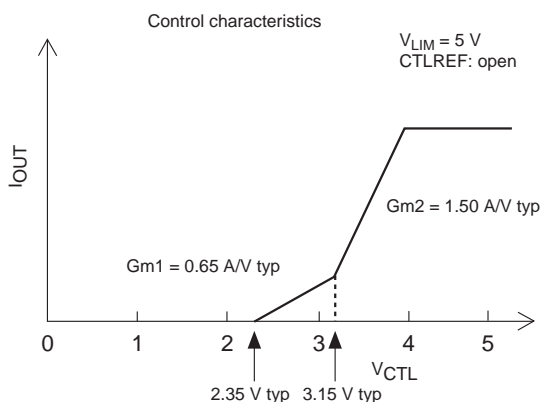
	Source → sink	Hall input			FR
		U	V	W	
1	V → W	H	H	L	H
	W → V				L
2	U → W	H	L	L	H
	W → U				L
3	U → V	H	L	H	H
	V → U				L
4	W → V	L	L	H	H
	V → W				L
5	W → U	L	H	H	H
	U → W				L
6	V → U	L	H	L	H
	U → V				L

Note: 1. The "H" state for FR means a voltage of 2.75 V or higher, and the "L" state means a voltage of 2.25 V or lower. (When $V_{CC} = 5 \text{ V}$.)

2. For the Hall inputs, the input "H" state means the state in which the (+) input for that phase is at least 0.01 V higher than the (-) input for that phase. Similarly, the "L" state means the state in which the (+) input for that phase is at least 0.01 V lower than the (-) input for that phase.

3. Since this drive technique is a 180° power application technique, the phase that is neither the source phase nor the sink phase does not turn completely off.

Control and Current Limiting Functions



Pin Functions

Pin	Function	Equivalent circuit diagram
U _{IN+} U _{IN-}	U phase Hall element input. Logic H refers to the state where IN+ > IN-	<p style="text-align: right;">A12207</p>
V _{IN+} V _{IN-}	V phase Hall element input. Logic H refers to the state where IN+ > IN-	
W _{IN+} W _{IN-}	W phase Hall element input. Logic H refers to the state where IN+ > IN-	
U _{OUT} V _{OUT} W _{OUT}	U phase output. V phase output. (These pins include internal spark killer diodes.) W phase output.	<p style="text-align: right;">A12208</p>
V _S	Output block power supply.	
Rf(POWER) Rf(SENSE)	Output current detection. Current feedback is applied to the control block by inserting the resistor R _f between these pins and ground. Also, both the lower side saturation prevention circuit and the torque ripple correction circuit operate according to the voltage on this pin. In particular, since this voltage sets the oversaturation prevention level, the lower side oversaturation prevention operation can be degraded if the value of this resistor is set too low. Note that the PWR pin and the SENSE pin must be connected together.	<p style="text-align: right;">A12209</p>
CTL	Speed control. This circuit implements constant current drive based on current feedback from the R _f pin. G _m = 0.58 A/V typ at R _f = 0.5 Ω	
LIM	Current limiter function control. The output current can be modified linearly by the voltage on this pin. Slope = 0.5 A/V typ at R _f = 0.5 Ω	
CTLREF (LB1987/D)		

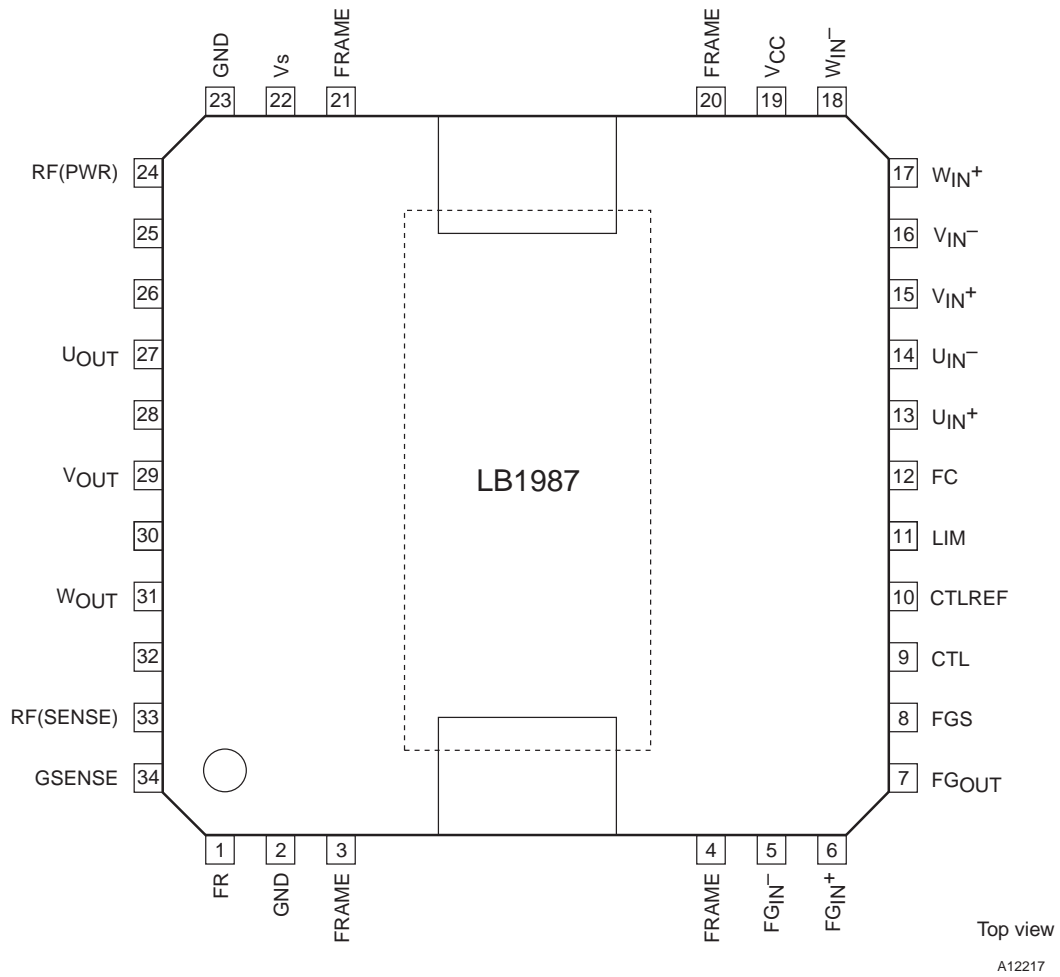
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LB1987, 1987D, 1987M, 1987H

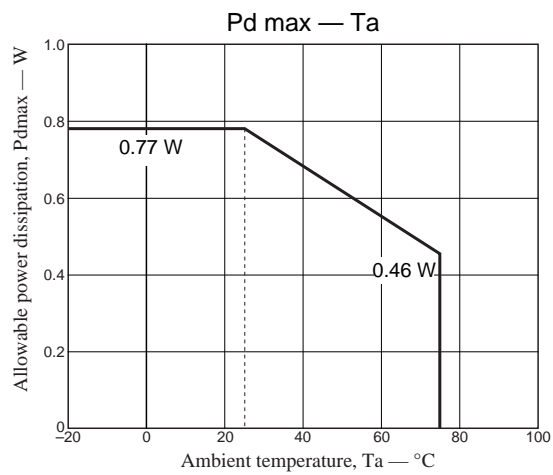
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Pin	Function	Equivalent circuit diagram
FR	Forward/reverse selection. The direction (forward or reverse) is selected by the voltage applied to this pin. ($V_{th} = 2.5 V_{typ}$ at $V_{CC} = 5 V$)	
ADJ	External torque ripple correction ratio adjustment. To adjust the correction ratio, apply the stipulated voltage to the ADJ pin from a low-impedance external circuit. If the applied voltage is increased, the correction ratio falls, and if the applied voltage is lowered, the correction ratio increases. The range of variation is from 0 to two times the correction ratio when the pin is left open. (This pin is set to about $V_{CC}/2$ internally, and has an input impedance of about 5 k Ω .)	
FG _{IN-}	Input used when the FG amplifier inverting input is used. Connect a feedback resistor between the FG _{OUT} pin and this pin.	
FG _{IN+}	Non-inverting input used when the FG amplifier is used as a differential input amplifier. No bias is applied internally.	
FG _{OUT}	FG amplifier output. This pin includes an internal load resistor.	
FC	Speed control loop frequency characteristics correction.	
GND	Ground for all systems other than the output transistors. Note that the lowest potential of the output transistors is determined by the R _f pin.	
FGS	FG pulse output. This pin includes an internal load resistor. (The output impedance is about 3 k Ω .)	
V _{CC}	Power supply for all IC internal circuits other than the output block. This power supply must be stabilized to prevent ripple or other noise from entering the circuit.	
GSENSE	Ground sensing. The influence of the common ground impedance on R _f can be excluded by connecting this pin to ground near the R _f resistor side of the motor ground wiring that includes R _f . (This pin must not be left open.)	

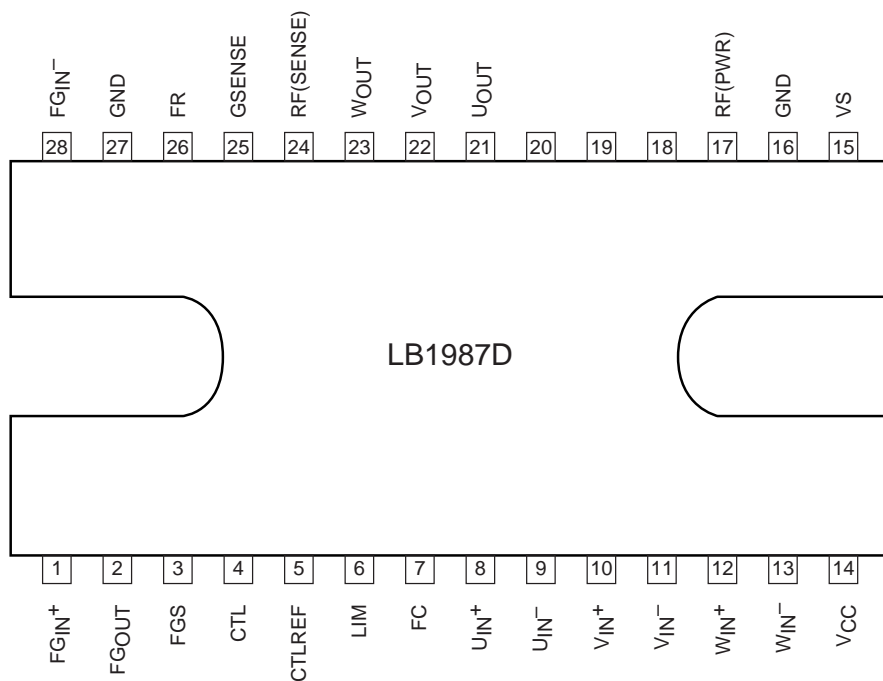
Pin Assignment



Note: The FRAME pins must be connected to ground for ground potential stabilization.

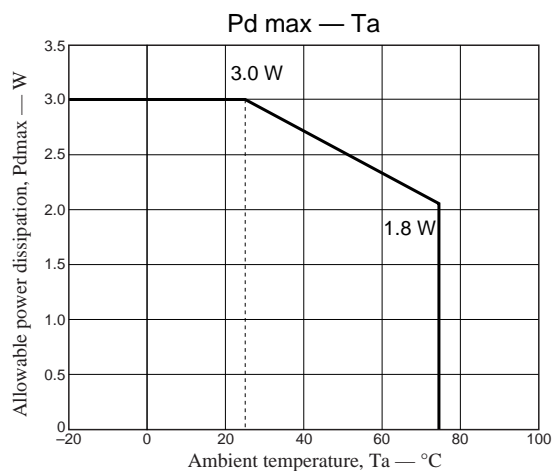


Pin Assignment



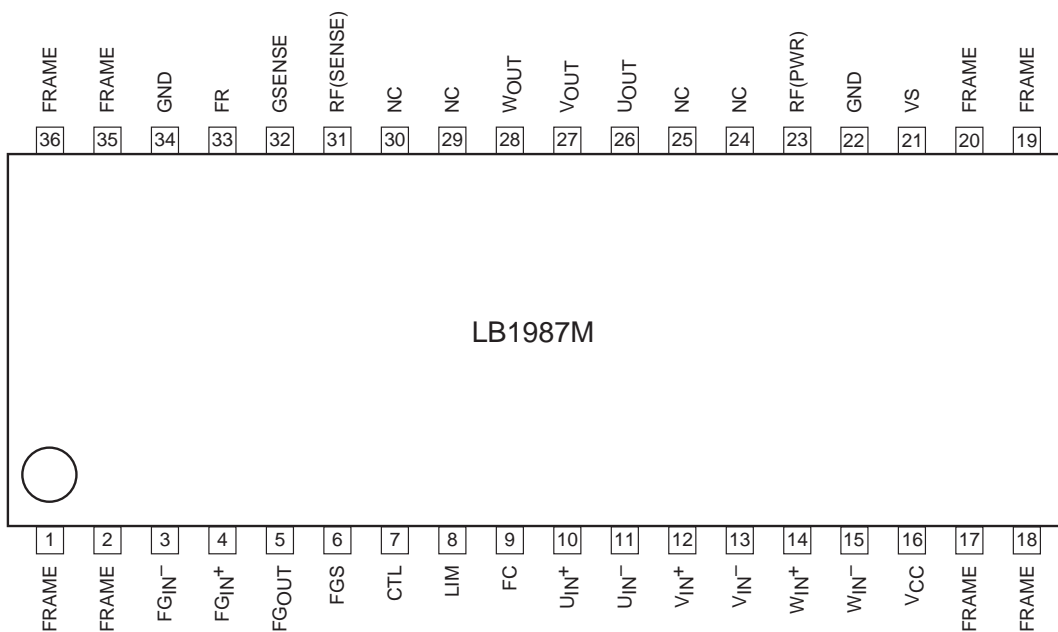
Top view

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LB1987, 1987D, 1987M, 1987H

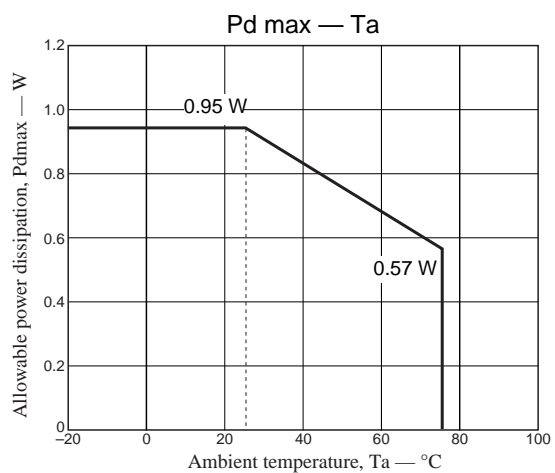
Pin Assignment



Top view

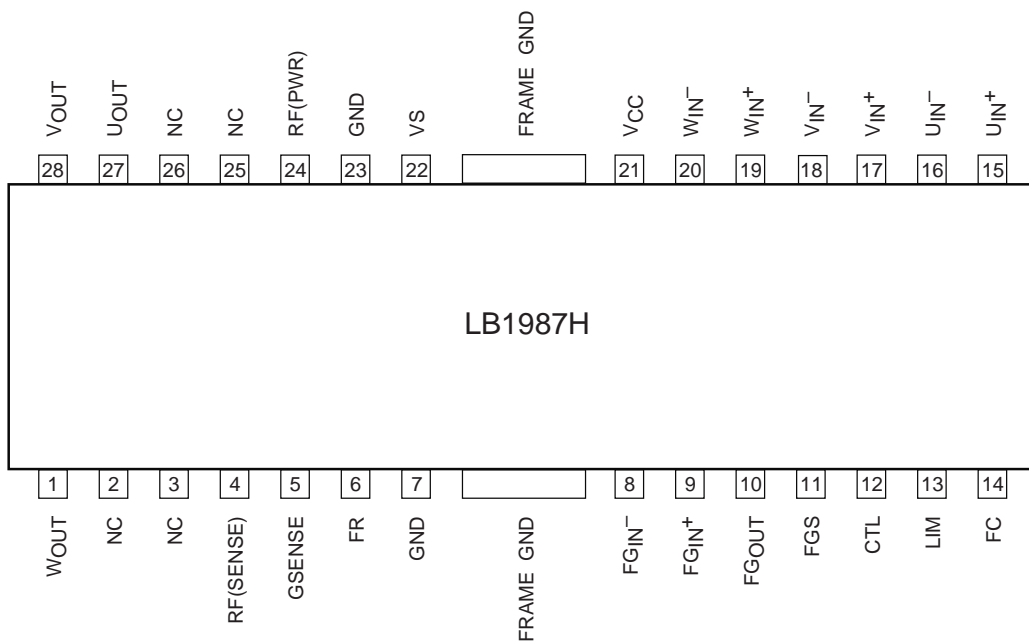
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Note: Although the FRAME pins and the GND pin are not connected internally in the IC, the FRAME pins must be connected to the GND pin externally for ground potential stabilization.



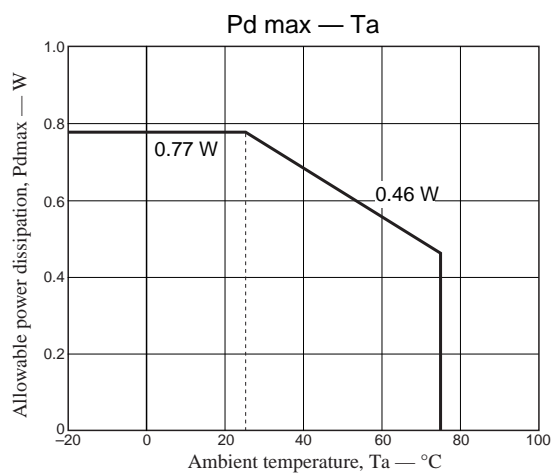
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Pin Assignment

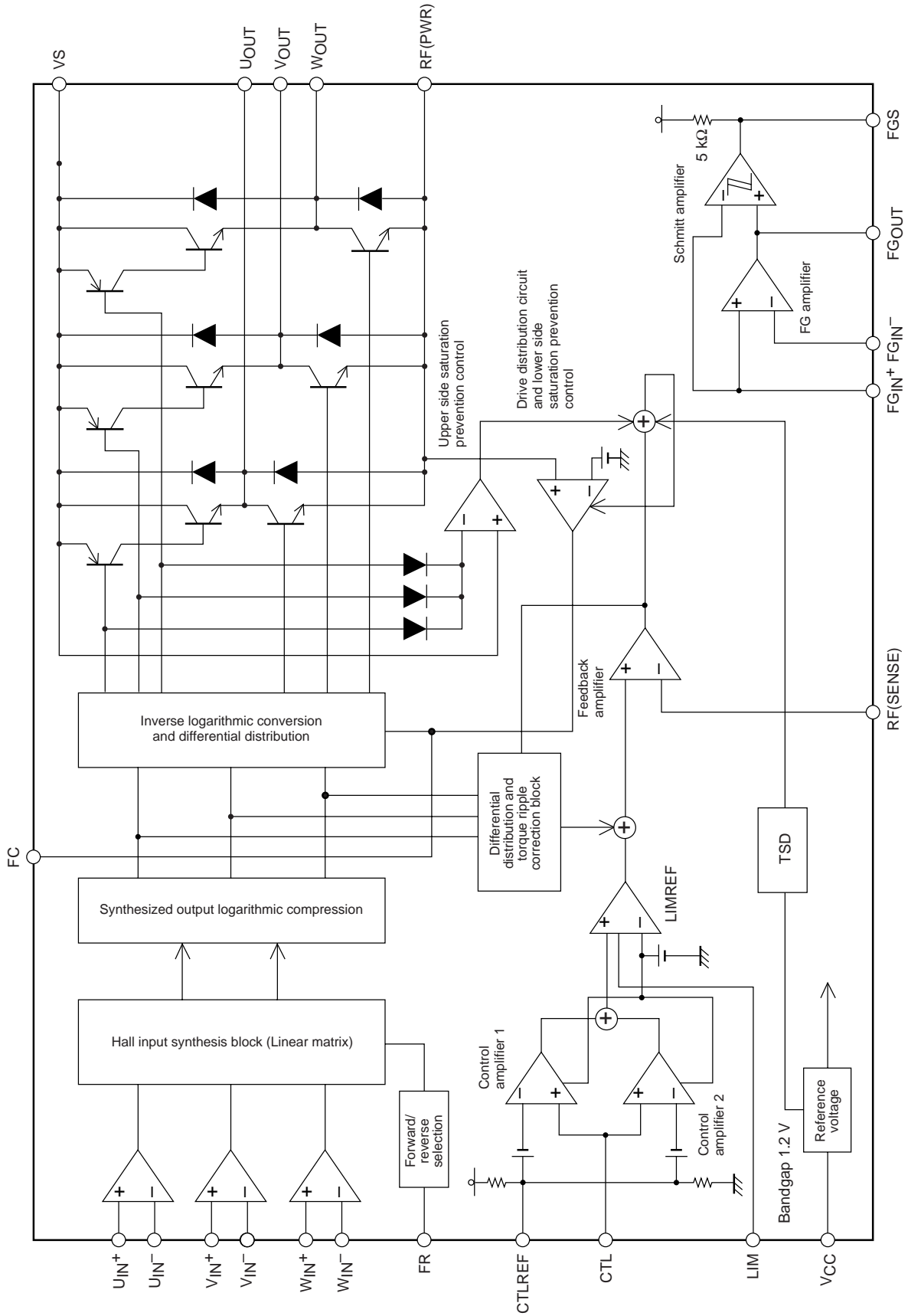


Top view

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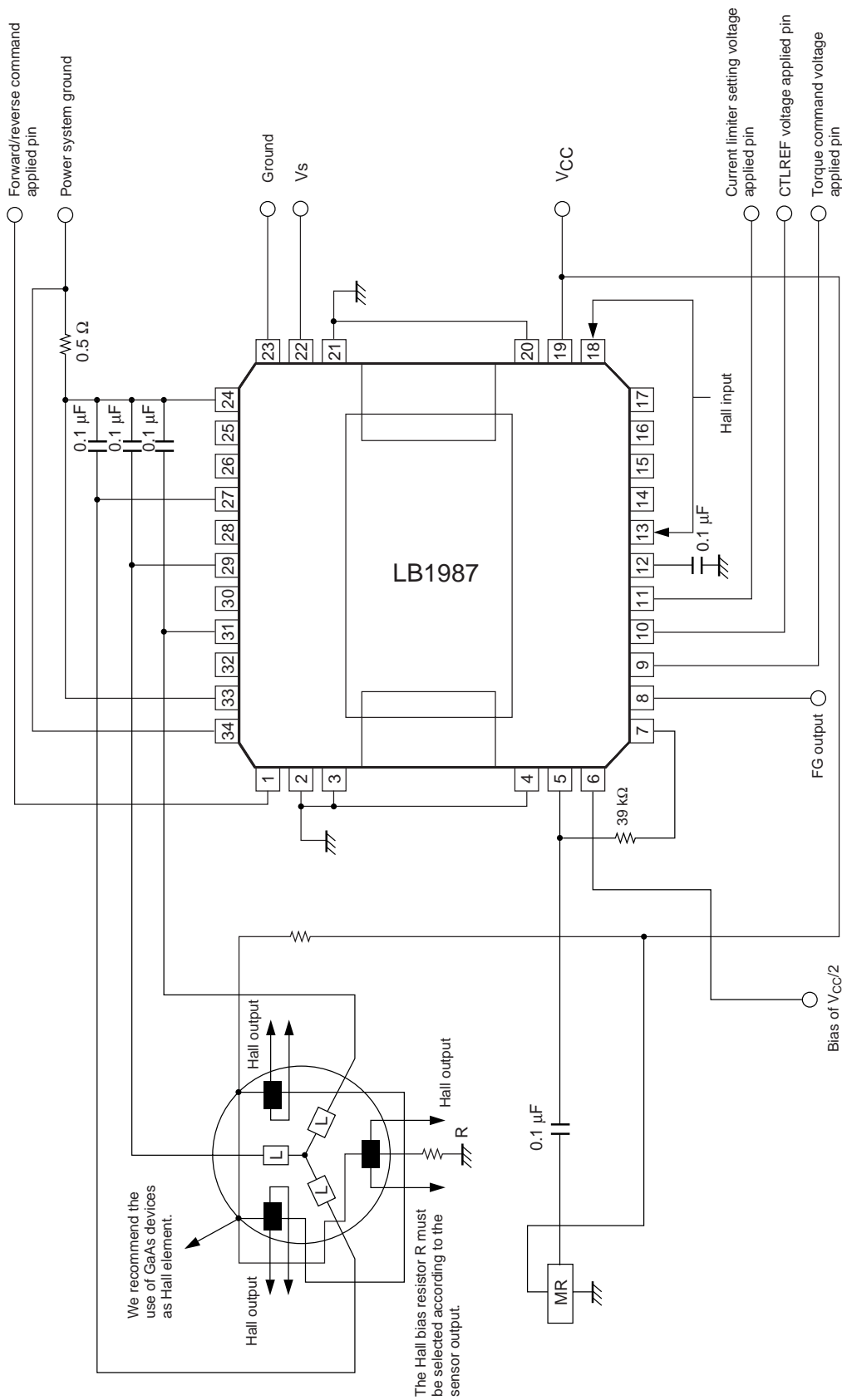


Block Diagram



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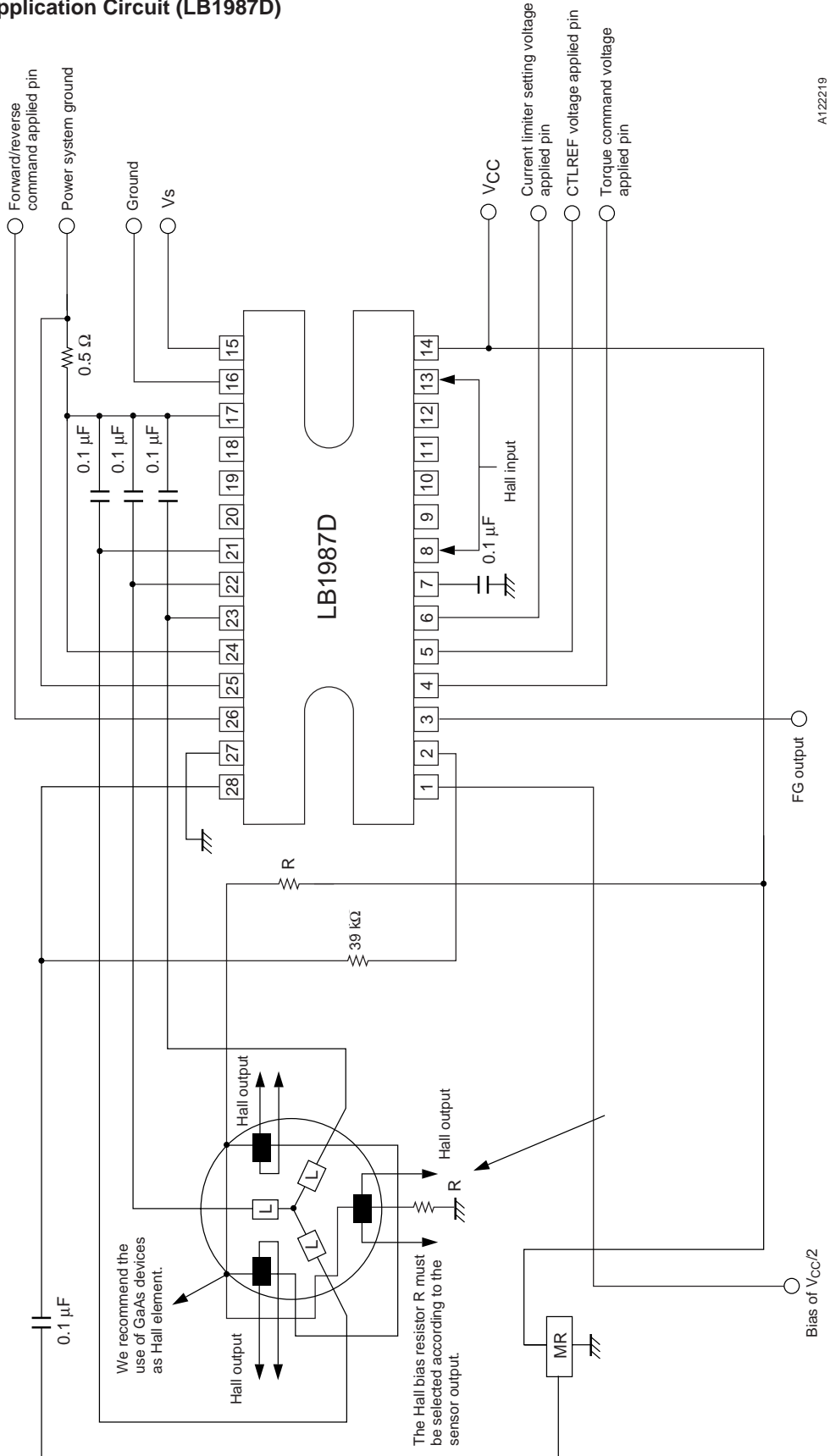
Sample Application Circuit (LB1987)



Note: The component values shown in this application circuit example are merely provided as examples, and circuit operating characteristics are not guaranteed.

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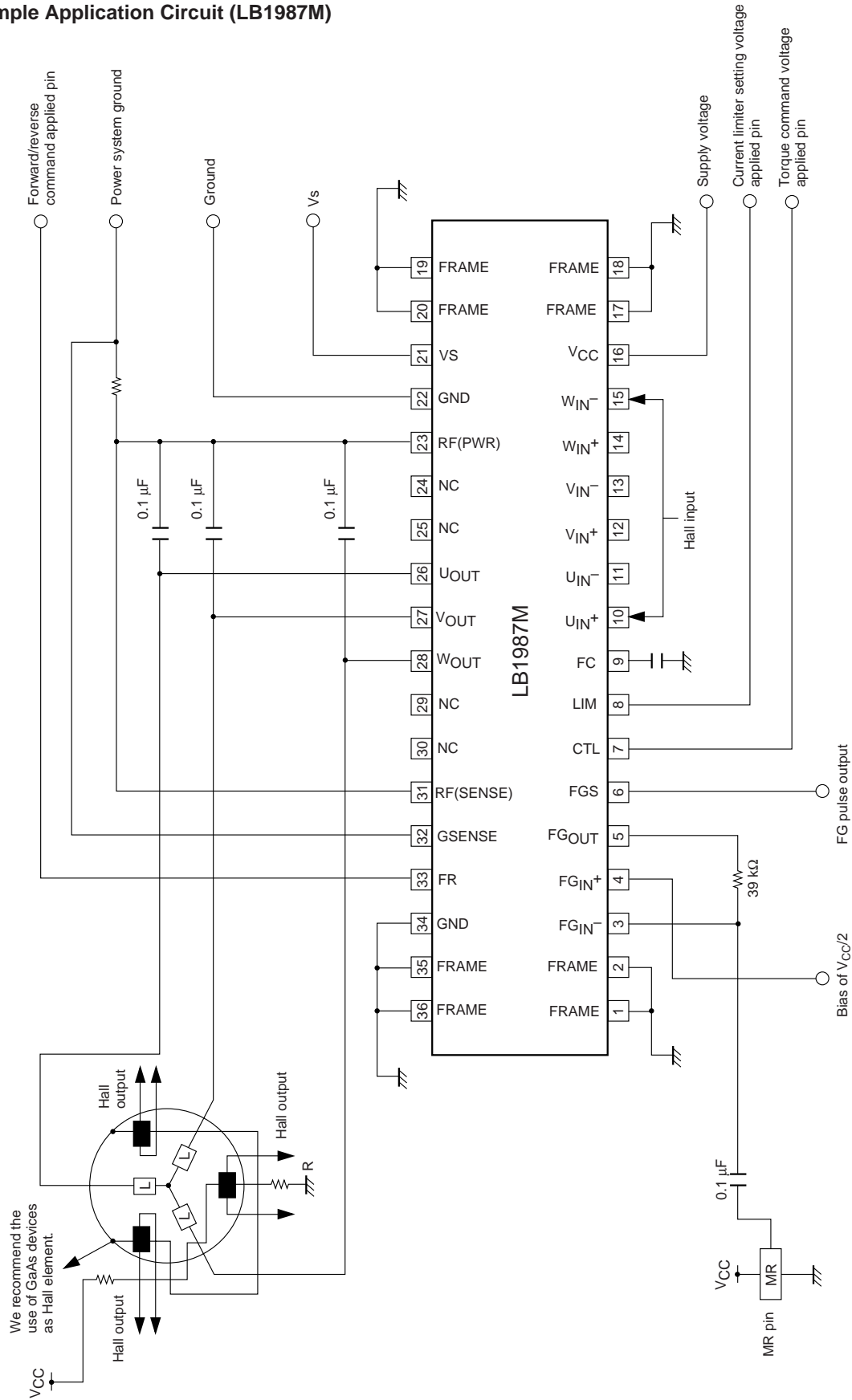
Sample Application Circuit (LB1987D)



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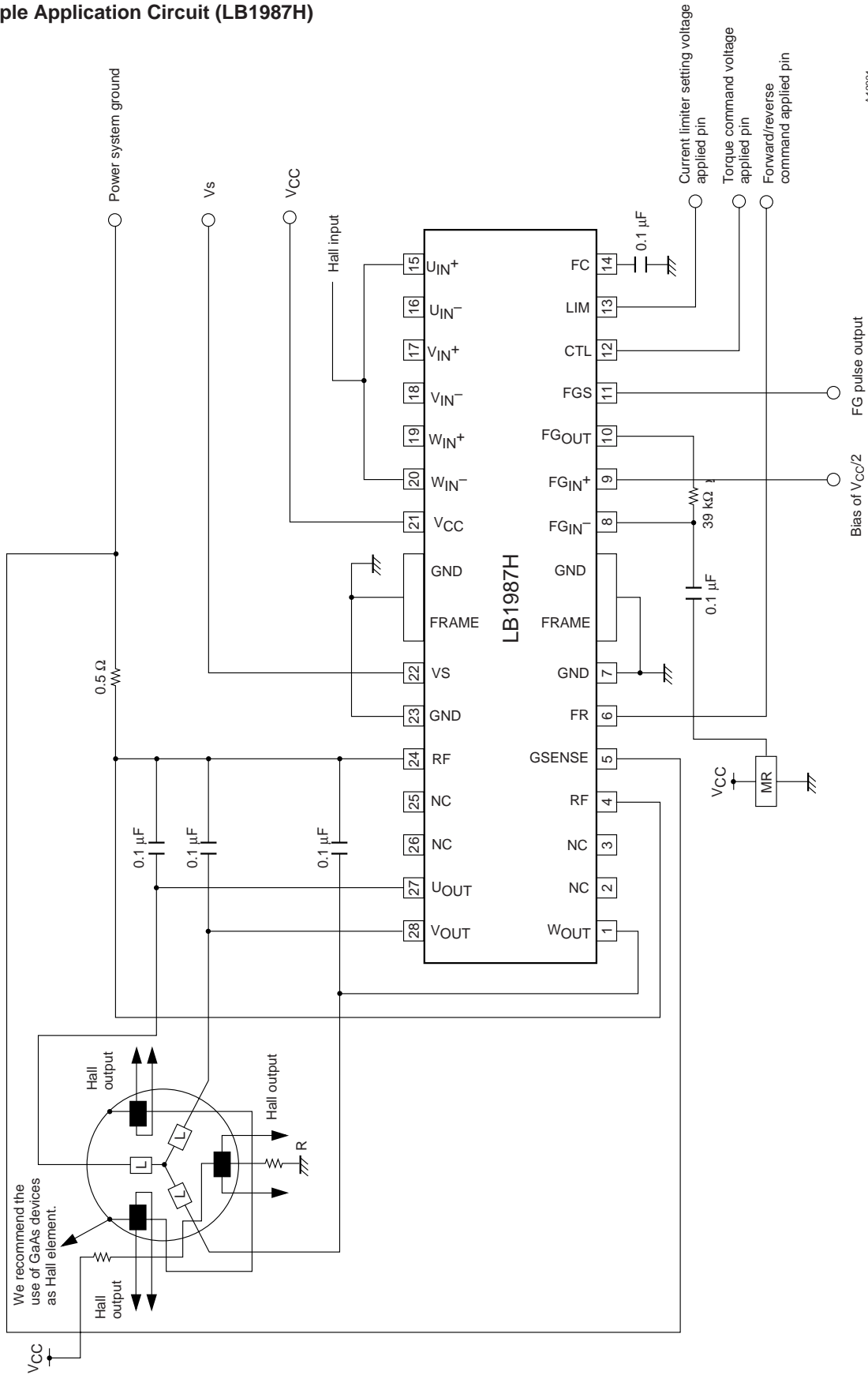
Note: The component values shown in this application circuit example are merely provided as examples, and circuit operating characteristics are not guaranteed.

Sample Application Circuit (LB1987M)



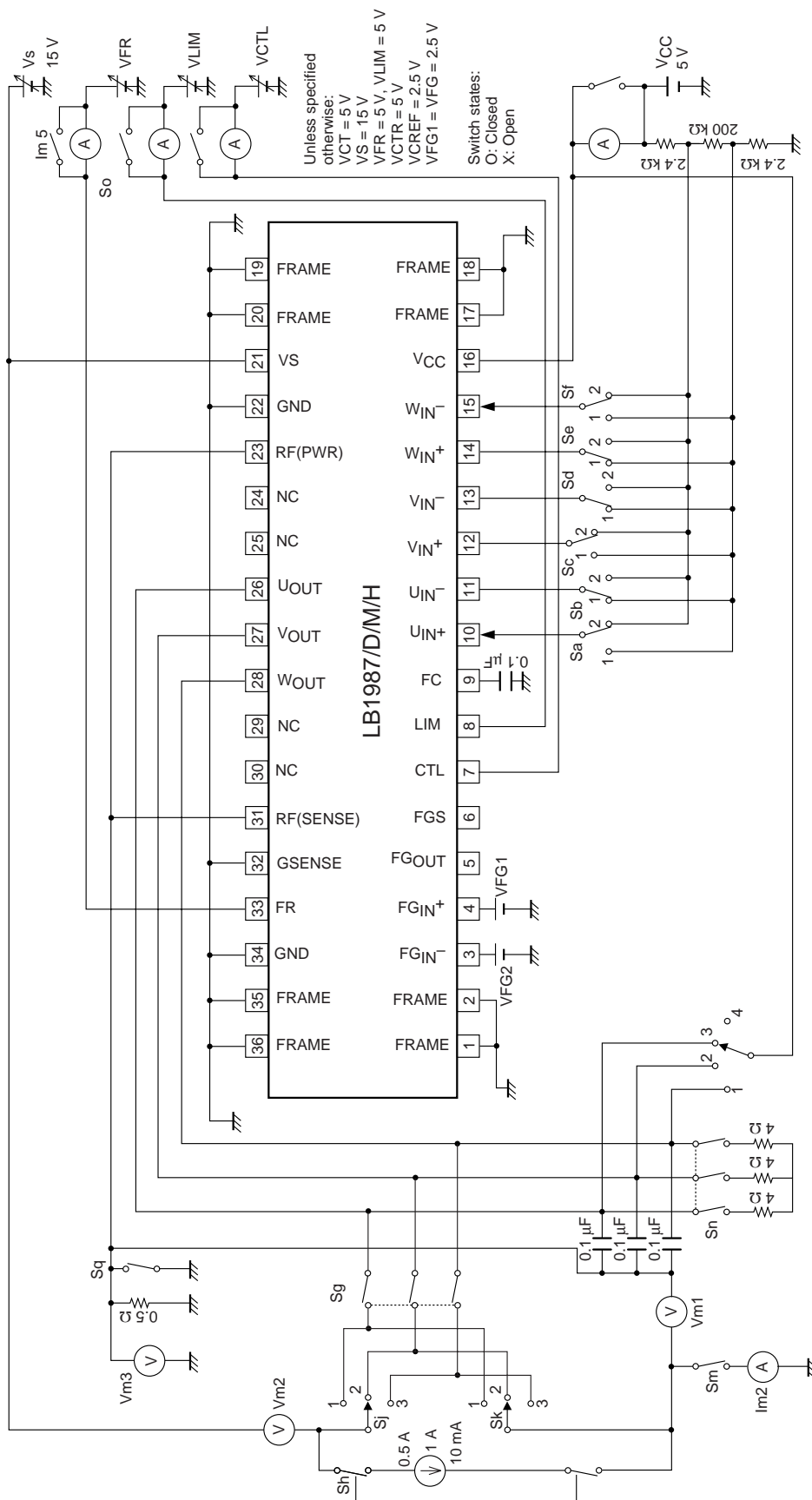
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Sample Application Circuit (LB1987H)



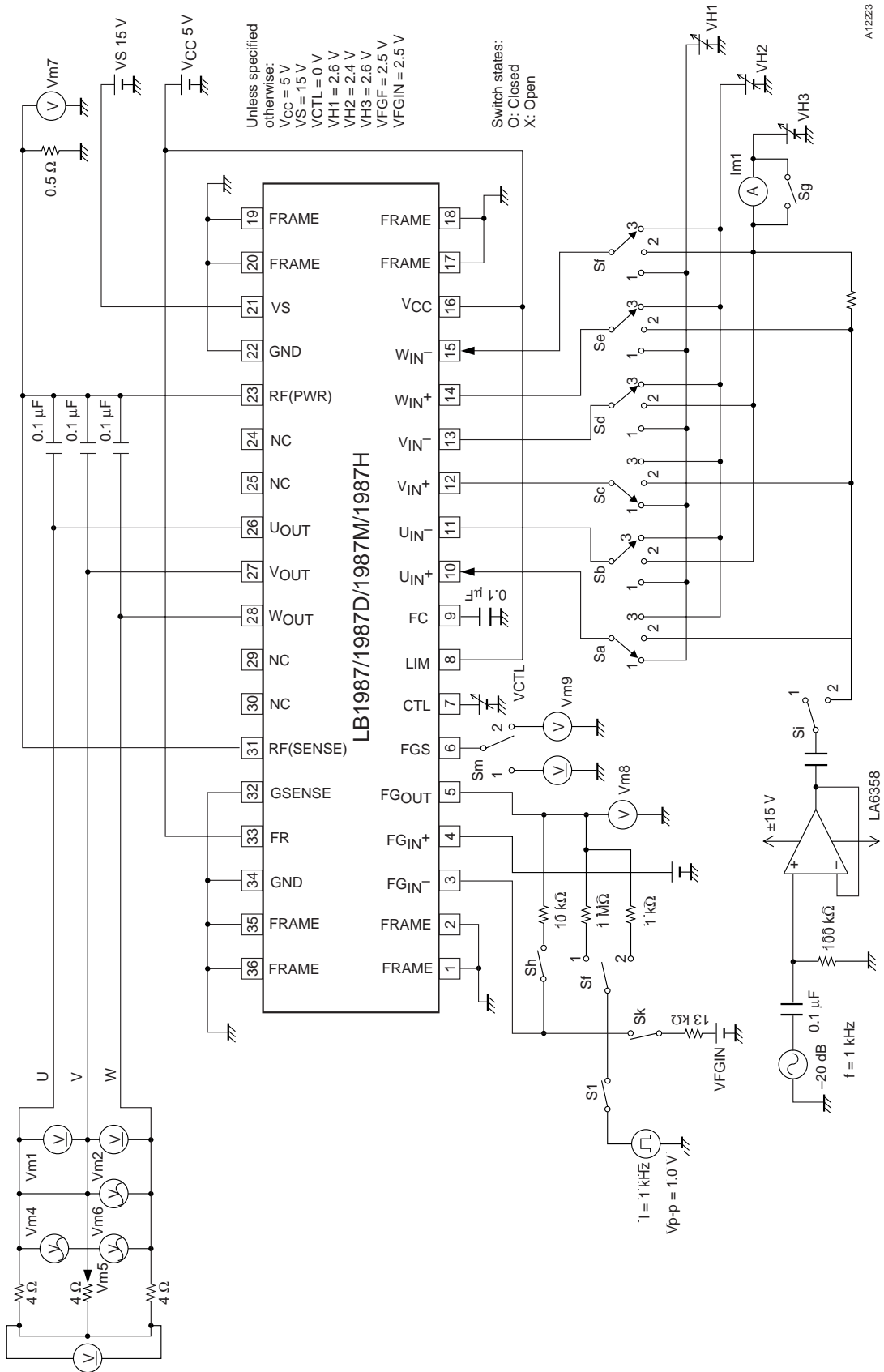
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Test Circuit 1



A12222

Test Circuit 2



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