Omnidirectional Microphone with Bottom Port and I²S Digital Output

Data Sheet

ADMP441

FEATURES

- Digital I²S interface with high precision 24-bit data
- High SNR of 61 dBA
- High sensitivity of −26 dBFS
- Flat frequency response from 60 Hz to 15 kHz
- Low current consumption of 1.4 mA
- High PSR of −75 dBFS
- Small 4.72 mm × 3.76 mm × 1 mm surface-mount package
- Compatible with Sn/Pb and Pb-free solder processes
- RoHS/WEEE compliant

APPLICATIONS

- Teleconferencing systems
- Gaming consoles
- Mobile devices
- Laptops
- Tablets
- Security systems

FUNCTIONAL BLOCK DIAGRAM

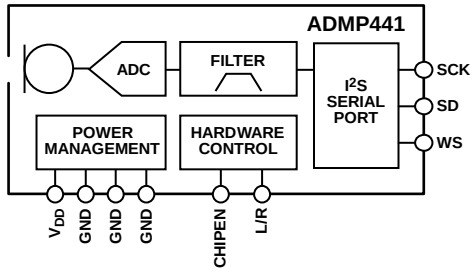

Figure 1.

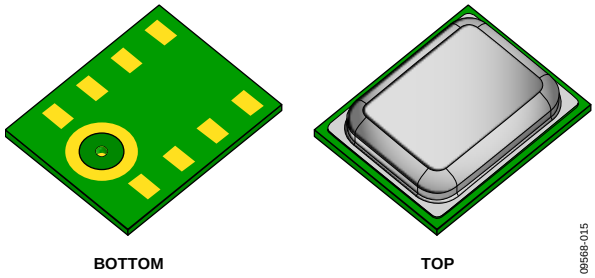

Figure 2. Isometric Views of ADMP441 Microphone Package

GENERAL DESCRIPTION

The ADMP441[1] is a high performance, low power, digital output, omnidirectional MEMS microphone with a bottom port. The complete ADMP441 solution consists of a MEMS sensor, signal conditioning, an analog-to-digital converter, antialiasing filters, power management, and an industry standard 24-bit I²S interface. The I²S interface allows the ADMP441 to connect directly to digital processors, such as DSPs and microcontrollers, without the need for an audio codec in the system.

The ADMP441 has a high SNR and high sensitivity, making it an excellent choice for far field applications. The ADMP441 has a flat wideband frequency response, resulting in natural sound with high intelligibility.

The ADMP441 is available in a thin 4.72 mm × 3.76 mm × 1 mm surface-mount package. It is reflow solder compatible with no sensitivity degradation. The ADMP441 is halide free.

[1] Protected by U.S. Patents 7,449,356; 7,825,484; 7,885,423; and 7,961,897. Other patents are pending.

Rev. B
Document Feedback

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10/11—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, V_{DD} = 2.4 V, SCK = 3.072 MHz, SPL = 104 dB (3.16 Pa rms), unless otherwise noted. All minimum and maximum specifications are guaranteed. Typical specifications are not guaranteed.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
PERFORMANCE						
Directionality				Omni		
Sensitivity at 94 dB SPL[1]		1 kHz, 104 dB SPL	−29	−26	−23	dBFS
Signal-to-Noise Ratio	SNR	20 kHz bandwidth, A-weighted		61		dBA
Equivalent Input Noise	EIN	20 kHz bandwidth, A-weighted		33		dBA SPL
Dynamic Range		Derived from EIN and maximum acoustic input		87		dB
Frequency Response[2]		Low frequency –3 dB point		60		Hz
		High frequency –3 dB point		15		kHz
		Deviation limits from flat response within pass band		−3/+2		dB
Total Harmonic Distortion	THD	104 dB SPL			3	%
Power Supply Rejection	PSR	217 Hz, 100 mV p-p square wave superimposed on V_{DD}		−75		dBFS
Maximum Acoustic Input		Peak		120		dB SPL
Noise Floor		20 Hz to 20 kHz, A-weighted, rms		−87		dBFS
POWER SUPPLY						
Supply Voltage	V_{DD}		1.8		3.3	V
Supply Current	I_{DD}					
V_{DD} = 1.8 V						
Normal Mode				1.4	1.6	mA
Standby					0.8	mA
Power-Down					2	µA
V_{DD} = 3.3 V						
Normal Mode				2.2	2.5	mA
Standby					0.8	mA
Power-Down					4.5	µA
DIGITAL FILTER						
Group Delay				17.25/f_S		sec
		f_S = 48 kHz		359		µs
		f_S = 16 kHz		1078		µs
Pass-Band Ripple					±0.04	dB
Stop-Band Attenuation				60		dB
Pass Band		0.423 × f_S		20.3		kHz

[1] The peak-to-peak amplitude is relative to peak-to-peak amplitude of 2^{24} – 1. The stimulus is a 104 dB SPL sinusoid having rms amplitude of 3.1623 Pa. Sensitivity is relative to 1 Pa.
[2] See Figure 6 and Figure 8.

I²S DIGITAL INPUT/OUTPUT

$-40°C < T_A < +85°C$, $1.8\ V < V_{DD} < 3.3\ V$, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Limit[1] Min	Limit[1] Max	Unit
DIGITAL INPUT					
Voltage Input Low (L/R, WS, SCK)	V_{IL}		0	$0.25 \times V_{DD}$	V
Voltage Input High (L/R, WS, SCK)	V_{IH}		$0.7 \times V_{DD}$	V_{DD}	V
SD DIGITAL OUTPUT					
Voltage Output Low	V_{OL}	$V_{DD} = 1.8\ V$, $I_{SINK} = 0.25\ mA$		$0.1 \times V_{DD}$	V
Voltage Output Low	V_{OL}	$V_{DD} = 1.8\ V$, $I_{SINK} = 0.7\ mA$		$0.3 \times V_{DD}$	V
Voltage Output High	V_{OH}	$V_{DD} = 1.8\ V$, $I_{SINK} = 0.7\ mA$	$0.7 \times V_{DD}$		V
Voltage Output High	V_{OH}	$V_{DD} = 1.8\ V$, $I_{SINK} = 0.25\ mA$	$0.9 \times V_{DD}$		V
Voltage Output Low	V_{OL}	$V_{DD} = 3.3\ V$, $I_{SINK} = 0.5\ mA$		$0.1 \times V_{DD}$	V
Voltage Output Low	V_{OL}	$V_{DD} = 3.3\ V$, $I_{SINK} = 1.7\ mA$		$0.3 \times V_{DD}$	V
Voltage Output High	V_{OH}	$V_{DD} = 3.3\ V$, $I_{SINK} = 1.7\ mA$	$0.7 \times V_{DD}$		V
Voltage Output High	V_{OH}	$V_{DD} = 3.3\ V$, $I_{SINK} = 0.5\ mA$	$0.9 \times V_{DD}$		V

[1] Limits based on characterization results; not production tested.

Table 3. Serial Data Port Timing Specifications

Parameter	Description	Min	Max	Unit
t_{SCH}	SCK high	50		ns
t_{SCL}	SCK low	50		ns
t_{SCP}	SCK period	312		ns
f_{SCK}	SCK frequency	0.5	3.2	MHz
t_{WSS}	WS setup	0		ns
t_{WSH}	WS hold	20		ns
f_{WS}	WS frequency	7.8	49.3	kHz

TIMING DIAGRAM

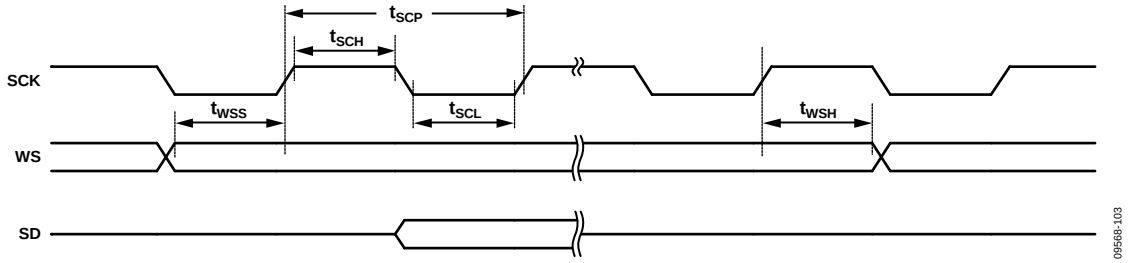


Figure 3. Serial Data Port Timing

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage (V_{DD})	−0.3 V to +3.6 V
Sound Pressure Level	160 dB
Mechanical Shock	10,000 *g*
Vibration	Per MIL-STD-883 Method 2007, Test Condition B
Operating Temperature Range	−40°C to +85°C
Digital Pin Input Voltage	−0.3 V to V_{DD} + 0.3 V or 3.6 V, whichever is less

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

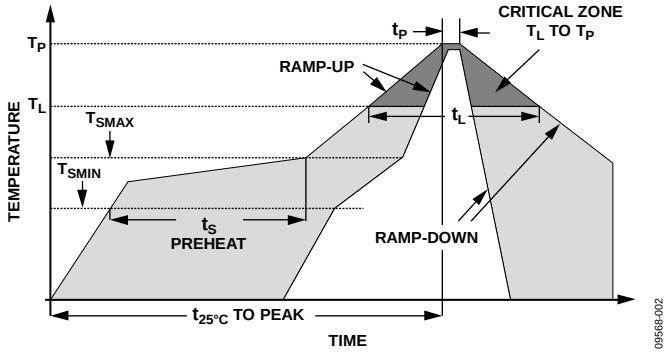


Figure 4. Recommended Soldering Profile Limits

Table 5. Recommended Soldering Profile Limits

Profile Feature	Sn63/Pb37	Pb-Free
Average Ramp Rate (T_L to T_P)	1.25°C/sec max	1.25°C/sec max
Preheat		
Minimum Temperature (T_{SMIN})	100°C	100°C
Maximum Temperature (T_{SMAX})	150°C	200°C
Time (T_{SMIN} to T_{SMAX}), t_S	60 sec to 75 sec	60 sec to 75 sec
Ramp-Up Rate (T_{SMAX} to T_L)	1.25°C/sec	1.25°C/sec
Time Maintained Above Liquidous (t_L)	45 sec to 75 sec	~50 sec
Liquidous Temperature (T_L)	183°C	217°C
Peak Temperature (T_P)	215°C +3°C/−3°C	260°C +0°C/−5°C
Time Within 5°C of Actual Peak Temperature (t_P)	20 sec to 30 sec	20 sec to 30 sec
Ramp-Down Rate	3°C/sec max	3°C/sec max
Time 25°C ($t_{25°C}$) to Peak Temperature	5 minute max	5 minute max

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

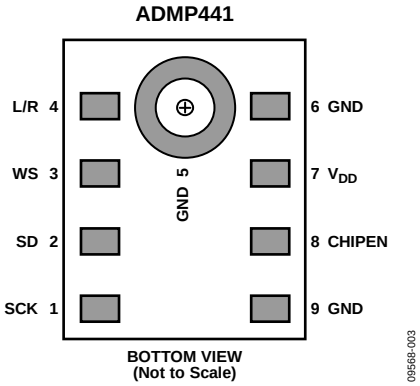


Figure 5. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1	SCK	Input	Serial Data Clock for I²S Interface.
2	SD	Output	Serial Data Output for I²S Interface. This pin tristates when not actively driving the appropriate output channel. The SD trace should have a 100 kΩ pull-down resistor to discharge the line during the time that all microphones on the bus have tristated their outputs.
3	WS	Input	Serial Data-Word Select for I²S Interface.
4	L/R	Input	Left/Right Channel Select. When set low, the microphone outputs its signal in the left channel of the I²S frame; when set high, the microphone outputs its signal in the right channel.
5	GND	Ground	Ground. Connect to ground on the PCB.
6	GND	Ground	Ground. Connect to ground on the PCB.
7	V_{DD}	Power	Power, 1.8 to 3.3 V. This pin should be decoupled to Pin 6 with a 0.1 µF capacitor.
8	CHIPEN	Input	Microphone Enable. When set low (ground), the microphone is disabled and put in power-down mode. When set high (V_{DD}), the microphone is enabled.
9	GND	Ground	Ground. Connect to ground on the PCB.

TYPICAL PERFORMANCE CHARACTERISTICS

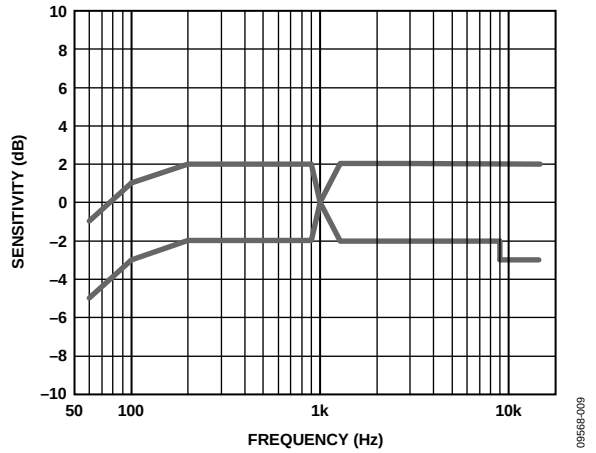


Figure 6. Frequency Response Mask

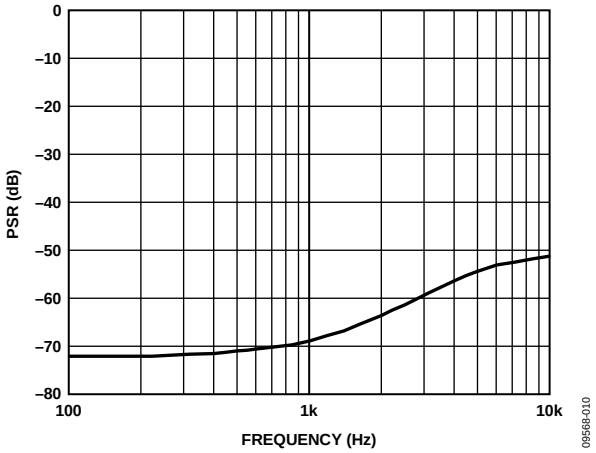


Figure 7. Typical Power Supply Rejection vs. Frequency

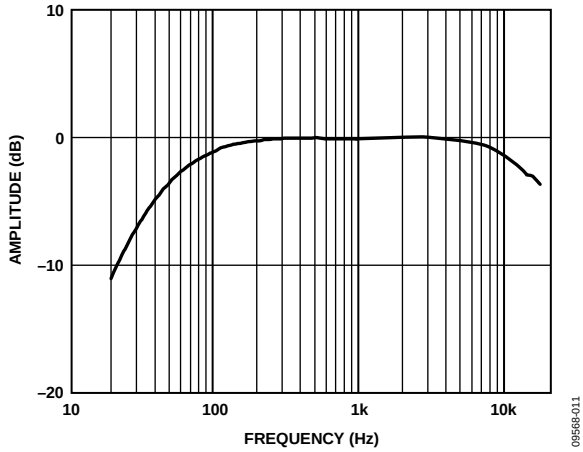


Figure 8. Typical Frequency Response (Measured)

THEORY OF OPERATION

The ADMP441 is a high performance, low power, digital output, omnidirectional MEMS microphone with a bottom port. The complete ADMP441 solution consists of a MEMS sensor, signal conditioning, an analog-to-digital converter, anti-aliasing filters, power management, and an industry standard 24-bit I²S interface.

The ADMP441 complies with the TIA-920 *Telecommunications Telephone Terminal Equipment Transmission Requirements for Wideband Digital Wireline Telephones* standard.

UNDERSTANDING SENSITIVITY

The casual user of digital microphones may have difficulty understanding the sensitivity specification. Unlike an analog microphone (whose specification is easily confirmed with an oscilloscope), the digital microphone output has no obvious unit of measure.

The ADMP441 has a nominal sensitivity of −26 dBFS at 1 kHz with an applied sound pressure level of 94 dB. The units are in decibels referred to full scale. The ADMP441 default full-scale peak output word is $2^{23} - 1$ (integer representation), and −26 dBFS of that scale is $(2^{23} - 1) \times 10^{(-26/20)} = 420{,}426$. A pure acoustic tone at 1 kHz having a 1 Pa rms amplitude results in an output digital signal whose peak amplitude is 420,426.

Although the industry uses a standard specification of 94 dB SPL, the ADMP441 test method applies a 104 dB SPL signal. The higher sound pressure level reduces noise and improves repeatability. The ADMP441 has excellent gain linearity, and the sensitivity test result at 94 dB is derived with very high confidence from the test data.

POWER MANAGEMENT

The ADMP441 has three different power states: normal operation, standby mode, and power-down mode.

Normal Operation

The microphone becomes operational 2^{18} clock cycles (85 ms with SCK at 3.072 MHz) after initial power-up. The CHIPEN pin then controls the power modes. The part is in normal operation mode when SCK is active and the CHIPEN pin is high.

Standby Mode

The microphone enters standby mode when the serial data clock SCK stops and CHIPEN is high. Normal operation resumes 2^{14} clock cycles (5 ms with SCK at 3.072 MHz) after SCK restarts.

The ADMP441 should not be transitioned from standby to power-down mode, or vice versa. Standby mode is only intended to be entered from the normal operation state.

Power-Down Mode

The microphone enters power-down mode when CHIPEN is low, regardless of the SCK operation. Normal mode operation resumes 2^{17} SCK clock cycles (43 ms with SCK at 3.072 MHz) after CHIPEN returns high while SCK is active.

It always takes 2^{17} clock cycles to restart the ADMP441 after V_{DD} is applied.

It is not recommended to supply active clocks (WS and SCK) to the ADMP441 while there is no power supplied to V_{DD}. Doing this continuously turns on ESD protection diodes, which may affect long-term reliability of the microphone.

STARTUP

The microphones have zero output for the first 2^{18} SCK clock cycles (85 ms with SCK at 3.072 MHz) following power-up.

I²S DATA INTERFACE

The slave serial data port's format is I²S, 24-bit, twos complement. There must be 64 SCK cycles in each WS stereo frame, or 32 SCK cycles per data-word. The L/R control pin determines whether the ADMP441 outputs data in the left or right channel. For a stereo application, the SD pins of the left and right ADMP441 microphones should be tied together as shown in Figure 9. The format of a stereo I²S data stream is shown in Figure 10. Figure 11 and Figure 12 show the formats of a mono microphone data stream for left and right microphones, respectively.

Data Output Mode

The output data pin (SD) is tristated when it is not actively driving I²S output data. SD immediately tristates after the LSB is output so that another microphone can drive the common data line.

The SD trace should have a pull-down resistor to discharge the line during the time that all microphones on the bus have tristated their outputs. A 100 kΩ resistor is sufficient for this, as shown in Figure 9.

Data-Word Length

The output data-word length is 24 bits per channel. The ADMP441 must always have 64 clock cycles for every stereo data-word ($f_{SCK} = 64 \times f_{WS}$).

Data-Word Format

The default data format is I²S (twos complement), MSB-first. In this format, the MSB of each word is delayed by one SCK cycle from the start of each half-frame.

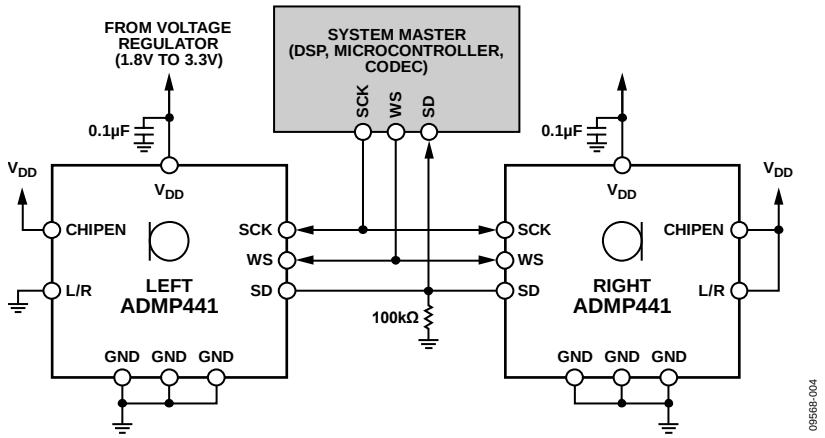


Figure 9. System Block Diagram

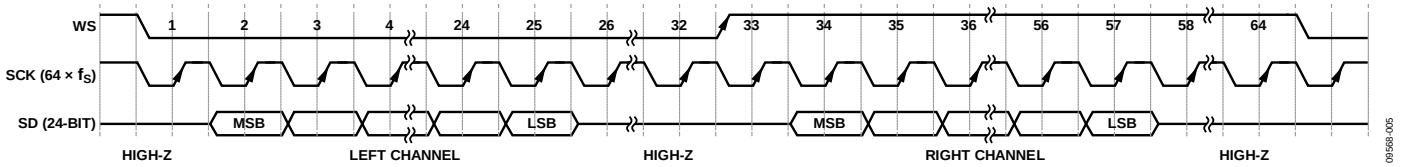


Figure 10. Stereo Output I²S Format

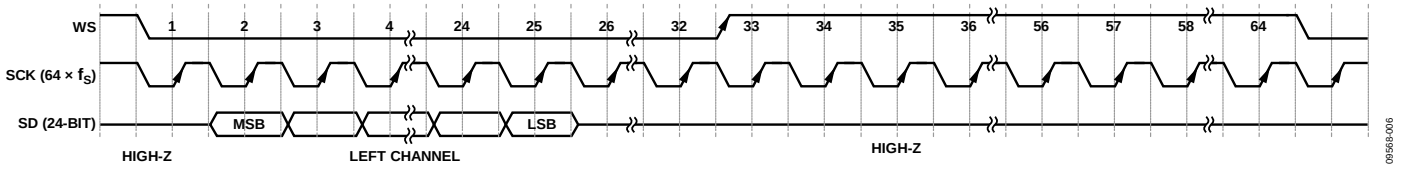


Figure 11. Mono Output I²S Format Left Channel (L/R = 0)

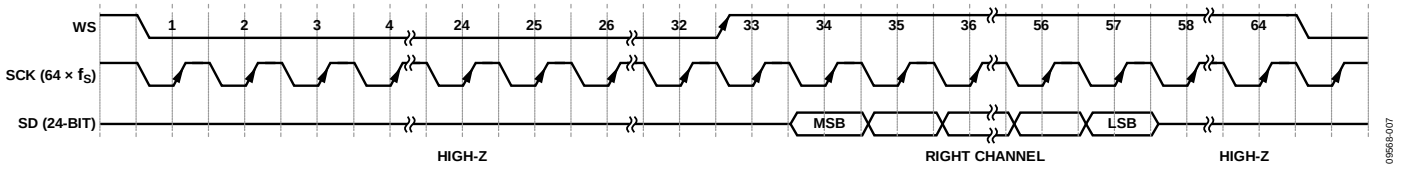


Figure 12. Mono Output I²S Format Right Channel (L/R = 1)

DIGITAL FILTER CHARACTERISTICS

The ADMP441 has an internal digital band-pass filter. A high-pass filter eliminates unwanted low frequency signals. A low-pass filter allows the user to scale the pass band with the sampling frequency as well as perform required noise reduction.

High-Pass Filter

The ADMP441 incorporates a high-pass filter to remove unwanted dc and very low frequency components. Table 7 shows the high-pass characteristics for a nominal sampling rate of 48 kHz. The cutoff frequency scales with changes in sampling rate.

Table 7. High-Pass Filter Characteristics

Frequency	Attenuation
3.7 Hz	−3.0 dB
10.4 Hz	−0.5 dB
21.6 Hz	−0.1 dB

This digital filter response is in addition to the natural high-pass response of the ADMP441 MEMS acoustic transducer that has a −3 dB cutoff of 60 Hz.

Low-Pass Filter

The analog-to-digital converter in the ADMP441 is a single-bit, high order, sigma-delta (Σ-Δ) running at a high oversampling ratio. The noise shaping of the converter pushes the majority of the noise well above the audio band and gives the microphone a wide dynamic range. However, it does require a good quality low-pass filter to eliminate the high frequency noise.

Figure 13 shows the response of this digital low-pass filter included in the microphone. The pass band of the filter extends to 0.423 × f_S and, in that band, has an unnoticeable 0.04 dB of ripple. The high frequency cutoff of −6 dB occurs at 0.5 × f_S. A 48 kHz sampling rate results in a pass band of 20.3 kHz and a half amplitude corner at 24 kHz; the stop-band attenuation of the filter is greater than 60 dB. Note that these filter specifications scale with sampling frequency.

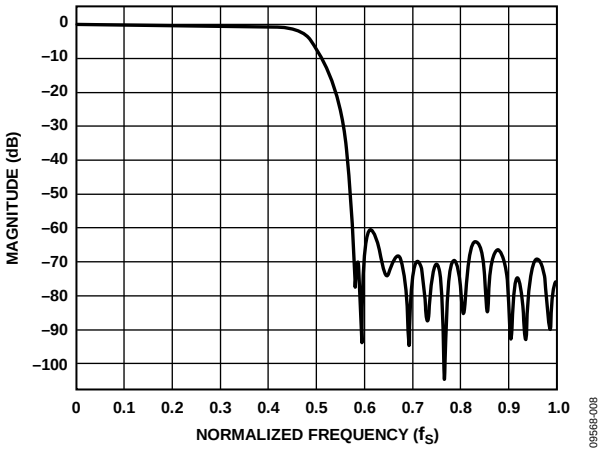


Figure 13. Digital Low-Pass Filter Magnitude Response

APPLICATIONS INFORMATION

POWER SUPPLY DECOUPLING

For best performance and to avoid potential parasitic artifacts, placing a 0.1 µF ceramic type X7R or better capacitor between Pin 7 (V_{DD}) and ground is strongly recommended. The capacitor should be placed as close to Pin 7 as possible.

The connections to each side of the capacitor should be as short as possible, and the trace should stay on a single layer with no vias. For maximum effectiveness, locate the capacitor equidistant from the power and ground pins or, when equidistant placement is not possible, slightly closer to the power pin. Thermal connections to the ground planes should be made on the far side of the capacitor, as shown in Figure 14.

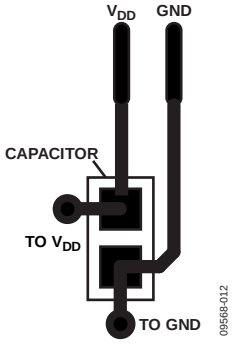


Figure 14. Recommended Power Supply Bypass Capacitor Layout

HANDLING INSTRUCTIONS

Pick-and-Place Equipment

The MEMS microphone can be handled using standard pick-and-place and chip shooting equipment. Care should be taken to avoid damage to the MEMS microphone structure as follows:

- Use a standard pickup tool to handle the microphone. Because the microphone hole is on the bottom of the package, the pickup tool can make contact with any part of the lid surface.
- Do not pick up the microphone with a vacuum tool that makes contact with the bottom side of the microphone. Do not pull air out of or blow air into the microphone port.
- Do not use excessive force to place the microphone on the PCB.

Reflow Solder

For best results, the soldering profile should be in accordance with the recommendations of the manufacturer of the solder paste used to attach the MEMS microphone to the PCB. It is recommended that the solder reflow profile does not exceed the limit conditions specified in Figure 4 and Table 5.

Board Wash

When washing the PCB, ensure that water does not make contact with the microphone port. Blow-off procedures and ultrasonic cleaning must not be used.

SUPPORTING DOCUMENTATION

Evaluation Board User Guide

UG-303, *EVAL-ADMP441Z-FLEX: Bottom-Port I²S Output MEMS Microphone Evaluation Board*

UG-362, *EVAL-ADMP441Z SDP Daughter Board for the ADMP441 I²S MEMS Microphone*

Circuit Note

CN-0208, *High Performance Digital MEMS Microphone's Simple Interface to SigmaDSP Audio Processor with I²S Output*

CN-0266, *High Performance Digital MEMS Microphone Standard Digital Audio Interface to Blackfin DSP*

Application Notes

AN-1003 Application Note, *Recommendations for Mounting and Connecting Analog Devices, Inc., Bottom-Ported MEMS Microphones*

AN-1068 Application Note, *Reflow Soldering of the MEMS Microphone*

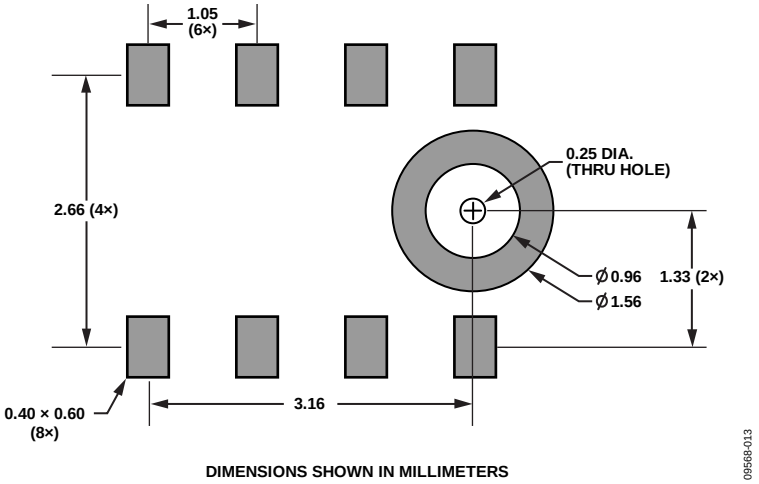
AN-1112 Application Note, *Microphone Specifications and Terms Explained*

AN-1124 Application Note, *Recommendations for Sealing Analog Devices, Inc., Bottom-Port MEMS Microphones from Dust and Liquid Ingress*

AN-1140 Application Note, *Microphone Array Beamfoaming*

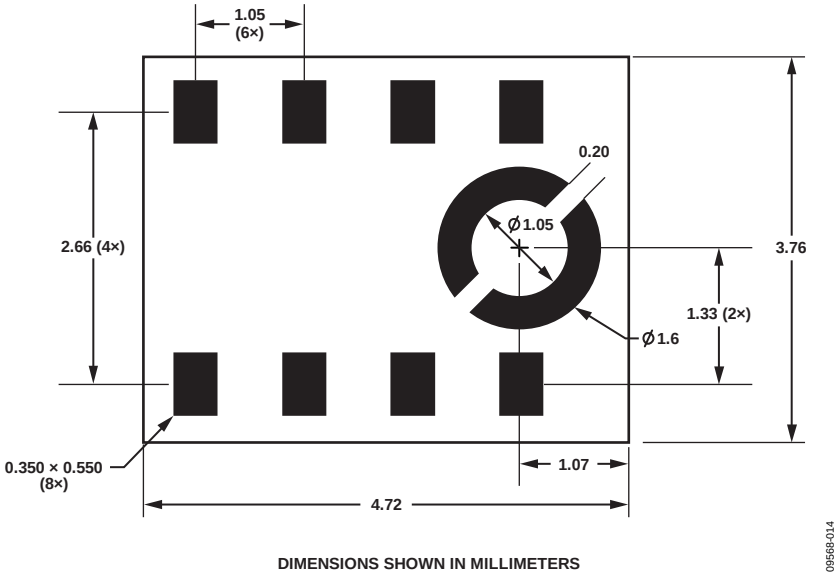
For additional information, visit www.analog.com/mic.

LAYOUT AND DESIGN RECOMMENDATIONS



DIMENSIONS SHOWN IN MILLIMETERS

Figure 15. Recommended Printed Circuit Board Land Pattern
(Dimensions shown in millimeters)



DIMENSIONS SHOWN IN MILLIMETERS

Figure 16. Recommended Printed Circuit Board Solder Paste Mask Pattern
(Dimensions shown in millimeters)

OUTLINE DIMENSIONS

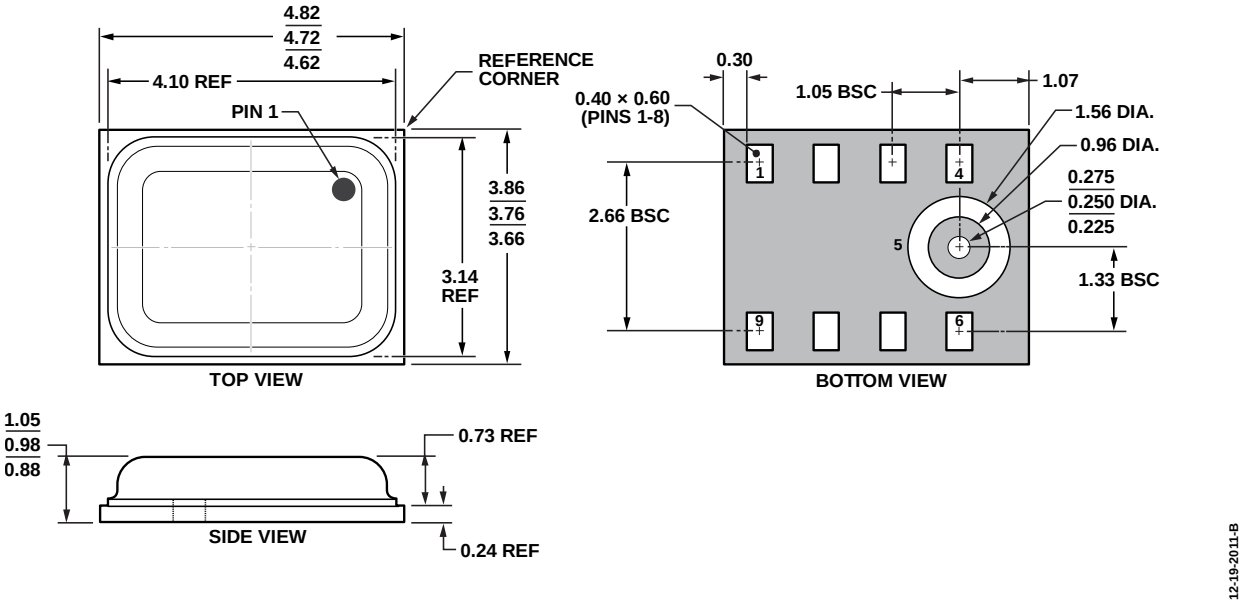


Figure 17. 9-Terminal Chip Array Small Outline No Lead Cavity [LGA_CAV]
4.72 mm × 3.76 mm × 1 mm Body
(CE-9-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option[2]	Ordering Quantity
ADMP441ACEZ-RL	−40°C to +85°C	9-Terminal LGA_CAV, 13″ Tape and Reel	CE-9-1	4,500
ADMP441ACEZ-RL7	−40°C to +85°C	9-Terminal LGA_CAV, 7″ Tape and Reel	CE-9-1	1,000
EVAL-ADMP441Z		Evaluation Board		
EVAL-ADMP441Z-FLEX		Flex Evaluation Board		

[1] Z = RoHS Compliant Part.
[2] This package option is halide-free.

NOTES

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