



1Gb NAND FLASH

HY27US081G1M

HY27US161G1M

This document is a general product description and is subject to change without notice. Hynix does not assume any responsibility for use of circuits described. No patent licenses are implied.

Rev 0.2 / May. 2007



Document Title
1Gbit (128Mx8bit / 64Mx16bit) NAND Flash Memory

Revision History

Revision No.	History	Draft Date	Remark																											
0.01	Initial Draft.	Nov. 11. 2005	Preliminary																											
0.02	1) Delete PRE pin. 2) Delete Lock mechanism. 3) Delete FBGA Package. - Figure & dimension are changed.	Dec. 01. 2005	Preliminary																											
0.03	1) Change DC characteristics (Table 8) <table border="1"><thead><tr><th rowspan="2"></th><th colspan="2">Icc1</th><th colspan="2">Icc2</th><th colspan="2">Icc3</th></tr><tr><th>Typ</th><th>Max</th><th>Typ</th><th>Max</th><th>Typ</th><th>Max</th></tr></thead><tbody><tr><td>Before</td><td>15</td><td>30</td><td>15</td><td>30</td><td>15</td><td>30</td></tr><tr><td>After</td><td>10</td><td>20</td><td>10</td><td>20</td><td>10</td><td>20</td></tr></tbody></table>		Icc1		Icc2		Icc3		Typ	Max	Typ	Max	Typ	Max	Before	15	30	15	30	15	30	After	10	20	10	20	10	20	Dec. 14. 2005	Preliminary
	Icc1		Icc2		Icc3																									
	Typ	Max	Typ	Max	Typ	Max																								
Before	15	30	15	30	15	30																								
After	10	20	10	20	10	20																								
0.04	1) Add ECC algorithm. (1bit/512bytes) 2) Correct Read ID Cycle & Read ID naming 3) Correct Copy back program 4) Change DC and Operating Characteristics	Mar. 28. 2006	Preliminary																											
0.1	1) Correct Read ID Cycle 2) Change NOP 3) Correct copy back function	Oct. 02. 2006	Preliminary																											
0.2	1) Correct figure 32.	May. 18. 2007	Preliminary																											

FEATURES SUMMARY

HIGH DENSITY NAND FLASH MEMORIES

- Cost effective solutions for mass storage applications

NAND INTERFACE

- x8 or x16 bus width.
- Multiplexed Address/ Data
- Pinout compatibility for all densities

SUPPLY VOLTAGE

- VCC = 2.7 to 3.6V : HY27USxx1G1M

Memory Cell Array

- = (512+16) Bytes x 32 Pages x 8,192 Blocks
- = (256+8) Words x 32 Pages x 8,192 Blocks

PAGE SIZE

- x8 device : (512 + 16 spare) Bytes
 : HY27US081G1M
- x16 device : (256+ 8 spare) Words
 : HY27US161G1M

BLOCK SIZE

- x8 device: (16K + 512 spare) Bytes
- x16 device: (8K + 256 spare) Words

PAGE READ / PROGRAM

- Random access: 15us (max.)
- Sequential access: 50ns (min.)
- Page program time: 200us (typ.)

COPY BACK PROGRAM MODE

- Fast page copy without external buffering

FAST BLOCK ERASE

- Block erase time: 2ms (Typ.)

STATUS REGISTER

ELECTRONIC SIGNATURE

- 1st cycle : Manufacturer Code
- 2nd cycle : Device Code
- 3rd cycle: Internal chip number, Cell Type, Number of Simultaneously Programmed Pages.
- 4th cycle: Page size, Block size, Organization, Spare size

CHIP ENABLE DON'T CARE OPTION

- Simple interface with microcontroller

AUTOMATIC PAGE 0 READ AT POWER-UP OPTION

- Boot from NAND support
- Automatic Memory Download

SERIAL NUMBER OPTION

HARDWARE DATA PROTECTION

- Program/Erase locked during Power transitions

DATA INTEGRITY

- 100,000 Program/Erase cycles (with 4bit/528byte ECC)
- 10 years Data Retention

PACKAGE

- HY27US(08/16)1G1M-T(P)
 - : 48-Pin TSOP1 (12 x 20 x 1.2 mm)
 - HY27US(08/16)1G1M-T (Lead)
 - HY27US(08/16)1G1M-TP (Lead Free)
- HY27US081G1M-S(P)
 - : 48-Pin USOP1 (12 x 17 x 0.65 mm)
 - HY27US081G1M-S (Lead)
 - HY27US081G1M-SP (Lead Free)

1. SUMMARY DESCRIPTION

The HYNIX HY27US(08/16)1G1M series is a 128Mx8bit with spare 4Mx8 bit capacity. The device is offered in 3.3V Vcc Power Supply.

Its NAND cell provides the most cost-effective solution for the solid state mass storage market.

The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased.

The device contains 8192 blocks, composed by 32 pages consisting in two NAND structures of 16 series connected Flash cells.

A program operation allows to write the 512-byte page in typical 200us and an erase operation can be performed in typical 2ms on a 16Kbyte(X8 device) block.

Data in the page mode can be read out at 50ns cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command input. This interface allows a reduced pin count and easy migration towards different densities, without any rearrangement of footprint.

Commands, Data and Addresses are synchronously introduced using \overline{CE} , \overline{WE} , ALE and CLE input pin.

The on-chip Program/Erase Controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data.

The modifying can be locked using the \overline{WP} input pin.

The output pin R/B (open drain buffer) signals the status of the device during each operation. In a system with multiple memories the R/B pins can be connected all together to provide a global status signal.

Even the write-intensive systems can take advantage of the HY27US(08/16)1G1M extended reliability of 100K program/erase cycles by providing ECC (Error Correcting Code) with real time mapping-out algorithm.

Optionally the chip could be offered with the \overline{CE} don't care function. This option allows the direct download of the code from the NAND Flash memory device by a microcontroller, since the \overline{CE} transitions do not stop the read operation.

The copy back function allows the optimization of defective blocks management: when a page program operation fails the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase.

The HYNIX HY27US(08/16)1G1M series is available in 48 - TSOP1 12x20 mm, 48 - USOP1 12 x 17 mm.

1.1 Product List

PART NUMBER	ORIZATION	VCC RANGE	PACKAGE
HY27US081G1M	x8	2.7V - 3.6 Volt	48TSOP1 / 48USOP1
HY27US161G1M	x16		

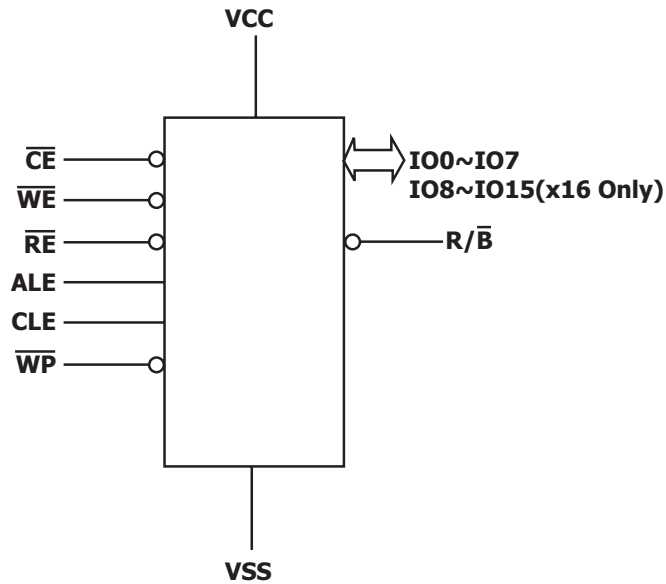


Figure1: Logic Diagram

IO15 - IO8	Data Inputs / Outputs (x16 Only)
IO7 - IO0	Data Inputs / Outputs
CLE	Command latch enable
ALE	Address latch enable
\overline{CE}	Chip Enable
\overline{RE}	Read Enable
\overline{WE}	Write Enable
\overline{WP}	Write Protect
R/ \overline{B}	Ready / Busy
Vcc	Power Supply
Vss	Ground
NC	No Connection

Table 1: Signal Names

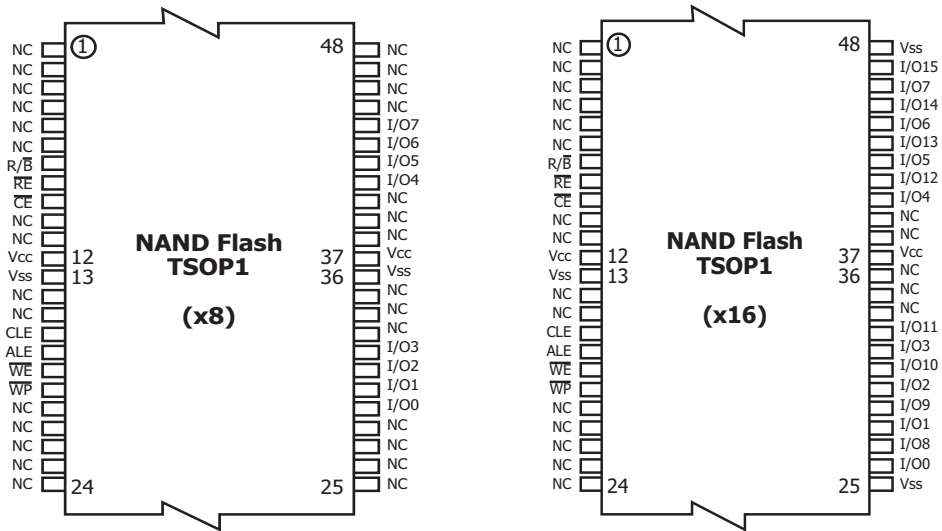


Figure 2. 48TSOP1 Contactions, x8 and x16 Device

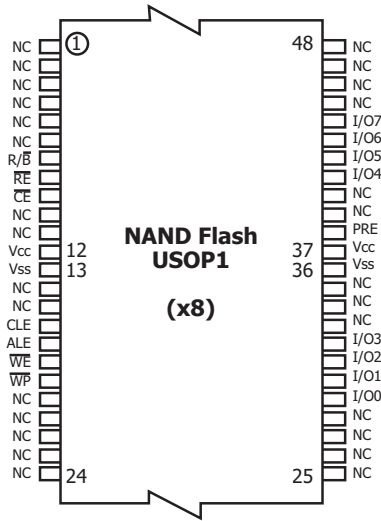


Figure 3. 48USOP1 Contactions, x8 Device

1.2 PIN DESCRIPTION

Pin Name	Description
I00-I07 I08-I015(1)	DATA INPUTS/OUTPUTS The IO pins allow to input command, address and data and to output data during read / program operations. The inputs are latched on the rising edge of Write Enable (\overline{WE}). The I/O buffer float to High-Z when the device is deselected or the outputs are disabled.
CLE	COMMAND LATCH ENABLE This input activates the latching of the IO inputs inside the Command Register on the Rising edge of Write Enable (\overline{WE}).
ALE	ADDRESS LATCH ENABLE This input activates the latching of the IO inputs inside the Address Register on the Rising edge of Write Enable (\overline{WE}).
\overline{CE}	CHIP ENABLE This input controls the selection of the device. When the device is busy \overline{CE} low does not deselect the memory.
\overline{WE}	WRITE ENABLE This input acts as clock to latch Command, Address and Data. The IO inputs are latched on the rise edge of \overline{WE} .
\overline{RE}	READ ENABLE The \overline{RE} input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of \overline{RE} which also increments the internal column address counter by one.
\overline{WP}	WRITE PROTECT The \overline{WP} pin, when Low, provides an Hardware protection against undesired modify (program / erase) operations.
R/ \overline{B}	READY BUSY The Ready/Busy output is an Open Drain pin that signals the state of the memory.
VCC	SUPPLY VOLTAGE The VCC supplies the power for all the operations (Read, Write, Erase).
VSS	GROUND
NC	NO CONNECTION

Table 2: Pin Description

NOTE:

1. For x16 version only
2. A 0.1uF capacitor should be connected between the Vcc Supply Voltage pin and the Vss Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.

	IO0	IO1	IO2	IO3	IO4	IO5	IO6	IO7
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A9	A10	A11	A12	A13	A14	A15	A16
3rd Cycle	A17	A18	A19	A20	A21	A22	A23	A24
4th Cycle	A25	A26	L ⁽¹⁾	L ⁽¹⁾	L ⁽¹⁾	L ⁽¹⁾	L ⁽¹⁾	L ⁽¹⁾

Table 3: Address Cycle Map(x8)

NOTE:

1. L must be set to Low.
2. A8 is set to LOW or High by the 00h or 01h Command.

	IO0	IO1	IO2	IO3	IO4	IO5	IO6	IO7	IO8-IO15
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7	L ⁽¹⁾
2nd Cycle	A9	A10	A11	A12	A13	A14	A15	A16	L ⁽¹⁾
3rd Cycle	A17	A18	A19	A20	A21	A22	A23	A24	L ⁽¹⁾
4th Cycle	A25	A26	L ⁽¹⁾	L ⁽¹⁾	L ⁽¹⁾	L ⁽¹⁾	L ⁽¹⁾	L ⁽¹⁾	L ⁽¹⁾

Table 4: Address Cycle Map(x16)

NOTE:

1. L must be set to Low.

FUNCTION	1st CYCLE	2nd CYCLE	3rd CYCLE	4th CYCLE	Acceptable command during busy
READ 1	00h/01h	-	-		
READ 2	50h	-	-		
READ ID	90h	-	-		
RESET	FFh	-	-		Yes
PAGE PROGRAM	80h	10h	-		
COPY BACK PGM	00h	8Ah	10h		
BLOCK ERASE	60h	D0h	-		
READ STATUS REGISTER	70h	-	-		Yes

Table 5: Command Set

CLE	ALE	\overline{CE}	\overline{WE}	\overline{RE}	\overline{WP}	MODE	
H	L	L	Rising	H	X	Read Mode	Command Input
L	H	L	Rising	H	X		Address Input(4 cycles)
H	L	L	Rising	H	H	Write Mode	Command Input
L	H	L	Rising	H	H		Address Input(4 cycles)
L	L	L	Rising	H	H	Data Input	
L	L	L ⁽¹⁾	H	Falling	X	Sequential Read and Data Output	
L	L	L	H	H	X	During Read (Busy)	
X	X	X	X	X	H	During Program (Busy)	
X	X	X	X	X	H	During Erase (Busy)	
X	X	X	X	X	L	Write Protect	
X	X	H	X	X	0V/Vcc	Stand By	

Table 6: Mode Selection

NOTE:

1. With the \overline{CE} don't care option \overline{CE} high during latency time does not stop the read operation

2. BUS OPERATION

There are six standard bus operations that control the device. These are Command Input, Address Input, Data Input, Data Output, Write Protect, and Standby.

Typically glitches less than 5 ns on Chip Enable, Write Enable and Read Enable are ignored by the memory and do not affect bus operations.

2.1 Command Input.

Command Input bus operation is used to give a command to the memory device. Command are accepted with Chip Enable low, Command Latch Enable High, Address Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modifying operation (write/erase) the Write Protect pin must be high. See figure 5 and table 12 for details of the timings requirements. Command codes are always applied on IO7:0, disregarding the bus configuration (X8/X16).

2.2 Address Input.

Address Input bus operation allows the insertion of the memory address. Four cycles are required to input the addresses for the 1Gbit devices. Addresses are accepted with Chip Enable low, Address Latch Enable High, Command Latch Enable low and Read Enable high and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/erase) the Write Protect pin must be high. See figure 6 and table 12 for details of the timings requirements. Addresses are always applied on IO7:0, disregarding the bus configuration (X8/X16).

In addition, addresses over the addressable space are disregarded even if the user sets them during command insertion.

2.3 Data Input.

Data Input bus operation allows to feed to the device the data to be programmed. The data insertion is serially and timed by the Write Enable cycles. Data are accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low, Read Enable High, and Write Protect High and latched on the rising edge of Write Enable. See figure 7 and table 12 for details of the timings requirements.

2.4 Data Output.

Data Output bus operation allows to read data from the memory array and to check the status register content, the lock status and the ID data. Data can be serially shifted out toggling the Read Enable pin with Chip Enable low, Write Enable High, Address Latch Enable low, and Command Latch Enable low. See figures 13 to 17 and table 12 for details of the timings requirements.

2.5 Write Protect.

Hardware Write Protection is activated when the Write Protect pin is low. In this condition modify operation do not start and the content of the memory is not altered. Write Protect pin is not latched by Write Enable to ensure the protection even during the power up.

2.6 Standby.

In Standby mode the device is deselected, outputs are disabled and Power Consumption is reduced.

3. DEVICE OPERATION

3.1 Page Read.

Upon initial device power up, the device defaults to Read1 mode. This operation is also initiated by writing 00h to the command register along with followed by the four address input cycles. Once the command is latched, it does not need to be written for the following page read operation.

Three types of operations are available: random read, serial page read and sequential row read.

The random read mode is enabled when the page address is changed. The 528 bytes (x8 device) or 264 word (x16 device) of data within the selected page are transferred to the data registers in less than access random read time t_R (15us). The system controller can detect the completion of this data transfer t_R (15us) by analyzing the output of R/B pin. Once the data in a page is loaded into the registers, they may be read out in 50ns cycle time by sequentially pulsing \overline{RE} . High to low transitions of the \overline{RE} clock output the data starting from the selected column address up to the last column address.

After the data of last column address is clocked out, the next page is automatically selected for sequential row read. Waiting t_R again allows reading the selected page. The sequential row read operation is terminated by bringing \overline{CE} high.

The way the Read1 and Read2 commands work is like a pointer set to either the main area or the spare area. Writing the Read2 command user may selectively access the spare area of bytes 512 to 527. Addresses A0 to A3 set the starting address of the spare area while addresses A4 to A7 are ignored. Unless the operation is aborted, the page address is automatically incremented for sequential row

Read as in Read1 operation and spare sixteen bytes of each page may be sequentially read. The Read1 command (00h/01h) is needed to move the pointer back to the main area. Figure_10 to 12 show typical sequence and timings for each read operation.

Devices with automatic read of page0 at power up can be provided on request.

3.2 Page Program.

The device is programmed basically on a page basis, but it does allow multiple partial page programming of a byte or consecutive bytes up to 528 (x8 device), in a single page program cycle.

The number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed 8; for example, 4 times for main array (X8 device: 1time/512byte, X16 device: 1time/256word) and 4 times for spare array (X8 device: 1time/16byte, X16 device: 1time/8word).

The addressing may be done in any random order in a block. A page program cycle consists of a serial data loading period in which up to 528 bytes (x8 device) or 264 word (x16 device) of data may be loaded into the page register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. Serial data loading can be started from 2nd half array by moving pointer. About the pointer operation, please refer to Figure_22.

The data-loading sequence begins by inputting the Serial Data Input command (80h), followed by the four address input cycles and then serial data loading. The Page Program confirm command (10h) starts the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal Program Erase Controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered, with \overline{RE} and \overline{CE} low, to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/B output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit (I/O 0) may be checked Figure_14

The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

3.3 Block Erase.

The Erase operation is done on a block (16K Byte) basis. It consists of an Erase Setup command (60h), a Block address loading and an Erase Confirm Command (D0h). The Erase Confirm command (D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.

The block address loading is accomplished in four cycles depending on the device density. Only block addresses (A14 to A26) are needed while A9 to A13 is ignored. At the rising edge of \overline{WE} after the erase confirm command input, the internal Program Erase Controller handles erase and erase-verify. When the erase operation is completed, the Write Status Bit (I/O 0) may be checked. Figure_16 details the sequence.

3.4 Copy-Back Program.

The copy-back program is provided to quickly and efficiently rewrite data stored in one page within the plane to another page within the same plane without using an external memory. Since the time-consuming sequential-reading and its reloading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block also need to be copied to the newly assigned free block. The operation for performing a copy-back program is a sequential execution of page-read without burst-reading cycle and copying-program with the address of destination page. A normal read operation with "00h" command and the address of the source page moves the whole 528byte data into the internal buffer. As soon as the device returns to Ready state, Page-Copy Data-input command (8Ah) with the address cycles of destination page followed may be written. The Program Confirm command (10h) is required to actually begin the programming operation.

Copy-Back Program operation is allowed only within the same memory plane. Once the Copy-Back Program is finished, any additional partial page programming into the copied pages is prohibited before erase. Plane address must be the same between source and target page

"When there is a program-failure at Copy-Back operation, error is reported by pass/fail status. But, if Copy-Back operations are accumulated over time, bit error due to charge loss is not checked by external error detection/correction scheme. For this reason, two bit error correction is recommended for the use of Copy-Back operation."

Figure 15 shows the command sequence for the copy-back operation.

The Copy Back Program operation requires three steps:

- 1. The source page must be read using the Read A command (one bus write cycle to setup the command and then 3 bus cycles to input the source page address.) This operation copies all 264 Words/ 528 Bytes from the page into the page Buffer.
- 2. When the device returns to the ready state (Ready/Busy High), the second bus write cycle of the command is given with the 4cycles to input the target page address. A26, A25 must be the same for the Source and Target Pages.
- 3. Then the confirm command is issued to start the P/E/R Controller.

Note:

- 1. Copy-Back Program operation is allowed only within the same memory plane.
- 2. On the same plane, It's prohibited to operate copy-back program from an odd address page (source page) to an even address page (target page) or from an even address page (source page) to an odd address page (target page). Therefore, the copy-back program is permitted just between odd address pages or even address pages.

3.5 Read Status Register.

The device contains a Status Register which may be read to find out whether read, program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of \overline{CE} or \overline{RE} , whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/B pins are common-wired. \overline{RE} or \overline{CE} does not need to be toggled for updated status. Refer to table 13 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, a read command (00h or 50h) should be given before sequential page read cycle.

3.6 Read ID.

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Two read cycles sequentially output the manufacturer code (ADh), the device code and 3rd, 4 cycle ID respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 17 shows the operation sequence, while tables 15 explain the byte meaning.

3.7 Reset.

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value E0h when \overline{WP} is high. Refer to table 14 for device status after reset operation. If the device is already in reset state a new reset command will not be accepted by the command register. The R/B pin transitions to low for tRST after the Reset command is written. Refer to figure 19.

4. OTHER FEATURES

4.1 Data Protection & Power on/off Sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever V_{cc} is below about 2.0V(3.3V device). \overline{WP} pin provides hardware protection and is recommended to be kept at VIL during power-up and power-down. A recovery time of minimum 10 μ s is required before internal circuit gets ready for any command sequences as shown in Figure 20. The two-step command sequence for program/erase provides additional software protection.

If the power is dropped during the ready read/write/erase operation, Power protection function may not guaranteed the data. Power protection function is only available during the power on/off sequence.

4.2 Ready/Busy.

The device has a Ready/Busy output that provides method of indicating the completion of a page program, erase, copy-back, cache program and random read completion. The R/\overline{B} pin is normally high and goes to low when the device is busy (after a reset, read, program, erase operation). It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/\overline{B} outputs to be Or-tied. Because pull-up resistor value is related to $t_r(R/\overline{B})$ and current drain during busy (I_{busy}), an appropriate value can be obtained with the following reference chart (Fig 21). Its value can be determined by the following guidance.

4.3 Power-On Auto-Read

The device is designed to offer automatic reading of the first page without command and address input sequence during power-on.

An internal voltage detector enables auto-page read functions when V_{cc} reaches about 1.8V.

Serial access may be done after power-on without latency. Power-On Auto Read mode is available only on 3.3V device.

Parameter	Symbol	Min	Typ	Max	Unit
Valid Block Number	NvB	8032		8192	Blocks

Table 6: Valid Blocks Number

NOTE:

1. The 1st block is guaranteed to be a valid block up to 1K cycles with ECC. (1bit/528bytes)

Symbol	Parameter	Value	Unit
		3.3V	
TA	Ambient Operating Temperature (Commercial Temperature Range)	0 to 70	℃
	Ambient Operating Temperature (Extended Temperature Range)	-25 to 85	℃
	Ambient Operating Temperature (Industrial Temperature Range)	-40 to 85	℃
TBIAS	Temperature Under Bias	-50 to 125	℃
TSTG	Storage Temperature	-65 to 150	℃
V _{IO} ⁽²⁾	Input or Output Voltage	-0.6 to 4.6	V
V _{CC}	Supply Voltage	-0.6 to 4.6	V

Table 7: Absolute maximum ratings

NOTE:

1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.
2. Minimum Voltage may undershoot to -2V during transition and for less than 20ns during transitions.

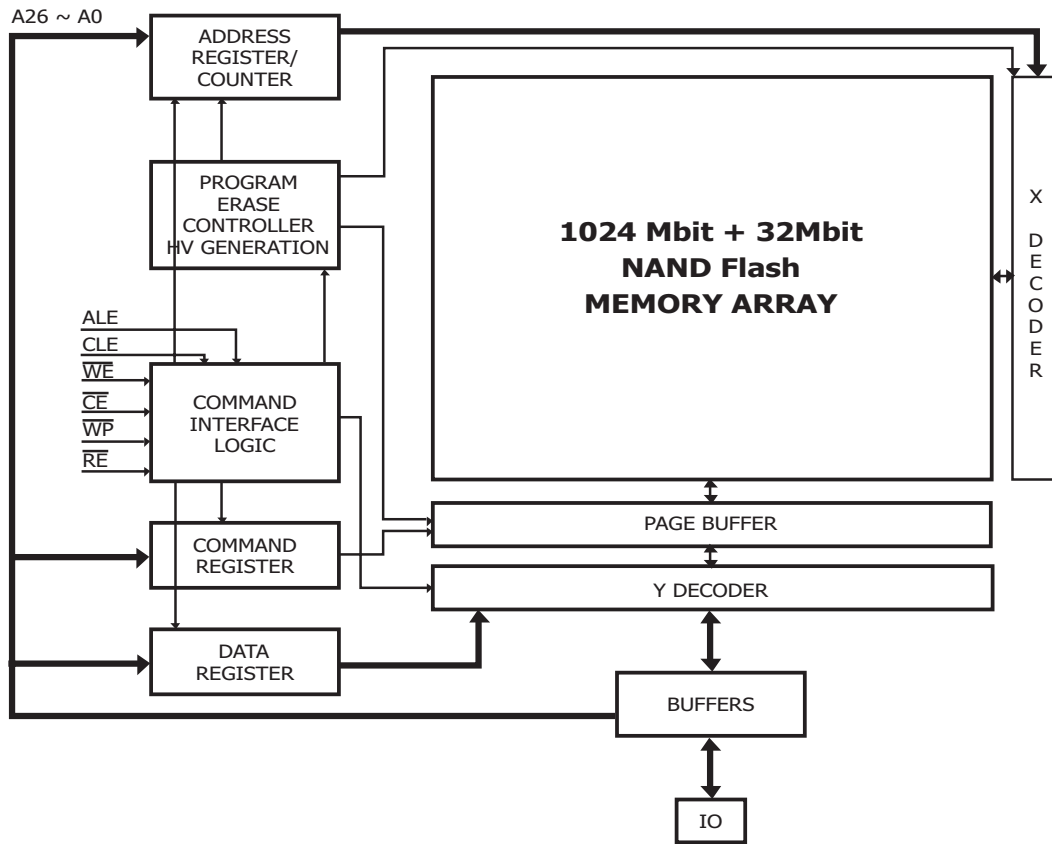


Figure 4: Block Diagram

Parameter		Symbol	Test Conditions	3.3Volt			Unit
				Min	Typ	Max	
Operating Current	Sequential Read	I _{CC1}	t _{RC} =50ns CE=V _{IL} , I _{OUT} =0mA	-	10	20	mA
	Program	I _{CC2}	-	-	10	20	mA
	Erase	I _{CC3}	-	-	10	20	mA
Stand-by Current (TTL)		I _{CC4}	CE=V _{IH} , WP=PRE=0V/V _{CC}	-		1	mA
Stand-by Current (CMOS)		I _{CC5}	CE=V _{CC} -0.2, WP=PRE=0V/V _{CC}	-	10	50	uA
Input Leakage Current		I _{LI}	V _{IN} =0 to V _{CC} (max)	-	-	± 10	uA
Output Leakage Current		I _{LO}	V _{OUT} =0 to V _{CC} (max)	-	-	± 10	uA
Input High Voltage		V _{IH}	-	0.8 x V _{CC}	-	V _{CC} +0.3	V
Input Low Voltage		V _{IL}	-	-0.3	-	0.2xV _{CC}	V
Output High Voltage Level		V _{OH}	I _{OH} =-400uA	2.4	-	-	V
Output Low Voltage Level		V _{OL}	I _{OL} =2.1mA	-	-	0.4	V
Output Low Current (R/B)		I _{OL} (R/B)	V _{OL} =0.4V	8	10	-	mA

Table 8: DC and Operating Characteristics

Parameter	Value
	3.3Volt
Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load (2.7V - 3.3V)	1 TTL GATE and CL=50pF
Output Load (3.0V - 3.6V)	1 TTL GATE and CL=100pF

Table 9: AC Conditions

Item	Symbol	Test Condition	Min	Max	Unit
Input / Output Capacitance	C _{I/O}	V _{IL} =0V	-	10	pF
Input Capacitance	C _{IN}	V _{IN} =0V	-	10	pF

Table 10: Pin Capacitance (TA=25C, F=1.0MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Program Time	t _{PROG}	-	200	500	us
Number of partial Program Cycles in the same page	Main Array	NOP	-	4	Cycles
	Spare Array	NOP	-	4	Cycles
Block Erase Time	t _{BERS}	-	2	3	ms

Table 11: Program / Erase Characteristics



Preliminary
HY27US(08/16)1G1M Series
1Gbit (128Mx8bit / 64Mx16bit) NAND Flash

Parameter	Symbol	3.3Volt		Unit
		Min	Max	
CLE Setup time	tCLS	0		ns
CLE Hold time	tCLH	10		ns
$\overline{\text{CE}}$ setup time	tCS	0		ns
$\overline{\text{CE}}$ hold time	tCH	10		ns
$\overline{\text{WE}}$ pulse width	tWP	25 ⁽¹⁾		ns
ALE setup time	tALS	0		ns
ALE hold time	tALH	10		ns
Data setup time	tDS	20		ns
Data hold time	tDH	10		ns
Write Cycle time	tWC	50		ns
$\overline{\text{WE}}$ High hold time	tWH	15		ns
Data Transfer from Cell to register	tR		15	us
ALE to $\overline{\text{RE}}$ Delay	tAR	10		ns
CLE to $\overline{\text{RE}}$ Delay	tCLR	10		ns
Ready to $\overline{\text{RE}}$ Low	tRR	20		ns
$\overline{\text{RE}}$ Pulse Width	tRP	25		ns
$\overline{\text{WE}}$ High to Busy	tWB		100	ns
Read Cycle Time	tRC	50		ns
$\overline{\text{RE}}$ Access Time	tREA		30	ns
$\overline{\text{RE}}$ High to Output High Z	tRHZ		30	ns
$\overline{\text{CE}}$ High to Output High Z	tCHZ		20	ns
$\overline{\text{RE}}$ or $\overline{\text{CE}}$ high to Output hold	tOH	10		ns
$\overline{\text{RE}}$ High Hold Time	tREH	15		ns
Output High Z to $\overline{\text{RE}}$ low	tIR	0		ns
$\overline{\text{CE}}$ Access Time	tCEA		45	ns
$\overline{\text{WE}}$ High to $\overline{\text{RE}}$ low	tWHR	60		ns
Last $\overline{\text{RE}}$ High to busy (at sequential read)	tRB		100	ns
$\overline{\text{CE}}$ High to Ready (in case of interception by $\overline{\text{CE}}$ at read)	tCRY		60+tr(R/B#) ⁽⁴⁾	ns
$\overline{\text{CE}}$ High Hold Time (at the last serial read) ⁽³⁾	tCEH	100		ns
Device Resetting Time (Read / Program / Erase)	tRST		5/10/500 ⁽²⁾	us
Write Protection time	tWW ⁽⁵⁾	100		ns

Table 12: AC Timing Characteristics

NOTE:

1. If tcs is less than 10ns tWP must be minimum 35ns, otherwise, tWP may be minimum 25ns.
2. If Reset Command (FFh) is written at Ready state, the device goes into Busy for maximum 5us
3. To break the sequential read cycle, $\overline{\text{CE}}$ must be held for longer time than tCEH.
4. The time to Ready depends on the value of the pull-up resistor tied R/B# pin.ing time.
5. Program / Erase Enable Operation : $\overline{\text{WP}}$ high to $\overline{\text{WE}}$ High.
 Program / Erase Disable Operation : $\overline{\text{WP}}$ Low to $\overline{\text{WE}}$ High.

IO	Page Program	Block Erase	Read	CODING
0	Pass / Fail	Pass / Fail	NA	Pass: '0' Fail: '1'
1	NA	NA	NA	-
2	NA	NA	NA	-
3	NA	NA	NA	-
4	NA	NA	NA	-
5	Ready/Busy	Ready/Busy	Ready/Busy	Active: '0' Idle: '1'
6	Ready/Busy	Ready/Busy	Ready/Busy	Busy: '0' Ready: '1'
7	Write Protect	Write Protect	Write Protect	Protected: '0' Not Protected: '1'

Table 13: Status Register Coding

DEVICE IDENTIFIER CYCLE	DESCRIPTION
1st	Manufacturer Code
2nd	Device Identifier
3rd	Internal chip number, cell Type, Number of simultaneously Programmed pages
4th	Page size, Spare size, Block size, Organization

Table 14: Device Identifier Coding

Part Number	Voltage	Bus Width	1st cycle (Manufacture Code)	2nd cycle (Device Code)	3rd Cycle	4th Cycle
HY27US081G1M	3.3V	x8	ADh	79h	A5h	00h
HY27US161G1M	3.3V	x16	ADh	74h	A5h	00h

Table 15: Read ID Data Table

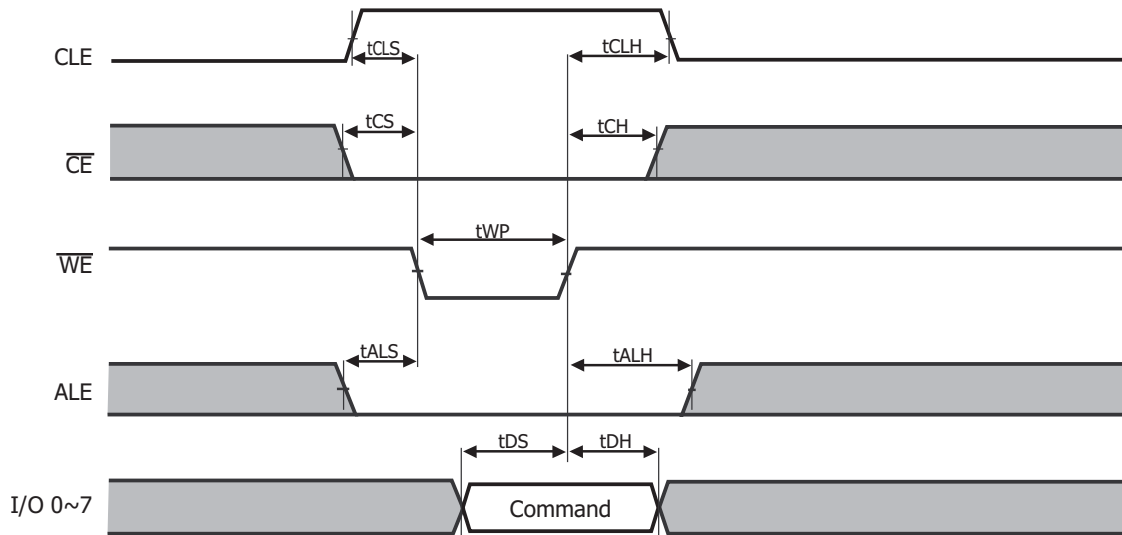


Figure 5: Command Latch Cycle

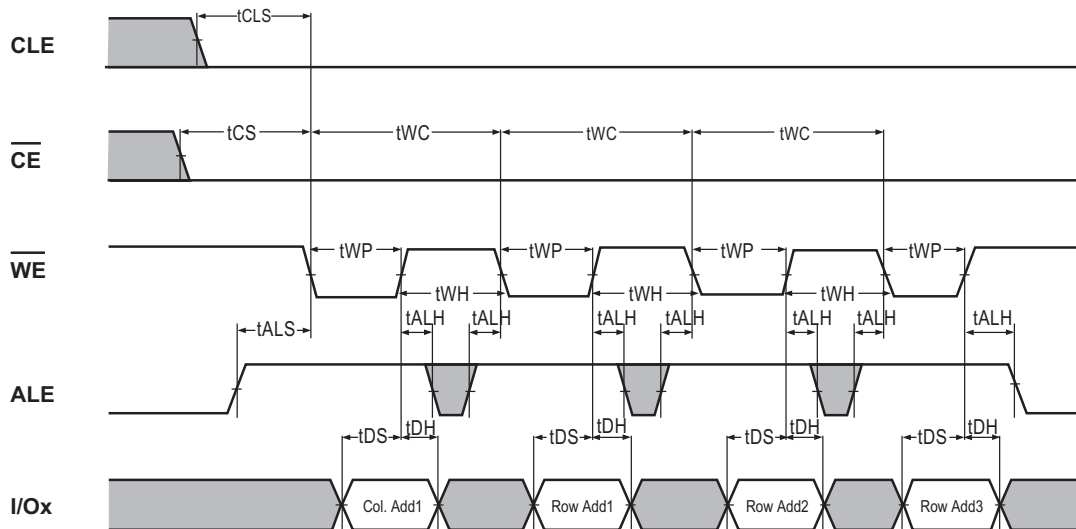


Figure 6: Address Latch Cycle

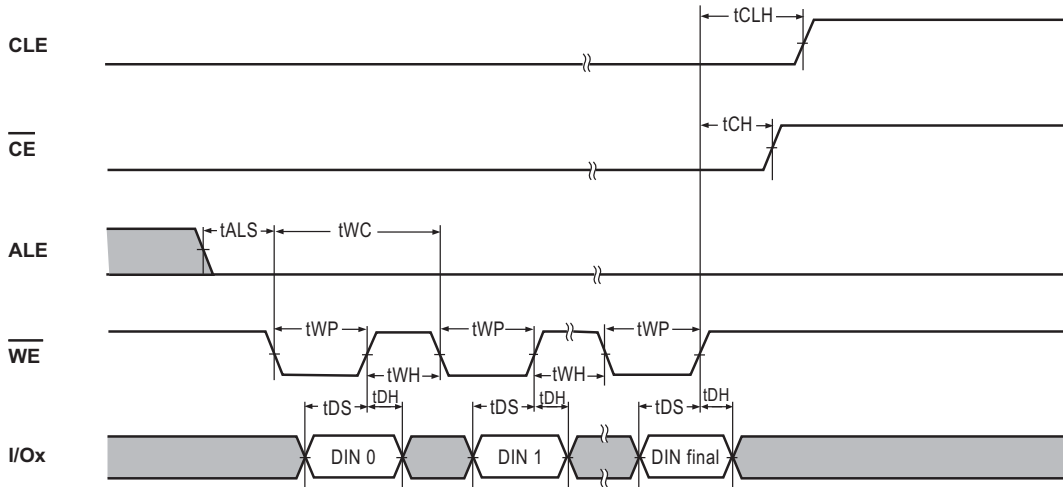
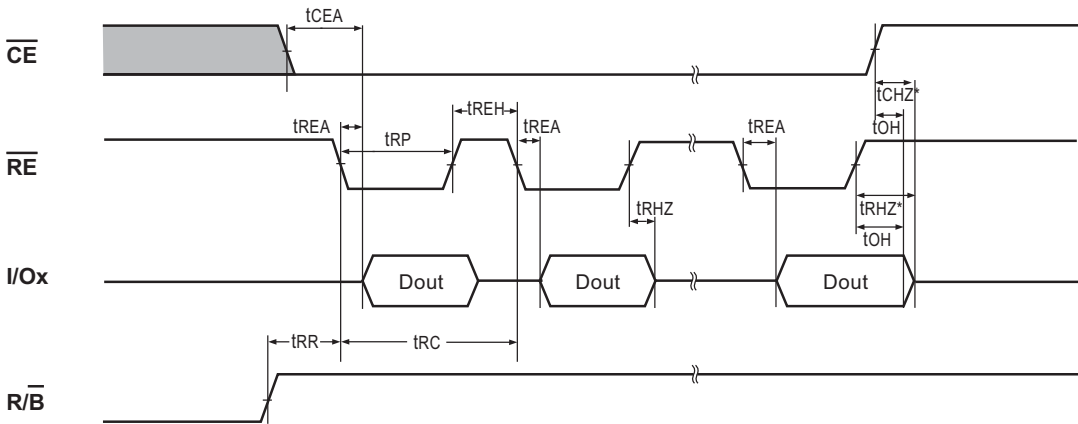


Figure 7. Input Data Latch Cycle



Notes : Transition is measured $\pm 200\text{mV}$ from steady state voltage with load.
 This parameter is sampled and not 100% tested.

Figure 8: Sequential Out Cycle after Read (CLE=L, WE=H, ALE=L)

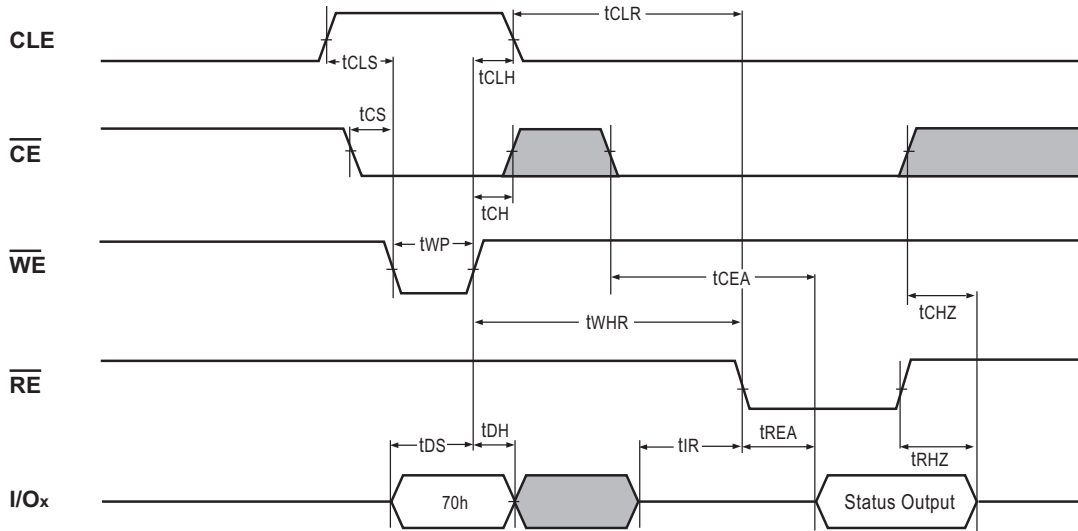


Figure 9: Status Read Cycle

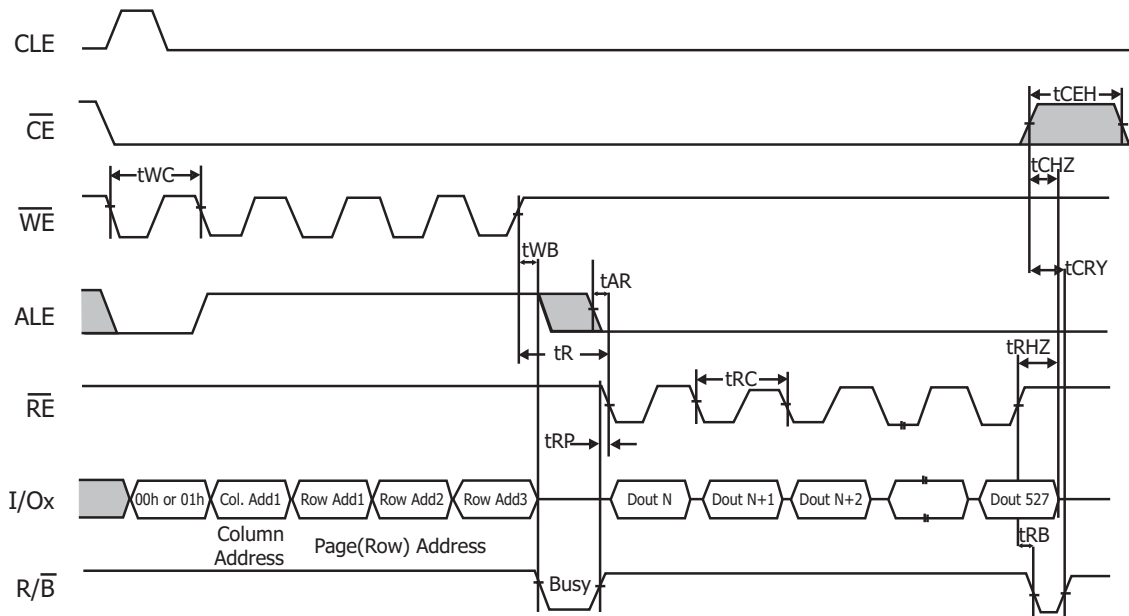


Figure 10: Read1 Operation (Read One Page)

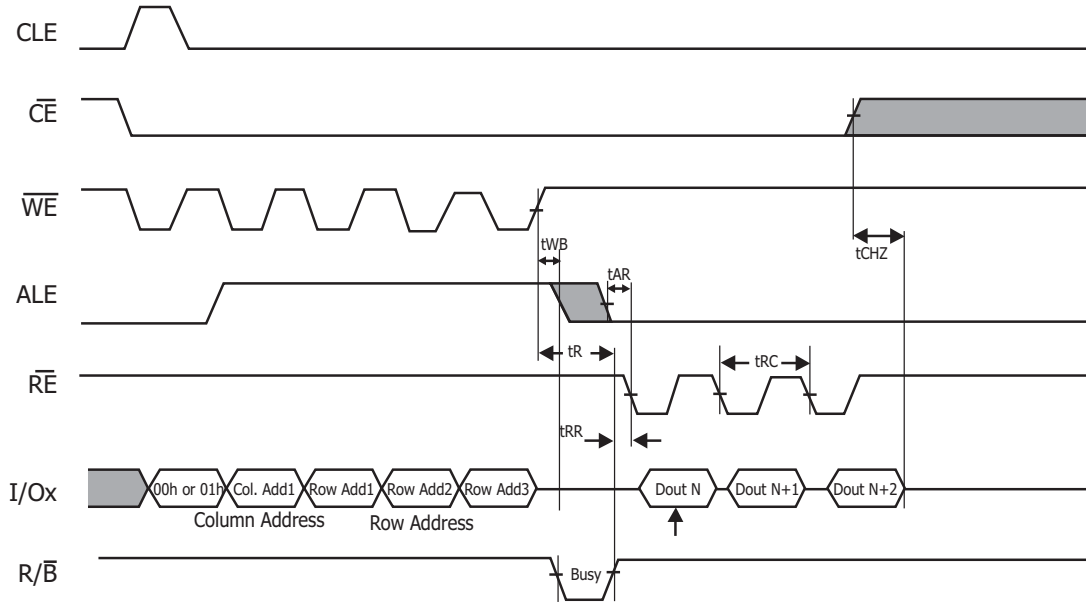


Figure 11: Read1 Operation intercepted by \overline{CE}

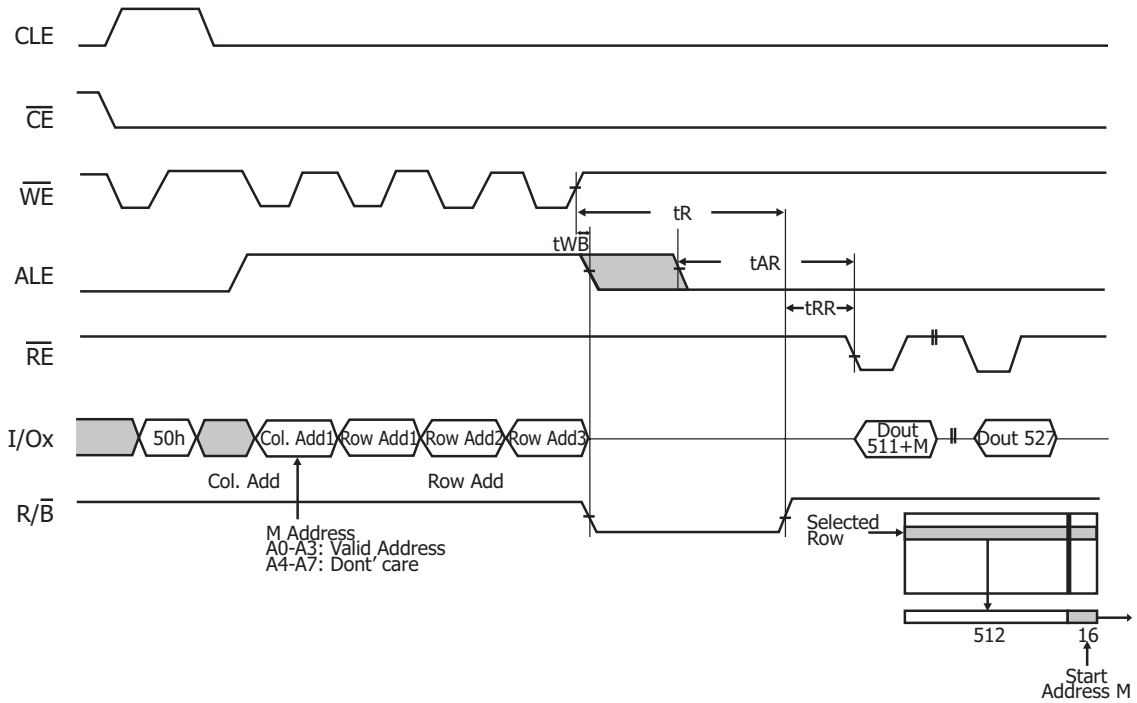


Figure 12: Read2 Operation (Read One Page)

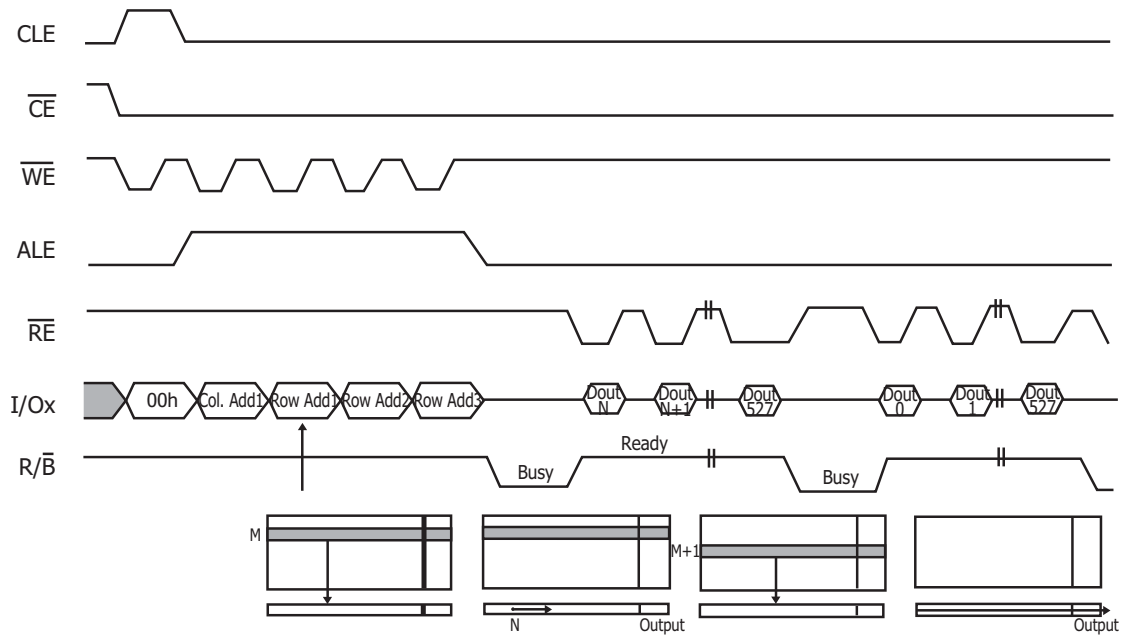


Figure 13: Sequential Row Read Operation Within a Block

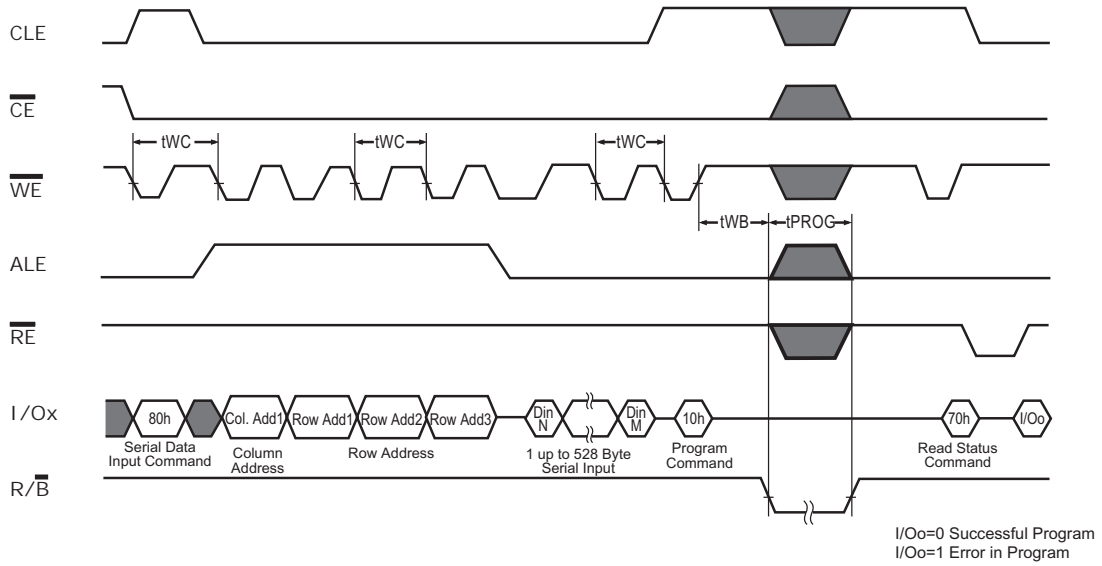
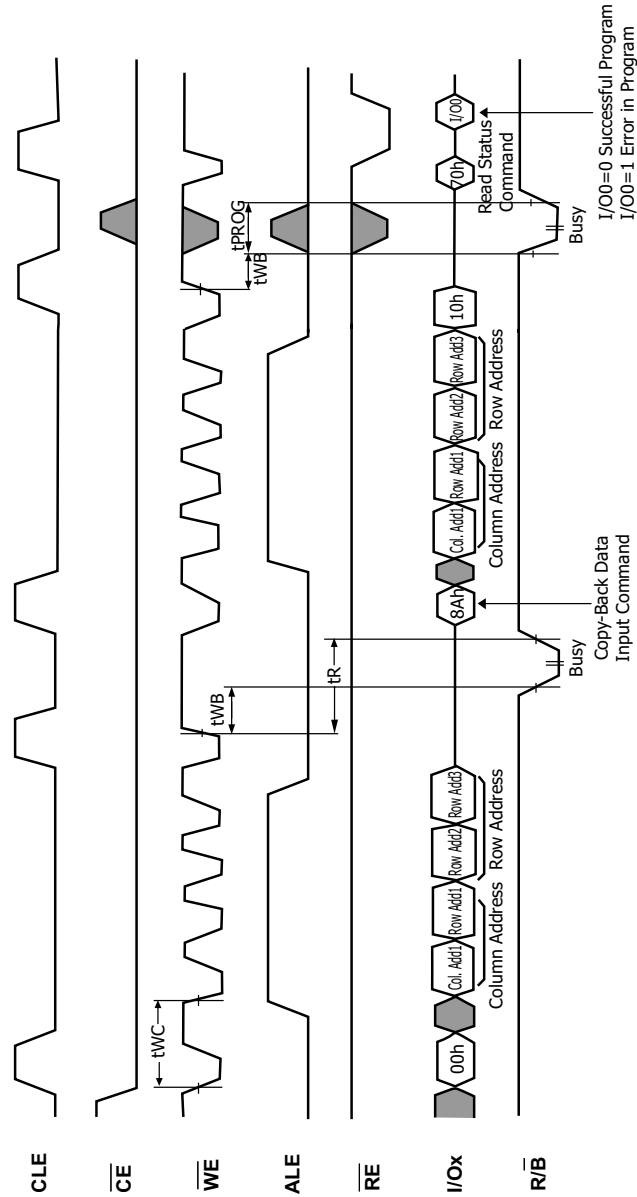


Figure 14: Page Program Operation



Note : t_{ADL} is the time from the WE# rising edge of final address cycle to the WE# rising edge fo first data cycle.

Figure 15 : Copy Back Program

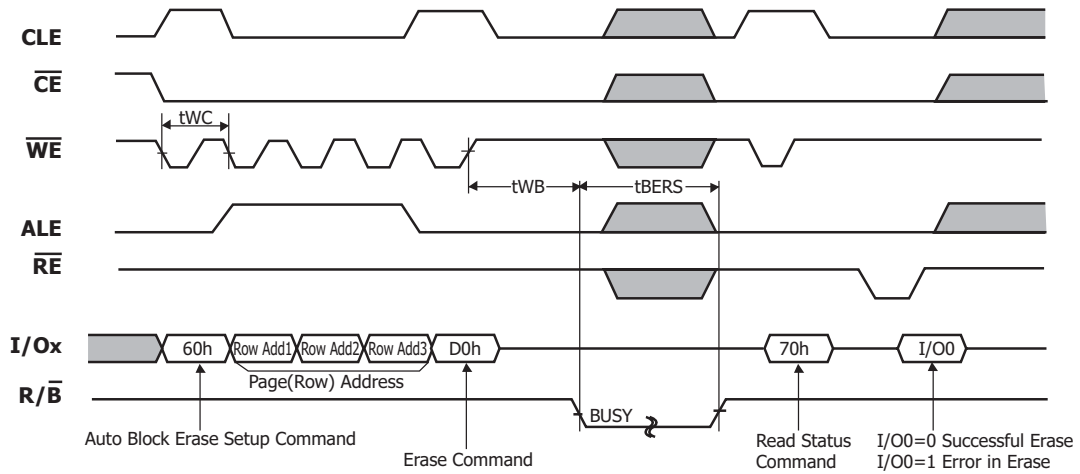


Figure 16: Block Erase Operation (Erase One Block)

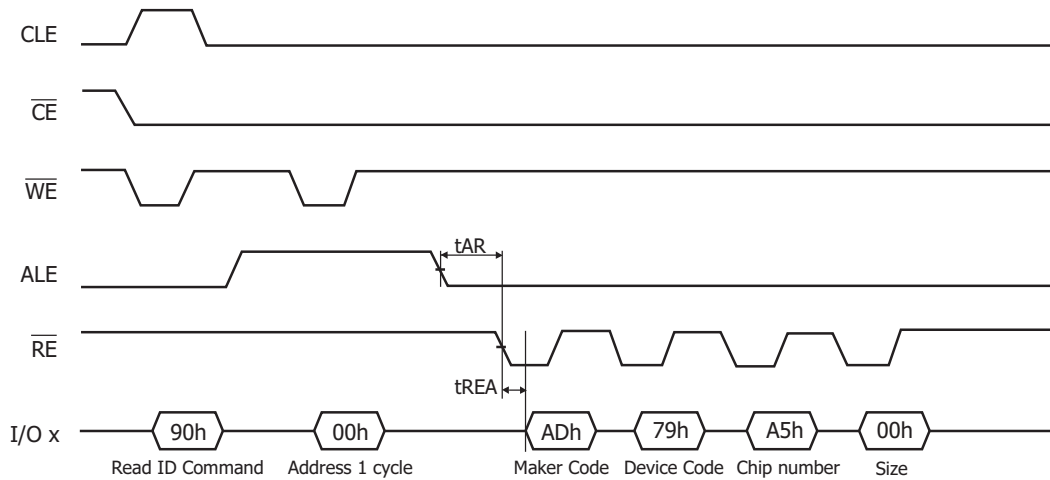


Figure 17 : Read ID Operation

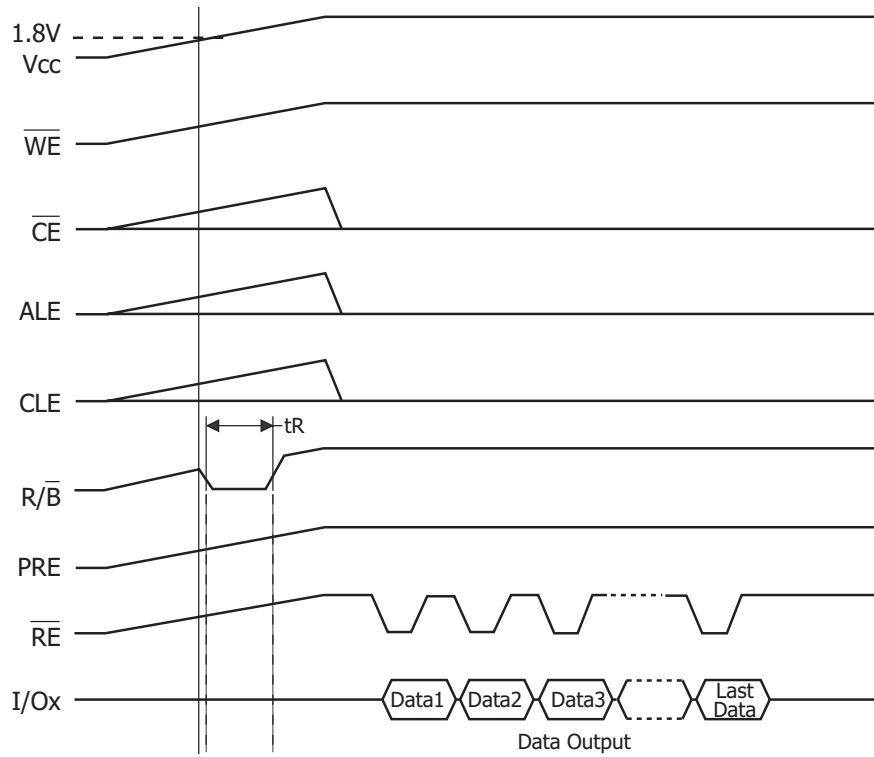


Figure 18 : Automatic Read at Power On

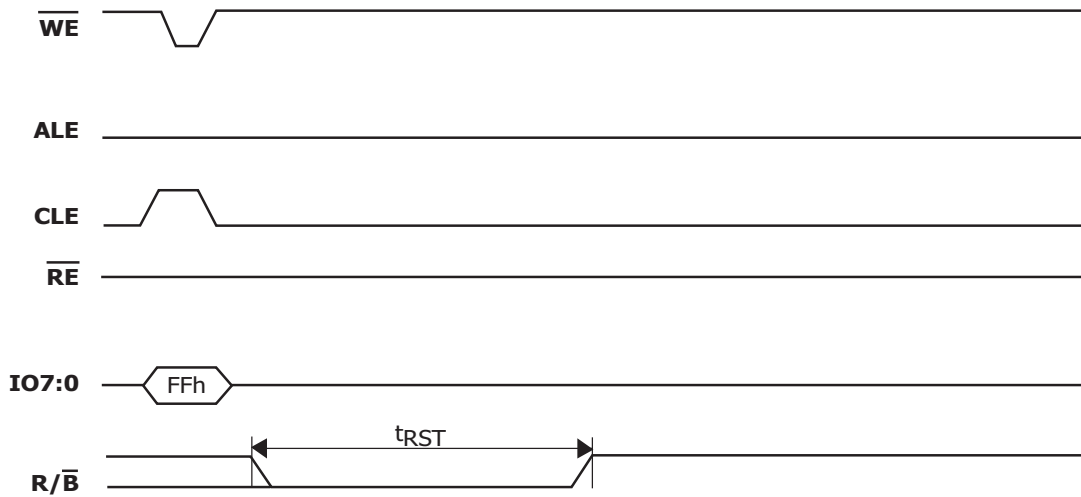


Figure 19 : Reset Operation

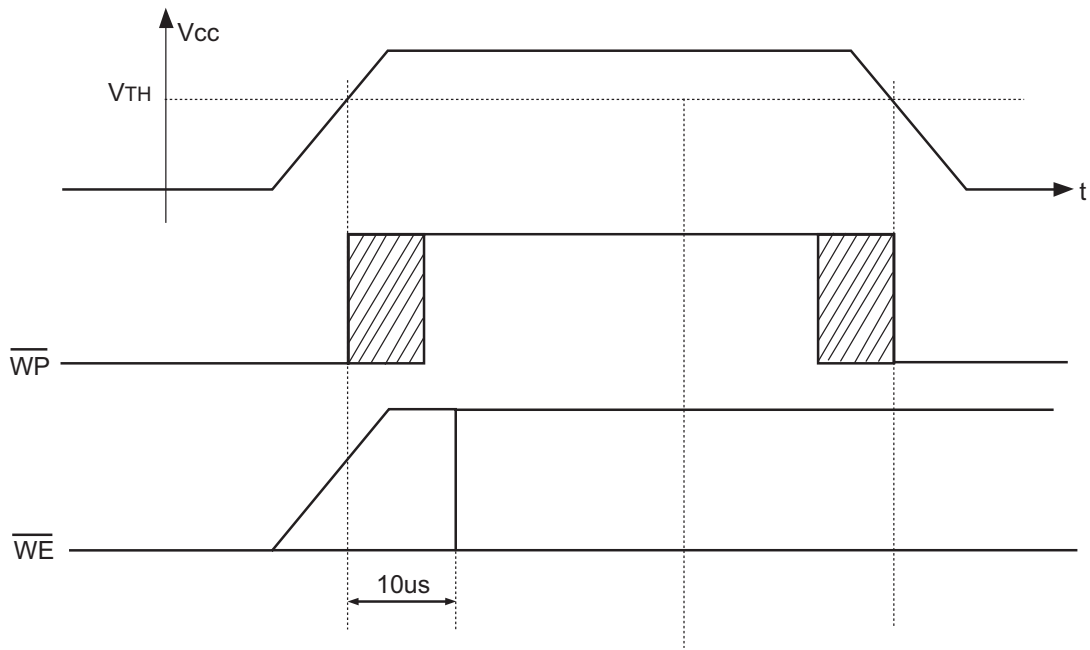


Figure 20: Power On and Data Protection Timing

VTH = 2.5 Volt for 3.3 Volt Supply devices

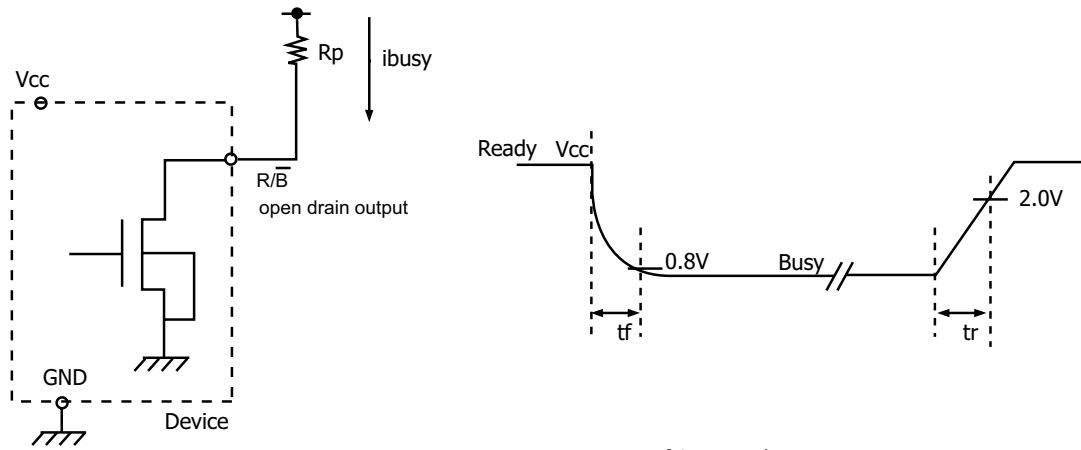
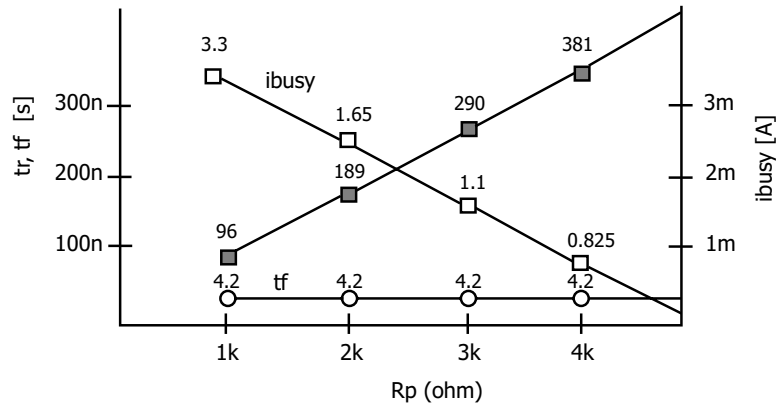


Fig. Rp vs tr, tf & Rp vs ibusy

@ Vcc = 3.3V, Ta = 25°C, CL=100pF



Rp value guidance

$$R_p(\min) = \frac{V_{cc}(\text{Max.}) - V_{OL}(\text{Max.})}{I_{OL} + \sum I_L} = \frac{3.2V}{8mA + \sum I_L}$$

where IL is the sum of the input currents of all devices tied to the R/B pin.

Rp(max) is determined by maximum permissible limit of tr

Figure 21: Ready/Busy Pin electrical specifications

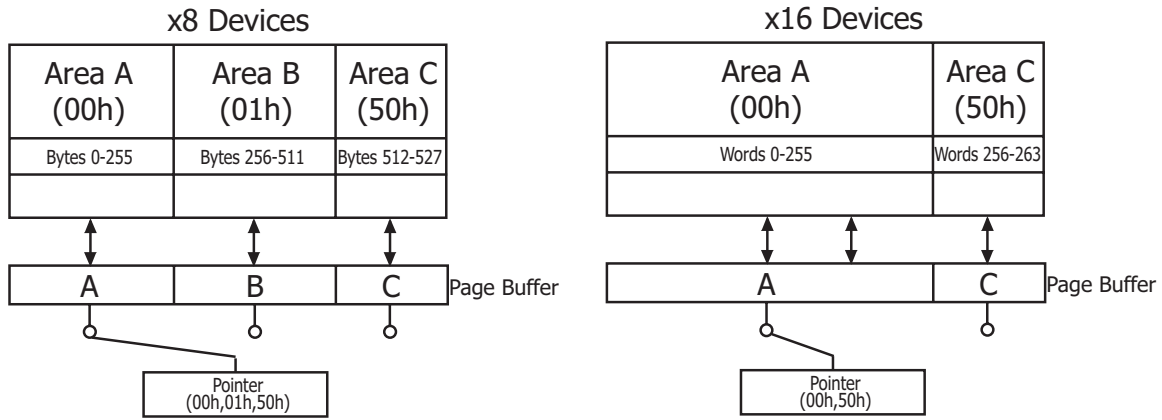


Figure 22: Pointer operations

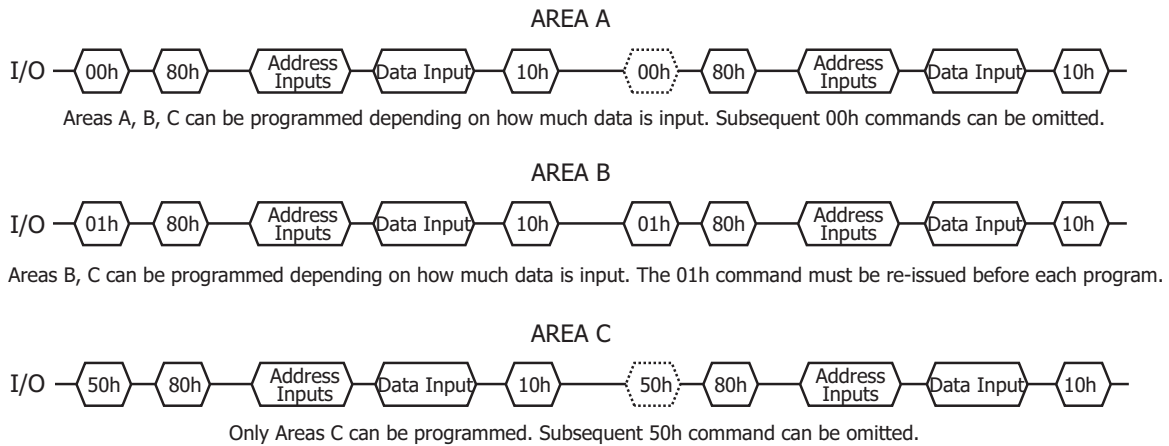


Figure 23: Pointer Operations for programming

System Interface Using \overline{CE} don't care

To simplify system interface, \overline{CE} may be deasserted during data loading or sequential data-reading as shown below. So, it is possible to connect NAND Flash to a microprocessor. The only function that was removed from standard NAND Flash to make \overline{CE} don't care read operation was disabling of the automatic sequential read function.

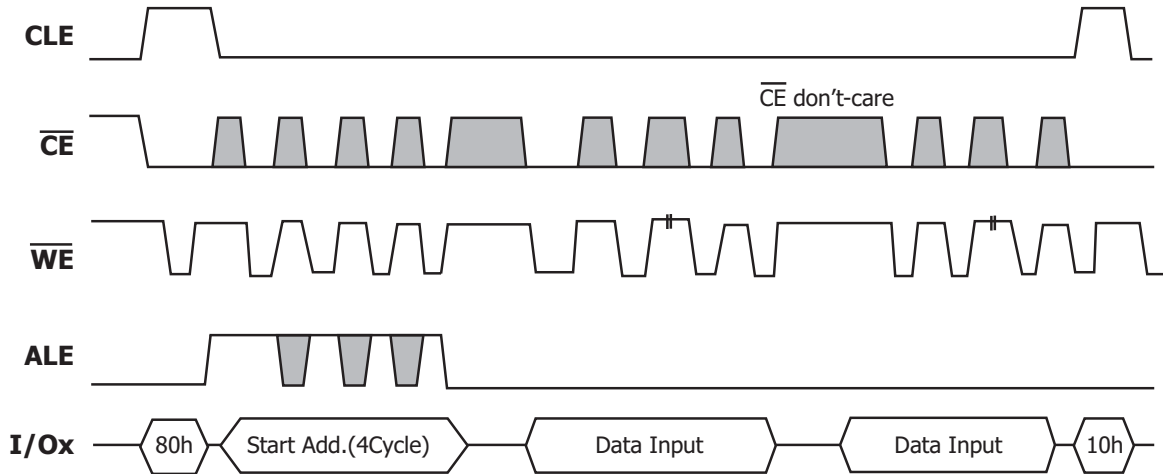


Figure 24: Program Operation with \overline{CE} don't-care.

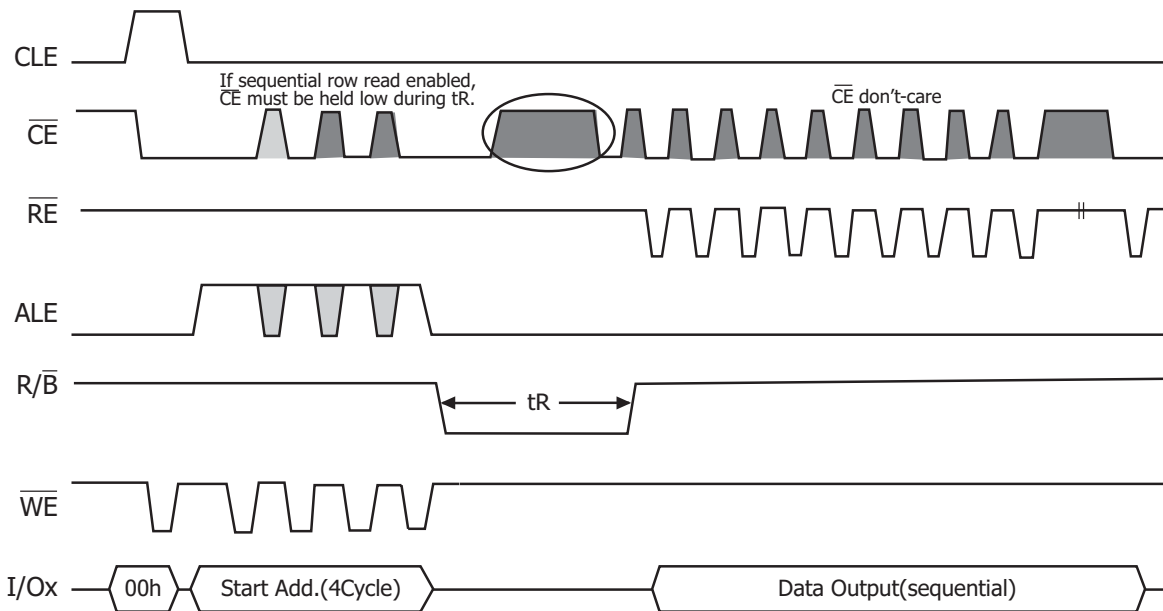


Figure 25: Read Operation with \overline{CE} don't-care.

Bad Block Management

Devices with Bad Blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A Bad Block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor. The devices are supplied with all the locations inside valid blocks erased (FFh/FFFFh).

The Bad Block Information is written prior to shipping. Any block where the 6th Byte/ 1st Word in the spare area of the 1st or 2nd page (if the 1st page is Bad) does not contain FFh/FFFFh is a Bad Block. The Bad Block Information must be read before any erase is attempted as the Bad Block Information may be erased. For the system to be able to recognize the Bad Blocks based on the original information it is recommended to create a Bad Block table following the flowchart shown in Figure 26. The 1st block, which is placed on 00h block address is guaranteed to be a valid block.

Block Replacement

Over the lifetime of the device additional Bad Blocks may develop. In this case the block has to be replaced by copying the data to a valid block. These additional Bad Blocks can be identified as attempts to program or erase them will give errors in the Status Register.

As the failure of a page program operation does not affect the data in other pages in the same block, the block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block.

The Copy Back Program command can be used to copy the data to a valid block.

See the "Copy Back Program" section for more details.

Refer to Table 16 for the recommended procedure to follow if an error occurs during an operation.

Operation	Recommended Procedure
Erase	Block Replacement
Program	Block Replacement or ECC (with 4bit/528byte)
Read	ECC (with 4bit/528byte)

Table 16: Block Failure

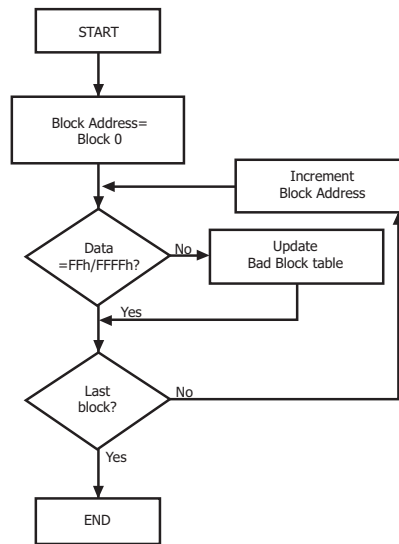


Figure 26: Bad Block Management Flowchart

Write Protect Operation

The Erase and Program Operations are automatically reset when \overline{WP} goes Low ($t_{WW} = 100\text{ns, min}$). The operations are enabled and disabled as follows (Figure 27~30)

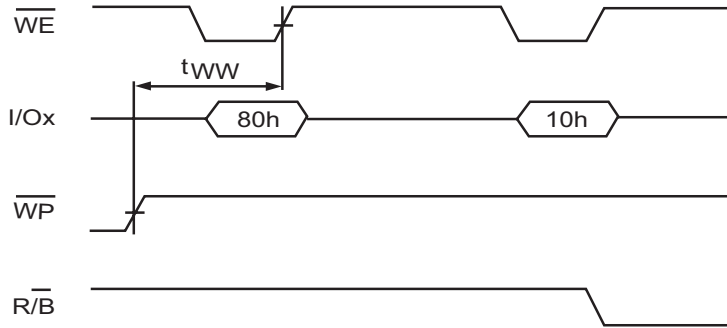


Figure 27: Enable Programming

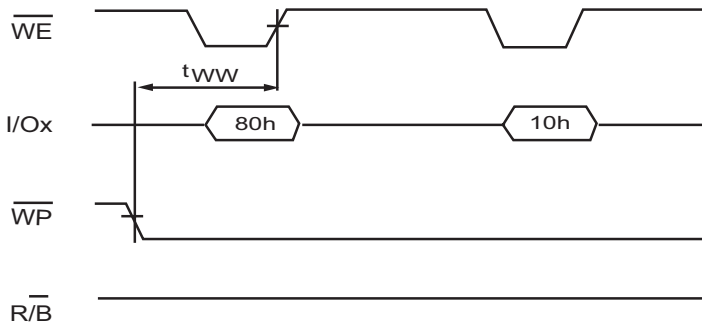


Figure 28: Disable Programming

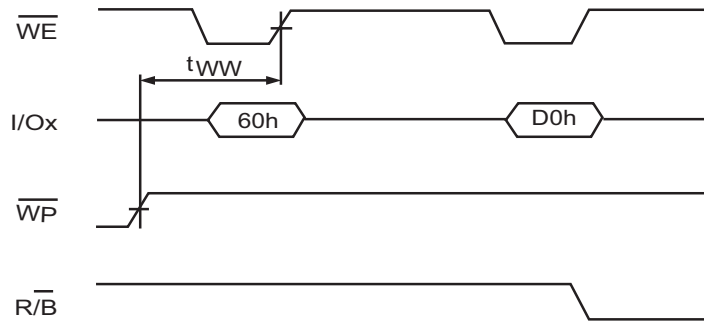


Figure 29: Enable Erasing

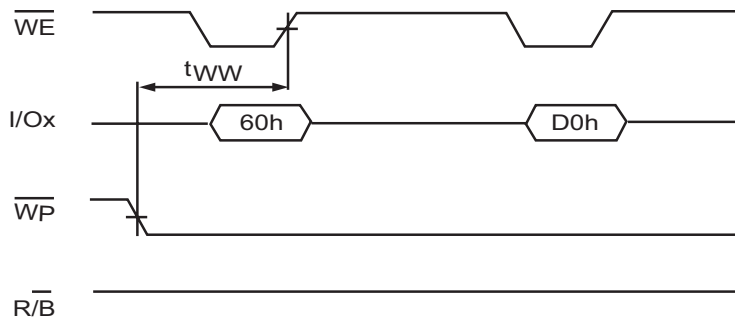


Figure 30: Disable Erasing

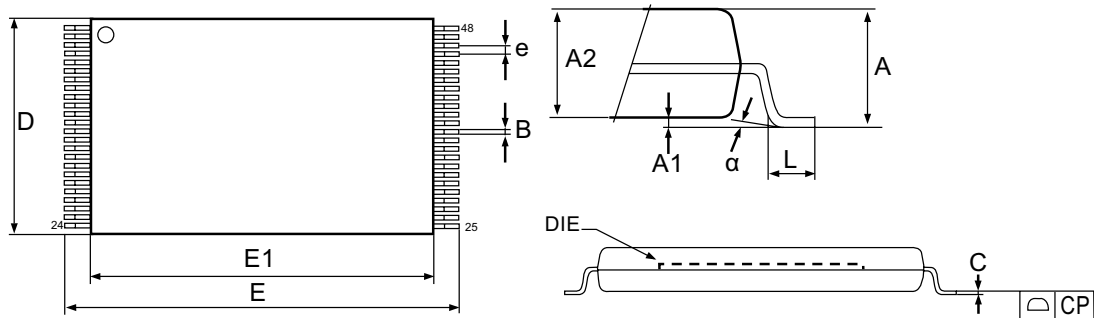


Figure 31: 48pin-TSOP1, 12 x 20mm, Package Outline

Symbol	millimeters		
	Min	Typ	Max
A			1.200
A1	0.050		0.150
A2	0.980		1.030
B	0.170		0.250
C	0.100		0.200
CP			0.100
D	11.910	12.000	12.120
E	19.900	20.000	20.100
E1	18.300	18.400	18.500
e		0.500	
L	0.500		0.680
alpha	0		5

Table 17: 48pin-TSOP1, 12 x 20mm, Package Mechanical Data

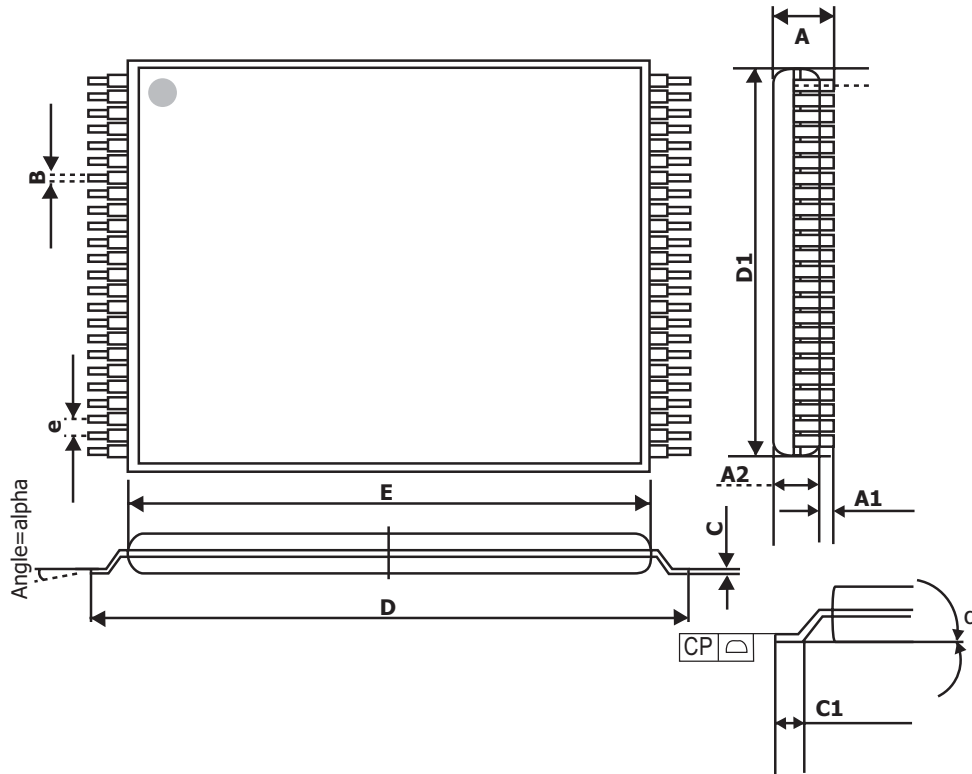
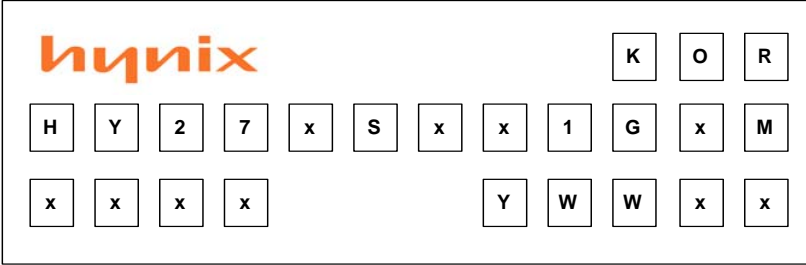


Figure 32. 48pin-USOP1, 12 x 17mm, Package Outline

Symbol	millimeters		
	Min	Typ	Max
A			0.650
A1	0	0.050	0.080
A2	0.470	0.520	0.570
B	0.130	0.160	0.230
C	0.065	0.100	0.175
C1	0.450	0.650	0.750
CP			0.100
D	16.900	17.000	17.100
D1	11.910	12.000	12.120
E	15.300	15.400	15.500
e		0.500	
alpha	0		8

Table 18: 48pin-USOP1, 12 x 17mm, Package Mechanical Data

MARKING INFORMATION - TSOP1/USOP

Packag	Marking Example
TSOP1 / USOP	

- hynix	: Hynix Symbol
- KOR	: Origin Country
- HY27xSxx1GxM xxxx : Part Number	
HY: Hynix	
27: NAND Flash	
x: Power Supply	: U(2.7V~3.6V)
S: Classification	: Single Level Cell+ Double Die+ Small Block
xx: Bit Organization	: 08(x8), 16(x16)
1G: Density	: 1Gbit
x: Mode	: 1(1nCE & 1R/nB; Sequential Row Read Enable) 2(1nCE & 1R/nB; Sequential Row Read Disable)
M: Version	: 1st Generation
- x: Package Type : T(48-TSOP1), S(48-USOP)	
- x: Package Material : Blank(Normal), P(Lead Free)	
- x: Operating Temperature : C(0℃ ~ 70℃), E(-25℃ ~ 85℃) M(-30℃ ~ 85℃), I(-40℃ ~ 85℃)	
- x: Bad Block : B(Included Bad Block), S(1~5 Bad Block), P(All Good Block)	
- Y: Year (ex: 5=year 2005, 06= year 2006)	
- ww: Work Week (ex: 12= work week 12)	
- xx: Process Code	
Note	
- Capital Letter	: Fixed Item
- Small Letter	: Non-fixed Item