8Gb NAND FLASH

HY27UG088G5M
HY27UG088GDM

Document Title
8Gbit (1Gx8bit) NAND Flash Memory

Revision History

<table>
<tr><th>Revision No.</th><th>History</th><th>Draft Date</th><th>Remark</th></tr>
<tr><td>0.0</td><td>Initial Draft.</td><td>Sep. 08. 2005</td><td>Initial</td></tr>
<tr><td>0.1</td><td>1) Add HY27UG088G5M & HY27UG088GDM Products.
- Texts & figures are added.
2) Change Ac Characteristics
<table>
<tr><td></td><td>tR</td><td>tAR</td><td>tREA</td><td>tRHZ</td><td>tCHZ</td><td>tCEA</td></tr>
<tr><td>Before</td><td>20</td><td>10</td><td>18</td><td>30</td><td>30</td><td>25</td></tr>
<tr><td>After</td><td>25</td><td>15</td><td>20</td><td>50</td><td>50</td><td>35</td></tr>
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<table>
<tr><td></td><td>tCLS</td><td>tWP</td><td>tDS</td><td>tWC</td><td>tADL</td><td>tRP</td><td>tRC</td></tr>
<tr><td>Before</td><td>12</td><td>12</td><td>12</td><td>25</td><td>70</td><td>12</td><td>25</td></tr>
<tr><td>After</td><td>15</td><td>15</td><td>15</td><td>30</td><td>100</td><td>15</td><td>30</td></tr>
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3) Add tCRRH (100ns, Min)
- tCRRH: cache Read $\overline{RE}$ High
4) Change 3rd Read ID
- 3rd Read ID is changed to C1h
- 3rd Byte of Device Identifier Table is added.
5) Change NOP
- Number of Partial Program Cycle in the same page is changed to 4.
6) Delete Concurrent Operation.</td><td>Oct. 23. 2005</td><td>Preliminary</td></tr>
<tr><td>0.2</td><td>1) Change AC Characteristics
<table>
<tr><td></td><td>tREA</td><td>tCEA</td><td>tCS</td></tr>
<tr><td>Before</td><td>20</td><td>35</td><td>20</td></tr>
<tr><td>After</td><td>25</td><td>30</td><td>25</td></tr>
</table></td><td>Nov. 16. 2005</td><td>Preliminary</td></tr>
</table>

Revision History

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<table>
<tr><th>Revision No.</th><th>History</th><th>Draft Date</th><th>Remark</th></tr>
<tr><td>0.3</td><td>1) Correct Read ID naming
2) Add ECC algorithm. (1bit/512bytes)
3) Change valid block number (max)
<table>
<tr><td></td><td>valid block number</td></tr>
<tr><td>Before</td><td>8092</td></tr>
<tr><td>After</td><td>8192</td></tr>
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4) Change NOP
5) Change DC characterics
<table>
<tr><td rowspan="2"></td><td colspan="2">ICC1</td><td colspan="2">ICC2</td><td colspan="2">ICC3</td></tr>
<tr><td>Typ</td><td>Max</td><td>Typ</td><td>Max</td><td>Typ</td><td>Max</td></tr>
<tr><td>Before</td><td>25</td><td>45</td><td>25</td><td>45</td><td>25</td><td>45</td></tr>
<tr><td>After</td><td>15</td><td>30</td><td>15</td><td>30</td><td>15</td><td>30</td></tr>
</table>
6) Delete TSOP 1CE package dimension & figures.</td><td>Jun. 20. 2006</td><td>Preliminary</td></tr>
<tr><td>0.4</td><td>1) Delete Preliminary.</td><td>Jul. 10. 2006</td><td></td></tr>
<tr><td>0.5</td><td>1) Correct copy back function.</td><td>Oct. 02. 2006</td><td></td></tr>
<tr><td>0.6</td><td>1) Delete PRE function.
2) Delete Lock & Unlock function.
3) Delete Auto Read function.</td><td>Dec. 26. 2006</td><td></td></tr>
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FEATURES SUMMARY

HIGH DENSITY NAND FLASH MEMORIES

- Cost effective solutions for mass storage applications

NAND INTERFACE

- x8 width.
- Multiplexed Address/ Data
- Pinout compatibility for all densities

SUPPLY VOLTAGE

- 3.3V device: VCC = 2.7 to 3.6V : HY27UG088G(5/D)M

Memory Cell Array

= (2K+ 64) Bytes x 64 Pages x 8,192 Blocks

PAGE SIZE

- x8 device : (2K + 64 spare) Bytes
  : HY27UG088G(5/D)M

BLOCK SIZE

- x8 device: (128K + 4K spare) Bytes

PAGE READ / PROGRAM

- Random access: 25us (max.)
- Sequential access: 30ns (min.)
- Page program time: 200us (typ.)

COPY BACK PROGRAM MODE

- Fast page copy without external buffering

CACHE PROGRAM MODE

- Internal Cache Register to improve the program throughput

FAST BLOCK ERASE

- Block erase time: 2ms (Typ.)

STATUS REGISTER

ELECTRONIC SIGNATURE

- 1st cycle: Manufacturer Code
- 2nd cycle: Device Code

CHIP ENABLE DON'T CARE

- Simple interface with microcontroller

SERIAL NUMBER OPTION

HARDWARE DATA PROTECTION

- Program/Erase locked during Power transitions

DATA INTEGRITY

- 100,000 Program/Erase cycles (with 1bit/512byte ECC)
- 10 years Data Retention

PACKAGE

- HY27UG088G5M-T(P)
  : 48-Pin TSOP1 (12 x 20 x 1.2 mm)
  - HY27UG088G5M-T (Lead)
  - HY27UG088G5M-TP (Lead Free)

- HY27UG088GDM-UP
  :52- ULGA (12 x 17 x 0.65 mm)
  - HY27UG088GDM-DP (Lead Free)

1. SUMMARY DESCRIPTION

The HYNIX HY27UG088G(5/D)M series is a 1Gx8bit with spare 32Mx8 bit capacity. The device is offered in 3.3V Vcc Power Supply.
Its NAND cell provides the most cost-effective solution for the solid state mass storage market.
The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased.
The device contains 8192 blocks, composed by 64 pages consisting in two NAND structures of 32 series connected Flash cells.
A program operation allows to write the 2112-byte page in typical 200us and an erase operation can be performed in typical 2ms on a 128K-byte(X8 device) block.
Data in the page mode can be read out at 30ns cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command input. This interface allows a reduced pin count and easy migration towards different densities, without any rearrangement of footprint.
Commands, Data and Addresses are synchronously introduced using $\overline{CE}$, $\overline{WE}$, ALE and CLE input pin.
The on-chip Program/Erase Controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data.
The modifying can be locked using the $\overline{WP}$ input pin.
The output pin R/$\overline{B}$ (open drain buffer) signals the status of the device during each operation. In a system with multiple memories the R/$\overline{B}$ pins can be connected all together to provide a global status signal.
Even the write-intensive systems can take advantage of the HY27UG088G(2/5/D)M extended reliability of 100K program/erase cycles by providing ECC (Error Correcting Code) with real time mapping-out algorithm.

The chip could be offered with the $\overline{CE}$ don't care function. This function allows the direct download of the code from the NAND Flash memory device by a microcontroller, since the $\overline{CE}$ transitions do not stop the read operation.

The copy back function allows the optimization of defective blocks management: when a page program operation fails the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase.

The cache program feature allows the data insertion in the cache register while the data register is copied into the flash array. This pipelined program operation improves the program throughput when long files are written inside the memory.

A cache read feature is also implemented. This feature allows to dramatically improve the read throughput when consecutive pages have to be streamed out.

This device includes also extra features like OTP/Unique ID area, Read ID2 extension.

The HYNIX HY27UG088G(5/D)M series is available in 48 - TSOP1 12 x 20 mm, 52-ULGA 12 x 17 mm.

1.1 Product List

PART NUMBER	ORIZATION	VCC RANGE	PACKAGE
HY27UG088G5M	x8	2.7V - 3.6 Volt	48TSOP1
HY27UG088GDM	x8	2.7V - 3.6 Volt	52-ULGA

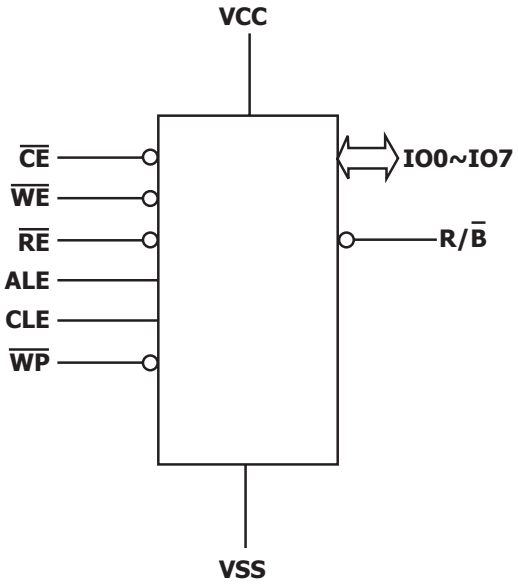


Figure1: Logic Diagram

IO7 - IO0	Data Input / Outputs
CLE	Command latch enable
ALE	Address latch enable
$\overline{CE}$	Chip Enable
$\overline{RE}$	Read Enable
$\overline{WE}$	Write Enable
$\overline{WP}$	Write Protect
R/$\overline{B}$	Ready / Busy
Vcc	Power Supply
Vss	Ground
NC	No Connection

Table 1: Signal Names

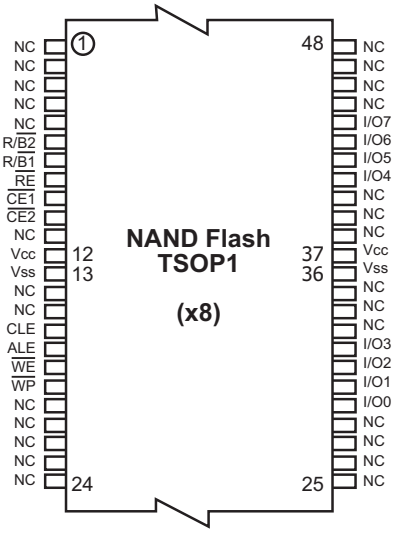


Figure 2. 48TSOP1 Contactions, x8 Device (2CE)

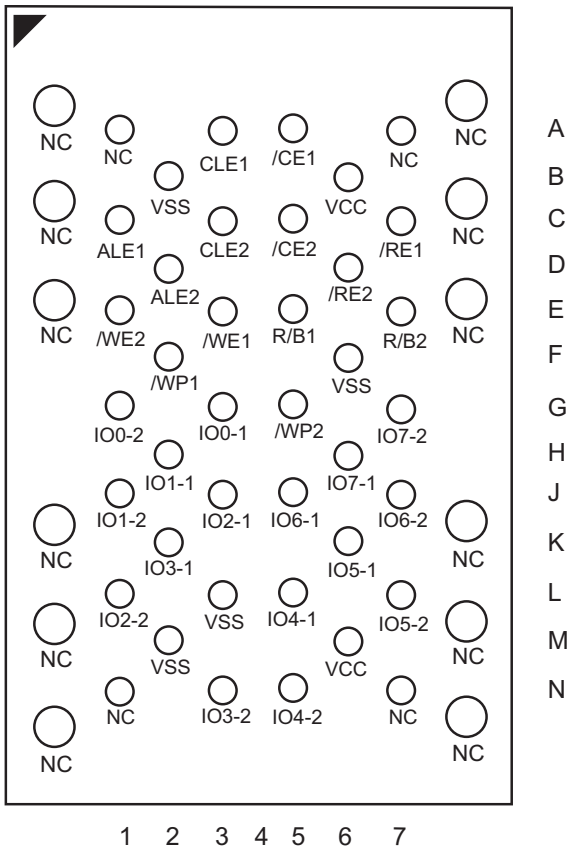


Figure 3. 52-ULGA Contactions, x8 Device, Dual interface
(Top view through package)

1.2 PIN DESCRIPTION

Pin Name	Description
IO0-IO7	**DATA INPUTS/OUTPUTS** The IO pins allow to input command, address and data and to output data during read / program operations. The inputs are latched on the rising edge of Write Enable ($\overline{WE}$). The I/O buffer float to High-Z when the device is deselected or the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** This input activates the latching of the IO inputs inside the Command Register on the Rising edge of Write Enable ($\overline{WE}$).
ALE	**ADDRESS LATCH ENABLE** This input activates the latching of the IO inputs inside the Address Register on the Rising edge of Write Enable ($\overline{WE}$).
$\overline{CE1}$, $\overline{CE2}$	**CHIP ENABLE** This input controls the selection of the device. When the device is busy $\overline{CE1}$, $\overline{CE2}$ low does not deselect the memory.
$\overline{WE}$	**WRITE ENABLE** This input acts as clock to latch Command, Address and Data. The IO inputs are latched on the rise edge of $\overline{WE}$.
$\overline{RE}$	**READ ENABLE** The $\overline{RE}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of $\overline{RE}$ which also increments the internal column address counter by one.
$\overline{WP}$	**WRITE PROTECT** The $\overline{WP}$ pin, when Low, provides an Hardware protection against undesired modify (program / erase) operations.
R/$\overline{B1}$, R/$\overline{B2}$	**READY BUSY** The Ready/Busy output is an Open Drain pin that signals the state of the memory.
VCC	**SUPPLY VOLTAGE** The VCC supplies the power for all the operations (Read, Write, Erase).
VSS	GROUND
NC	NO CONNECTION

Table 2: Pin Description

NOTE:

1. A 0.1uF capacitor should be connected between the VCC Supply Voltage pin and the VSS Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.

	IO0	IO1	IO2	IO3	IO4	IO5	IO6	IO7
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A8	A9	A10	A11	L(1)	L(1)	L(1)	L(1)
3rd Cycle	A12	A13	A14	A15	A16	A17	A18	A19
4th Cycle	A20	A21	A22	A23	A24	A25	A26	A27
5th Cycle	A28	A29	L(1)	L(1)	L(1)	L(1)	L(1)	L(1)

Table 3: Address Cycle Map(2CE & Dual)

NOTE:

1. L must be set to Low.

FUNCTION	1st CYCLE	2nd CYCLE	3rd CYCLE	Acceptable command during busy
READ 1	00h	30h	-	
READ FOR COPY-BACK	00h	35h	-	
READ ID	90h	-	-	
RESET	FFh	-	-	Yes
PAGE PROGRAM (start)	80h	10h	-	
COPY BACK PGM (start)	85h	10h	-	
CACHE PROGRAM	80h	15h	-	
BLOCK ERASE	60h	D0h	-	
READ STATUS REGISTER	70h	-	-	Yes
RANDOM DATA INPUT	85h	-	-	
RANDOM DATA OUTPUT	05h	E0h	-	
CACHE READ START	00h	31h	-	
CACHE READ EXIT	34h	-	-	

Table 4: Command Set

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	MODE	
H	L	L	Rising	H	X	Read Mode	Command Input
L	H	L	Rising	H	X		Address Input(5 cycles)
H	L	L	Rising	H	H	Write Mode	Command Input
L	H	L	Rising	H	H		Address Input(5 cycles)
L	L	L	Rising	H	H	Data Input	
L	L	L(1)	H	Falling	X	Sequential Read and Data Output	
L	L	L	H	H	X	During Read (Busy)	
X	X	X	X	X	H	During Program (Busy)	
X	X	X	X	X	H	During Erase (Busy)	
X	X	X	X	X	L	Write Protect	
X	X	H	X	X	0V/Vcc	Stand By	

Table 5: Mode Selection

NOTE:

1. With the $\overline{CE}$ high during latency time does not stop the read operation

2. BUS OPERATION

There are six standard bus operations that control the device. These are Command Input, Address Input, Data Input, Data Output, Write Protect, and Standby.
Typically glitches less than 5 ns on Chip Enable, Write Enable and Read Enable are ignored by the memory and do not affect bus operations.

2.1 Command Input.

Command Input bus operation is used to give a command to the memory device. Command are accepted with Chip Enable low, Command Latch Enable High, Address Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modifying operation (write/erase) the Write Protect pin must be high. See figure 5 and table 12 for details of the timings requirements. Command codes are always applied on IO7:0, disregarding the bus configuration (X8).

2.2 Address Input.

Address Input bus operation allows the insertion of the memory address. To insert the 30(1) addresses needed to access the 8Gbit 5 clock cycles are needed. Addresses are accepted with Chip Enable low, Address Latch Enable High, Command Latch Enable low and Read Enable high and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/erase) the Write Protect pin must be high. See figure 6 and table 12 for details of the timings requirements. Addresses are always applied on IO7:0, disregarding the bus configuration (X8).

2.3 Data Input.

Data Input bus operation allows to feed to the device the data to be programmed. The data insertion is serially and timed by the Write Enable cycles. Data are accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low, Read Enable High, and Write Protect High and latched on the rising edge of Write Enable. See figure 7 and table 12 for details of the timings requirements.

2.4 Data Output.

Data Output bus operation allows to read data from the memory array and to check the status register content, the ID data. Data can be serially shifted out toggling the Read Enable pin with Chip Enable low, Write Enable High, Address Latch Enable low, and Command Latch Enable low. See figures 8,10,11 and table 12 for details of the timings requirements.

2.5 Write Protect.

Hardware Write Protection is activated when the Write Protect pin is low. In this condition modify operation do not start and the content of the memory is not altered. Write Protect pin is not latched by Write Enable to ensure the protection even during the power up.

2.6 Standby.

In Standby mode the device is deselected, outputs are disabled and Power Consumption is reduced.

NOTE:

1. 29 addresses are needed to access HY27UG088G5M & HY27UG088GDM.

3. DEVICE OPERATION

3.1 Page Read.

Page read operation is initiated by writing 00h and 30h to the command register along with five address cycles. In two consecutive read operations, the second one doesn't need 00h command, which five address cycles and 30h command initiates that operation. Two types of operations are available : random read, serial page read. The random read mode is enabled when the page address is changed. The 2112 bytes (X8 device) of data within the selected page are transferred to the data registers in less than 25us(tR). The system controller may detect the completion of this data transfer (tR) by analyzing the output of R/B pin. Once the data in a page is loaded into the data registers, they may be read out in 30ns cycle time by sequentially pulsing $\overline{RE}$. The repetitive high to low transitions of the $\overline{RE}$ clock make the device output the data starting from the selected column address up to the last column address.

The device may output random data in a page instead of the consecutive sequential data by writing random data output command.

The column address of next data, which is going to be out, may be changed to the address which follows random data output command.

Random data output can be operated multiple times regardless of how many times it is done in a page.

3.2 Page Program.

The device is programmed basically by page, but it does allow multiple partial page programming of a word or consecutive bytes up to 2112 (X8 device) , in a single page program cycle. The number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed 4 times for main array (X8 device:1time/512byte) and 4 times for spare array (X8 device:1time/16byte).

The addressing should be done in sequential order in a block [1]. A page program cycle consists of a serial data loading period in which up to 2112bytes (X8 device) or 1056words (X16 device) of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the five cycle address inputs and then serial data. The words other than those to be programmed do not need to be loaded. The device supports random data input in a page. The column address of next data, which will be entered, may be changed to the address which follows random data input command (85h). Random data input may be operated multiple times regardless of how many times it is done in a page.

The Page Program confirm command (10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write state controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit (I/O 0) may be checked. The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register. Figure 14 details the sequence.

3.3 Block Erase.

The Erase operation is done on a block basis. Block address loading is accomplished in three cycles initiated by an Erase Setup command (60h). Only address A18 to A29 (X8) is valid while A12 to A17 (X8) is ignored. The Erase Confirm command (D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions. At the rising edge of $\overline{WE}$ after the erase confirm command input, the internal write controller handles erase and erase-verify. Once the erase process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of an erase by monitoring the R/$\overline{B}$ output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while erasing is in progress. When the erase operation is completed, the Write Status Bit (I/O 0) may be checked.
Figure 19 details the sequence.

3.4 Copy-Back Program.

The copy-back program is configured to quickly and efficiently rewrite data stored in one page without utilizing an external memory. Since the time-consuming cycles of serial access and re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block also need to be copied to the newly assigned free block. The operation for performing a copy-back program is a sequential execution of page-read without serial access and copying-program with the address of destination page. A read operation with "35h" command and the address of the source page moves the whole 2112byte (X8 device) data into the internal data buffer. As soon as the device returns to Ready state, Copy Back command (85h) with the address cycles of destination page may be written. The Program Confirm command (10h) is required to actually begin the programming operation. Data input cycle for modifying a portion or multiple distant portions of the source page is allowed as shown in Figure 16.

"When there is a program-failure at Copy-Back operation, error is reported by pass/fail status. But, if Copy-Back operations are accumulated over time, bit error due to charge loss is not checked by external error detection/correction scheme. For this reason, two bit error correction is recommended for the use of Copy-Back operation."

Figure 16 shows the command sequence for the copy-back operation.

The Copy Back Program operation requires three steps:

1. The source page must be read using the Read A command (one bus write cycle to setup the command and then 5 bus write cycles to input the source page address). This operation copies all 2KBytes from the page into the Page Buffer.
2. When the device returns to the ready state (Ready/Busy High), the second bus write cycle of the command is given with the 5bus cycles to input the target page address. A29 must be the same for the Source and Target Pages.
3. Then the confirm command is issued to start the P/E/R Controller.

NOTE:

1. Copy-Back Program operation is allowed only within the same memory plane.
2. On the same plane, It's prohibited to operate copy-back program from an odd address page (source page) to an even address page (target page) or from an even address page (source page) to an odd address page (target page). Therefore, the copy-back program is permitted just between odd address pages or even address pages.

3.5 Read Status Register.

The device contains a Status Register which may be read to find out whether read, program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/$\overline{B}$ pins are common-wired. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status. Refer to table 13 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command (00h) should be given before starting read cycles. See figure 10 for details of the Read Status operation.

3.6 Read ID.

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Four read cycles sequentially output the manufacturer code (ADh), and the device code and 3rd cycle ID, 4th cycle ID, respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 20 shows the operation sequence, while tables 15 explain the byte meaning.

3.7 Reset.

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value E0h when $\overline{WP}$ is high. Refer to table 13 for device status after reset operation. If the device is already in reset state a new reset command will not be accepted by the command register. The R/$\overline{B}$ pin transitions to low for tRST after the Reset command is written. Refer to figure 25.

3.8 Cache Program.

Cache Program is an extension of Page Program, which is executed with 2112byte (X8 device) data registers, and is available only within a block. Since the device has 1 page of cache memory, serial data input may be executed while data stored in data register are programmed into memory cell. After writing the first set of data up to 2112byte (X8 device) or 1056word (X16 device) into the selected cache registers, Cache Program command (15h) instead of actual Page Program (10h) is input to make cache registers free and to start internal program operation. To transfer data from cache registers to data registers, the device remains in Busy state for a short period of time (tCBSY) and has its cache registers ready for the next data-input while the internal programming gets started with the data loaded into data registers. Read Status command (70h) may be issued to find out when cache registers become ready by polling the Cache-Busy status bit (I/O 6). Pass/fail status of only the previous page is available upon the return to Ready state. When the next set of data is input with the Cache Program command, tCBSY is affected by the progress of pending internal programming. The programming of the cache registers is initiated only when the pending program cycle is finished and the data registers are available for the transfer of data from cache registers. The status bit (I/O5) for internal Ready/Busy may be polled to identify the completion of internal programming.

If the system monitors the progress of programming only with R/$\overline{B}$, the last page of the target programming sequence must be programmed with actual Page Program command (10h). If the Cache Program command (15h) is used instead, status bit (I/O5) must be polled to find out when the last programming is actually finished before starting other operations such as read. Pass/fail status is available in two steps. I/O 1 returns with the status of the previous page upon Ready or I/O6 status bit changing to "1", and later I/O 0 with the status of current page upon true Ready (returning from internal programming) or I/O 5 status bit changing to "1". I/O 1 may be read together when I/O 0 is checked. See figure 18 for more details.

NOTE : Since programming the last page does not employ caching, the program time has to be that of Page Program. However, if the previous program cycle with the cache data has not finished, the actual program cycle of the last page is initiated only after completion of the previous cycle, which can be expressed as the following formula.

tPROG= Program time for the last page+ Program time for the (last -1)th page -
(Program command cycle time + Last page data loading time)

The value for A29 from second to the last page address must be same as the value given to A29 in first address.

3.9 Cache Read

Cache read operation allows automatic download of consecutive pages, up to the whole device. Immediately after 1st latency end, while user can start reading out data, device internally starts reading following page.
Start address of 1st page is at page start (A<10:0>=00h), after 1st latency time (tr) , automatic data download will be uninterrupted. In fact latency time is 25us, while download of a page require at least 100us for x8 device.
Cache read operation command is like standard read, except for confirm code (30h for standard read, 31h for cache read) user can check operation status using :

- R/$\overline{B}$ ('0' means latency ongoing, download not possible, '1' means download of n page possible, even if device internally is active on n+1 page
- Status register (SR<6> behave like R/$\overline{B}$, SR<5> is '0' when device is internally reading and '1' when device is idle)

To exit cache read operation a cache read exit command (34h) must be issued. this command can be given any time (both device idle and reading).
If device is active (SR<5>=0) it will go idle within 5us, while if it is not active, device itself will go busy for a time shorter then tRBSY before becoming again idle and ready to accept any further commands.
If user arrives reading last byte/word of the memory array, then has to stop by giving a cache read exit command.
Random data output is not available in cache read.

Cache read operation must be done only block by block if system needs to avoid reading also from invalid blocks.

4. OTHER FEATURES

4.1 Data Protection & Power on/off Sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 2V(3.3V device). $\overline{WP}$ pin provides hardware protection and is recommended to be kept at VIL during power-up and power-down. A recovery time of minimum 10us is required before internal circuit gets ready for any command sequences as shown in Figure 26. The two-step command sequence for program/erase provides additional software protection.

If the power is dropped during the ready read/write/erase operation, Power protection function may not guaranteed the data. Power protection function is only available during the power on/off sequence.

4.2 Ready/Busy.

The device has a Ready/Busy output that provides method of indicating the completion of a page program, erase, copy-back, cache program and random read completion. The R/$\overline{B}$ pin is normally high and goes to low when the device is busy (after a reset, read, program, erase operation). It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{B}$ outputs to be Or-tied. Because pull-up resistor value is related to tr(R/$\overline{B}$) and current drain during busy (Ibusy), an appropriate value can be obtained with the following reference chart (Fig 27). Its value can be determined by the following guidance.

Parameter	Symbol	Min	Typ	Max	Unit
Valid Block Number	N_{VB}	8032		8192	Blocks

Table 6: Valid Blocks Number

NOTE:

1. The 1st block is guaranteed to be a valid block up to 1K cycles with ECC. (1bit/512bytes)

Symbol	Parameter	Value	Unit
		3.3V	
T_A	Ambient Operating Temperature (Commercial Temperature Range)	0 to 70	℃
	Ambient Operating Temperature (Extended Temperature Range)	-25 to 85	℃
	Ambient Operating Temperature (Industry Temperature Range)	-40 to 85	℃
T_{BIAS}	Temperature Under Bias	-50 to 125	℃
T_{STG}	Storage Temperature	-65 to 150	℃
V_{IO}(2)	Input or Output Voltage	-0.6 to 4.6	V
Vcc	Supply Voltage	-0.6 to 4.6	V

Table 7: Absolute maximum ratings

NOTE:

1. Except for the rating “Operating Temperature Range”, stresses above those listed in the Table “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

2. Minimum Voltage may undershoot to -2V during transition and for less than 20ns during transitions.

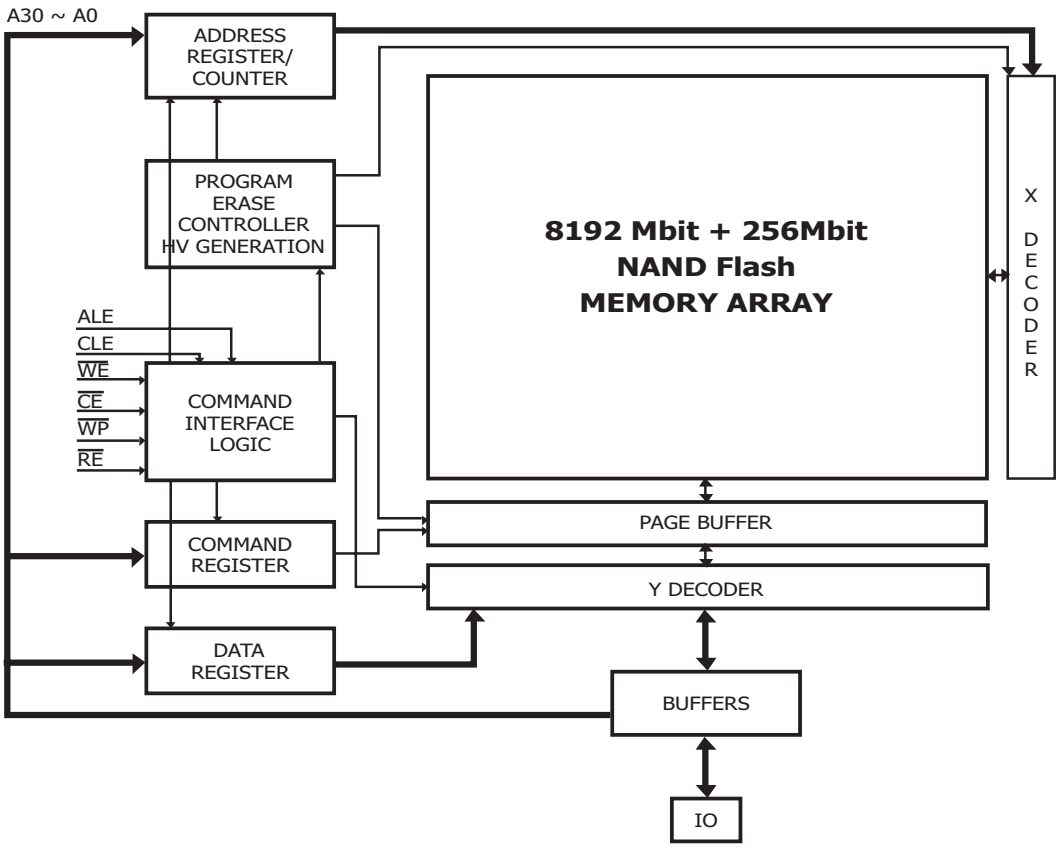


Figure 4: Block Diagram

Parameter		Symbol	Test Conditions		3.3Volt			Unit
					Min	Typ	Max	
Operating Current	Sequential Read	I_{CC1}	t_{RC}=30ns, $\overline{CE}$=V_{IL}, I_{OUT}=0mA		-	15	30	mA
	Program	I_{CC2}	-		-	15	30	mA
	Erase	I_{CC3}	-		-	15	30	mA
Stand-by Current (TTL)		I_{CC4}	$\overline{CE}$=V_{IH}, $\overline{WP}$=0V/Vcc		-		1	mA
Stand-by Current (CMOS)		I_{CC5}	$\overline{CE}$=Vcc-0.2, $\overline{WP}$=0V/Vcc		-	20	100	uA
Input Leakage Current		I_{LI}	V_{IN}=0 to Vcc (max)	Single & 2CE	-	-	± 20	uA
				Dual	-	-	± 10	uA
Output Leakage Current		I_{LO}	V_{OUT} =0 to Vcc (max)	Single & 2CE	-	-	± 20	uA
				Dual	-	-	± 10	uA
Input High Voltage		V_{IH}	-		Vccx0.8	-	Vcc+0.3	V
Input Low Voltage		V_{IL}	-		-0.3	-	Vccx0.2	V
Output High Voltage Level		V_{OH}	I_{OH}=-400uA		2.4	-	-	V
Output Low Voltage Level		V_{OL}	I_{OL}=2.1mA		-	-	0.4	V
Output Low Current (R/$\overline{B}$)		I_{OL} (R/$\overline{B}$)	V_{OL}=0.4V		8	10	-	mA

Table 8: DC and Operating Characteristics

Parameter	Value
	3.3Volt
Input Pulse Levels	0V to Vcc
Input Rise and Fall Times	5ns
Input and Output Timing Levels	Vcc/2
Output Load (2.7V - 3.3V)	1 TTL GATE and CL=50pF
Output Load (3.0 - 3.6V)	1 TTLGATE and CL=100pF

Table 9: AC Conditions

Item	Symbol	Test Condition	Min	Max		Unit
				HY27UG088G5M-T(P)	HY27UG088GDM-UP	
Input / Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	20	15	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	20	15	pF

Table 10: Pin Capacitance (TA=25C, F=1.0MHz)

Parameter		Symbol	Min	Typ	Max	Unit
Program Time		t_{PROG}	-	200	700	us
Dummy Busy Time for Cache Program		t_{CBSY}	-	3	700	us
Dummy Busy Time for Cache Read		t_{RBSY}	-	5	-	us
Number of partial Program Cycles in the same page	Main Array	NOP	-	-	4	Cycles
	Spare Array	NOP	-	-	4	Cycles
Block Erase Time		t_{BERS}	-	2	3	ms

Table 11: Program / Erase Characteristics

Parameter	Symbol	3.3Volt		Unit
		Min	Max	
CLE Setup time	tCLS	15		ns
CLE Hold time	tCLH	5		ns
$\overline{CE}$ setup time	tCS	25		ns
$\overline{CE}$ hold time	tCH	5		ns
$\overline{WE}$ pulse width	tWP	15		ns
ALE setup time	tALS	15		ns
ALE hold time	tALH	5		ns
Data setup time	tDS	15		ns
Data hold time	tDH	5		ns
Write Cycle time	tWC	30		ns
$\overline{WE}$ High hold time	tWH	10		ns
Address to Data Loading Time	tADL(2)	100		ns
Data Transfer from Cell to register	tR		25	us
ALE to $\overline{RE}$ Delay	tAR	15		ns
CLE to $\overline{RE}$ Delay	tCLR	15		ns
Ready to $\overline{RE}$ Low	tRR	20		ns
$\overline{RE}$ Pulse Width	tRP	15		ns
$\overline{WE}$ High to Busy	tWB		100	ns
Read Cycle Time	tRC	30		ns
$\overline{RE}$ Access Time	tREA		25	ns
$\overline{RE}$ High to Output High Z	tRHZ		50	ns
$\overline{CE}$ High to Output High Z	tCHZ		50	ns
Cache read $\overline{RE}$ High	tCRRH	100		ns
$\overline{RE}$ High to Output Hold	tRHOH	15		ns
$\overline{RE}$ Low to Output Hold	tRLOH	5		ns
$\overline{CE}$ High to Output Hold	tCOH	15		ns
$\overline{RE}$ High Hold Time	tREH	10		ns
Output High Z to $\overline{RE}$ low	tIR	0		ns
$\overline{CE}$ Access Time	tCEA		30	ns
$\overline{WE}$ High to $\overline{RE}$ low	tWHR	60		ns
Device Resetting Time (Read / Program / Copy-Back Program / Erase)	tRST		5/10/40/500(1)	us
Write Protection time	tWW(3)	100		ns

Table 12: AC Timing Characteristics

NOTE:

1. If Reset Command (FFh) is written at Ready state, the device goes into Busy for maximum 5us
2. tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle.
3. Program / Erase Enable Operation : $\overline{WP}$ high to $\overline{WE}$ High.

   Program / Erase Disable Operation : $\overline{WP}$ Low to $\overline{WE}$ High.

IO	Page Program	Block Erase	Cache Program	Read	Cache Read	CODING
0	Pass / Fail	Pass / Fail	Pass / Fail (N)	NA		Pass: '0' Fail: '1'
1	NA	NA	Pass / Fail (N-1)	NA		Pass: '0' Fail: '1' (Only for Cache Program, else Don't care)
2	NA	NA	NA	NA		-
3	NA	NA	NA	NA		-
4	NA	NA	NA	NA		-
5	Ready/Busy	Ready/Busy	P/E/R Controller Bit	Ready/Busy	P/E/R Controller Bit	Active: '0' Idle: '1'
6	Ready/Busy	Ready/Busy	Cache Register Free	Ready/Busy	Ready/Busy	Busy: '0' Ready': '1'
7	Write Protect	Write Protect	Write Protect	Write Protect		Protected: '0' Not Protected: '1'

Table 13: Status Register Coding

DEVICE IDENTIFIER CYCLE	DESCRIPTION
1st	Manufacturer Code
2nd	Device Identifier
3rd	Internal chip number, cell Type, Number of Simultaneously Programmed pages.
4th	Page Size, Block Size, Spare Size, Organization

Table 14: Device Identifier Coding

Part Number	Voltage	Bus Width	1st cycle (Manufacture Code)	2nd cycle (Device Code)	3rd Cycle	4th Cycle
HY27UG088G5M	3.3V	x8	ADh	DCh	80h	95h
HY27UG088GDM	3.3V	x8	ADh	DCh	80h	95h

Table 15: Read ID Data Table

	Description	IO7	IO6	IO5 IO4	IO3 IO2	IO1 IO0
Internal Chip Number	1 2 4 8					0 0 0 1 1 0 1 1
Cell Type	2 Level Cell 4 Level Cell 8 Level Cell 16 Level Cell				0 0 0 1 1 0 1 1	
Number of Simultaneously Programmed Pages	1 2 4 8			0 0 0 1 1 0 1 1		
Interleave Program Between multiple chips	Not Support Support		0 1			
Cache Program	Not Support Support	0 1				

Table 16: 3rd Byte of Device Idendifier Description

	Description	IO7	IO6	IO5-4	IO3	IO2	IO1-0
Page Size (Without Spare Area)	1K 2K Reserved Reserved						0 0 0 1 1 0 1 1
Spare Area Size (Byte / 512Byte)	8 16					0 1	
Serial Access Time	50ns/30ns 25ns Reserved Reserved	0 1 0 1			0 0 1 1		
Block Size (Without Spare Area)	64K 128K 256K Reserved			0 0 0 1 1 0 1 1			
Organization	X8 X16		0 1				

Table 17: 4th Byte of Device Identifier Description

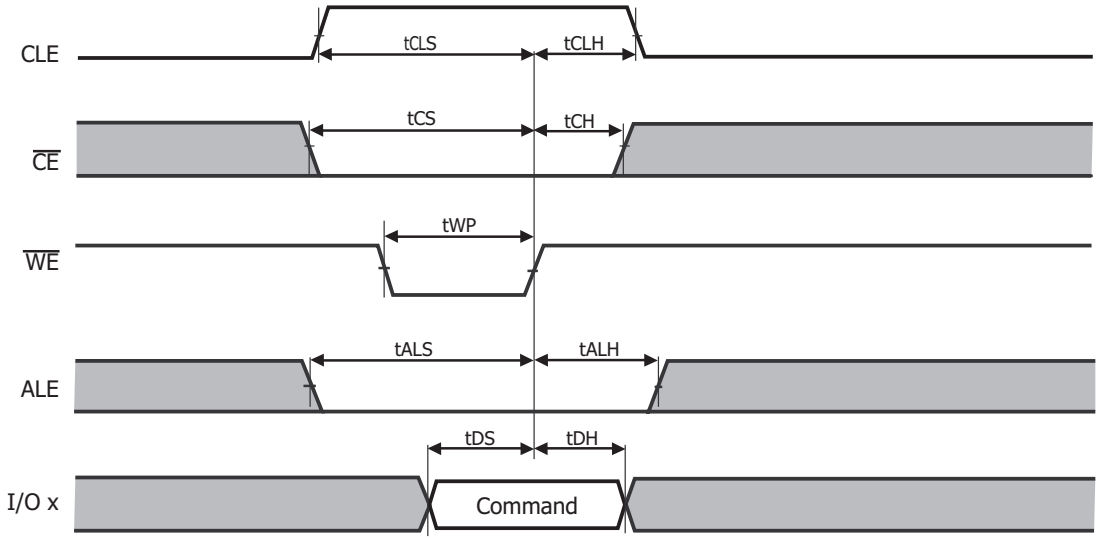


Figure 5: Command Latch Cycle

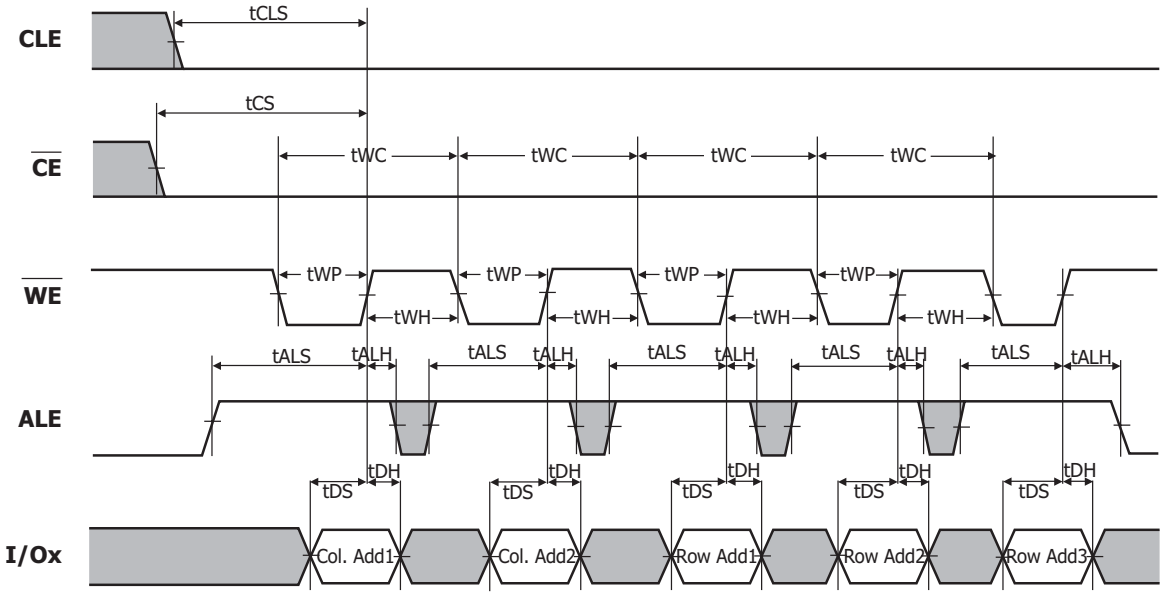
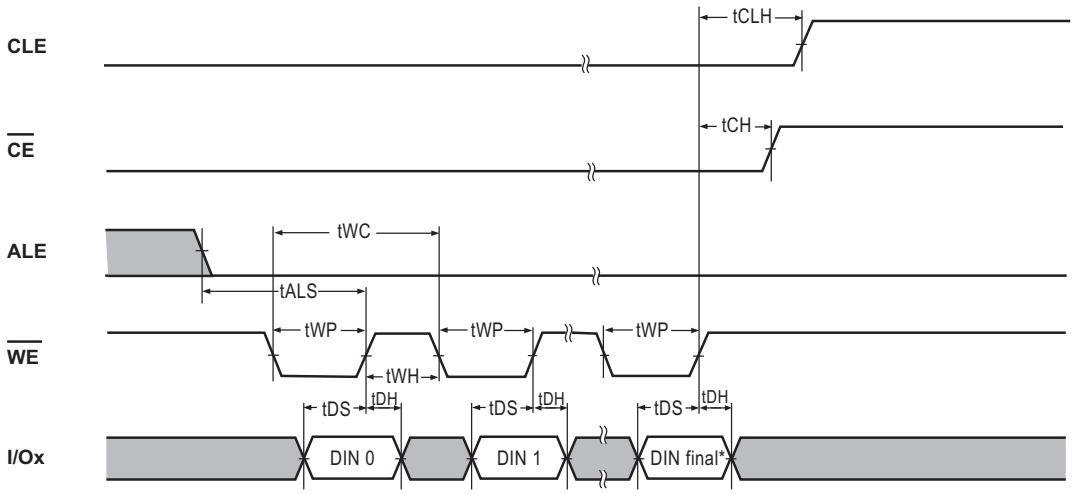
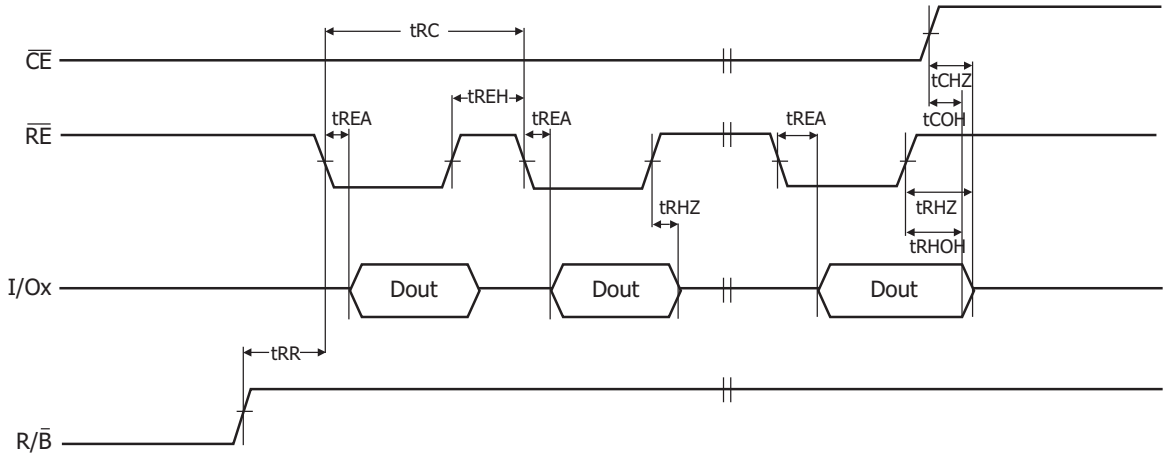


Figure 6: Address Latch Cycle



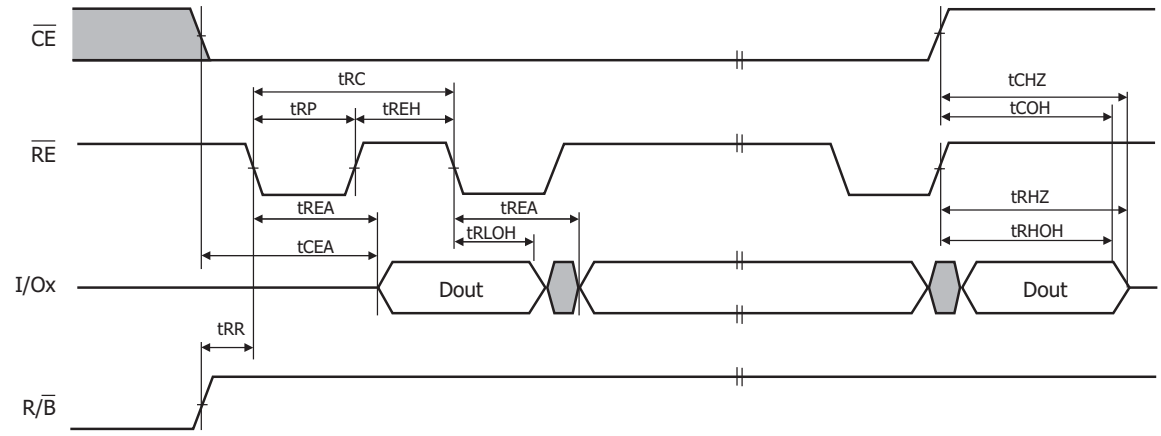
Notes: DIN final means 2,112

Figure 7. Input Data Latch Cycle



Notes: Transition is measured +/-200mV from steady state voltage with load.
This parameter is sampled and not 100% tested. (tCHZ, tRHZ)
tRLOH is valid when frequency is higher than 33MHz.
tRHOH starts to be valid when frequency is lower than 33MHz.

Figure 8: Sequential Out Cycle after Read (CLE=L, $\overline{WE}$=H, ALE=L)



Notes: Transition is measured +/-200mV from steady state voltage with load.
This parameter is sampled and not 100% tested. (tCHZ, tRHZ)
tRLOH is valid when frequency is higher than 33MHz.
tRHOH starts to be valid when frequency is lower than 33MHz.

Figure 9: Sequential Out Cycle after Read (EDO Type CLE=L, $\overline{WE}$=H, ALE=L)

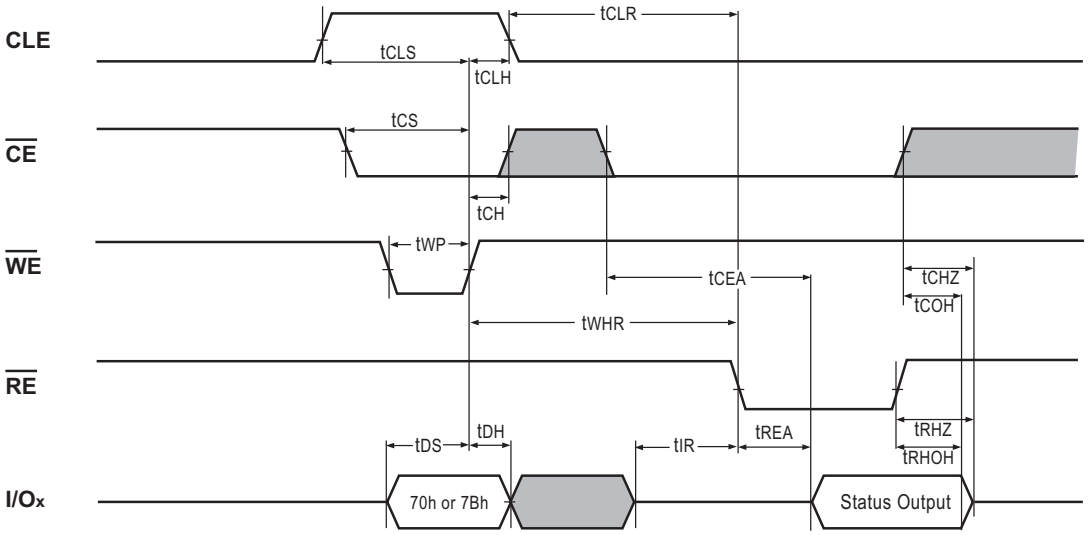


Figure 10: Status Read Cycle

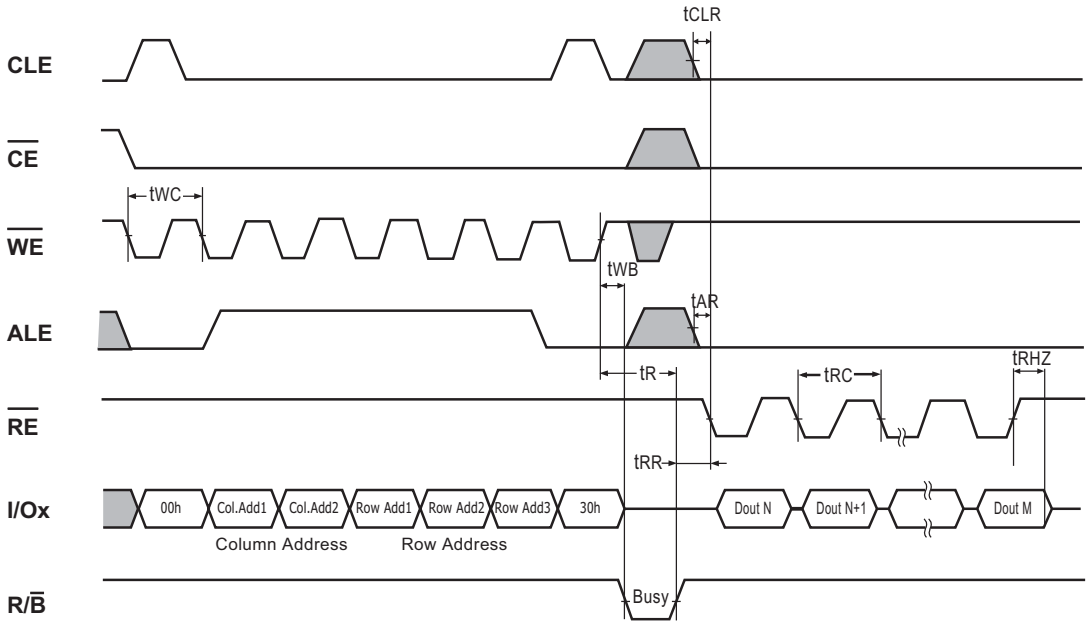


Figure 11: Read1 Operation (Read One Page)

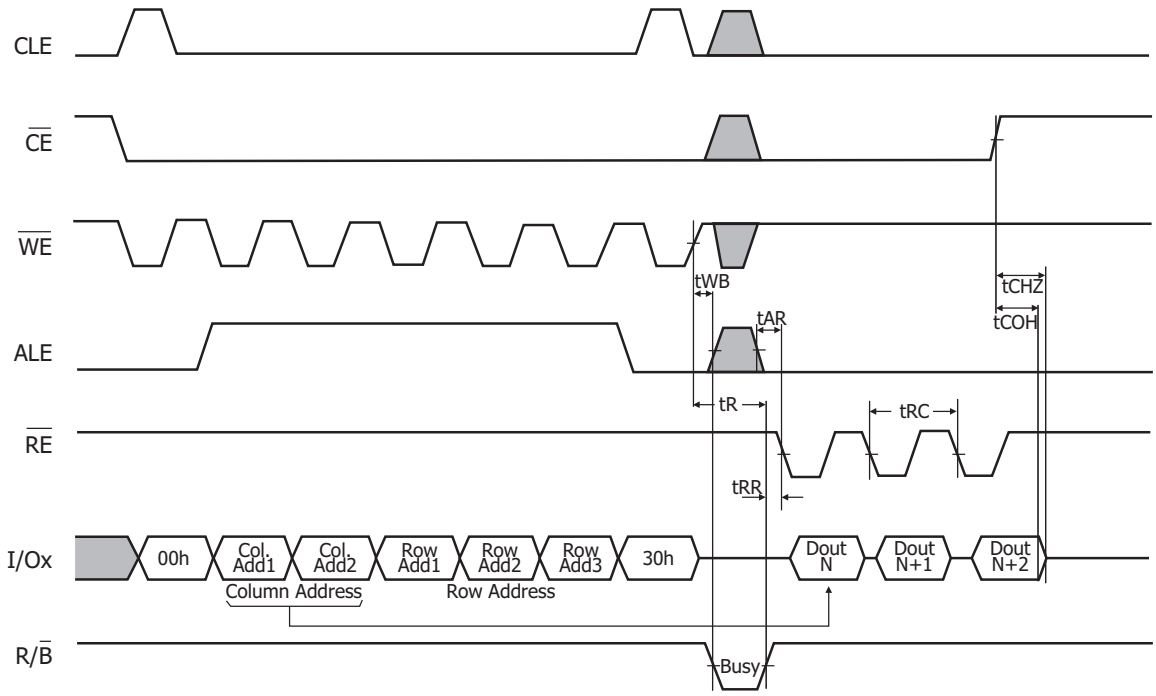


Figure 12: Read1 Operation intercepted by $\overline{CE}$

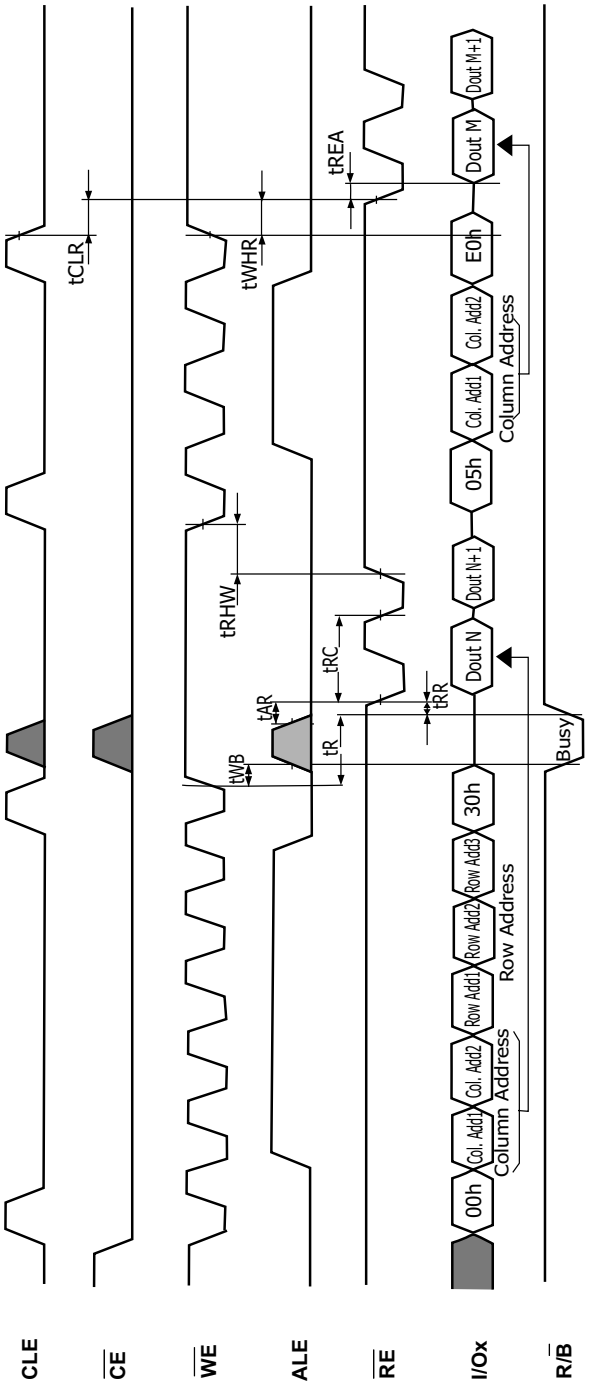


Figure 13 : Random Data output

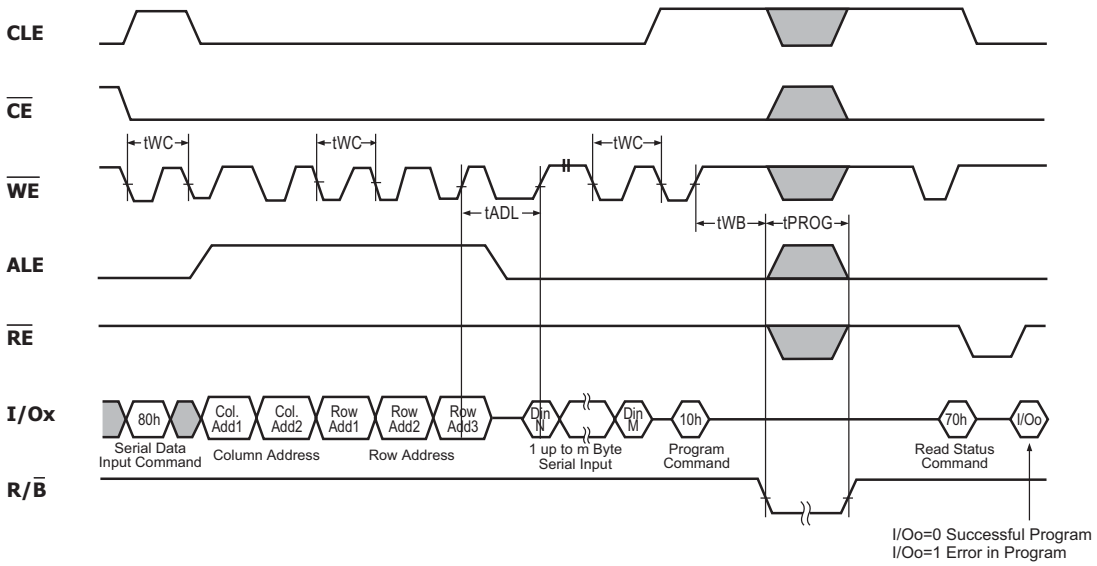


Figure 14: Page Program Operation

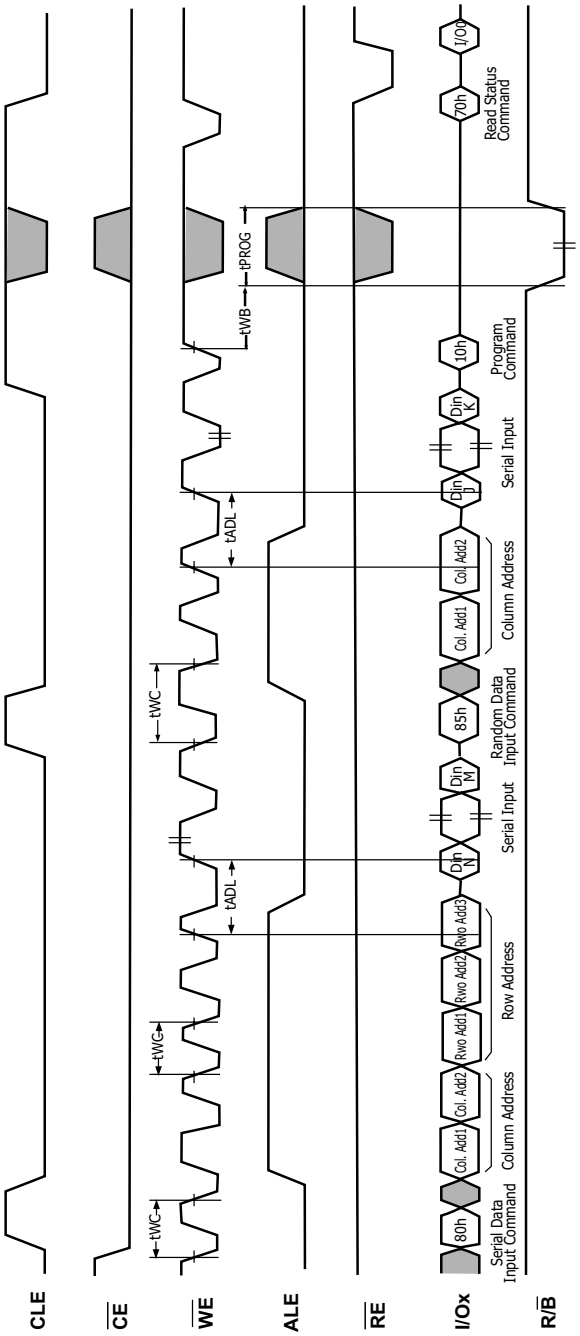


Figure 15 : Random Data In

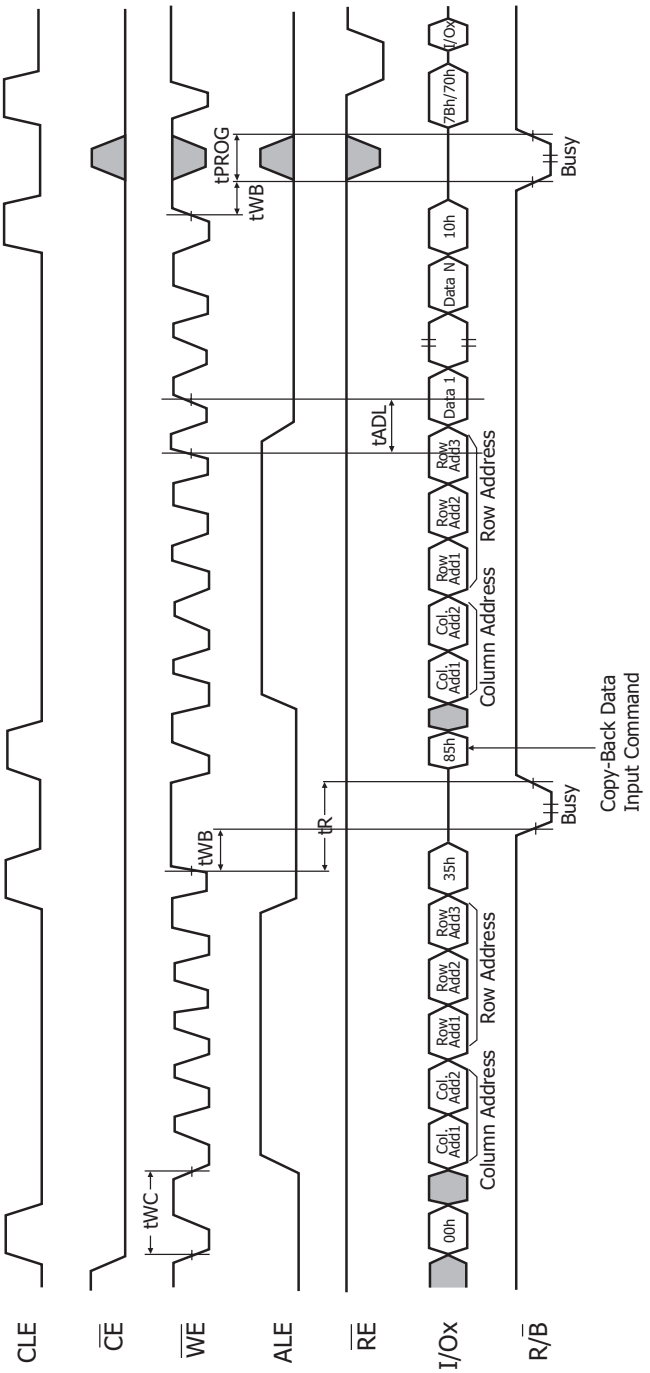


Figure 16 : Copy Back Program

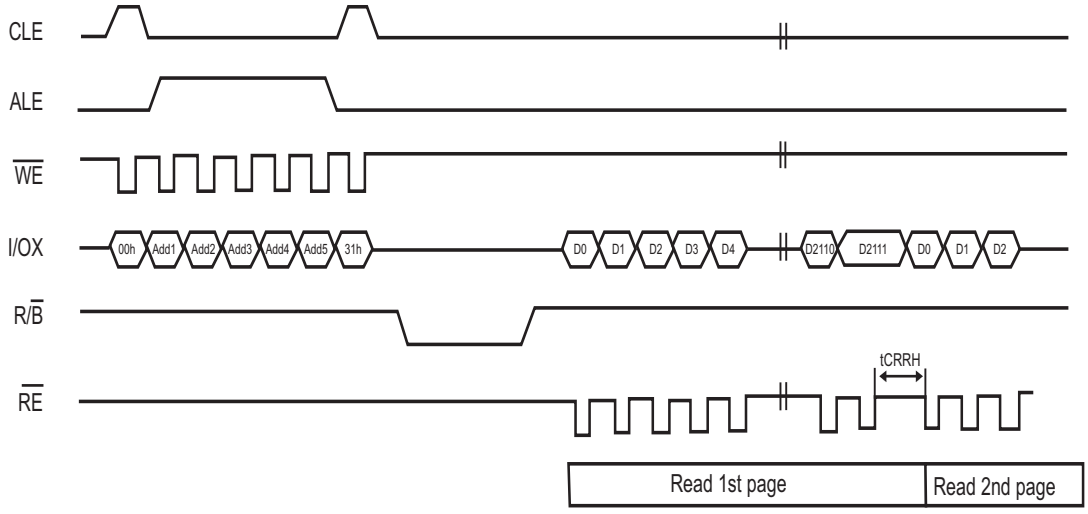


Figure 17: Cache Read $\overline{RE}$ high

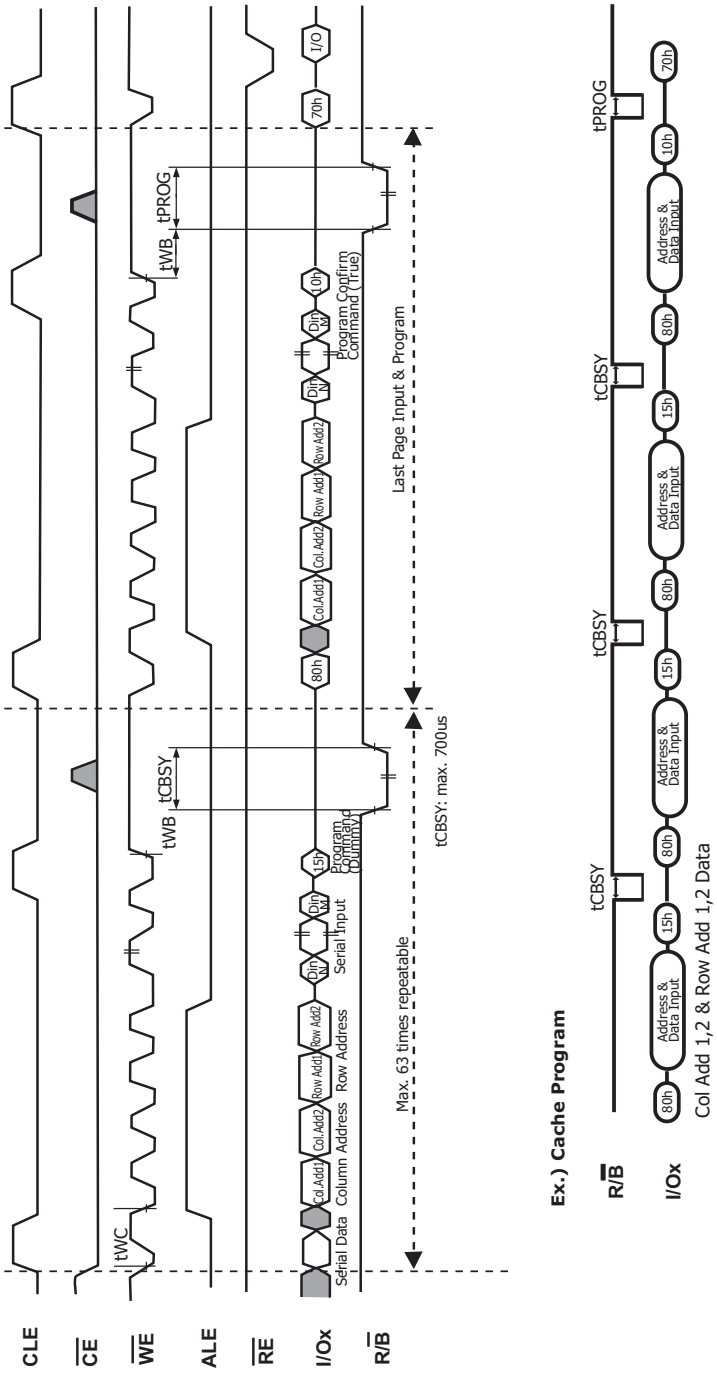


Figure 18 : Cache Program

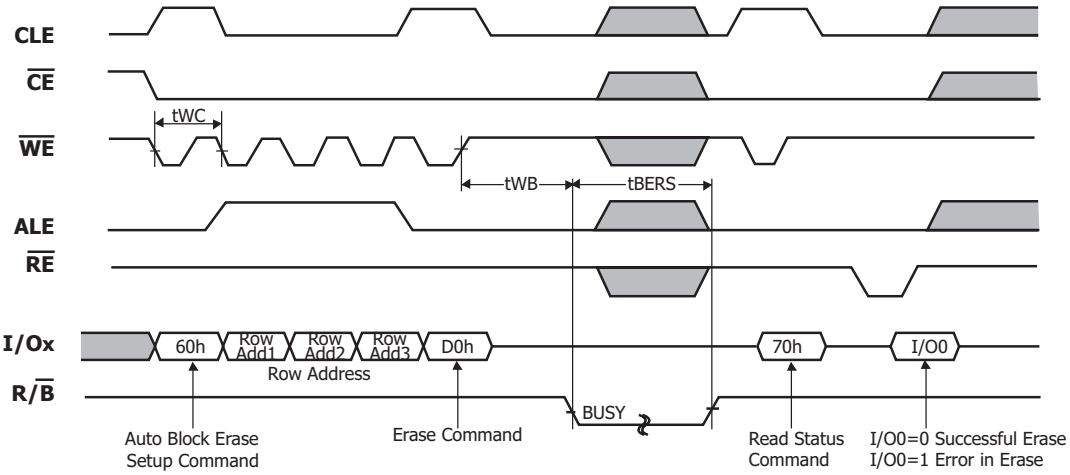


Figure19: Block Erase Operation (Erase One Block)

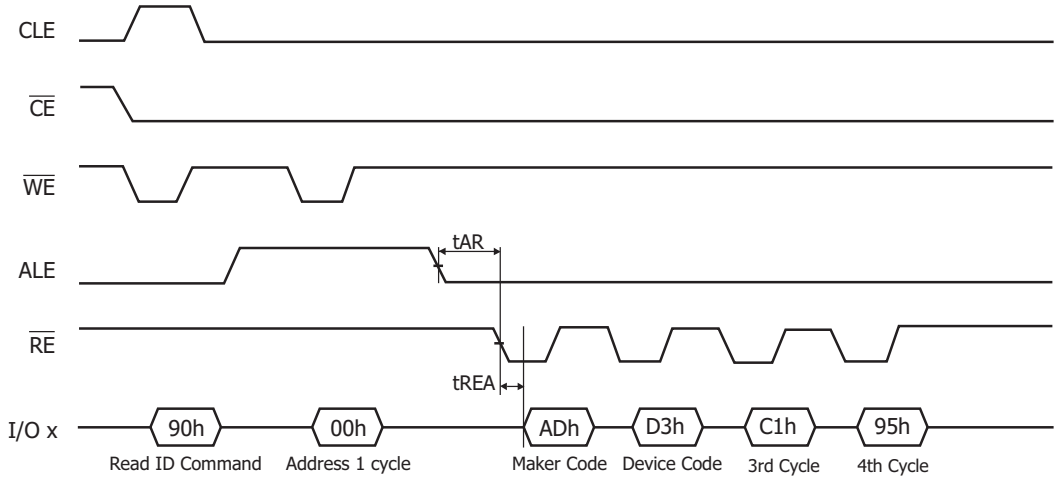


Figure 20: Read ID Operation

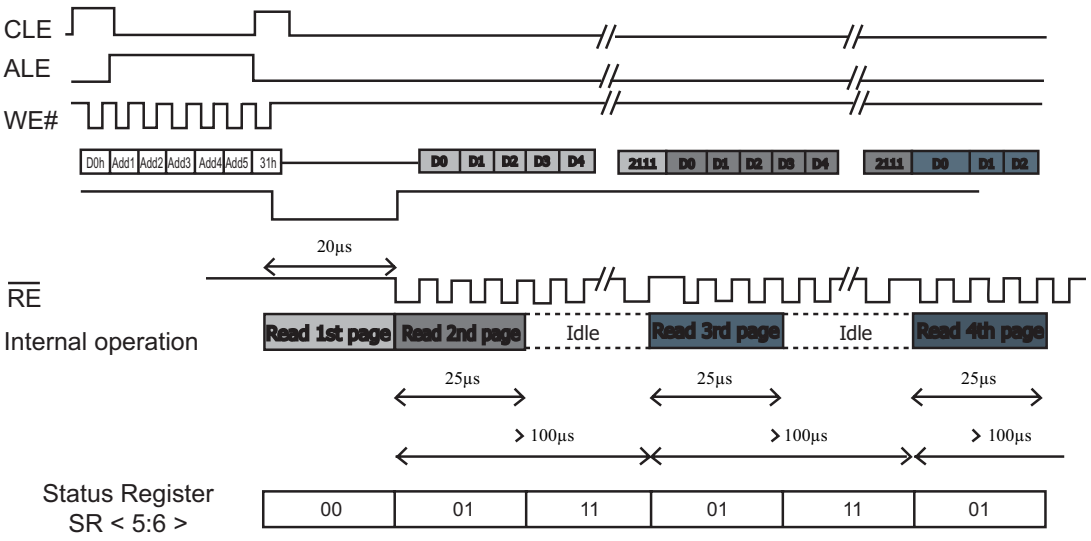


Figure 21: start address at page start :after 1st latency uninterrupted data flow

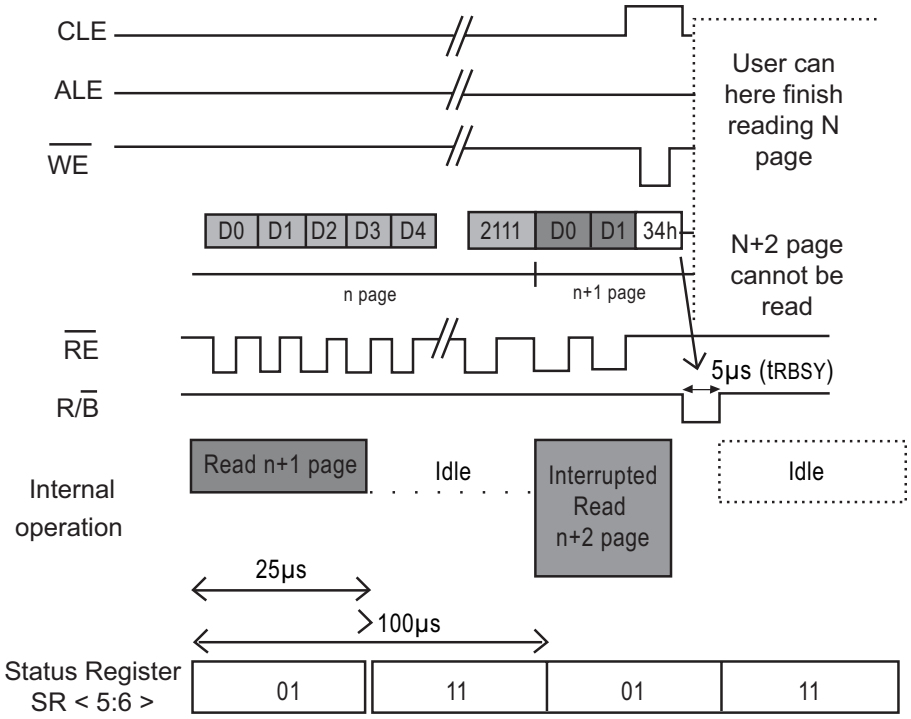


Figure 22: exit from cache read in 5us when device internally is reading

System Interface Using CE don't care

To simplify system interface, CE may be deasserted during data loading or sequential data-reading as shown below. So, it is possible to connect NAND Flash to a microporcessor. The only function that was removed from standard NAND Flash to make CE don't care read operation was disabling of the automatic sequential read function.

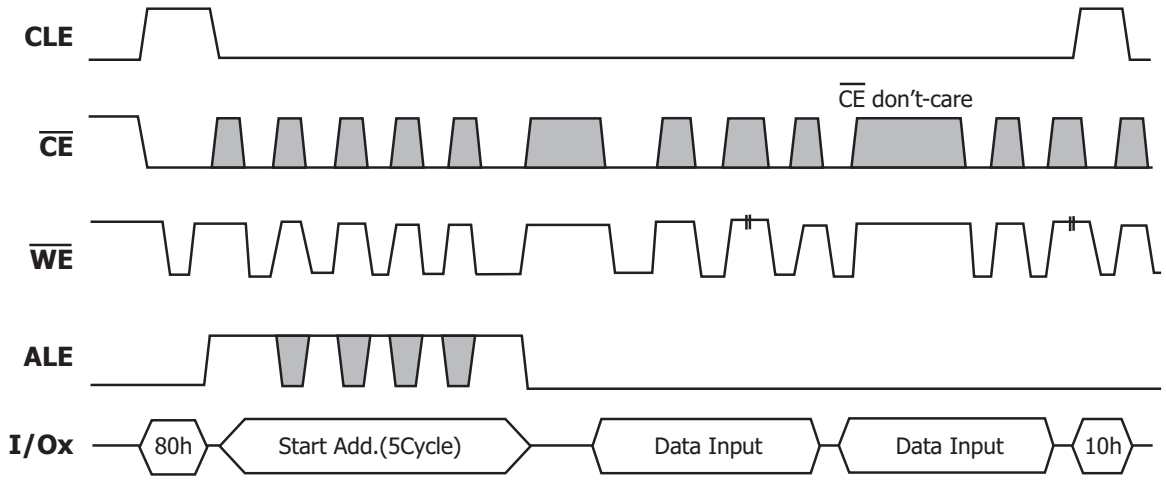


Figure 23: Program Operation with CE don't-care.

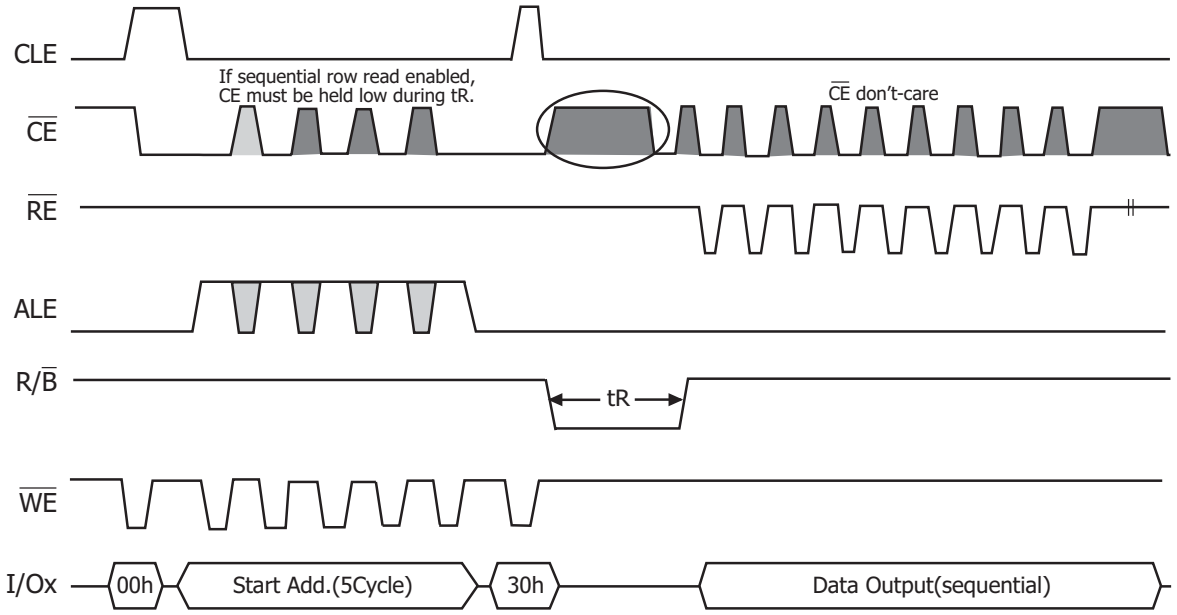


Figure 24: Read Operation with CE don't-care.

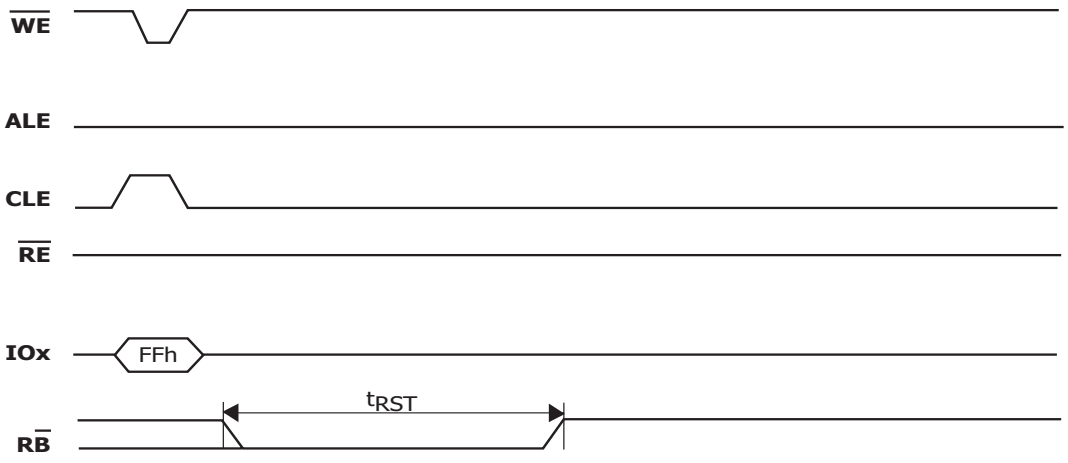


Figure 25: Reset Operation

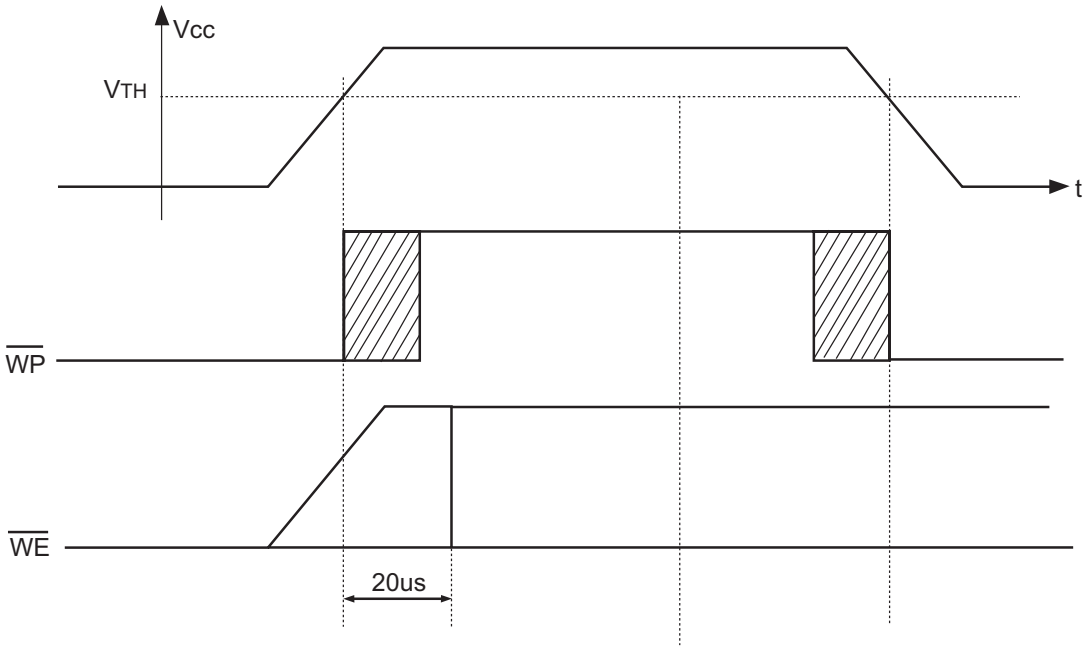
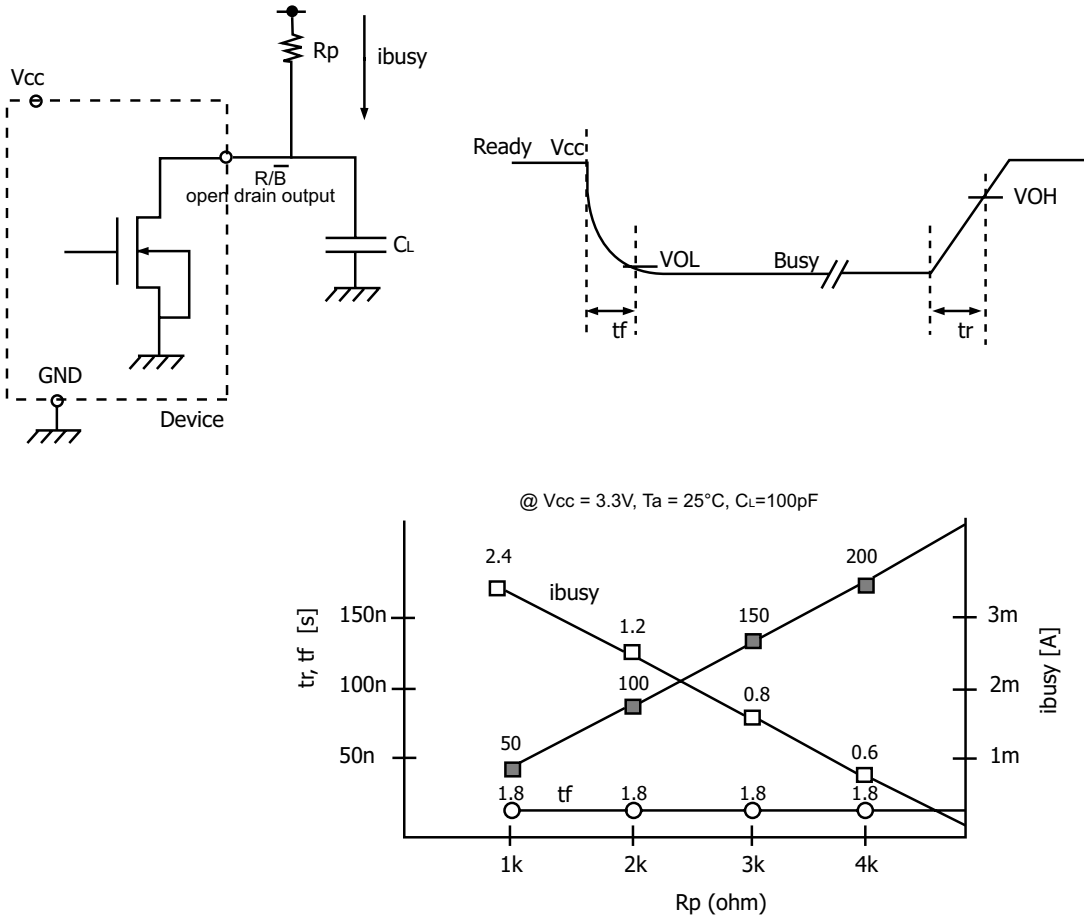


Figure 26: Power On and Data Protection Timing

VTH = 2.5 Volt for 3.3 Volt Supply devices



Rp value guidence

$$Rp(min, 3.3V\ part) = \frac{Vcc\ (Max.) - V_{OL}\ (Max.)}{I_{OL} + \sum I_L} = \frac{3.2V}{8mA + \sum I_L}$$

where IL is the sum of the input currnts of all devices tied to the R/$\overline{B}$ pin.

Rp(max) is determined by maximum permissible limit of tr

Figure 27: Ready/Busy Pin electrical specifications

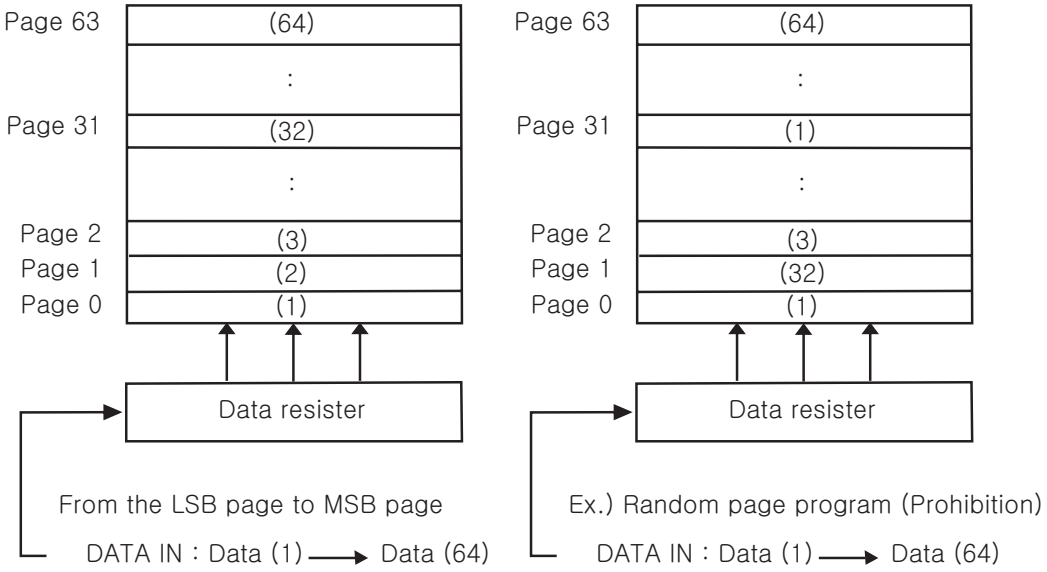


Figure 28 : page programming within a block

Bad Block Management

Devices with Bad Blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A Bad Block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor. The devices are supplied with all the locations inside valid blocks erased(FFh). The Bad Block Information is written prior to shipping. Any block where the 1st Byte in the spare area of the 1st or 2nd page(if the 1st page is Bad) does not contain FFh is a Bad Block. The Bad Block Information must be read before any erase is attempted as the Bad Block Information may be erased. For the system to be able to recognize the Bad Blocks based on the original information it is recommended to create a Bad Block table following the flowchart shown in Figure 29. The 1st block, which is placed on 00h block address is guaranteed to be a valid block.

Bad Replacement

Over the lifetime of the device additional Bad Blocks may develop. In this case the block has to be replaced by copying the data to a valid block. These additional Bad Blocks can be identified as attempts to program or erase them will give errors in the Status Register.
As the failure of a page program operation does not affect the data in other pages in the same block, the block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block. The Copy Back Program command can be used to copy the data to a valid block.
See the "Copy Back Program" section for more details.
Refer to Table 18 for the recommended procedure to follow if an error occurs during an operation.

Operation	Recommended Procedure
Erase	Block Replacement
Program	Block Replacement or ECC (with 1bit/512byte)
Read	ECC (with 1bit/512byte)

Table 18: Block Failure

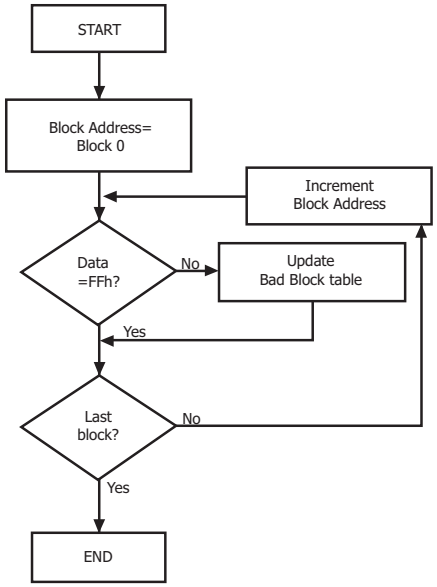


Figure 29: Bad Block Management Flowchart

Write Protect Operation

The Erase and Program Operations are automatically reset when $\overline{WP}$ goes Low (tWW = 100ns, min). The operations are enabled and disabled as follows (Figure 30~33)

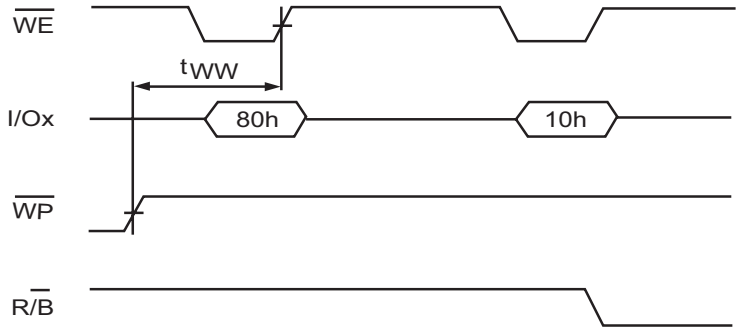


Figure 30: Enable Programming

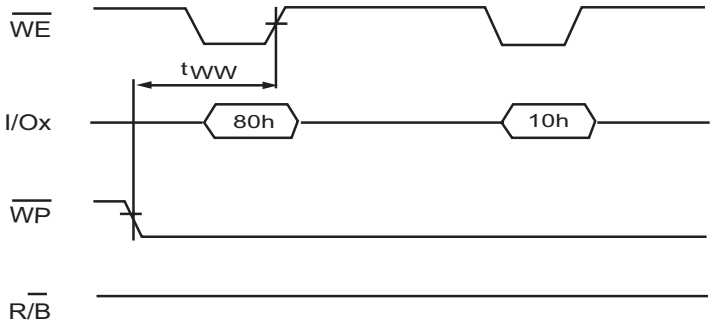


Figure 31: Disable Programming

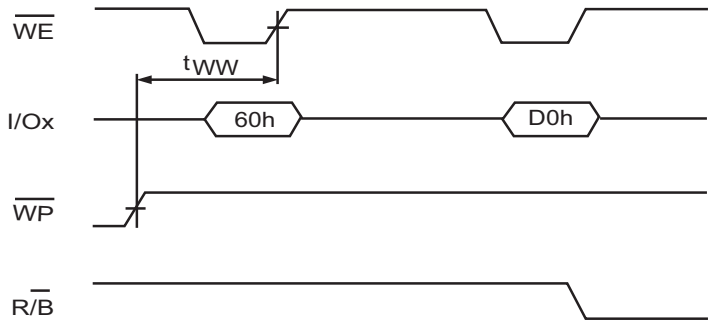


Figure 32: Enable Erasing

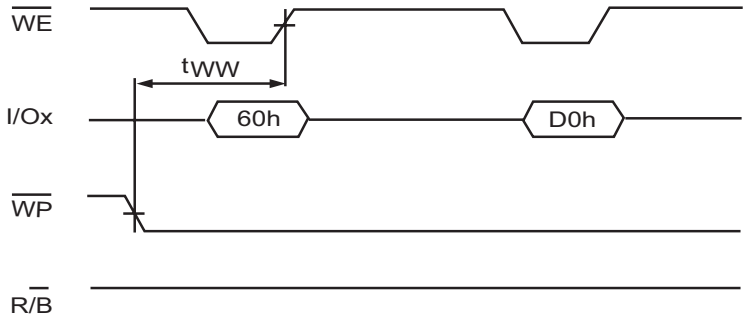


Figure 33: Disable Erasing

5. APPENDIX : Extra Features

5.1 Addressing for program operation

Within a block, the pages must be programmed consecutively from LSB (least significant bit) page of the block to MSB (most significant bit) page of the block. Random address programming is prohibited. See Fig. 34.

5.2 Stacked Devices Access

A small logic inside the devices allows the possibility to stack up to 2 devices in a single package without changing the pinout of the memory. To do this the internal address register can store up to $30^{(1)}$ addresses(512Mbyte addressing field) and basing on the 2 MSB pattern each device inside the package can decide if remain active (1 over 4) or “hang up” the connection entering the Stand-By.

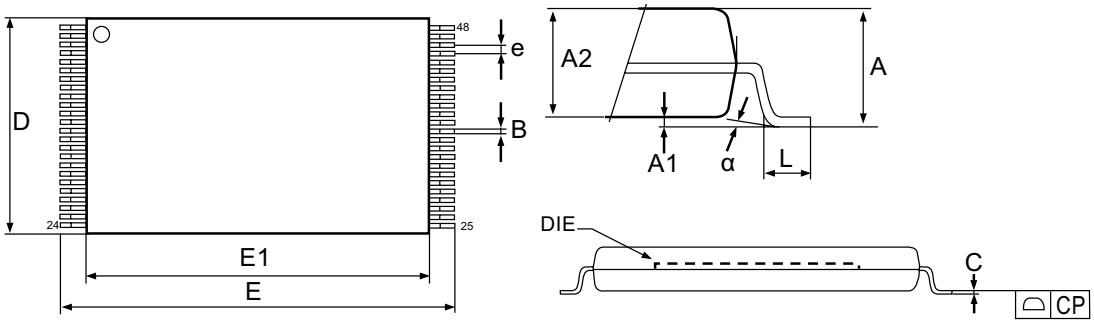


Figure 34. 48-TSOP1 - 48-lead Plastic Thin Small Outline, 12 x 20mm, Package Outline

Symbol	millimeters		
	Min	Typ	Max
A			1.200
A1	0.050		0.150
A2	0.980		1.030
B	0.170		0.250
C	0.100		0.200
CP			0.100
D	11.910	12.000	12.120
E	19.900	20.000	20.100
E1	18.300	18.400	18.500
e		0.500	
L	0.500		0.680
alpha	0		5

Table 19: 48-TSOP1 - 48-lead Plastic Thin Small Outline, 12 x 20mm, Package Mechanical Data

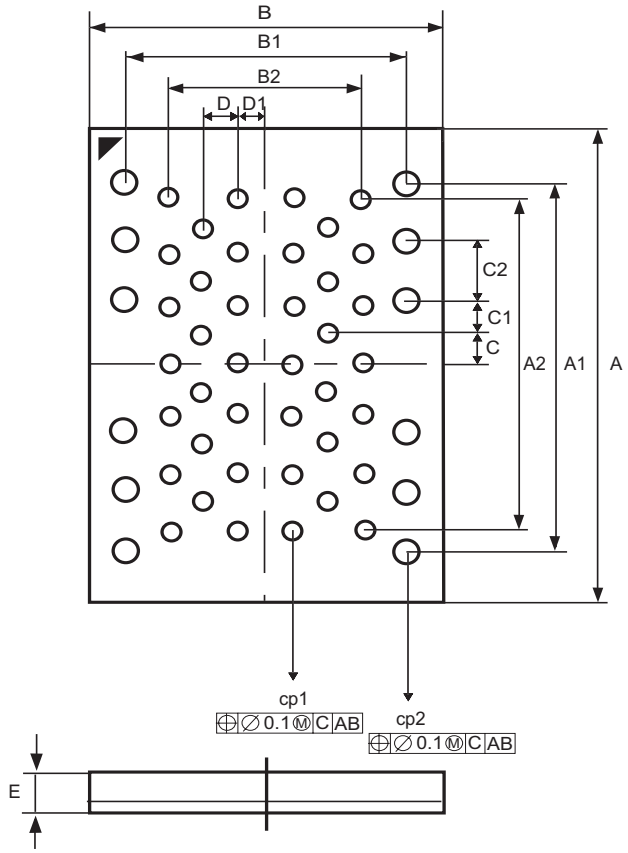
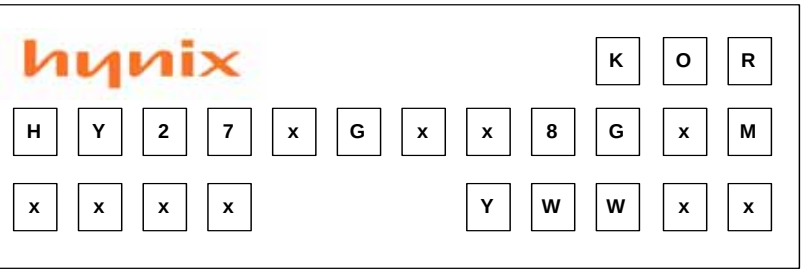


Figure 35. 51-ULGA, 12 x 17mm, Package Outline
(Top view through package)

Symbol	millimeters		
	Min	Typ	Max
A	16.90	17.00	17.10
A1		13.00	
A2		12.00	
B	11.90	12.00	12.10
B1		10.00	
B2		6.00	
C		1.00	
C1		1.50	
C2		2.00	
D		1.00	
D1		1.00	
E	0.55	0.60	0.65
CP1	0.65	0.70	0.75
CP2	0.95	1.00	1.05

Table 20: 52-ULGA, 12 x 17mm, Package Mechanical Data

MARKING INFORMATION- TSOP1/ULGA

Packag	Marking Example
TSOP1 / ULGA	

- hynix	: Hynix Symbol
- KOR	: Origin Country
- HY27xGxx8GxM xxxx	: Part Number
HY: Hynix	
27: NAND Flash	
x: Power Supply	: U(2.7V~3.6V)
G: Classification	: Single Level Cell+Double Die+Large Block
xx: Bit Organization	: 08(x8)
8G: Density	: 8Gbit
x: Mode	: 5(2nCE & 2R/nB; Sequential Row Read Disable)
	: D(Dual interface; Sequential Row Read Disable)
M: Version	: 1st Generation
x: Package Type	: T(48-TSOP1), U(52-ULGA)
x: Package Material	: Blank(Normal), P(Lead Free)
x: Operating Temperature	: C(0℃~70℃), E(-25℃~85℃)
	M(-30℃~85℃), I(-40℃~85℃)
x: Bad Block	: B(Included Bad Block), S(1~5 Bad Block),
	P(All Good Block)
- Y: Year (ex: 5=year 2005, 06= year 2006)	
- ww: Work Week (ex: 12= work week 12)	
- xx: Process Code	
Note	
- Capital Letter	: Fixed Item
- Small Letter	: Non-fixed Item