Document Title
512Mbit (64Mx8bit / 32Mx16bit) NAND Flash Memory

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial Draft.	Sep. 2004	Preliminary
0.1	1) Correct part number (change mode) - 2A -> 1A (sequential row read : disable -> enable) 2) Correct Table.5 & Table 12 - Correct Command Set - correct AC timing characteristics (tWP : 40 -> 25ns, tWH : 20 ->15ns) 3) Correct Summary description & page.7 - The cache feature is deleted in summary description. - Note.3 is deleted. (page.7) 4) Add System interface using CE don't care (page. 38) 5) Change TSOP1, WSOP1,FBGA package dimension & figures. - Change TSOP1, WSOP1, FBGA package mechanical data - Change TSOP1, WSOP package figures 6) Correct TSOP1, WSOP1 Pin configuration - 38th NC pin has been changed Lockpre (figure 2,3) 7) Add Bad block Management	Oct. 22. 2004	Preliminary
0.2	1) LOCKPRE is changed to PRE - Texts, Table and figures are changed. 2) Change Command set - Read A,B are changed to Read1. - Read C is changed to Read2. 3) Change AC, DC characterics - tRB, tCRY, tCEH and tOH are added. 4) Correct Program time (max) - before : 700us - after : 500us 5) Edit figures - Address names are changed. 6) Change FBGA Package Dimension - FD1 : 1.70(before) -> 0.90(after)	Mar. 08. 2005	Preliminary

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<tr><td>0.3</td><td>
1) Change AC Characteristics (1.8V device)
<table>
<tr><td></td><td>tRC</td><td>tRP</td><td>tREH</td><td>tWC</td><td>tWP</td><td>tWH</td><td>tREA</td></tr>
<tr><td>before</td><td>50</td><td>25</td><td>15</td><td>50</td><td>25</td><td>15</td><td>30</td></tr>
<tr><td>after</td><td>60</td><td>40</td><td>20</td><td>60</td><td>40</td><td>20</td><td>40</td></tr>
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2) Change AC Parameter
<table>
<tr><td></td><td>tCRY(3.3V)</td><td>tCRY(1.8V)</td><td>tOH</td></tr>
<tr><td>Before</td><td>50+tr(R/B#)</td><td>50+tr(R/B#)</td><td>15</td></tr>
<tr><td>After</td><td>60+tr(R/B#)</td><td>80+tr(R/B#)</td><td>10</td></tr>
</table>
3) Change Figure 20,22
4) Add Read ID Table
5) Change PAD Configuration
- GND is changed to VSS.
6) Add Marking Information
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<tr><td>0.4</td><td>
1) The test condition for I_{CC1} operating current is corrected.
<table>
<tr><td></td><td>tCRY(3.3V)</td></tr>
<tr><td>Before</td><td>t_{RC}=50ns,
CE#=V_{IL},
I_{OUT}=0mA</td></tr>
<tr><td>After</td><td>t_{RC}(1.8V=60ns,
3.3V=50ns)
CE#=V_{IL},
I_{OUT}=0mA</td></tr>
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<tr><td>0.5</td><td>1) The test conditions is corrected.
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<tr><td></td><td>Test Conditions (ICC1)</td><td>Test Conditions (ILI, ILO)</td></tr>
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CE#=VIL,
IOUT=0mA</td><td>VIN=VOUT=0 to 3.6V</td></tr>
<tr><td>After</td><td>tRC(1.8V=60ns,
3.3V=50ns)
CE#=VIL,
IOUT=0mA</td><td>VIN=VOUT=(1.8V, 0 to 1.95V)
=(3.3V, 0 to 3.6V)</td></tr>
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2) Change VIL parameter (max.)
<table>
<tr><td></td><td>1.8V</td><td>3.3V</td></tr>
<tr><td>Before</td><td>0.2xVcc</td><td>0.2xVcc</td></tr>
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<tr><td>0.6</td><td>1) Correct the test Conditions (DC Characteristics table)
<table>
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<tr><td>Before</td><td>VIN=VOUT=(1.8V, 0 to 1.95V)
=(3.3V, 0 to 3.6V)</td></tr>
<tr><td>After</td><td>VIN=VOUT=0 to Vcc (max)</td></tr>
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2) Change AC Conditions table
3) Add tWW parameter (tWW = 100ns, min)
- Texts & Figures are added.
- tWW is added in AC timing characteristics table.</td><td>Jul. 22. 2005</td><td>Preliminary</td></tr>
<tr><td>0.7</td><td>1) Edit Copy Back Program operation step
2) Edit System Interface Using $\overline{CE}$ don't care Figures.
3) Change AC Characteristics (3.3V device)
<table>
<tr><td></td><td>tRP</td><td>tREA</td></tr>
<tr><td>before</td><td>30</td><td>35</td></tr>
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</table>
4) Correct Address Cycle Map.</td><td>Aug. 01. 2005</td><td>Preliminary</td></tr>
<tr><td>0.8</td><td>1) Correct PKG dimension (TSOP, USOP PKG)
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<tr><td></td><td>CP</td></tr>
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<tr><td>0.9</td><td>1) Correct USOP figure.</td><td>Nov. 07. 2005</td><td>Preliminary</td></tr>
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<tr><th>Revision No.</th><th>History</th><th>Draft Date</th><th>Remark</th></tr>
<tr><td>1.0</td><td>1) Delet Preliminary.</td><td>Nov. 08. 2005</td><td></td></tr>
<tr><td>1.1</td><td>1) Correct Figure 32.</td><td>Feb. 06. 2006</td><td></td></tr>
<tr><td>1.2</td><td>1) Add ECC algorithm. (1bit/512bytes)
2) Correct Read ID naming</td><td>May. 09. 2006</td><td></td></tr>
<tr><td>1.3</td><td>1) Change AC Parameter
<table><tr><td></td><td>tWHR</td></tr><tr><td>Before</td><td>60 ns</td></tr><tr><td>After</td><td>50 ns</td></tr></table></td><td>Jun. 20. 2006</td><td></td></tr>
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FEATURES SUMMARY

HIGH DENSITY NAND Flash MEMORIES

- Cost effective solutions for mass storage applications

NAND INTERFACE

- x8 or x16 bus width.
- Multiplexed Address/ Data
- Pinout compatibility for all densities

SUPPLY VOLTAGE

- 3.3V device: VCC = 2.7 to 3.6V : HY27USXX121A
- 1.8V device: VCC = 1.7 to 1.95V : HY27SSXX121A

Memory Cell Array

= (512+16) Bytes x 32 Pages x 4,096 Blocks

= (256+8) Words x 32 pages x 4,096 Blocks

PAGE SIZE

- x8 device : (512 + 16 spare) Bytes
  : HY27(U/S)S08121A
- x16 device: (256 + 8 spare) Words
  : HY27(U/S)S16121A

BLOCK SIZE

- x8 device: (16K + 512 spare) Bytes
- x16 device: (8K + 256 spare) Words

PAGE READ / PROGRAM

- Random access: 3.3V: 12us (max.)
  1.8V: 15us (max.)
- Sequential access: 3.3V device: 50ns (min.)
  1.8V device: 60ns (min.)
- Page program time: 200us (typ.)

COPY BACK PROGRAM MODE

- Fast page copy without external buffering

FAST BLOCK ERASE

- Block erase time: 2ms (Typ.)

STATUS REGISTER

ELECTRONIC SIGNATURE

- 1st cycle : Manufacturer Code
- 2nd cycle: Device Code

CHIP ENABLE DON'T CARE

- Simple interface with microcontroller

AUTOMATIC PAGE 0 READ AT POWER-UP OPTION

- Boot from NAND support
- Automatic Memory Download

SERIAL NUMBER OPTION

HARDWARE DATA PROTECTION

- Program/Erase locked during Power transitions

DATA INTEGRITY

- 100,000 Program/Erase cycles
  (with 1bit/512byte ECC)
- 10 years Data Retention

PACKAGE

- HY27(U/S)S(08/16)121A-T(P)
  : 48-Pin TSOP1 (12 x 20 x 1.2 mm)
  - HY27(U/S)S(08/16)121A-T (Lead)
  - HY27(U/S)S(08/16)121A-TP (Lead Free)

- HY27(U/S)S(08/16)121A-S(P)
  : 48-Pin USOP1 (12 x 17 x 0.65 mm)
  - HY27(U/S)S(08/16)121A-S (Lead)
  - HY27(U/S)S(08/16)121A-SP (Lead Free)

- HY27(U/S)S(08/16)121A-F(P)
  : 63-Ball FBGA (9 x 11 x 1.0 mm)
  - HY27(U/S)S(08/16)121A-F (Lead)
  - HY27(U/S)S(08/16)121A-FP (Lead Free)

1. SUMMARY DESCRIPTION

The HYNIX HY27(U/S)S(08/16)121A series is a 64Mx8bit with spare 2Mx8 bit capacity. The device is offered in 1.8V Vcc Power Supply and in 3.3V Vcc Power Supply.
Its NAND cell provides the most cost-effective solution for the solid state mass storage market.
The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased.
The device contains 4096 blocks, composed by 32 pages consisting in two NAND structures of 16 series connected Flash cells.
A program operation allows to write the 512-byte page in typical 200us and an erase operation can be performed in typical 2ms on a 16Kbyte(X8 device) block.
Data in the page mode can be read out at 50ns cycle time(3.3V device) per byte. The I/O pins serve as the ports for address and data input/output as well as command input. This interface allows a reduced pin count and easy migration towards different densities, without any rearrangement of footprint.
Commands, Data and Addresses are synchronously introduced using $\overline{CE}$, $\overline{WE}$, ALE and CLE input pin.
The on-chip Program/Erase Controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data.
The modifying can be lockde using the $\overline{WP}$ input pin.
The output pin R/$\overline{B}$ (open drain buffer) signals the status of the device during each operation. In a system with multiple memories the R/$\overline{B}$ pins can be connected all together to provide a global status signal.
Even the write-intensive systems can take advantage of the HY27(U/S)S(08/16)121A extended reliability of 100K program/erase cycles by providing ECC (Error Correcting Code) with real time mapping-out algorithm.

The chip could be offered with the $\overline{CE}$ don't care function. This function allows the direct download of the code from the NAND Flash memory device by a microcontroller, since the $\overline{CE}$

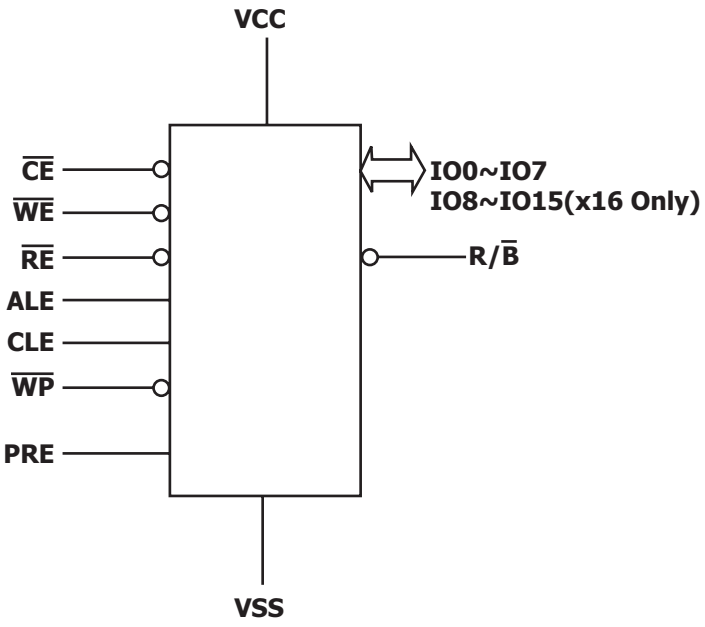


Figure1: Logic Diagram

IO15 - IO8	Data Input / Outputs (x16 Only)
IO7 - IO0	Data Input / Outputs
CLE	Command latch enable
ALE	Address latch enable
$\overline{CE}$	Chip Enable
$\overline{RE}$	Read Enable
$\overline{WE}$	Write Enable
$\overline{WP}$	Write Protect
R/$\overline{B}$	Ready / Busy
Vcc	Power Supply
Vss	Ground
NC	No Connection
PRE	Power-On Read Enable, Lock Unlock

Table 1: Signal Names

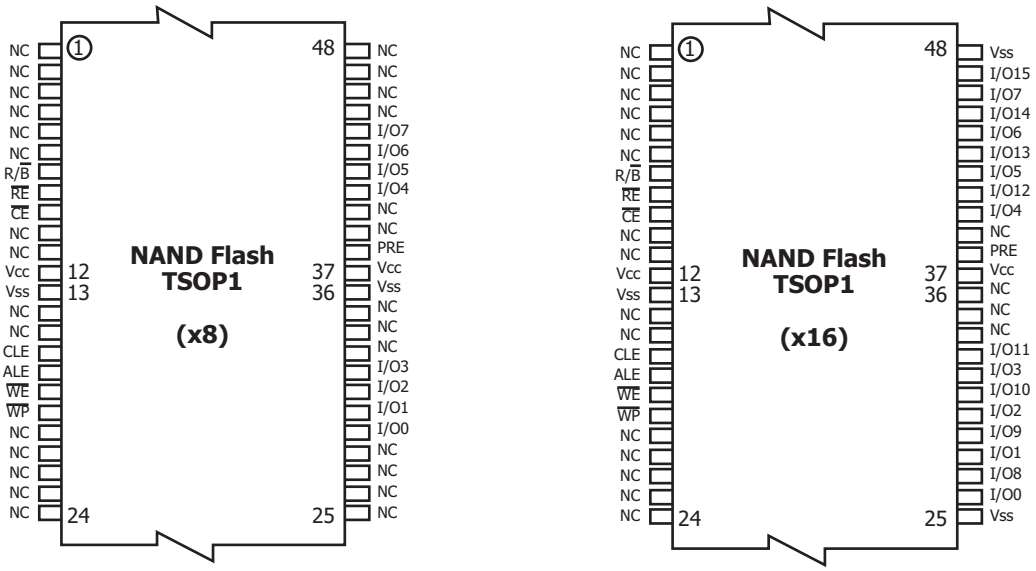


Figure 2. 48TSOP1 Contactions, x8 and x16 Device

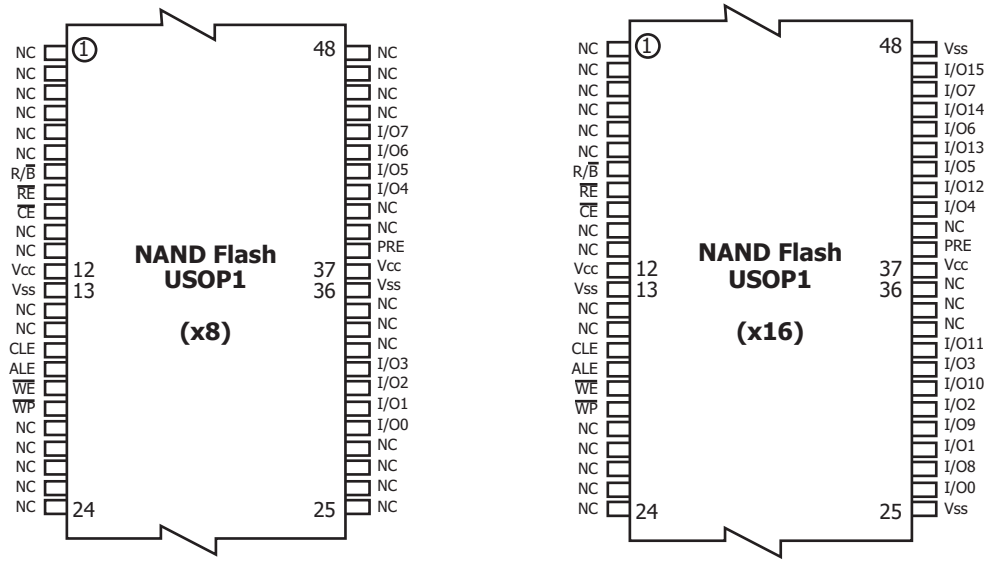


Figure 3. 48USOP1 Contactions, x8 and x16 Device

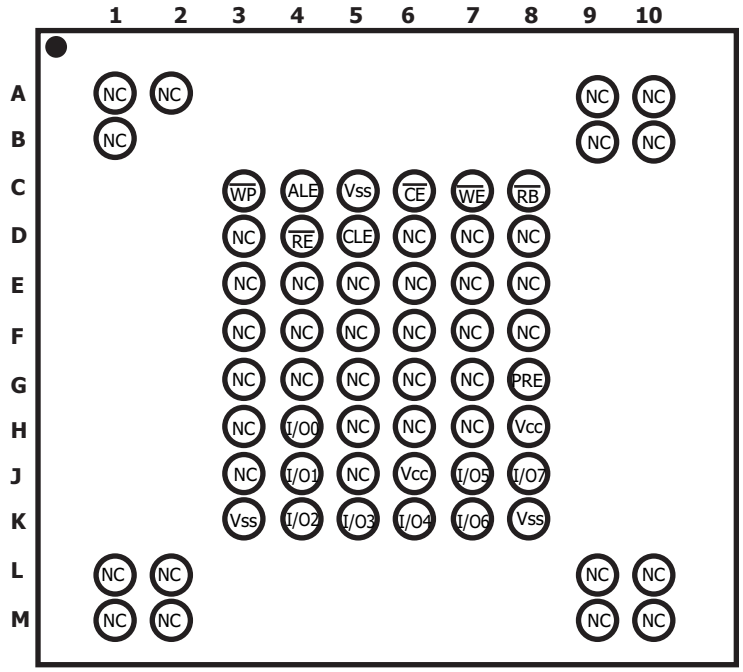


Figure 4. 63FBGA Contactions, x8 Device (Top view through package)

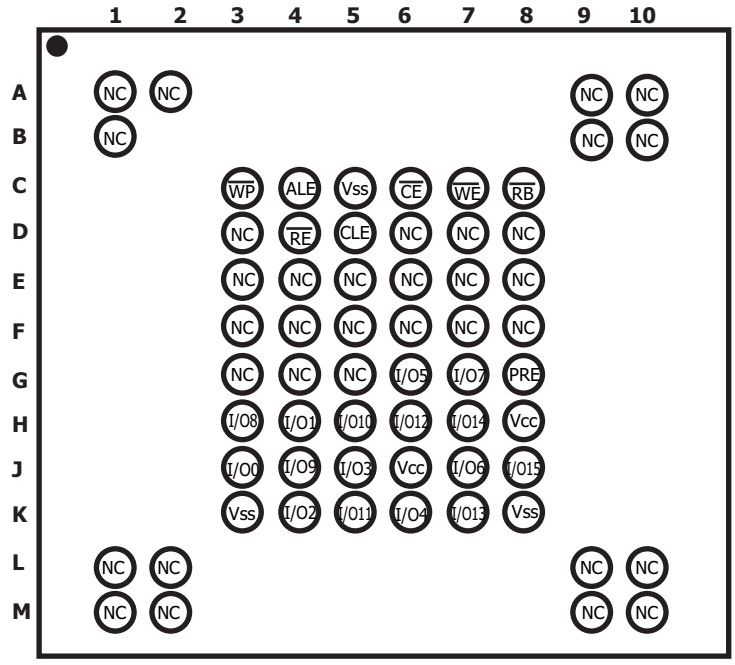


Figure 5. 63FBGA Contactions, x16 Device (Top view through package)

1.2 PIN DESCRIPTION

Pin Name	Description
IO0-IO7 IO8-IO15(1)	**DATA INPUTS/OUTPUTS** The IO pins allow to input command, address and data and to output data during read / program operations. The inputs are latched on the rising edge of Write Enable ($\overline{WE}$). The I/O buffer float to High-Z when the device is deselected or the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** This input activates the latching of the IO inputs inside the Command Register on the Rising edge of Write Enable ($\overline{WE}$).
ALE	**ADDRESS LATCH ENABLE** This input activates the latching of the IO inputs inside the Address Register on the Rising edge of Write Enable ($\overline{WE}$).
$\overline{CE}$	**CHIP ENABLE** This input controls the selection of the device. When the device is busy $\overline{CE}$ low does not deselect the memory.
$\overline{WE}$	**WRITE ENABLE** This input acts as clock to latch Command, Address and Data. The IO inputs are latched on the rise edge of $\overline{WE}$.
$\overline{RE}$	**READ ENABLE** The $\overline{RE}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of $\overline{RE}$ which also increments the internal column address counter by one.
$\overline{WP}$	**WRITE PROTECT** The $\overline{WP}$ pin, when Low, provides an Hardware protection against undesired modify (program / erase) operations.
R/$\overline{B}$	**READY BUSY** The Ready/Busy output is an Open Drain pin that signals the state of the memory.
VCC	**SUPPLY VOLTAGE** The VCC supplies the power for all the operations (Read, Write, Erase).
VSS	GROUND
NC	NO CONNECTION
PRE	To Enable and disable the Lock mechanism and Power On Auto Read. When PRE is a logic high, Block Lock mode and Power-On Auto-Read mode are enabled, and when PRE is a logic low, Block Lock mode and Power-On Auto-Read mode are disabled. Power-On Auto-Read mode is available only on 3.3V device. **Not using LOCK MECHANISM & POWER-ON AUTO-READ, connect it Vss or leave it NC.**

Table 2: Pin Description

NOTE:

1. For x16 version only
2. A 0.1uF capacitor should be connected between the Vcc Supply Voltage pin and the Vss Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.

	IO0	IO1	IO2	IO3	IO4	IO5	IO6	IO7
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A9	A10	A11	A12	A13	A14	A15	A16
3rd Cycle	A17	A18	A19	A20	A21	A22	A23	A24
4th Cycle	A25	L(1)	L(1)	L(1)	L(1)	L(1)	L(1)	L(1)

Table 3: Address Cycle Map(x8)

NOTE:
1. L must be set to Low.
2. A8 is set to LOW or High by the 00h or 01h Command.

	IO0	IO1	IO2	IO3	IO4	IO5	IO6	IO7	IO8-IO15
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7	L(1)
2nd Cycle	A9	A10	A11	A12	A13	A14	A15	A16	L(1)
3rd Cycle	A17	A18	A19	A20	A21	A22	A23	A24	L(1)
4th Cycle	A25	L(1)	L(1)	L(1)	L(1)	L(1)	L(1)	L(1)	L(1)

Table 4: Address Cycle Map(x16)

NOTE:
1. L must be set to Low.

FUNCTION	1st CYCLE	2nd CYCLE	3rd CYCLE	4th CYCLE	Acceptable command during busy
READ 1	00h/01h	-	-		
READ 2	50h	-	-		
READ ID	90h	-	-		
RESET	FFh	-	-		Yes
PAGE PROGRAM	80h	10h	-		
COPY BACK PGM	00h	8Ah	(10h)		
BLOCK ERASE	60h	D0h	-		
READ STATUS REGISTER	70h	-	-		Yes
LOCK BLOCK	2Ah				
LOCK TIGHT	2Ch				
UNLOCK (start area)	23h				
UNLOCK (end area)	24h				
READ LOCK STATUS	7Ah				

Table 5: Command Set

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	MODE	
H	L	L	Rising	H	X	Read Mode	Command Input
L	H	L	Rising	H	X		Address Input(4 cycles)
H	L	L	Rising	H	H	Write Mode	Command Input
L	H	L	Rising	H	H		Address Input(4 cycles)
L	L	L	Rising	H	H	Data Input	
L	L	L(1)	H	Falling	X	Sequential Read and Data Output	
L	L	L	H	H	X	During Read (Busy)	
X	X	X	X	X	H	During Program (Busy)	
X	X	X	X	X	H	During Erase (Busy)	
X	X	X	X	X	L	Write Protect	
X	X	H	X	X	0V/Vcc	Stand By	

Table 6: Mode Selection

NOTE:

1. With the $\overline{CE}$ high during latency time does not stop the read operation

2. BUS OPERATION

There are six standard bus operations that control the device. These are Command Input, Address Input, Data Input, Data Output, Write Protect, and Standby.
Typically glitches less than 5 ns on Chip Enable, Write Enable and Read Enable are ignored by the memory and do not affect bus operations.

2.1 Command Input.

Command Input bus operation is used to give a command to the memory device. Command are accepted with Chip Enable low, Command Latch Enable High, Address Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modifying operation (write/erase) the Write Protect pin must be high. See figure 7 and table 12 for details of the timings requirements. Command codes are always applied on IO7:0, disregarding the bus configuration (X8/X16).

2.2 Address Input.

Address Input bus operation allows the insertion of the memory address. Four cycles are required to input the addresses for the 512Mbit devices. Addresses are accepted with Chip Enable low, Address Latch Enable High, Command Latch Enable low and Read Enable high and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/erase) the Write Protect pin must be high. See figure 8 and table 12 for details of the timings requirements. Addresses are always applied on IO7:0, disregarding the bus configuration (X8/X16).
In addition, addresses over the addressable space are disregarded even if the user sets them during command insertion.

2.3 Data Input.

Data Input bus operation allows to feed to the device the data to be programmed. The data insertion is serially and timed by the Write Enable cycles. Data are accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low, Read Enable High, and Write Protect High and latched on the rising edge of Write Enable. See figure 9 and table 12 for details of the timings requirements.

2.4 Data Output.

Data Output bus operation allows to read data from the memory array and to check the status register content, the lock status and the ID data. Data can be serially shifted out toggling the Read Enable pin with Chip Enable low, Write Enable High, Address Latch Enable low, and Command Latch Enable low. See figures 10 to 14 and table 12 for details of the timings requirements.

2.5 Write Protect.

Hardware Write Protection is activated when the Write Protect pin is low. In this condition modify operation do not start and the content of the memory is not altered. Write Protect pin is not latched by Write Enable to ensure the protection even during the power up.

2.6 Standby.

In Standby mode the device is deselected, outputs are disabled and Power Consumption is reduced.

3. DEVICE OPERATION

3.1 Page Read.

Upon initial device power up, the device defaults to Read1 mode. This operation is also initiated by writing 00h to the command register along with followed by the four address input cycles. Once the command is latched, it does not need to be written for the following page read operation.
Three types of operations are available: random read, serial page read and sequential row read.
The random read mode is enabled when the page address is changed. The 528 bytes (x8 device) or 264 word (x16 device) of data within the selected page are transferred to the data registers in less than access random read time tR (12us, 3.3V device). The system controller can detect the completion of this data transfer tR (12us, 3.3V device) by analyzing the output of R/$\overline{B}$ pin. Once the data in a page is loaded into the registers, they may be read out in 50ns cycle time by sequentially pulsing $\overline{RE}$. High to low transitions of the $\overline{RE}$ clock output the data stating from the selected column address up to the last column address.
After the data of last column address is clocked out, the next page is automatically selected for sequential row read. Waiting tR again allows reading the selected page. The sequential row read operation is terminated by bringing $\overline{CE}$ high.
The way the Read1 and Read2 commands work is like a pointer set to either the main area or the spare area. Writing the Read2 command user may selectively access the spare area of bytes 512 to 527. Addresses A0 to A3 set the starting address of the spare area while addresses A4 to A7 are ignored. Unless the operation is aborted, the page address is automatically incremented for sequential row
Read as in Read1 operation and spare sixteen bytes of each page may be sequentially read. The Read1 command (00h/01h) is needed to move the pointer back to the main area. Figure_11 to 13 show typical sequence and timings for each read operation.
Devices with automatic read of page0 at power up can be provided on request.

3.2 Page Program.

The device is programmed basically on a page basis, but it does allow multiple partial page programming of a byte or consecutive bytes up to 528 (x8 device), in a single page program cycle. The number of consecutive partial page programming operations within the same page without an intervening erase operation must not exceed 1 for main array and 2 for spare array. The addressing may be done in any random order in a block. A page program cycle consists of a serial data loading period in which up to 528 bytes (x8 device) or 264 word (x16 device) of data may be loaded into the page register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. Serial data loading can be started from 2nd half array by moving pointer. About the pointer operation, please refer to Figure_29.
The data-loading sequence begins by inputting the Serial Data Input command (80h), followed by the four address input cycles and then serial data loading. The Page Program confirm command (10h) starts the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal P/E/R Controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered, with $\overline{RE}$ and $\overline{CE}$ low, to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit (I/O 0) may be checked Figure_17
The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

3.3 Block Erase.

The Erase operation is done on a block (16K Byte) basis. It consists of an Erase Setup command (60h), a Block address loading and an Erase Confirm Command (D0h). The Erase Confirm command (D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.

The block address loading is accomplished in two to four cycles depending on the device density. Only block addresses (A14 to A26) are needed while A9 to A13 is ignored.

At the rising edge of $\overline{WE}$ after the erase confirm command input, the internal P/E/R Controller handles erase and erase-verify. When the erase operation is completed, the Write Status Bit (I/O 0) may be checked. Figure_18 details the sequence.

3.4 Copy-Back Program.

The copy-back program is provided to quickly and efficiently rewrite data stored in one page within the plane to another page within the same plane without using an external memory. Since the time-consuming sequential-reading and its reloading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block also need to be copied to the newly assigned free block. The operation for performing a copy-back program is a sequential execution of page-read without burst-reading cycle and copying-program with the address of destination page. A normal read operation with "00h" command and the address of the source page moves the whole 528byte data into the internal buffer. As soon as the device returns to Ready state, Page-Copy Data-input command (8Ah) with the address cycles of destination page followed may be written. The Program Confirm command (10h) is not needed to actually begin the programming operation. For backward-compatibility, issuing Program Confirm command during copy-back does not affect correct device operation.

Copy-Back Program operation is allowed only within the same memory plane. Once the Copy-Back Program is finished, any additional partial page programming into the copied pages is prohibited before erase. Plane address must be the same between source and target page

"When there is a program-failure at Copy-Back operation, error is reported by pass/fail status. But, if Copy-Back operations are accumulated over time, bit error due to charge loss is not checked by external error detection/correction scheme. For this reason, two bit error correction is recommended for the use of Copy-Back operation."

Figure 17 shows the command sequence for the copy-back operation.

The Copy Back Program operation requires three steps:

- 1. The source page must be read using the Read A command (one bus write cycle to setup the command and then 4 cycle bus to input the source page address.) This operation copies all 264 Words/ 528 Bytes from the page into the page Buffer.
- 2. When the device returns to the ready state (Ready/Busy High), the second bus write cycle of the command is given with the 4cycles to input the target page address. A14 & A25 must be the same for the Source and Target Pages.
- 3. Then the confirm command is issued to start the P/E/R Controller.

3.5 Read Status Register.

The device contains a Status Register which may be read to find out whether read, program or erase operation is com pleted, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/$\overline{B}$ pins are common-wired. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status. Refer to table 13 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, a read command (00h or 50h) should be given before sequential page read cycle.

3.6 Read ID.

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Two read cycles sequentially output the manufacturer code (ADh), the device code. The command register remains in Read ID mode until further commands are issued to it. Figure 19 shows the operation sequence, while tables 16 explain the byte meaning.

3.7 Reset.

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value E0h when $\overline{WP}$ is high. Refer to table 12 for device status after reset operation. If the device is already in reset state a new reset command will not be accepted by the command register. The R/$\overline{B}$ pin transitions to low for tRST after the Reset command is written. Refer to figure 25.

4. OTHER FEATURES

4.1 Data Protection & Power on/off Sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 1.1V (1.8V device), 2.0V (3.3V device). $\overline{WP}$ pin provides hardware protection and is recommended to be kept at VIL during power-up and power-down. A recovery time of minimum 10us is required before internal circuit gets ready for any command sequences as shown in Figure 26. The two-step command sequence for program/erase provides additional software protection.
If the power is dropped during the ready read/write/erase operation, Power protection function may not guaranteed the data. Power protection function is only available during the power on/off sequence.

4.2 Ready/Busy.

The device has a Ready/Busy output that provides method of indicating the completion of a page program, erase, copy-back and random read completion. The R/$\overline{B}$ pin is normally high and goes to low when the device is busy (after a reset, read, program, erase operation). It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{B}$ outputs to be Or-tied. Because pull-up resistor value is related to tr(R/$\overline{B}$) and current drain during busy (Ibusy), an appropriate value can be obtained with the following reference chart (Fig 27). Its value can be determined by the following guidance.

4.3 Lock Block Feature

In high state of PRE pin, Block lock mode and Power on Auto read are enabled, otherwise it is regarded as NAND Flash without PRE pin.

Block Lock mode is enabled while PRE pin state is high, which is to offer protection features for NAND Flash data. The Block Lock mode is divided into Unlock, Lock, Lock-tight operation. Consecutive blocks protects data allows those blocks to be locked or lock-tighten with no latency. This block lock scheme offers two levels of protection. The first allows software control (command input method) of block locking that is useful for frequently changed data blocks, while the second requires hardware control ($\overline{WP}$ low pulse input method) before locking can be changed that is useful for protecting infrequently changed code blocks. The followings summarized the locking functionality.

- All blocks are in a locked state on power-up. Unlock sequence can unlock the locked blocks.
- The Lock-tight command locks blocks and prevents from being unlocked. Lock-tight state can be returned to lock state only by Hardware control(WP low pulse input).

1. Block lock operation

1) Lock
- Command Sequence: Lock block Command (2Ah). See Fig. 20.
- All blocks default to locked by power-up and Hardware control ($\overline{WP}$ low pulse input)
- Partial block lock is not available; Lock block operation is based on all block unit
- Unlocked blocks can be locked by using the Lock block command, and a lock block's status can be changed to unlock or lock-tight using the appropriate commands
- On the program or erase operation in Locked or Lock-tighten block, Busy state holds 1~10us(tLBSY)

2) Unlock

- Command Sequence: Unlock block Command (23h) + Start block address + Command (24h) + End block address. See Fig. 21.
- Unlocked blocks can be programmed or erased.
- An unlocked block's status can be changed to the locked or lock-tighten state using the appropriate sequence of commands.
- Only one consecutive area can be released to unlock state from lock state; Unlocking multi area is not available.
- Start block address must be nearer to the logical LSB (Least Significant Bit) than End block address.
- One block is selected for unlocking block when Start block address is same as End block address.

3) Lock-tight

- Command Sequence: Lock-tight block Command (2Ch). See Fig. 22.
- Lock-tighten blocks offer the user an additional level of write protection beyond that of a regular lock block. A block that is lock-tighten can't have its state changed by software control, only by hardware control ($\overline{WP}$ low pulse input); Unlocking multi area is not available
- Only locked blocks can be lock-tighten by lock-tight command.
- On the program or erase operation in Locked or Lock-tighten block, Busy state holds 1~10us(tLBSY)

4) Lock Block Boundaries after Unlock Command issuing

- If Start Block address = 0000h and End Block Address = FFFFh , the device is all unlocked
- If Start Block address = End Block Address = FFFFh , the device is all locked except for the last Block
- If Start Block address = End Block Address = 0000h , the device is all locked except for the first Block

2. Block lock Status Read

Block Lock Status can be read on a block basis to find out whether designated block is available to be programmed or erased. After writing 7Ah command to the command register and block address to be checked, a read cycle outputs the content of the Block Lock Status Register to the I/O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status. Block Lock Status Read is prohibited while the device is busy state.

Refer to table 15 for specific Status Register definitions. The command register remains in Block Lock Status Read mode until further commands are issued to it.

In high state of PRE pin, write protection status can be checked by Block Lock Status Read (7Ah) while in low state by Status Read (70h).

4.4 Power-On Auto-Read

The device is designed to offer automatic reading of the first page without command and address input sequence during power-on.

An internal voltage detector enables auto-page read functions when Vcc reaches about 1.8V. PRE pin controls activation of auto- page read function. Auto-page read function is enabled only when PRE pin is logic high state. Serial access may be done after power-on without latency. Power-On Auto Read mode is available only on 3.3V device.

Parameter	Symbol	Min	Typ	Max	Unit
Valid Block Number	N_{VB}	4016		4096	Blocks

Table 6: Valid Blocks Number

NOTE:

1. The 1st block is guaranteed to be a valid block up to 1K cycles without ECC. (1bit/512bytes)

Symbol	Parameter	Value		Unit
		1.8V	3.3V	
T_A	Ambient Operating Temperature (Commercial Temperature Range)	0 to 70	0 to 70	℃
	Ambient Operating Temperature (Extended Temperature Range)	-25 to 85	-25 to 85	℃
	Ambient Operating Temperature (Industrial Temperature Range)	-40 to 85	-40 to 85	℃
T_{BIAS}	Temperature Under Bias	-50 to 125	-50 to 125	℃
T_{STG}	Storage Temperature	-65 to 150	-65 to 150	℃
V_{IO}(2)	Input or Output Voltage	-0.6 to 2.7	-0.6 to 4.6	V
Vcc	Supply Voltage	-0.6 to 2.7	-0.6 to 4.6	V

Table 7: Absolute maximum ratings

NOTE:

1. Except for the rating “Operating Temperature Range”, stresses above those listed in the Table “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

2. Minimum Voltage may undershoot to -2V during transition and for less than 20ns during transitions.

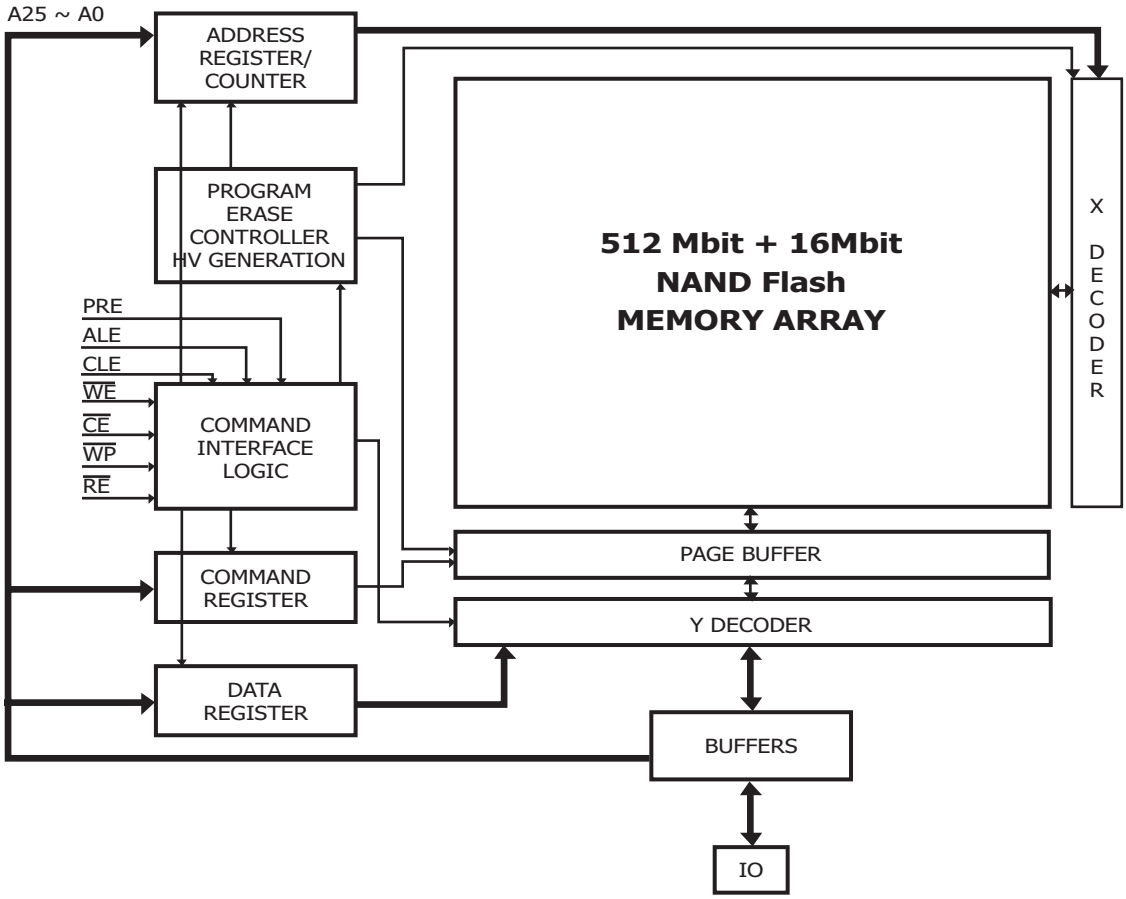


Figure 6: Block Diagram

Parameter		Symbol	Test Conditions	1.8Volt			3.3Volt			Unit
				Min	Typ	Max	Min	Typ	Max	
Operating Current	Sequential Read	I_{CC1}	t_{RC}(1.8V=60ns, 3.3V=50ns) $\overline{CE}$=V_{IL}, I_{OUT}=0mA	-	8	15	-	10	20	mA
	Program	I_{CC2}	-	-	8	15	-	10	20	mA
	Erase	I_{CC3}	-	-	8	15	-	10	20	mA
Stand-by Current (TTL)		I_{CC4}	$\overline{CE}$=V_{IH}, $\overline{WP}$=PRE=0V/Vcc	-	-	1	-		1	mA
Stand-by Current (CMOS)		I_{CC5}	$\overline{CE}$=Vcc-0.2, $\overline{WP}$=PRE=0V/Vcc	-	10	50	-	10	50	uA
Input Leakage Current		I_{LI}	V_{IN}=0 to Vcc (max)	-	-	± 10	-	-	± 10	uA
Output Leakage Current		I_{LO}	V_{OUT} =0 to Vcc (max)	-	-	± 10	-	-	± 10	uA
Input High Voltage		V_{IH}	-	Vcc-0.4	-	Vcc+0.3	2	-	Vcc+0.3	V
Input Low Voltage		V_{IL}	-	-0.3	-	0.4	-0.3	-	0.8	V
Output High Voltage Level		V_{OH}	I_{OH}=-100uA	Vcc-0.1	-	-	-	-	-	V
			I_{OH}=-400uA	-	-	-	2.4	-	-	V
Output Low Voltage Level		V_{OL}	I_{OL}=100uA	-	-	0.1	-	-	-	V
			I_{OL}=2.1mA	-	-	-	-	-	0.4	V
Output Low Current (R/$\overline{B}$)		I_{OL} (R/$\overline{B}$)	V_{OL}=0.2V	3	4	-	-	-	-	mA
			V_{OL}=0.4V	-	-	-	8	10	-	mA

Table 8: DC and Operating Characteristics

Parameter	Value	
	1.8Volt	3.3Volt
Input Pulse Levels	0V to Vcc	0.4V to 2.4V
Input Rise and Fall Times	5ns	5ns
Input and Output Timing Levels	Vcc / 2	1.5V
Output Load (1.7V - 1.95Volt & 2.7V - 3.3V)	1 TTL GATE and CL=30pF	1 TTL GATE and CL=50pF
Output Load (3.0V - 3.6V)		1 TTL GATE and CL=100pF

Table 9: AC Conditions

Item	Symbol	Test Condition	Min	Max	Unit
Input / Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	10	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	10	pF

Table 10: Pin Capacitance (TA=25C, F=1.0MHz)

Parameter		Symbol	Min	Typ	Max	Unit
Program Time		t_{PROG}	-	200	500	us
Dummy Busy Time for the Lock or Lock-tight Block		t_{LBSY}	-	5	10	us
Number of partial Program Cycles in the same page	Main Array	NOP	-	-	1	Cycles
	Spare Array	NOP	-	-	2	Cycles
Block Erase Time		t_{BERS}	-	2	3	ms

Table 11: Program / Erase Characteristics

Parameter	Symbol	1.8Volt		3.3Volt		Unit
		Min	Max	Min	Max	
CLE Setup time	tCLS	0		0		ns
CLE Hold time	tCLH	10		10		ns
$\overline{CE}$ setup time	tCS	0		0		ns
$\overline{CE}$ hold time	tCH	10		10		ns
$\overline{WE}$ pulse width	tWP	40		25(1)		ns
ALE setup time	tALS	0		0		ns
ALE hold time	tALH	10		10		ns
Data setup time	tDS	20		20		ns
Data hold time	tDH	10		10		ns
Write Cycle time	tWC	60		50		ns
$\overline{WE}$ High hold time	tWH	20		15		ns
Data Transfer from Cell to register	tR		15		12	us
ALE to $\overline{RE}$ Delay	tAR	10		10		ns
CLE to $\overline{RE}$ Delay	tCLR	10		10		ns
Ready to $\overline{RE}$ Low	tRR	20		20		ns
$\overline{RE}$ Pulse Width	tRP	40		25		ns
$\overline{WE}$ High to Busy	tWB		100		100	ns
Read Cycle Time	tRC	60		50		ns
$\overline{RE}$ Access Time	tREA		40		30	ns
$\overline{RE}$ High to Output High Z	tRHZ		30		30	ns
$\overline{CE}$ High to Output High Z	tCHZ		20		20	ns
$\overline{RE}$ or $\overline{CE}$ high to Output hold	tOH	10		10		ns
$\overline{RE}$ High Hold Time	tREH	20		15		ns
Output High Z to $\overline{RE}$ low	tIR	0		0		ns
$\overline{CE}$ Access Time	tCEA		45		45	ns
$\overline{WE}$ High to $\overline{RE}$ low	tWHR	50		50		ns
Last RE High to busy (at sequential read)	tRB		100		100	ns
$\overline{CE}$ High to Ready (in case of interception by $\overline{CE}$ at read)	tCRY		80+tr(R/B#)(4)		60+tr(R/B#)(4)	ns
$\overline{CE}$ High Hold Time (at the last serial read)(3)	tCEH	100		100		ns
Device Resetting Time (Read / Program / Erase)	tRST		5/10/500(2)		5/10/500(2)	us
Write Protection time	tWW(5)	100		100		ns

Table 12: AC Timing Characteristics

NOTE:

1. If tCS is less than 10ns tWP must be minimum 35ns, otherwise, tWP may be minimum 25ns.
2. If Reset Command (FFh) is written at Ready state, the device goes into Busy for maximum 5us
3. To break the sequential read cycle, $\overline{CE}$ must be held for longer time than tCEH.
4. The time to Ready depends on the value of the pull-up resistor tied R/$\overline{B}$ pin.
5. Program / Erase Enable Operation : $\overline{WP}$ high to $\overline{WE}$ High.
   Program / Erase Disable Operation : $\overline{WP}$ Low to $\overline{WE}$ High.

IO	Pagae Program	Block Erase	Read	CODING
0	Pass / Fail	Pass / Fail	NA	Pass: '0' Fail: '1'
1	NA	NA	NA	Pass: '0' Fail: '1' (Only for Cache Program, else Don't care)
2	NA	NA	NA	-
3	NA	NA	NA	-
4	NA	NA	NA	-
5	Ready/Busy	Ready/Busy	Ready/Busy	Active: '0' Idle: '1'
6	Ready/Busy	Ready/Busy	Ready/Busy	Busy: '0' Ready': '1'
7	Write Protect	Write Protect	Write Protect	Protected: '0' Not Protected: '1'

Table 13: Status Register Coding

DEVICE IDENTIFIER CYCLE	DESCRIPTION
1st	Manufacturer Code
2nd	Device Identifier

Table 14: Device Identifier Coding

Part Number	Voltage	Bus Width	1st cycle (Manufacture Code)	2nd cycle (Device Code)
HY27US08121A	3.3V	X8	ADh	76h
HY27US16121A	3.3V	X16	ADh	56h
HY27SS08121A	1.8V	X8	ADh	36h
HY27SS16121A	1.8V	X16	ADh	46h

Table 15: Read ID Table

	IO7~IO3	IO2(Unlock)	IO1(Lock)	IO0(Lock-tight)
Read 1) block case	X	0	1	0
Read 2) block case	X	1	1	0
Read 3) block case	X	0	0	1
Read 4) block case	X	1	0	1

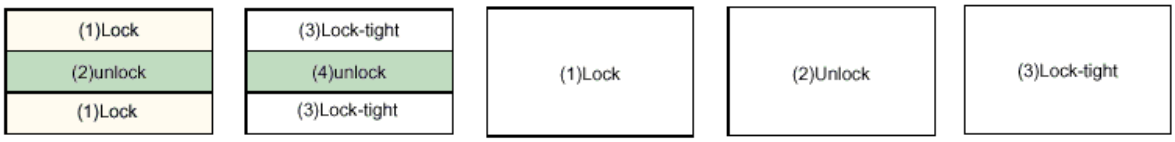


Table 16: Lock Status Code

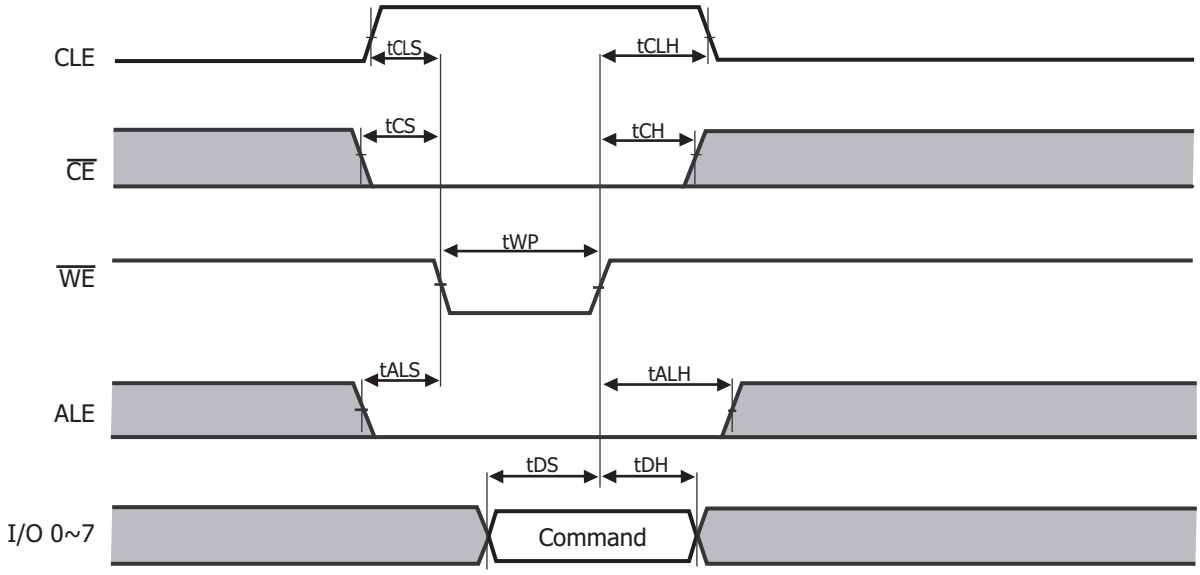


Figure 7: Command Latch Cycle

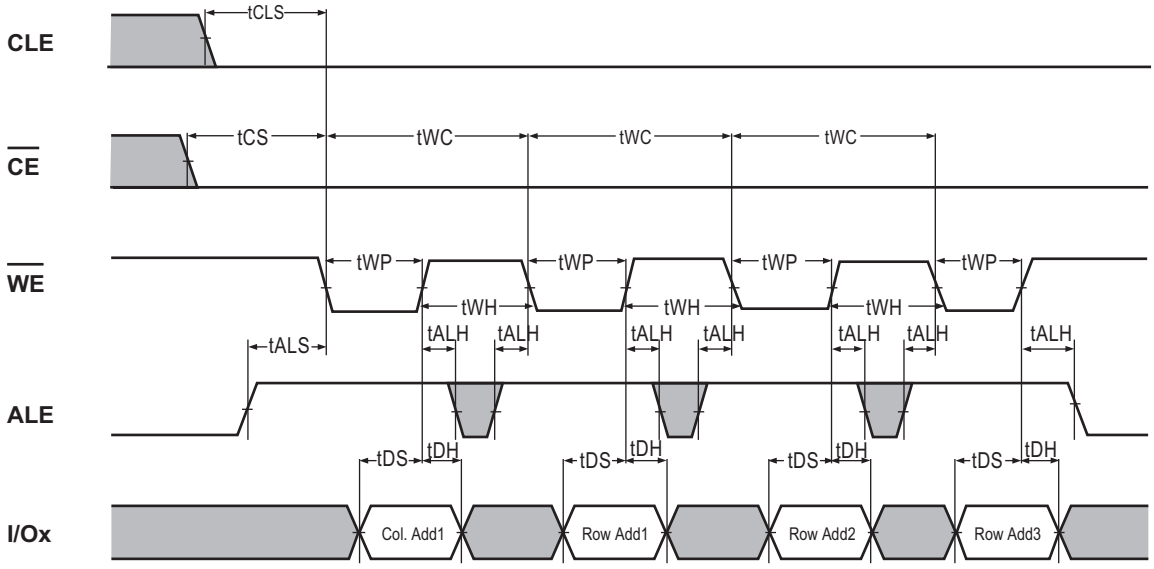


Figure 8: Address Latch Cycle

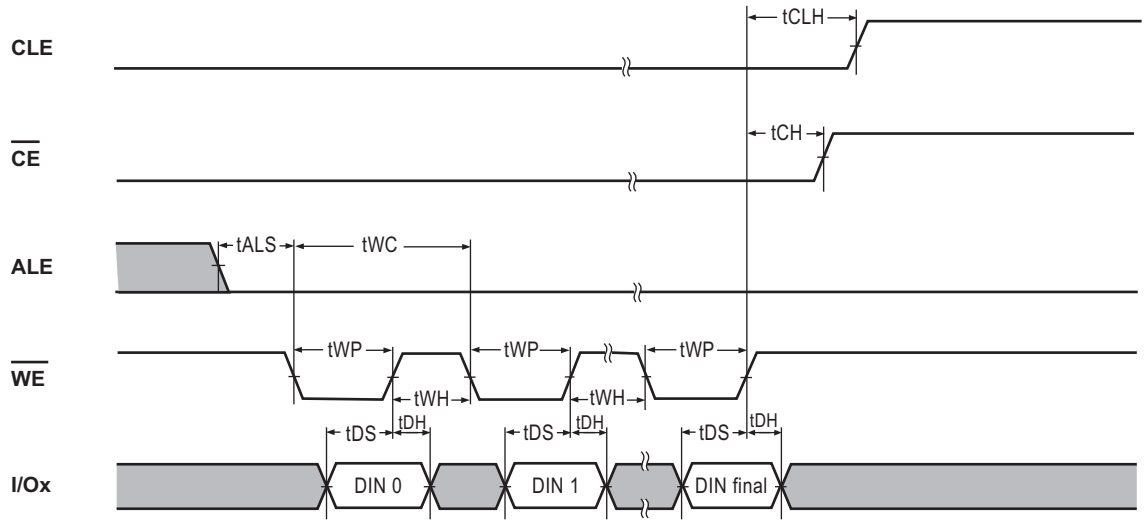
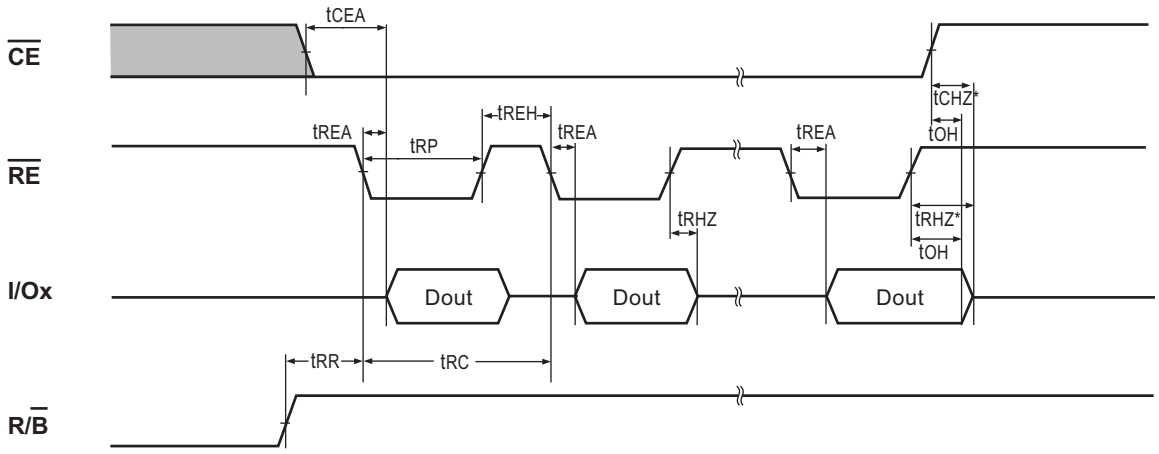


Figure 9. Input Data Latch Cycle



Notes : Transition is measured ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.

Figure 10: Sequential Out Cycle after Read (CLE=L, $\overline{WE}$=H, ALE=L)

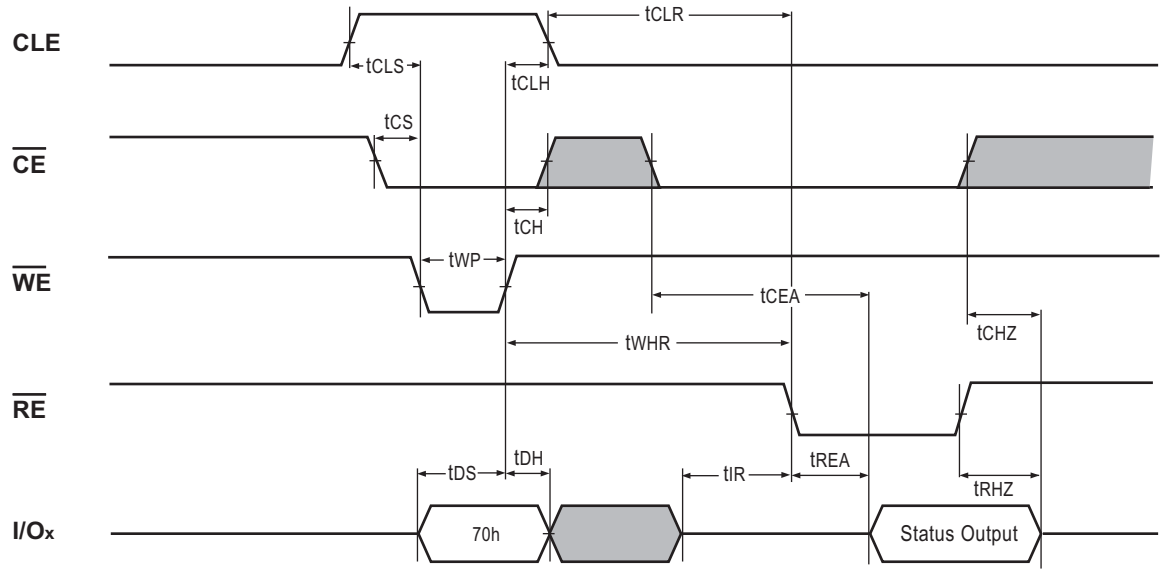


Figure 11: Status Read Cycle

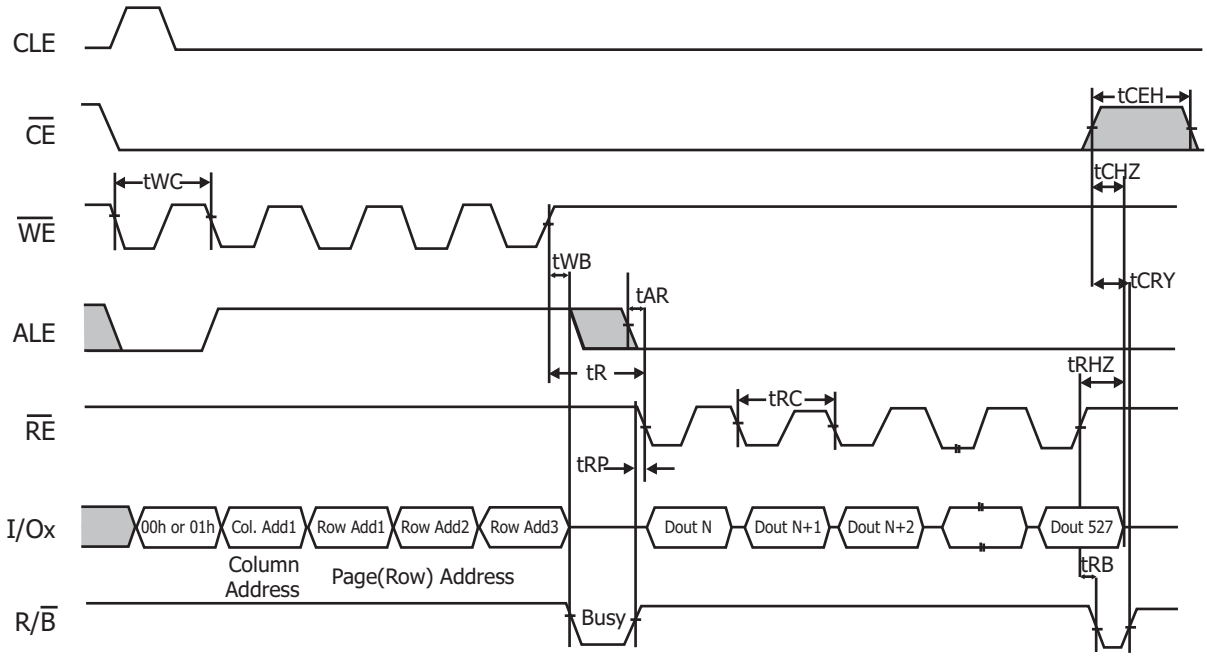


Figure 12: Read1 Operation (Read One Page)

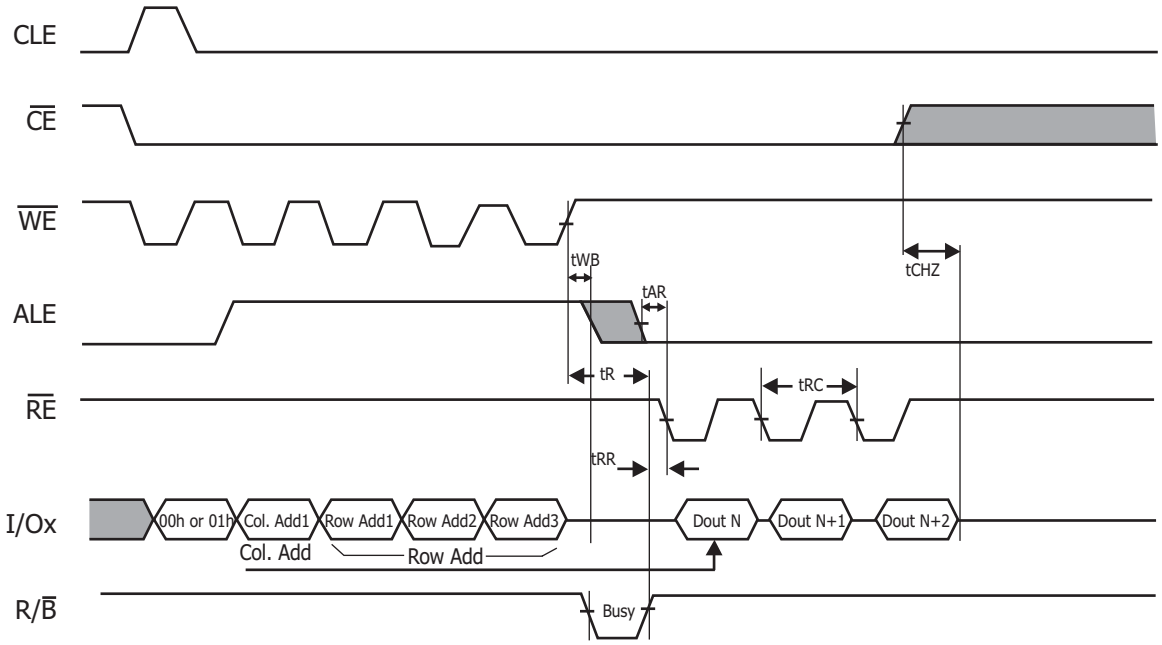


Figure 13: Read1 Operation intercepted by $\overline{CE}$

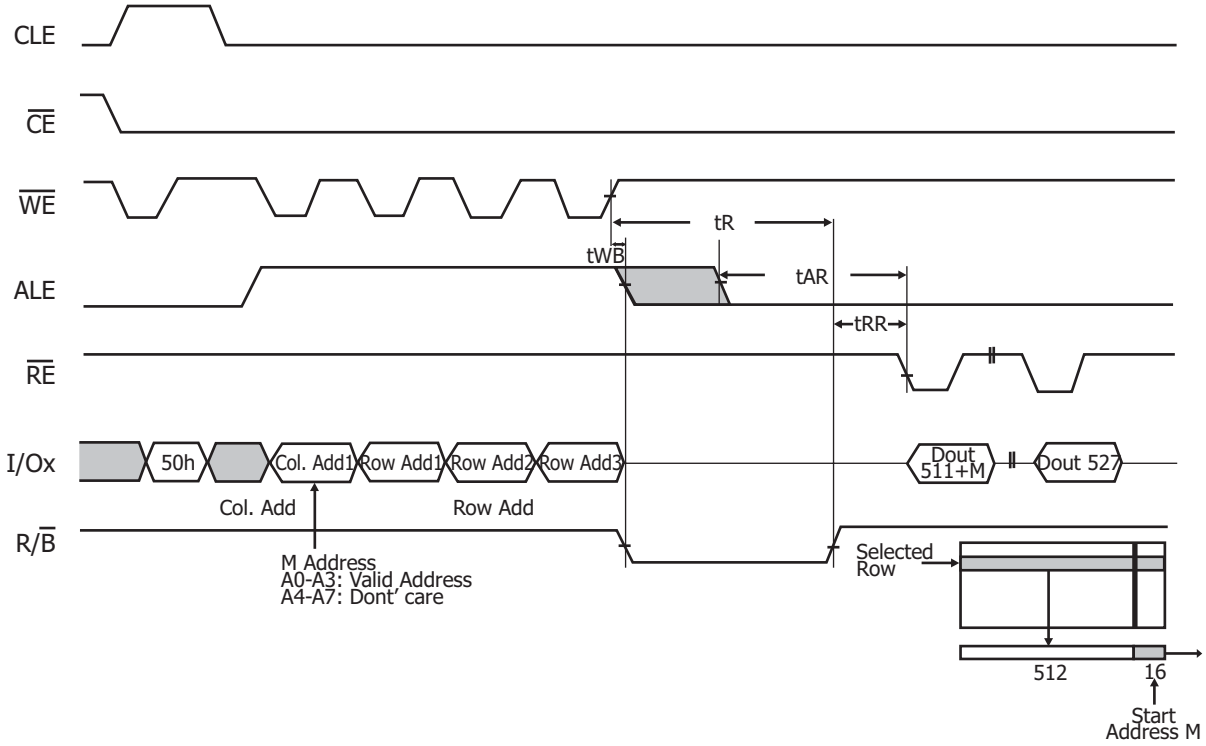


Figure 14: Read2 Operation (Read One Page)

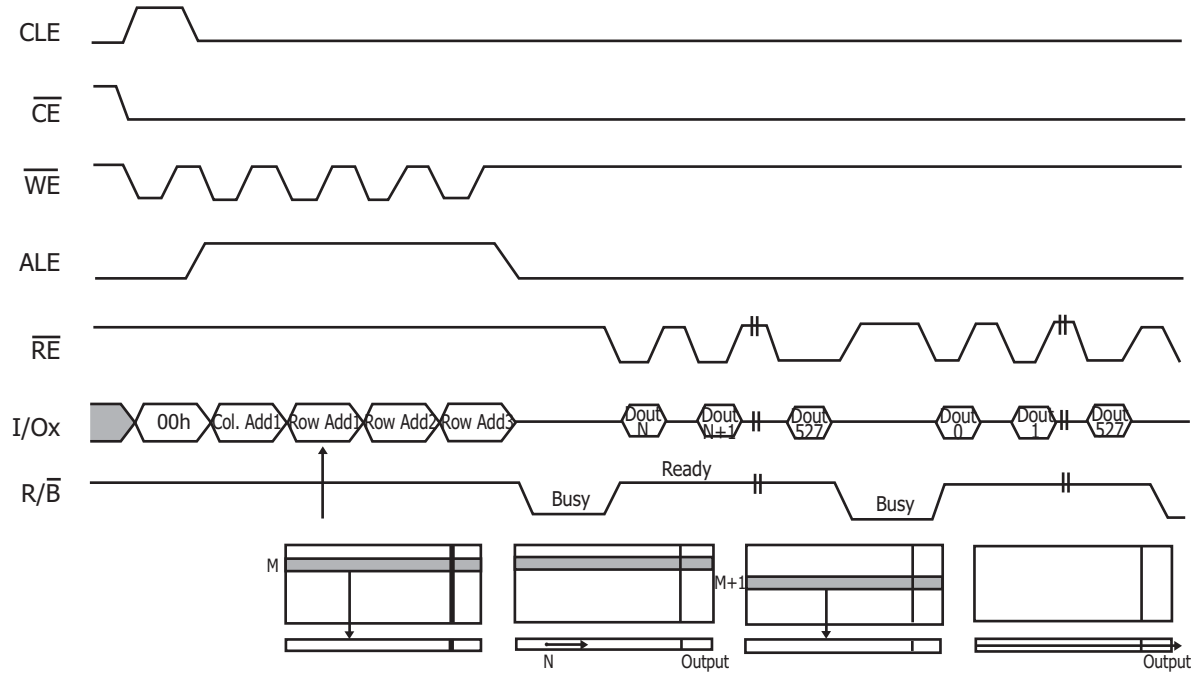


Figure 15: Sequential Row Read Operation Within a Block

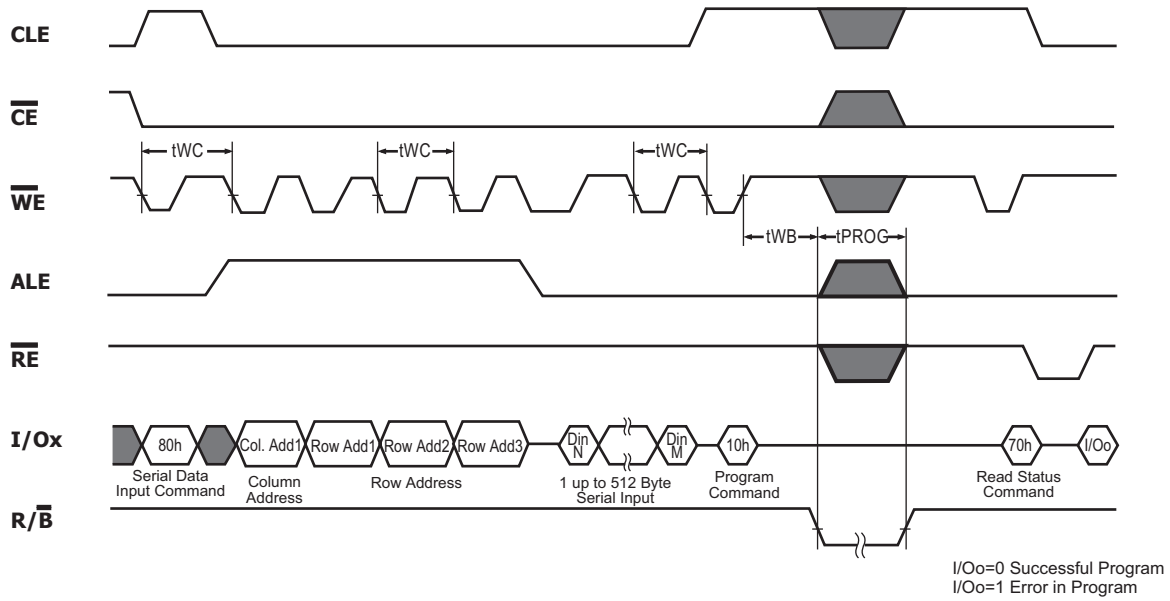


Figure 16: Page Program Operation

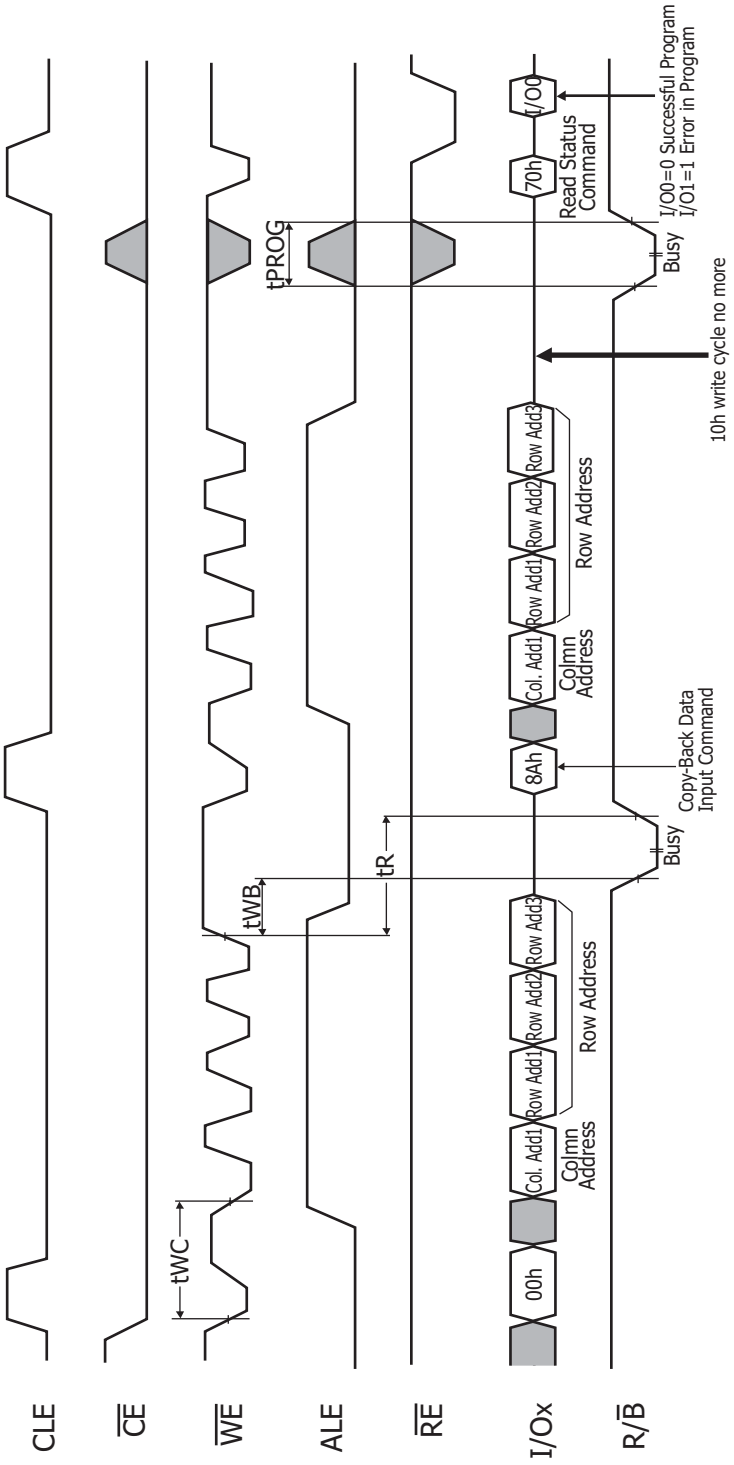


Figure 17 : Copy Back Program

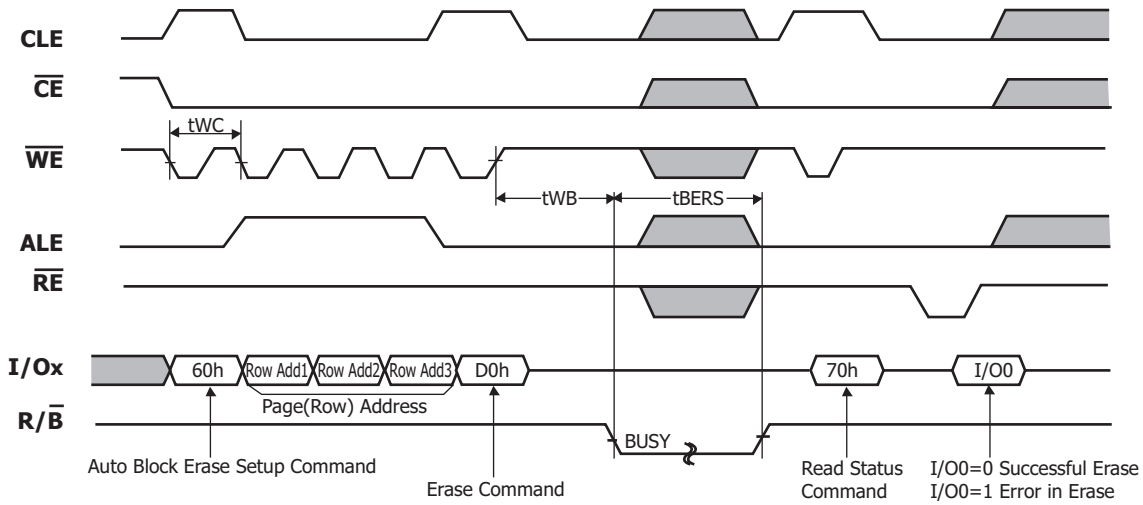


Figure 18: Block Erase Operation (Erase One Block)

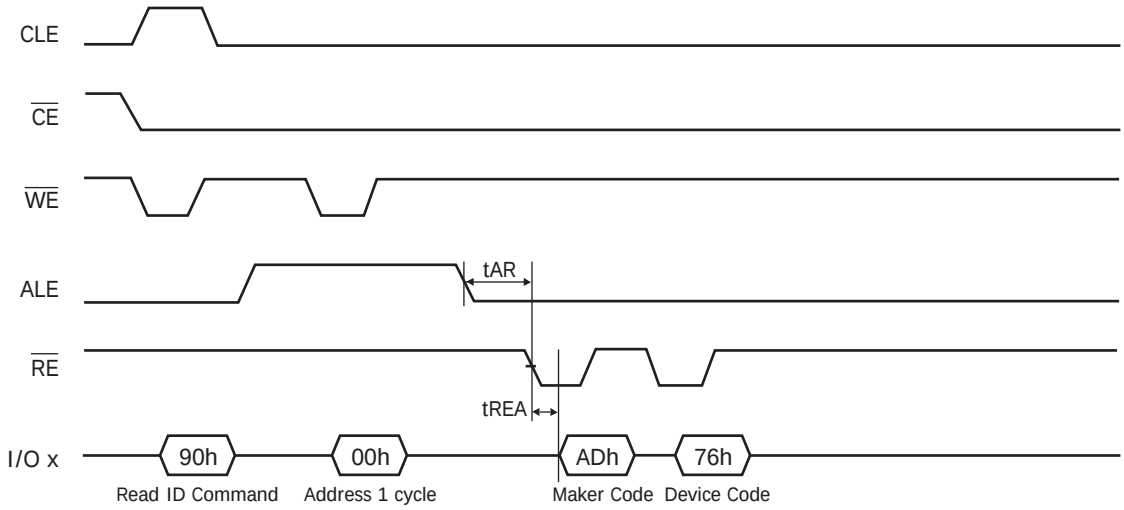


Figure 19: Read ID Operation

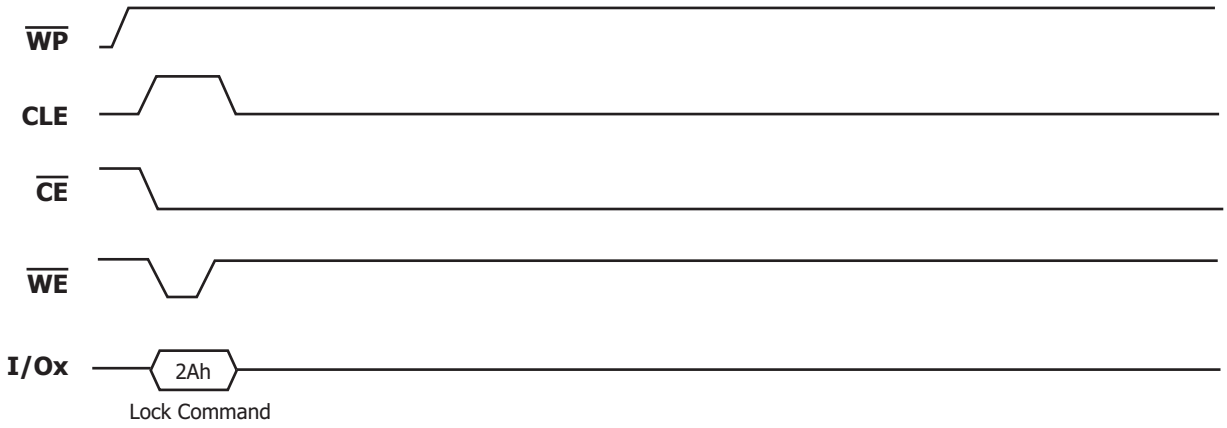


Figure 20: Lock Command

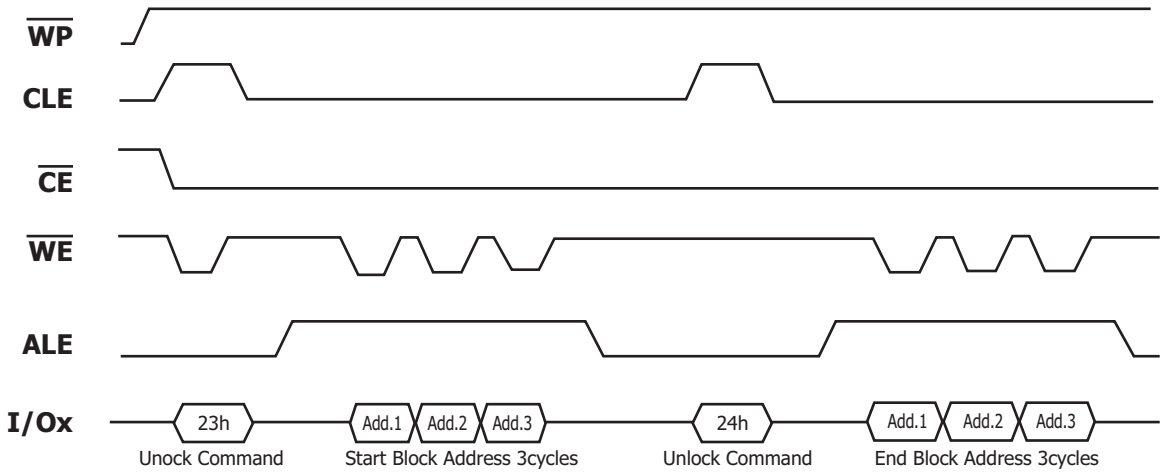


Figure 21: Unlock Command Sequence

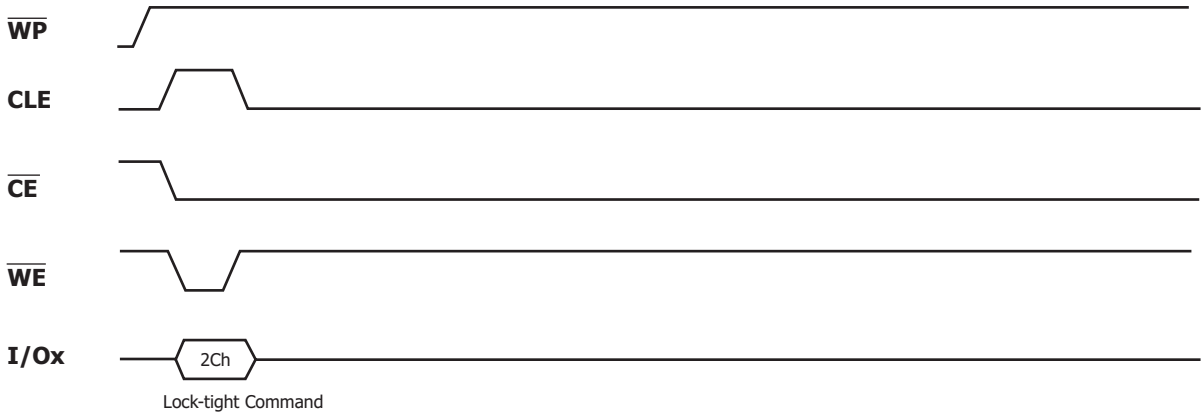


Figure 22: Lock Tight Command

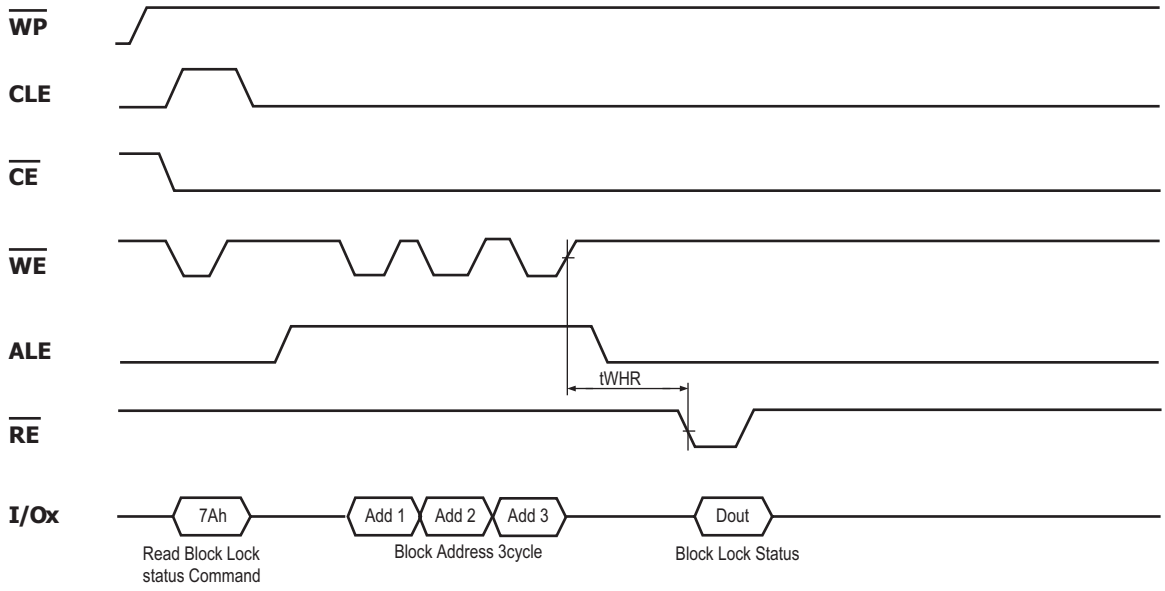


Figure 23: Lock Status Read Timing

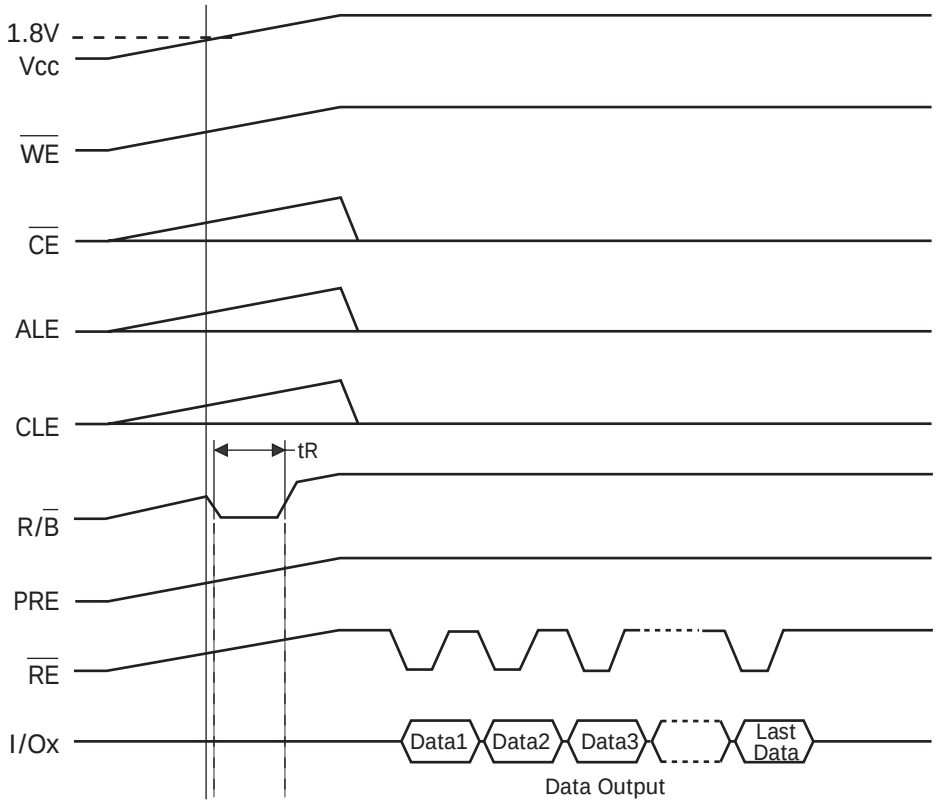


Figure 24: Automatic Read at Power On

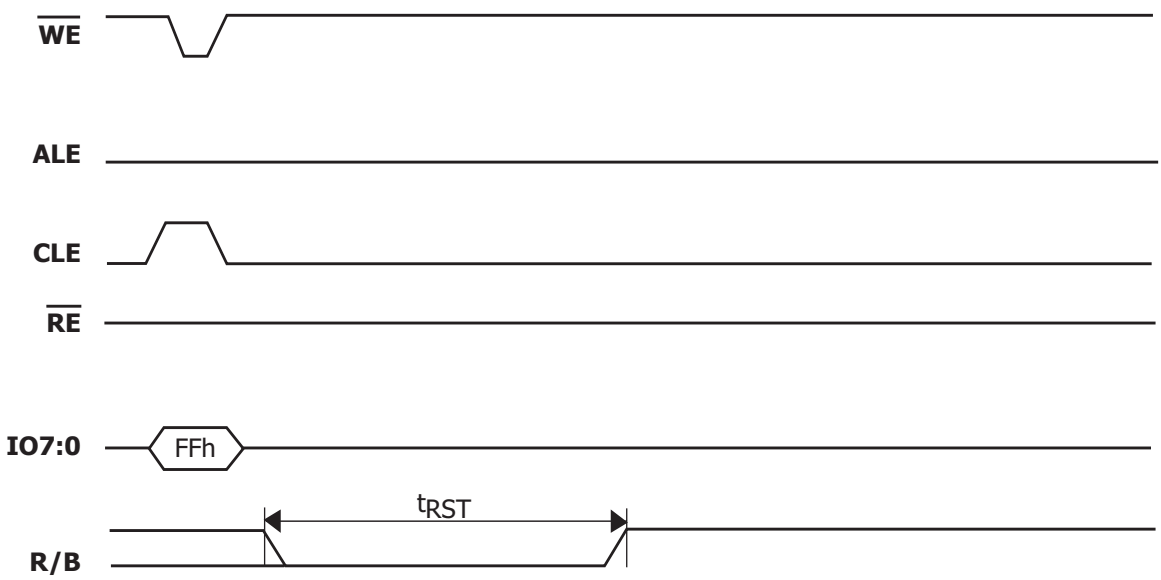


Figure 25: Reset Operation

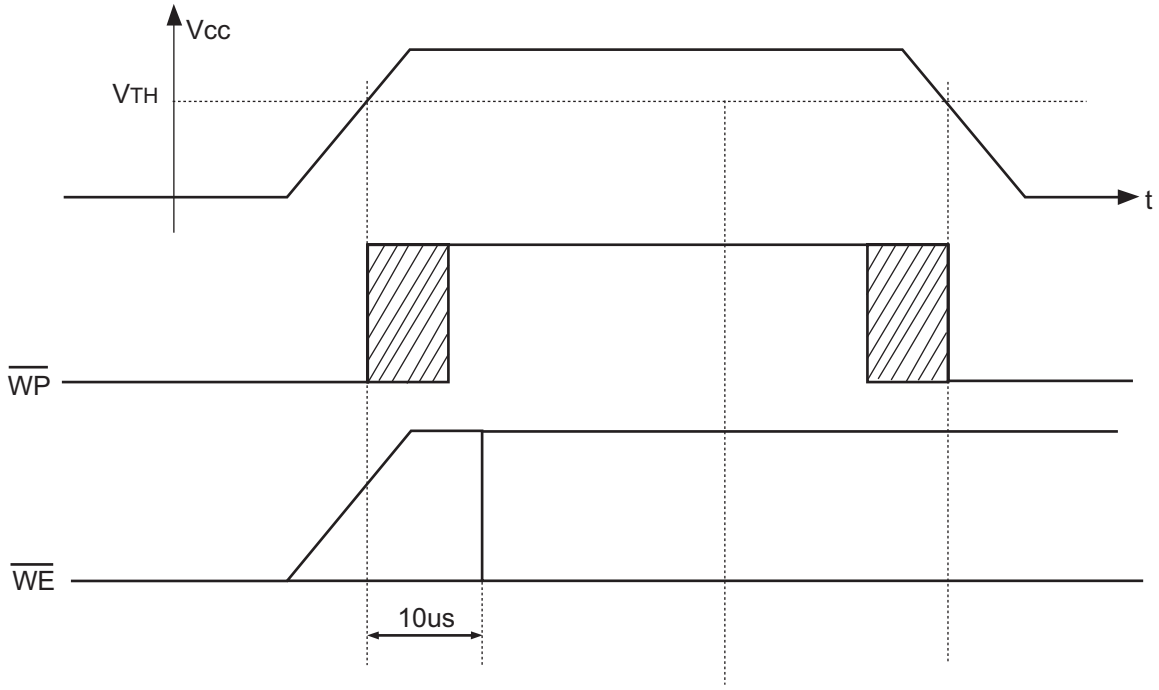


Figure 26: Power On/Off Timing

VTH = 1.5 Volt for 1.8 Volt Supply devices; 2.5 Volt for 3.3 Volt Supply devices

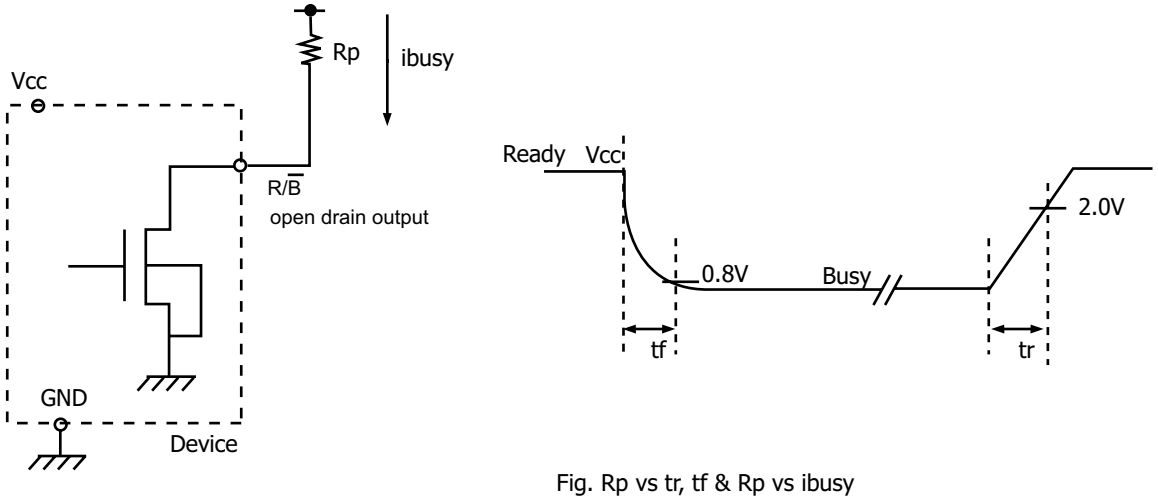
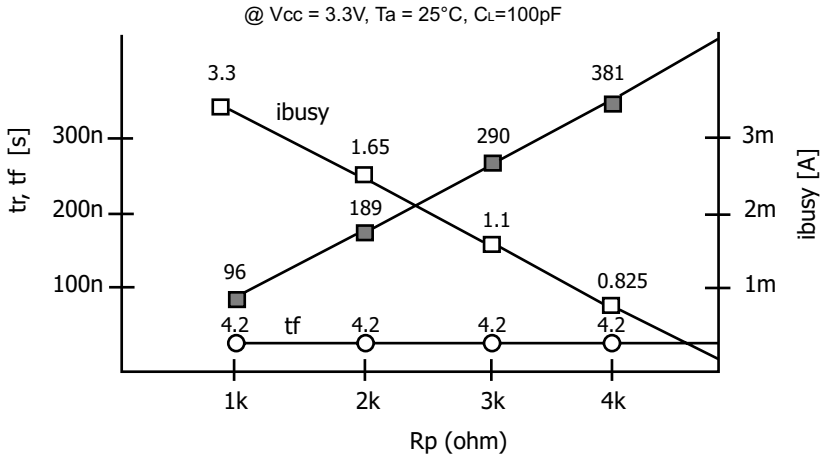


Fig. Rp vs tr, tf & Rp vs ibusy



Rp value guidence

$$Rp\ (min) = \frac{Vcc\ (Max.) - V_{OL}\ (Max.)}{I_{OL} + \sum I_L} = \frac{3.2V}{8mA + \sum I_L}$$

where IL is the sum of the input currnts of all devices tied to the R/$\overline{B}$ pin.

Rp(max) is determined by maximum permissible limit of tr

Figure 27: Ready/Busy Pin electrical specifications

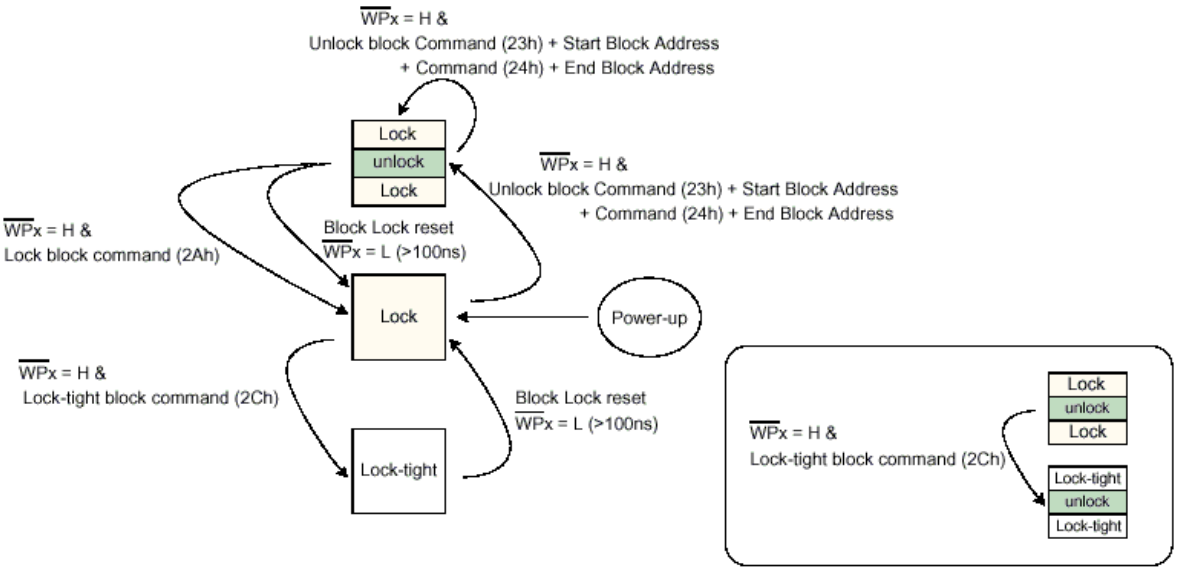


Figure 28: Lock/Unlock FSM Flow Cart

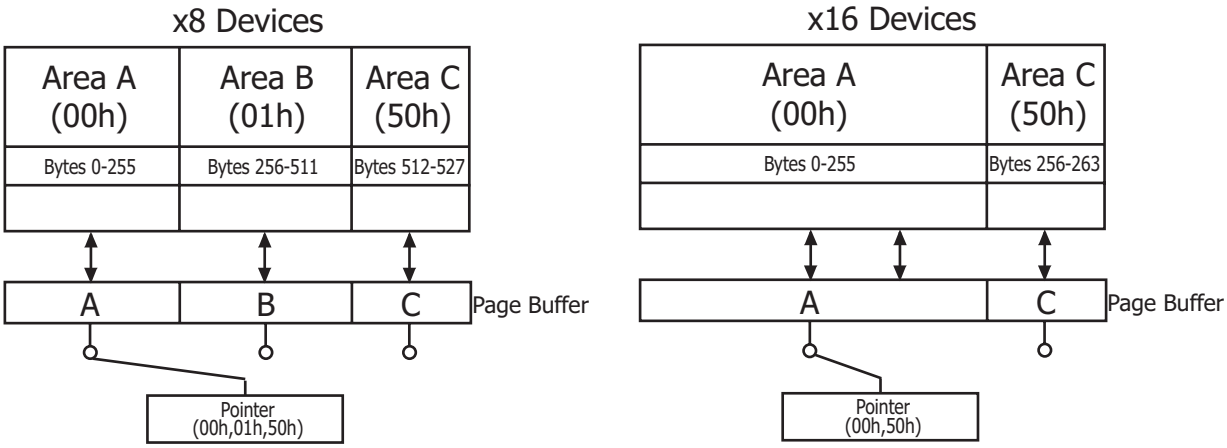


Figure 29: Pointer operations

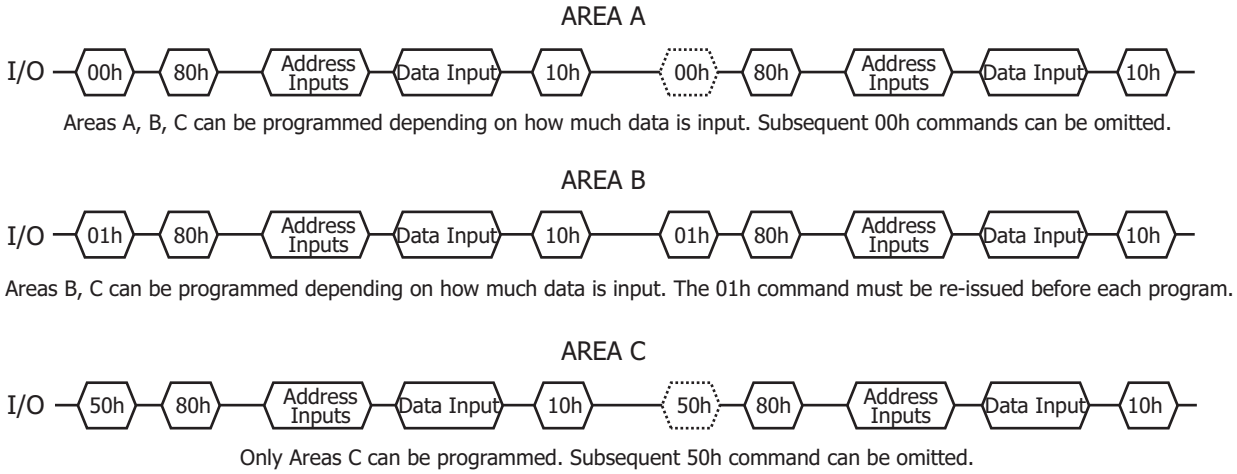


Figure 30: Pointer Operations for porgramming

System Interface Using $\overline{CE}$ don't care

To simplify system interface, $\overline{CE}$ may be inactive during data loading or sequential data-reading as shown below. So, it is possible to connect NAND Flash to a microprocessor. The only function that was removed from standard NAND Flash to make $\overline{CE}$ don't care read operation was disabling of the automatic sequential read function.

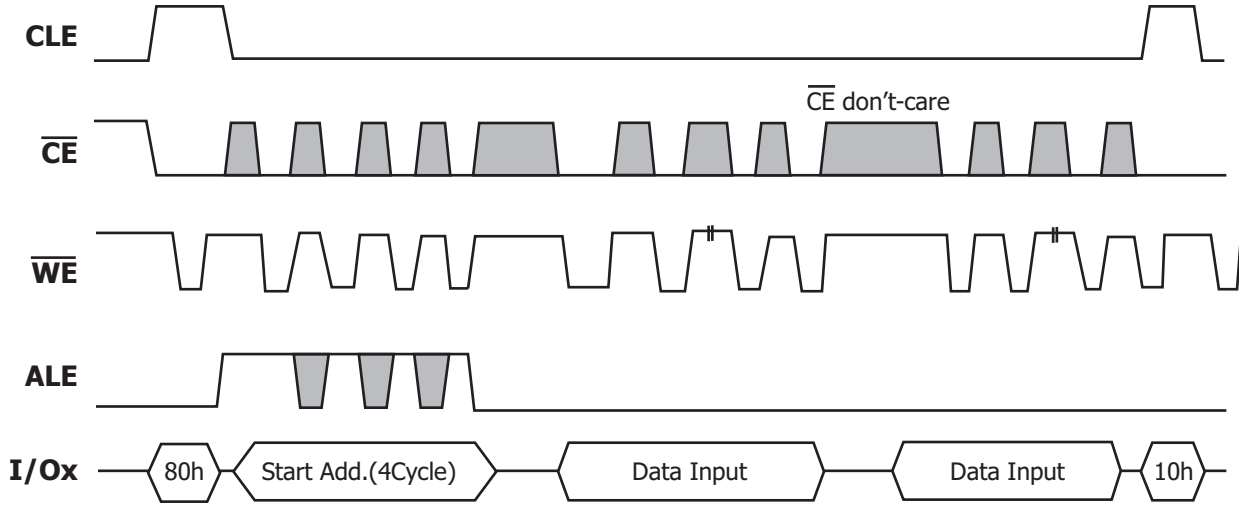


Figure 31: Program Operation with $\overline{CE}$ don't-care.

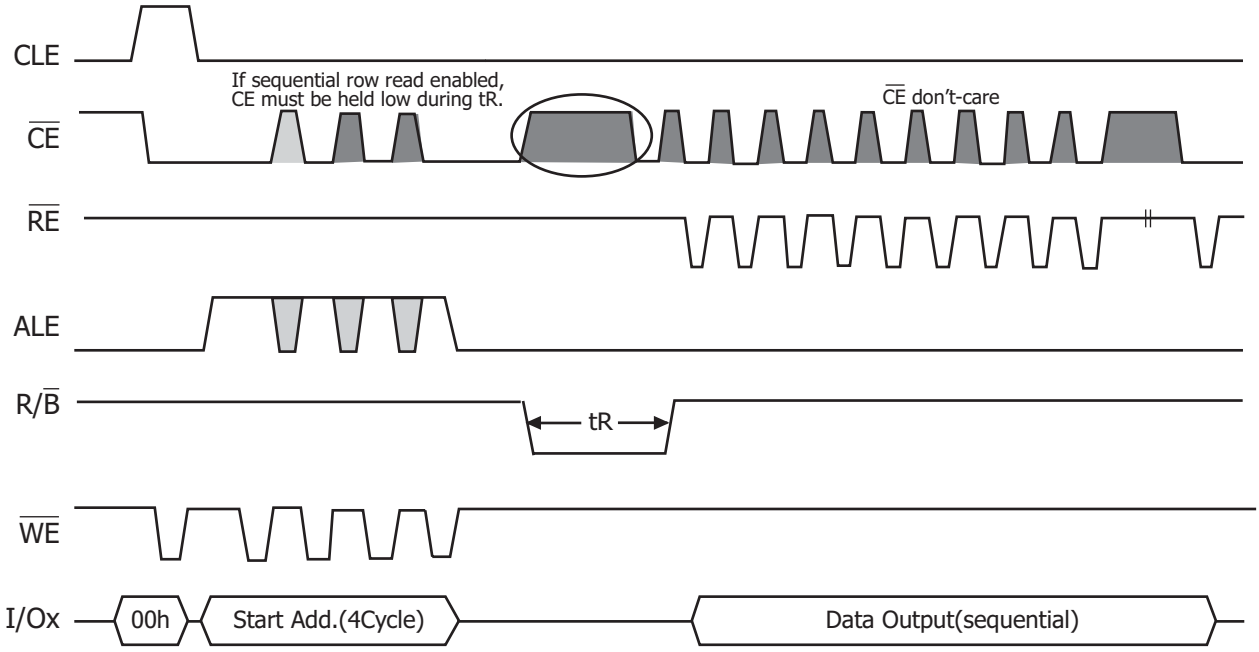


Figure 32: Read Operation with CE don't-care.

Bad Block Management

Devices with Bad Blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A Bad Block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor. The devices are supplied with all the locations inside valid blocks erased(FFh).

The Bad Block Information is written prior to shipping. Any block where the 6th Byte/ 3rd Word in the spare area of the 1st or 2nd page (if the 1st page is Bad) does not contain FFh is a Bad Block. The Bad Block Information must be read before any erase is attempted as the Bad Block Information may be erased. For the system to be able to recognize the Bad Blocks based on the original information it is recommended to create a Bad Block table following the flowchart shown in Figure 20. The 1st block, which is placed on 00h block address is guaranteed to be a valid block.

Block Replacement

Over the lifetime of the device additional Bad Blocks may develop. In this case the block has to be replaced by copying the data to a valid block. These additional Bad Blocks can be identified as attempts to program or erase them will give errors in the Status Register.

As the failure of a page program operation does not affect the data in other pages in the same block, the block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block. The Copy Back Program command can be used to copy the data to a valid block.

See the "Copy Back Program" section for more details.

Refer to Table 17 for the recommended procedure to follow if an error occurs during an operation.

Operation	Recommended Procedure
Erase	Block Replacement
Program	Block Replacement or ECC (with 1bit/512byte)
Read	ECC (with 1bit/512byte)

Table 17: Block Failure

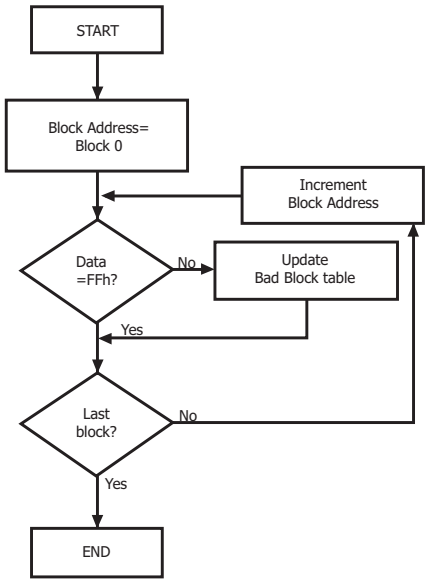


Figure 33: Bad Block Management Flowchart

Write Protect Operation

The Erase and Program Operations are automatically reset when $\overline{WP}$ goes Low (tWW = 100ns, min). The operations are enabled and disabled as follows (Figure 34~37)

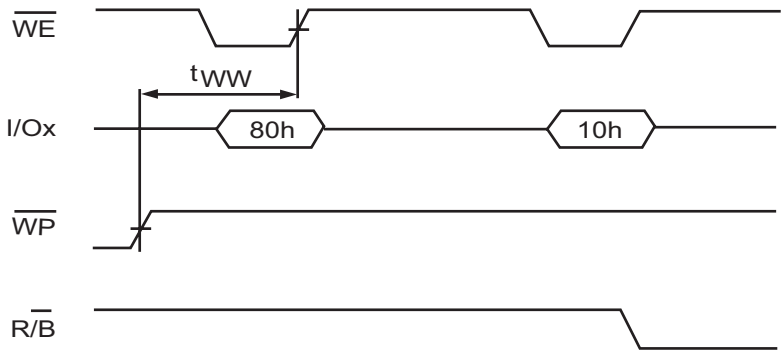


Figure 34: Enable Programming

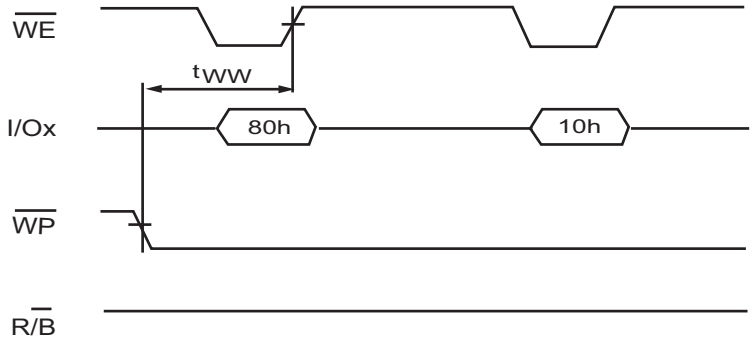


Figure 35: Disable Programming

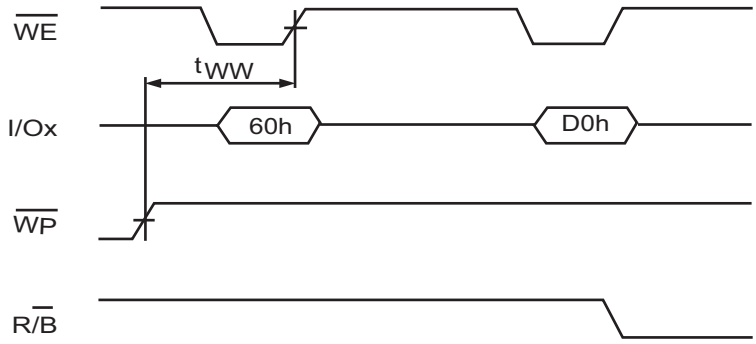


Figure 36: Enable Erasing

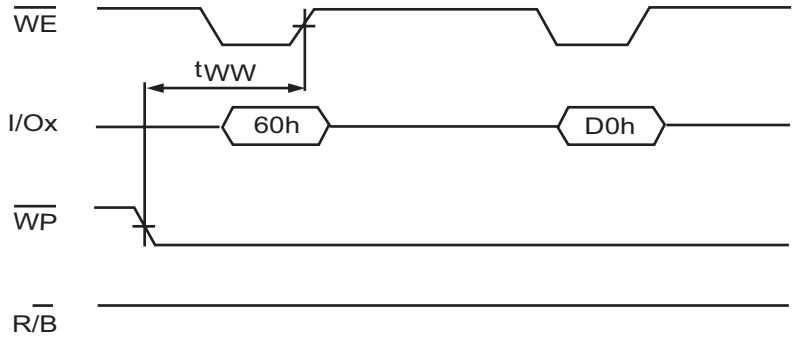


Figure 37: Disable Erasing

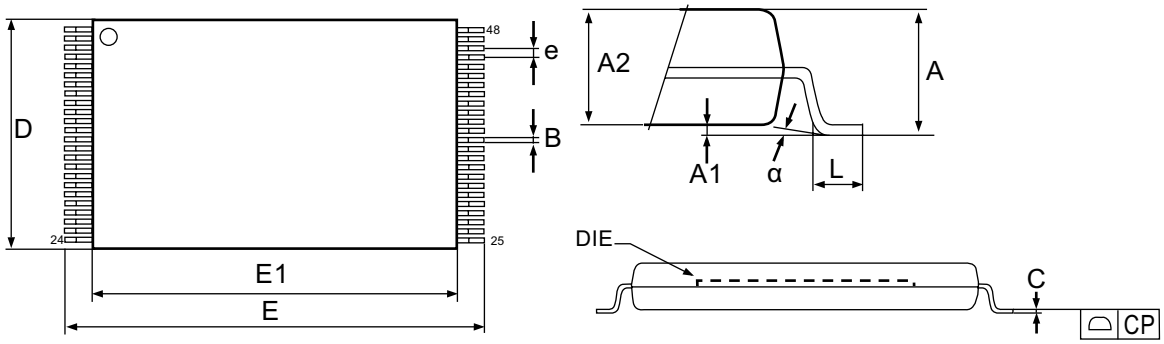


Figure 38: 48-pin TSOP1, 12 x 20mm, Package Outline

Symbol	millimeters		
	Min	Typ	Max
A			1.200
A1	0.050		0.150
A2	0.980		1.030
B	0.170		0.250
C	0.100		0.200
CP			0.100
D	11.910	12.000	12.120
E	19.900	20.000	20.100
E1	18.300	18.400	18.500
e		0.500	
L	0.500		0.680
alpha	0		5

Table 18: 48-pin TSOP1, 12 x 20mm, Package Mechanical Data

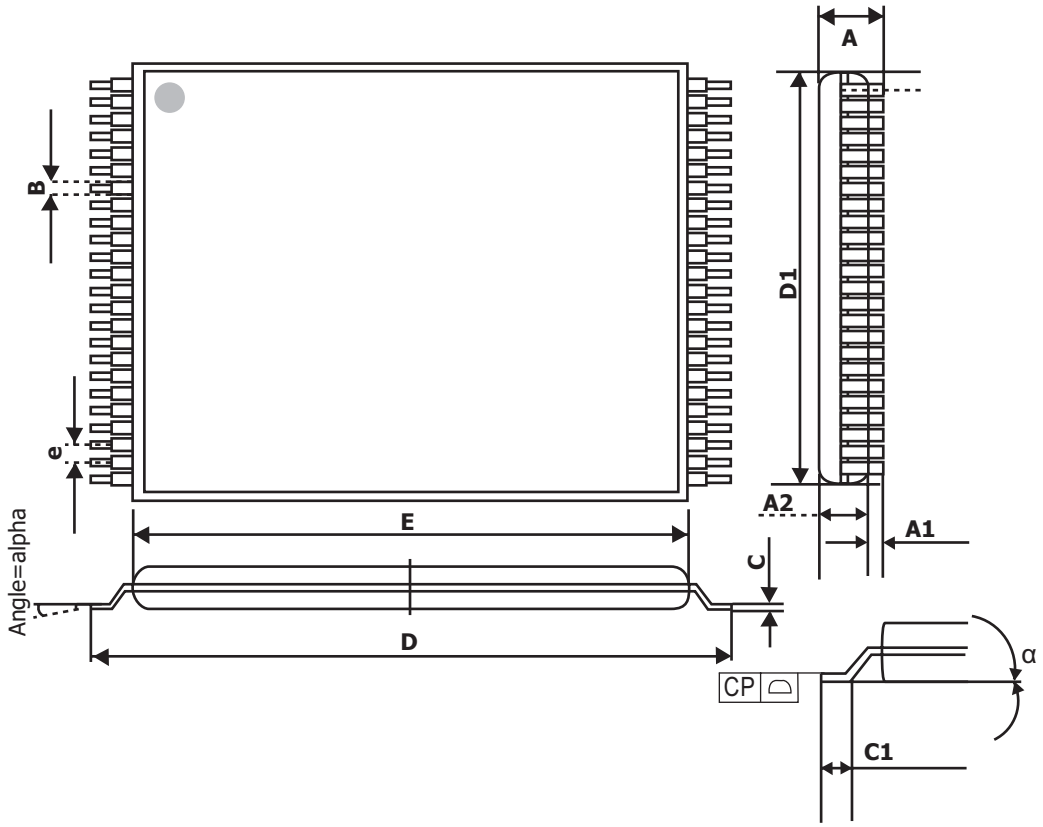


Figure 39. 48-pin USOP1, 12 x 17mm, Package Outline

Symbol	millimeters		
	Min	Typ	Max
A			0.650
A1	0	0.050	0.080
A2	0.470	0.520	0.570
B	0.130	0.160	0.230
C	0.065	0.100	0.175
C1	0.450	0.650	0.750
CP			0.100
D	16.900	17.000	17.100
D1	11.910	12.000	12.120
E	15.300	15.400	15.500
e		0.500	
alpha	0		8

Table 19: 48-pin USOP1, 12 x 17mm, Package Mechanical Data

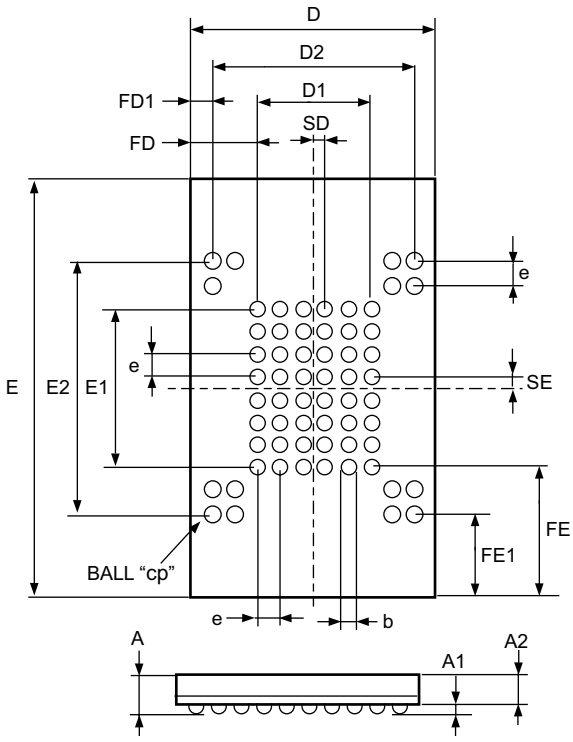


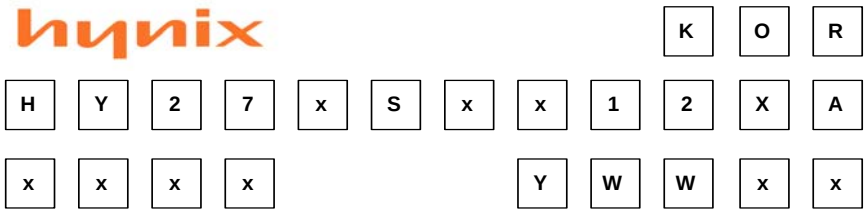
Figure 40. 63-ball FBGA - 9 x 11 ball array 0.8mm pitch, Pakage Outline

NOTE: Drawing is not to scale.

Symbol	Millimeters		
	Min	Typ	Max
A	0.80	0.90	1.00
A1	0.25	0.30	0.35
A2	0.55	0.60	0.65
b	0.40	0.45	0.50
D	8.90	9.00	9.10
D1		4.00	
D2		7.20	
E	10.90	11.00	11.10
E1		5.60	
E2		8.80	
e		0.80	
FD		2.50	
FD1		0.90	
FE		2.70	
FE1		1.10	
SD		0.40	
SE		0.40	

Table 20: 63-ball FBGA - 9 x 11 ball array 0.8mm pitch, Pakage Mechanical Data

MARKING INFORMATION - TSOP1/USOP

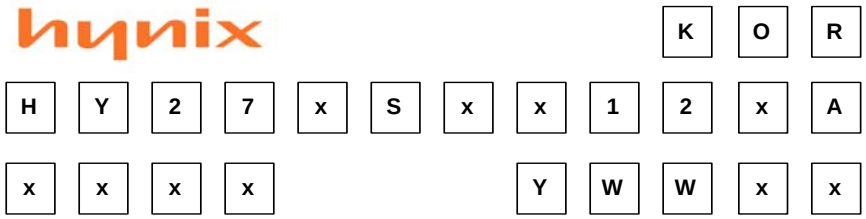
Packag	Marking Example
TSOP1 / USOP	

- hynix	: Hynix Symbol
- KOR	: Origin Country
- HY27xSxx12xA xxxx	: Part Number
HY: HYNIX	
27: NAND Flash	
x: Power Supply	: U(2.7V~3.6V), L(2.7V), S(1.8V)
S: Classification	: Single Level Cell+Single Die+Small Block
xx: Bit Organization	: 08(x8), 16(x16)
12: Density	: 512Mbit
x: Mode	: 1(1nCE & 1R/nB; Sequential Row Read enable)
	2(1nCE & 1R/nB; Sequential Row Read Disable)
A: Version	: 2nd Generation
x: Package Type	: T(48-TSOP1), S(48-USOP)
x: Package Material	: Blank(Normal), P(Lead Free)
x: Operating Temperature	: C(0℃~70℃), E(-25℃~85℃)
	M(-30℃~85℃), I(-40℃~85℃)
x: Bad Block	: B(Included Bad Block), S(1~5 Bad Block),
	P(All Good Block)
- Y: Year (ex: 5=year 2005, 06= year 2006)	
- ww: Work Week (ex: 12= work week 12)	
- xx: Process Code	

Note

- Capital Letter	: Fixed Item
- Small Letter	: Non-fixed Item

MARKING INFORMATION - FBGA

Packag	Marking Example
FBGA	

- hynix	: Hynix Symbol
- KOR	: Origin Country
- HY27xSxx12xA xxxx	: Part Number
HY: HYNIX	
27: NAND Flash	
x: Power Supply	: U(2.7V~3.6V), L(2.7V), S(1.8V)
S: Classification	: Single Level Cell+Single Die+Small Block
xx: Bit Organization	: 08(x8), 16(x16)
12: Density	: 512Mbit
x: Mode	: 1(1nCE & 1R/nB; Sequential Row Read Enable) 2(1nCE & 1R/nB; Sequential Row Read Disable)
A: Version	: 2nd Generation
x: Package Type	: F(63FBGA)
x: Package Material	: Blank(Normal), P(Lead Free)
x: Operating Temperature	: C(0℃~70℃), E(-25℃~85℃) M(-30℃~85℃), I(-40℃~85℃)
x: Bad Block	: B(Included Bad Block), S(1~5 Bad Block), P(All Good Block)
- Y: Year (ex: 5=year 2005, 06= year 2006)	
- ww: Work Week (ex: 12= work week 12)	
- xx: Process Code	
Note	
- Capital Letter	: Fixed Item
- Small Letter	: Non-fixed Item