10-bit Digital Differential Voltage and Current Monitor

FEATURES & APPLICATIONS

- **Real-time power monitoring for "Green" systems**
- **Differential Voltage Sensing of the DC-DC converter output voltage**
- **Supply-side current monitoring (10-bit ADC)**
- **10-bit ADC readout of supply voltage over I^2C bus**
- **Two programmable general purpose sensor inputs (COMP1/2) – UV/OV with FAULT Output**
- **Programmable glitch filters (COMP1/2)**
- **Programmable internal COMP1/2 VREF: 0.5V or 1.25V**
- **Operates from 2.7V to 5.5V supply**
- **Current sensing from 4.0V to 15V supply**
- **Programmable general-purpose inputs/outputs**
- **General-purpose 256-Byte EEPROM with Write Protect**
- **I^2C 2-wire serial bus for programming configuration and monitoring status**
- **28-lead 5x5 QFN package**

Applications

- **In-system test and control of Point-of-Load (POL)**
- **Power Supplies for Multi-voltage Processors, DSPs and ASICs**
- **Routers, Servers, Storage Area Networks**

INTRODUCTION

The SMM153 is a highly accurate power supply voltage/current supervisor and monitor that allows real-time power measurement for power-critical designs. The part includes an internal voltage reference to accurately monitor the supply to within ±1%. The SMM153 can read the differential voltage of the supply and voltage drop of the current sense resistor over the I^2C bus using an on-chip 10-bit ADC.

Two general purpose analog input pins are provided for sensing under- or over-voltage conditions. A programmable glitch filter associated with these inputs allows the user to ignore spurious noise signals. A FAULT# pin is asserted once either input set point is exceeded. The SMM153 also provides four programmable general-purpose inputs/outputs.

Using the I^2C interface, a host system can communicate with the SMM153 status register and utilize 256-bytes of nonvolatile memory. The SMM153 operates from +2.7V to +5.5V, however it can sense input current from an input supply of +4.0V to +15V. The device is offered in both commercial and industrial temperature ranges and the package is a space-saving 5x5 QFN-28 one.

TYPICAL APPLICATION

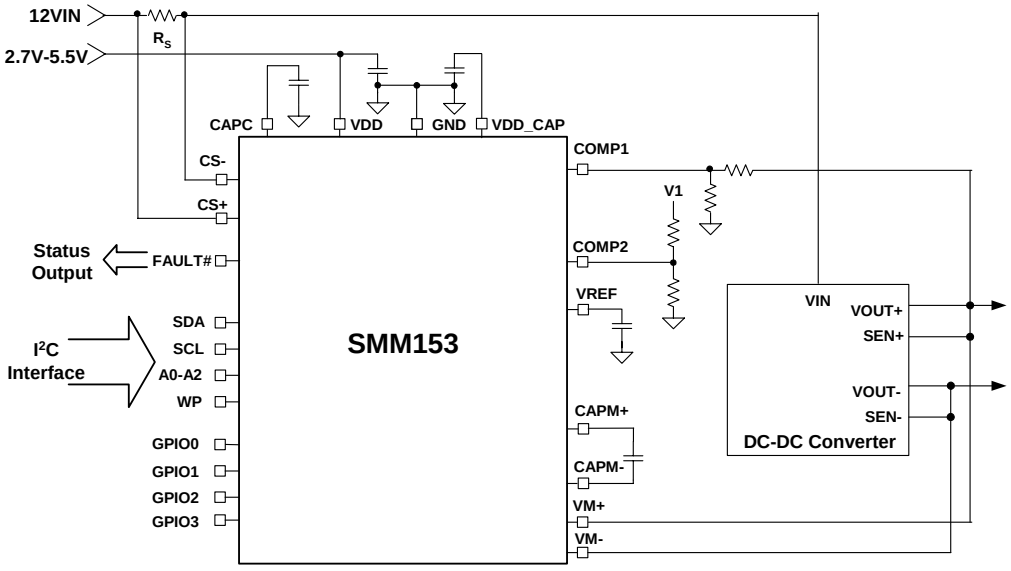


Figure 1 – Application with the SMM153 used to Monitor a DC/DC Converter.

Notes: R_S must be Kelvin sensed for maximum current sensing accuracy. This is an applications example only. Some components and values are not shown.

GENERAL DESCRIPTION

The SMM153 is a highly accurate power supply voltage/current supervisor and monitor that allows real-time power measurement for power-critical designs. This advance functionality allows the development of “Green” systems and introduces higher levels of system reliability.

The SMM153 senses converter input current using a Kelvin-connected sense resistor in series with the converter supply whose terminals are connected to the CS+ and CS- pins. The internal ADC, also used for measuring the converter’s output voltage, is used to measure the converter’s input current using the voltage dropped across the current sense resistor R_S (see Figure 1).

The SMM153 has two additional input pins and one additional output pin. The input pins, COMP1 and COMP2, are high impedance inputs, each connected to a comparator and compared against the internal reference. Each comparator can be independently programmed to monitor for under- or over-voltage conditions. When either of the COMP1 or COMP2 inputs are in fault the open-drain FAULT# output will be pulled low.

The SMM153 also provides real-time, differential voltage measurement of the converter output voltage. The differential sensing of the VM+ and VM- inputs eliminates the ground or low-side error sometimes encountered with a single-ended sensing schemes.

Programming of the SMM153 is performed over the industry standard I^2C 2-wire serial data interface. A status register is available to read the state of the part and a Write Protect (WP) pin is available to prevent writing to the configuration registers and EE memory.

The SMM153 also provides four programmable general-purpose inputs/outputs. The power-on state of these I/Os is determined via NV memory. Volatile programming allows the user to select the logic level (HIGH or LOW) of each I/O, which can also be read via a status register.

INTERNAL BLOCK DIAGRAM

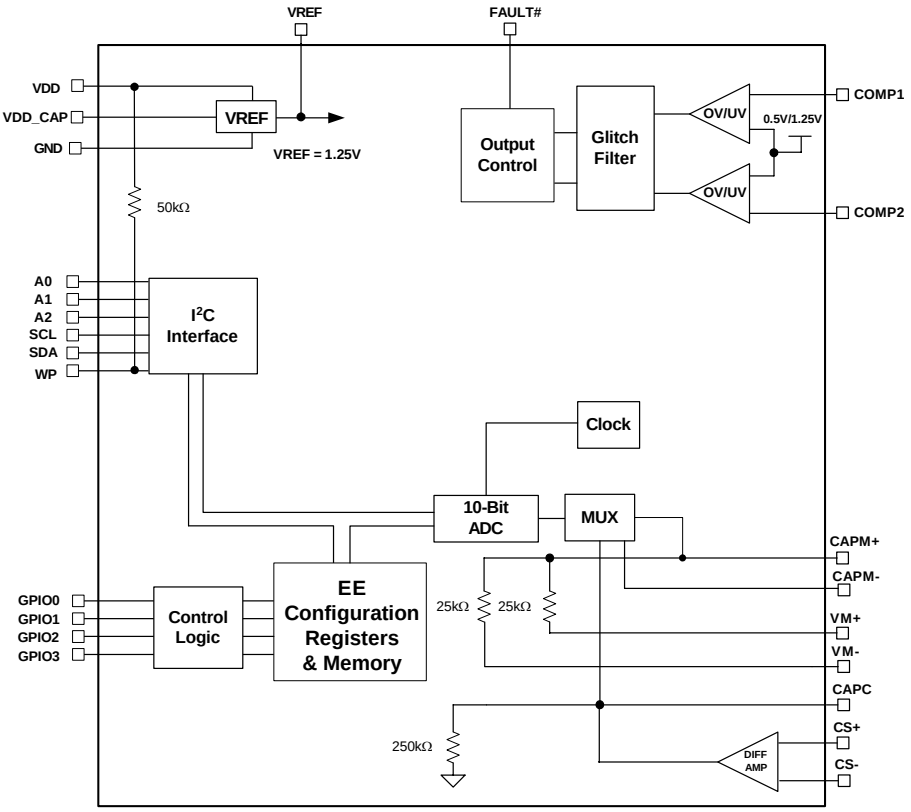
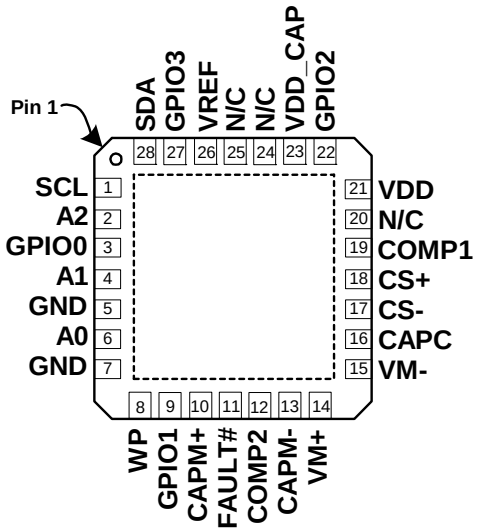


Figure 2 – SMM153 Controller Internal Block Diagram.

PACKAGE AND PIN CONFIGURATION

28-Pad 5x5 QFN
Top View



PIN DESCRIPTION

Pin Number	Pin Type	Pin Name	Pin Description
28	I/O	**SDA**	I^2C Bi-directional data line
1	I	**SCL**	I^2C clock input.
2	I	**A2**	The address pins are biased either to VDD, GND or left floating. This allows for a total of 21 distinct device addresses. When communicating with the SMM153 over the 2-wire bus these pins provide a mechanism for assigning a unique bus address.
4	I	**A1**	
6	I	**A0**	
3, 9, 22, 27	I/O	**GPIO0,1,2,3**	General purpose inputs/outputs.
8	I	**WP**	Programmable Write Protect active high/low input. When asserted, writes to the configuration registers and general purpose EE are not allowed. The WP input is internally tied to VDD with a 50KΩ resistor.
10, 13	CAP	**CAPM+, -**	External capacitor inputs used to filter the VM+/VM- inputs, 0.22μF.
14	I	**VM+**	Voltage monitor input. Connect to the DC-DC converter positive sense line or its +Vout pin.
15	I	**VM-**	Voltage monitor input. Connect to the DC-DC converter negative sense line or its -Vout pin.
18	I	**CS+**	Current monitor input + side. Kelvin connect to the input supply side of the current sense resistor.
17	I	**CS-**	Current monitor input - side. Kelvin connect to the load side of the current sense resistor.
26	PWR	**VREF**	Internal reference voltage of 1.25V. Connect to GND through a 0.1uF capacitor to improve noise immunity.
16	O	**CAPC**	External capacitor input used to filter the CS+/CS- input. Typical value: 1uF.
21	PWR	**VDD**	Power supply of the part.
23	PWR	**VDD_CAP**	External capacitor input used to filter the internal VDD supply rail.
5, 7	GND	**GND**	Ground of the part. The SMM153 ground pin should be connected to the ground of the device under control or to a star point ground. PCB layout should take into consideration ground drops.
19	I	**COMP1**	COMP1 and COMP2 are high impedance inputs, each connected internally to a comparator and compared against the internally programmable VREF voltage. Each comparator can be independently programmed to monitor for UV or OV. The monitor level is set externally with a resistive voltage divider.
12	I	**COMP2**	
11	O	**FAULT#**	When either of the COMP1 or COMP2 inputs are in fault the open-drain FAULT# output will be pulled low. A configuration option exists to disable the FAULT# output while the device is margining.
29	GND	**GND**	GND. The bottom side metal plate (Pad 29) should be connected on the PCB to GND for optimized noise performance.

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias .....-55°C to 125°C
Storage Temperature QFN .....-65°C to 150°C
Terminal Voltage with Respect to GND:
VDD Supply Voltage .....-0.3V to 6.0V
All Others ..... -0.3V to VDD + 0.7V
FAULT#..... GND to 15.0V
CS+, CS-..... -0.3V to 16.0V
Output Short Circuit Current 100mA
Reflow Solder Temperature (10 secs) .....240°C
Junction Temperature.....150°C
Human Body ESD Rating per JEDEC.....2000V
Machine Model ESD Rating per JEDEC.....200V
Latch-Up testing per JEDEC.....±100mA

RECOMMENDED OPERATING CONDITIONS

Temperature Range (Industrial).....–40°C to +85°C
(Commercial).....0°C to +70°C
CS+, CS- ..... 4.0V to 15V
VDD Supply Voltage ..... 2.7V to 5.5V
Inputs.....GND to VDD

Package Thermal Resistance (θ_{JA})
28-Pad QFN (Thermal pad connected to PCB).....37.2°C/W
28-Pad QFN (Thermal pad not connected to PCB)....66.5°C/W

Moisture Classification Level 3 (MSL 3) per J-STD- 020

RELIABILITY CHARACTERISTICS
Data Retention.....20 Years
Endurance.....100,000 Cycles

Note - The device is not guaranteed to function outside its operating rating. Stresses listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions outside those listed in the operational sections of the specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability. Devices are ESD sensitive. Handling precautions are recommended.

DC OPERATING CHARACTERISTICS

T_A= 0°C to +70°C, VDD = 2.7V to 5.5V, VCS = 4.0V to 15V, unless otherwise noted. All voltages are relative to GND. Note 6.

Symbol	Parameter	Notes	Min.	Typ.	Max	Unit
VDD	Supply Voltage		2.7	3.3	5.5	V
VM_{Range}	Sense Voltage Common Mode Range	VM+ pin voltage range, Note 5	-0.3		VDD	V
		VM- pin voltage range, Note 5	-0.3		+0.5	V
CS_{Range}	Current Sense Common Mode Voltage Range	CS+, CS- pin voltage range	4.0		15	V
I_{DD}	Supply Current from VDD			3		mA
V_{IH}	Input High Voltage SDA, SCL, WP	VDD = 2.7V	0.9xVDD		VDD	V
		VDD = 5.0V	0.7xVDD		VDD	
V_{IL}	Input Low Voltage SDA, SCL, WP	VDD = 2.7V			0.1xVDD	V
		VDD = 5.0V			0.3xVDD	
V_{OL}	Open Drain Output FAULT#	ISINK = 1mA		0.2		V
V_{AIH}	Address Input High Voltage, A2, A1, A0	VDD = 2.7V, $R_{pullup} \leq 300k\Omega$	0.9xVDD		VDD	V
		VDD = 5.0V, $R_{pullup} \leq 300k\Omega$	0.7xVDD		VDD	
V_{AIL}	Address Input Low Voltage, A2, A1, A0	VDD = 2.7V, $R_{pulldown} \leq 300k\Omega$			0.1xVDD	V
		VDD = 5.0V, $R_{pulldown} \leq 300k\Omega$			0.3xVDD	
I_{AIT}	Address Input Tristate Maximum Leakage – High Z	VDD = 2.7V	-3.0		+3.0	µA
OV/UV	Monitor Voltage Range	COMP1 and COMP2 pins	0		VDD	V

DC OPERATING CHARACTERISTICS (CONTINUED)

T_A= 0°C to +70°C, VDD = 2.7V to 5.5V, VCS = 4.0V to 15V, unless otherwise noted. All voltages are relative to GND. Note 6.

Symbol	Parameter	Notes	Min.	Typ.	Max	Unit
V_{HYST}	COMP1/2 DC Hysteresis	COMP1 and COMP2 pins, V_{TH}-V_{TL} Note 1		10		mV
$R_{Pull-Up}$	Input Pull-Up Resistors	See Pin Descriptions, Note 5		50		kΩ
VREF	Internal COMP1/2 Reference	VREF=1.25V	1.24	1.25	1.26	V
		VREF=0.5V	0.495	0.500	0.505	
VM_{ADC}	Voltage Monitor ADC Measure Range	VM+ - VM-, Note 5	0		VDD	V
VM_{ACC}	Voltage Monitor Accuracy	VM+ - VM- = 1.2V, Note 4	-1.0	±0.75	+1.0	%
		VM+ - VM- = 2.5V, Note 4	-1.0	±0.75	+1.0	%
R_{VM}	VM+, VM- Input Resistance			50		kΩ
$CMRR_{VM}$	Voltage Sense Common Mode Rejection Ratio	V_{CM} (VM+, VM-) = 0.5V – VDD, Note 5		62		dB
CS_{ADC}	Current Monitor ADC Measure Range	Minimum CS+ - CS- voltage		0		mV
		Maximum CS+ - CS- voltage		100		
CS_{ACC}	Current Sense Accuracy	$CS_{ADC} \geq$ 50mV, Note 2	-2		+2	%
		CS_{ADC} < 50mV, Note 2	-1		+1	mV
$CMRR_{CS}$	Current Sense Common Mode Rejection Ratio	V_{CM} (CS+, CS-) = 5.0V, Note 5		100		dB
		V_{CM} (CS+, CS-) = 12V, Note 5		80		

AC OPERATING CHARACTERISTICS

T_A= 0°C to +70°C, VDD = 2.7V to 5.5V, VCS = 4.0V to 15V, unless otherwise noted. All voltages are relative to GND. Note 6.

Symbol	Parameter	Notes	Min.	Typ.	Max	Unit
t_{ADC_DAC}	Monitor sampling/conversion period	Update period for ADC conversion and DAC update		1.8		ms
t_{GLITCH_COMP}	Programmable COMP1 & COMP2 glitch filter times			0		ms
				10		ms
				20		ms
				40		ms
				80		ms
				100		ms
				120		ms
				140		ms

I²C 2-WIRE SERIAL INTERFACE AC OPERATING CHARACTERISTICS – 100kHz

T_A= 0°C to +70°C, VDD = 2.7V to 5.5V unless otherwise noted. All voltages are relative to GND. See Figure 3 Timing Diagram.

Symbol	Description	Conditions	Min	Typ	Max	Units
f_{SCL}	SCL Clock Frequency		0		100	KHz
t_{LOW}	Clock Low Period		4.7			µs
t_{HIGH}	Clock High Period		4.0			µs
t_{BUF}	Bus Free Time	Before New Transmission, Note 5	4.7			µs
$t_{SU:STA}$	Start Condition Setup Time		4.7			µs
$t_{HD:STA}$	Start Condition Hold Time		4.0			µs
$t_{SU:STO}$	Stop Condition Setup Time		4.7			µs
t_{AA}	Clock Edge to Data Valid	SCL low to valid SDA (cycle n)	0.2		3.5	µs
t_{DH}	Data Output Hold Time	SCL low (cycle n+1) to SDA change	0.2			µs
t_R	SCL and SDA Rise Time	Note 5			1000	ns
t_F	SCL and SDA Fall Time	Note 5			300	ns
$t_{SU:DAT}$	Data In Setup Time		250			ns
$t_{HD:DAT}$	Data In Hold Time		0			ns
TI	Noise Filter SCL and SDA	Noise suppression		100		ns
t_{WR}	Write Cycle Time				5	ms

Note 1: V_{HYST} is measured with a 1.25V external voltage and is determined by subtracting Threshold Low from Threshold High, V_{TH}-V_{TL} while monitoring the FAULT# pin state. Actual DC Hysteresis is derived from the equation: ($V_{IN(COMP1/2)}$/V_{REF})(V_{HYST}). For example, if $V_{IN(COMP1/2)}$/=2.5V and V_{REF}=1.25V then Actual DC Hysteresis= (2.5V/1.25V)(0.003V)=6mV.
Note 2: Current sense accuracy depends on the current sense resistor tolerance. Kelvin sensing of the voltage drop across this resistor must be used to guarantee accuracy. Accuracy at the low range of the current monitor ADC will be adversely impacted by offset errors.
Note 3: It is recommended that ADC reads occur with a frequency of not more than 250Hz.
Note 4: Voltage accuracy is only guaranteed for factory-programmed settings. Changing voltage from the value reflected in the customer specific CSIR code may result in inaccuracies exceeding those specified above.
Note 5: Not 100% Production tested. Guaranteed by Design and/or characterization.
Note 6: All electrical parameters are guaranteed to function over the stated VDD, VCS and temperature range. Electrical parameters not specified as "guaranteed by design" are tested with a VDD voltage required of the specific application. For example, if the device is to be operated at 3.3V and VCS supply of 12V, it is tested with a VDD supply of 3.3V, +-10% and a VCS supply of 12V, +-10%.

TIMING DIAGRAMS

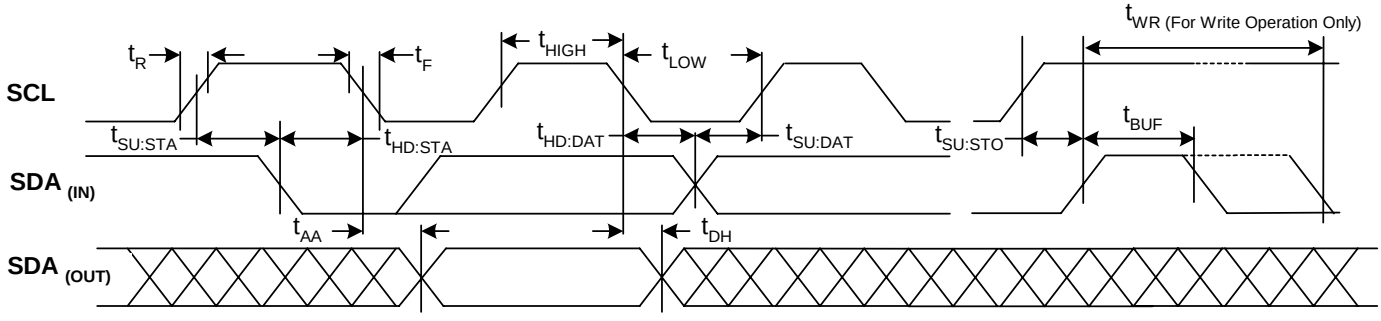


Figure 3. Basic I²C Serial Interface Timing

APPLICATIONS INFORMATION

DEVICE OPERATION

POWER SUPPLY

The SMM153 can be powered by a 2.7V to 5.5V input to the VDD pin (Figure 1). See Figure 4 as an example.

VOLTAGE REFERENCE

The SMM153 uses an internal voltage reference, VREF of 1.25V. Total accuracy of VREF is ±1.0% over temperature and supply variations.

MODES OF OPERATION

The SMM153 has three basic modes of operation: UV/OV monitoring, differential output voltage sensing and input current measuring mode. A detailed description of each mode and feature follows and can also be found in Application Note 68.

MONITOR

The SMM153 monitors the COMP1 and COMP2 pins. COMP1 and COMP2 are high impedance inputs, each connected internally to a comparator and compared against the programmable internal reference voltage. Each comparator can be independently programmed to monitor for either an under-voltage (UV) or an over-voltage (OV. The monitor level may be set externally with a resistive voltage divider. The COMPx pins can be connected to Vin, Vout or any voltage that needs to be monitored. The internal comparators COMP1/2 are compared to VREF, so the voltage dividers are set above or below the programmed VREF level depending on whether monitoring UV or OV. As an example, with VREF set to 1.25V, to monitor an OV of 1.7V on COMP1 and a UV of 1.3V on COMP2, the voltage divider resistors are:

For OV, RUpper = 1.37k, 1% RLower = 3.83k, 1%.

For UV, RUpper = 1.02k, 1% RLower = 25.5k, 1%.

The part can be programmed to trigger the FAULT# pin when either COMPx comparator has exceeded the UV or OV setting. The FAULT# output of the SMM153 is active as long as the triggering limit remains in a fault condition. When either of the COMP1 or COMP2 inputs are in fault, the open-drain FAULT# output will be pulled low.

GENERAL-PURPOSE INPUTS/OUTPUTS

The four integrated GPIOs are open drain type outputs. The pins should be pulled up externally to voltages ranging from 2.0V to 12V. Each I/O has Non-volatile memory setting associated with it that determines the power-on state of the pin. The status (High/Low) is read from bit 0 of registers 34h, 35h, 36h or 37h with 0=Low and 1=High. Additionally, the I/Os have a command bit that when written overrides the NV setting and sets the pin either high or low. The I/Os also have status bits to read the state of the pin as high or low. The command/status register for each I/O is addressed separately alleviating the need for the host controller to remember the state of the other I/Os when writing commands. More information can be found in Application Note 69.

STATUS REGISTER

A status register exists for I^2C polling of the status of the COMP1 and COMP2 inputs. Two bits in this status register reflect the current state of the inputs (1 = fault, 0 = no fault). Two additional bits show the state of the inputs latched by the FAULT# event (i.e. FAULT# output going active) programmed in the configuration. More information can be found in Application Note 69.

FAULTS

When either of the COMP1 or COMP2 inputs are in fault, the open-drain FAULT# output will be pulled low. The FAULT# is triggered only on the leading edge of a Fault. That is, a latched fault can be cleared while the Fault yet exists.

WRITE PROTECTION

Write protection for the SMM153 is located in a volatile register where the power-on state is defaulted to write protect. There are separate write protect modes for the configuration registers and memory. In order to remove write protection, the code 55_{HEX} is written to the write protection register.

Other codes will enable write protection. For example, writing 59_{HEX} will allow writes to the configuration register but not to the memory, while writing 35_{HEX} will allow writes to the memory but not to the configuration registers. The SMM153 also features a Write Protect pin (WP input) which, when asserted, prevents writing to the configuration registers and EE memory. In addition to these two forms of write protection there is a configuration register lock bit which, once programmed, does not allow the configuration registers to be changed.

A2, A1, A0

The address bits A[2:0] can be hard wired High or Low or may be left open (High-Z) to allow for a total of 21 distinct device addresses. When floating, the inputs can tolerate the amount of leakage as described by the specification I_{AIT}. An external 100k pull-up or pull down resistor is sufficient to set a High or Low logic level.

APPLICATIONS INFORMATION (CONTINUED)

CS+, CS-

Select a resistor value that will drop no more than 100mV (full scale) when full load is drawn by the converter or circuit being sensed by the resistor R_S (Figure 1). To obtain highest accuracy current-sensing, provide a Kelvin connection from the resistor to the CS+ and CS- pins. Do not allow the main current path circuit traces to inadvertently become a part of the current sense resistor. Kelvin connect directly at the resistor and follow the manufacturer's instructions for exact positioning of the traces for Kelvin sensing.

APPLICATIONS INFORMATION (CONTINUED)

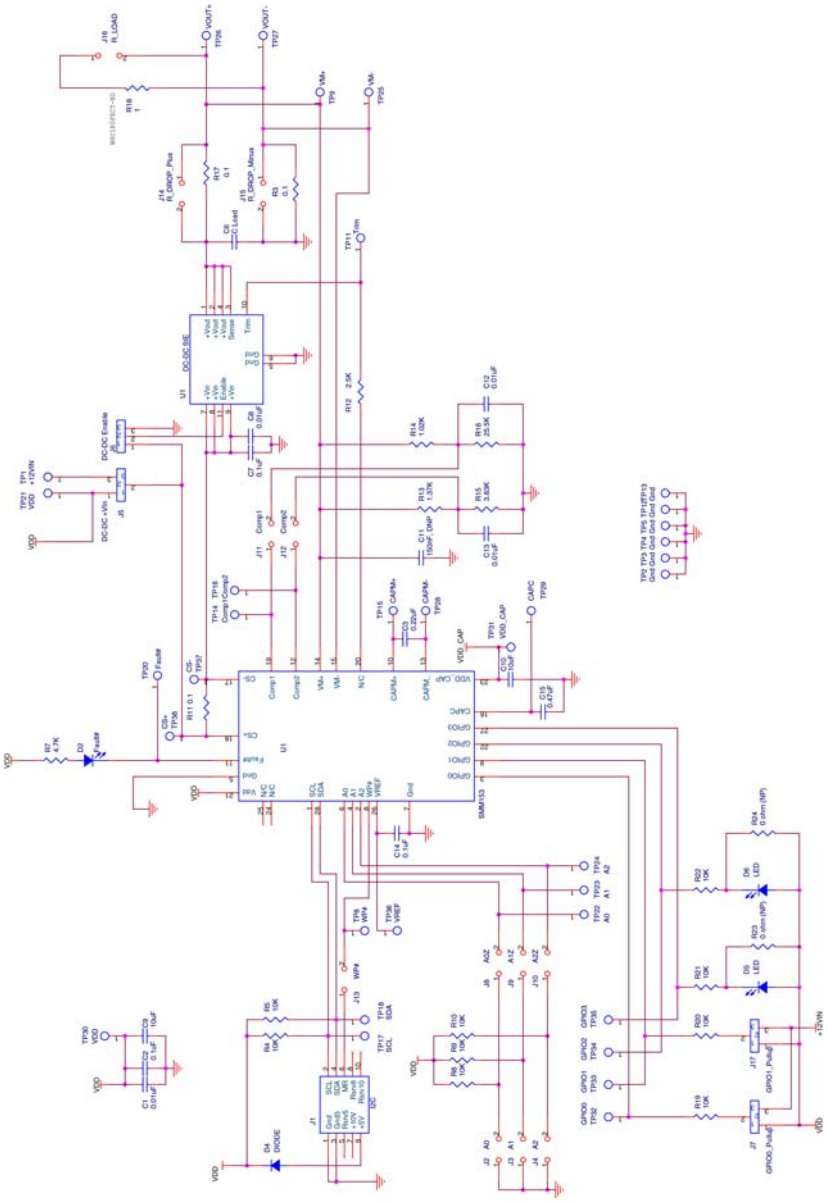


Figure 4 – Typical application schematic shows the SMM153 controlling a VIN=12V, VOUT=1.5V, DC/DC converter. This example, using the 1.25V VREF, also shows the COMP1/2 pins monitoring the DC/DC converter VOUT set to an OV of 1.7V on COMP1 and a UV of 1.3V on COMP2, the voltage divider resistors are:

For OV, R1 = 1.37k, 1% R3 = 3.83k, 1%, For UV, R2 = 1.02k, 1% R4 = 25.5k, 1%.

The Programming Supply jumper can be used to supply the SMM153 VDD voltage from the SMX3202 programmer when the device is programmed with board power off and the controlled supply unloaded.

APPLICATIONS INFORMATION (CONTINUED)

The end user can obtain the Summit SMX3202 programming system for device prototype development. The SMX3202 system consists of a programming Dongle, cable and Windows™ GUI software. It can be ordered on the website or from a local representative. The latest revisions of all software and an application brief describing the SMX3202 is available from the website (www.summitmicro.com).

The SMX3202 programming Dongle/cable interfaces directly between a PC's USB port and the target application. The device is then configured on-screen via an intuitive graphical user interface employing drop-down menus.

The Windows GUI software will generate the data and send it in I^2C serial bus format so that it can be directly downloaded to the SMM153 via the programming Dongle and cable. An example of the connection interface is shown in Figure 5.

When design prototyping is complete, the software can generate a HEX data file that should be transmitted to Summit for approval. Summit will then assign a unique customer ID to the HEX code and program production devices before the final electrical test operations. This will ensure proper device operation in the end application.

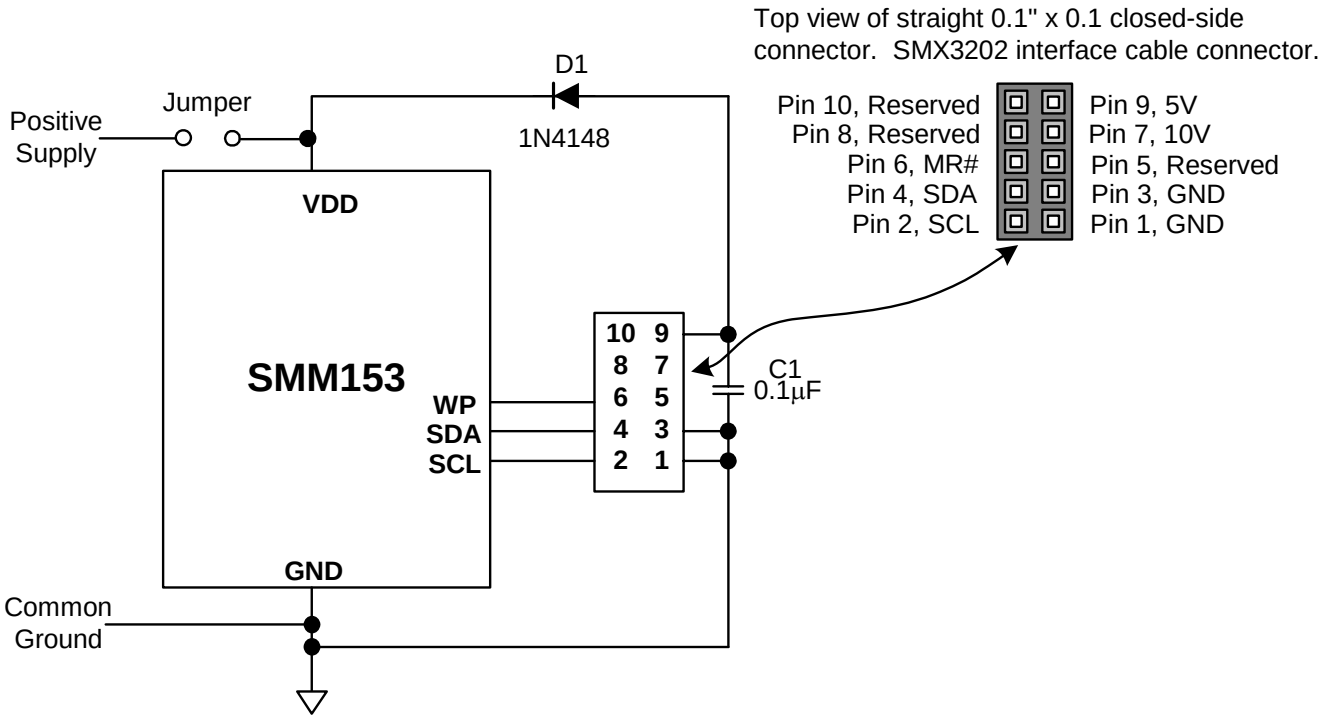


Figure 5 – SMX3202 Programmer I^2C serial bus connections to program the SMM153. The SMM153 has a Write Protect pin (WP input) which when, asserted, prevents writing to the configuration registers and EE memory. In addition, there is a configuration register lock bit, which, once programmed, does not allow the configuration registers to be changed.

I²C PROGRAMMING INFORMATION

SERIAL INTERFACE

Access to the configuration registers, general-purpose memory and command and status registers is carried out over an industry standard 2-wire serial interface (I^2C). SDA is a bi-directional data line and SCL is a clock input. Data is clocked in on the rising edge of SCL and clocked out on the falling edge of SCL. All data transfers begin with the most significant bit (MSB). During data transfers SDA must remain stable while SCL is high. Data is transferred in 8-bit packets with an intervening clock period in which an Acknowledge is provided by the device receiving data (SMM153). The SCL high period (t_{HIGH}) is used for generating Start and Stop conditions that precede and end most transactions on the serial bus. A high-to-low transition of SDA while SCL is high is considered a Start condition while a low-to-high transition of SDA while SCL is high is considered a Stop condition.

The interface protocol allows operation of multiple devices and types of devices on a single bus through unique device addressing. The address byte is comprised of a 4-bit device type identifier (slave address) and a unique (three-state) 3-bit bus address. The remaining bit indicates either a read or a write operation. Refer to Table 1 for a description of the address bytes used by the SMM153. Refer to Table 2 for an example of the unique address handling of the SMM153.

The device type identifier for the memory array, the configuration registers and the command and status registers are accessible with the same slave address. It can be set using the address pins as described in Table 2.

The bus address bits A[2:0] are hard wired only through address pins 2, 4 and 6 (A2, A1 and A0 respectively) or may be left open (Z) to allow for a total of 21 distinct device addresses. The bus address accessed in the address byte of the serial data stream must match the setting on the SMM153 address pins.

WRITE

Writing to the memory or configuration registers is illustrated in Figures 6, 7, 8, 10, 11 and 13. A Start condition followed by the address byte is provided by the host I^2C controller; the SMM153 responds with an Acknowledge; the host then responds by sending the memory address pointer or configuration register address pointer; the SMM153 responds with an acknowledge; the host then clocks in one byte of data. For memory and configuration register writes, up to 15 additional bytes of data can be clocked in by the host to write to consecutive addresses within the same page. After the last byte is clocked in and the host receives an Acknowledge, a Stop condition must be issued to initiate the nonvolatile write operation.

READ

The address pointer for the configuration registers, memory, command and status registers and ADC registers must be set before data can be read from the SMM153. This is accomplished by issuing a dummy write command, which is simply a write command that is not followed by a Stop condition. The dummy write command sets the address from which data is read. After the dummy write command is issued, a Start command followed by the address byte is sent from the host. The host then waits for an Acknowledge and then begins clocking data out of the slave device (SMM153). The first byte read is data from the address pointer set during the dummy write command. Additional bytes can be clocked out of consecutive addresses with the host providing an Acknowledge after each byte. After the data is read from the desired registers, the read operation is terminated by the host holding SDA high during the Acknowledge clock cycle and then issuing a Stop condition. Refer to Figures 9, 12 and 14 for an illustration of the read sequence.

WRITE PROTECTION

The SMM153 powers up into a write protected mode. Writing a code to the volatile write protection register (write only) can disable the write protection. The write protection register is located at address 38_{HEX}. Writing to the write protection register is shown in Figure 6.

Writing 0101_{BIN} to bits [7:4] of the write protection register allows writes to the general-purpose memory while writing 0101_{BIN} to bits [3:0] allow writes to the configuration registers. Write protection is re-enabled by writing other codes (not 0101_{BIN}) to the write protection register.

I²C PROGRAMMING INFORMATION (CONTINUED)

CONFIGURATION REGISTERS

The majority of the configuration registers are grouped with the general-purpose memory. Writing and reading the configuration registers is shown in Figures 7, 8 and 9.

Note: Configuration writes or reads of registers 00 to 03_{HEX} must not be performed while the SMM153 is margining.

GENERAL-PURPOSE MEMORY

The 256-byte general-purpose memory is located at any slave address. The bus address bits are hard wired by the address pins A2, A1 and A0. They can be tied low, high or left floating, (Hi-Z). Memory writes and reads are shown in Figures 10, 11 and 12.

COMMAND AND STATUS REGISTERS

Writes and reads of the command and status registers are shown in Figures 13 and 14.

GRAPHICAL USER INTERFACE (GUI)

Device configuration utilizing the Windows based SMM153 graphical user interface (GUI) is strongly recommended. The software is available from the Summit website (www.summitmicro.com). Using the GUI in conjunction with this datasheet simplifies the process of device prototyping and the interaction of the various functional blocks. A programming Dongle (SMX3200) is available from Summit to communicate with the SMM153. The Dongle connects directly to the parallel port of a PC and programs the device through a cable using the I²C bus protocol. See Figure 5 and the SMX3202 Data Sheet (www.summitmicro.com)..

Slave Address	Bus Address	Register Type
10XX	A2 A1 A0	Configuration Registers are located in 00_{HEX} thru 05_{HEX} and 30_{HEX} thru $3E_{HEX}$
		General-Purpose Memory is located in 40_{HEX} thru FF_{HEX}

Table 1 - Address bytes used by the SMB153.

Slave Address programmed as 10XX (Z = Hi-Z state)

Pins A[2:0]				
A2	**A1**	**A0**	**Slave Address**	**Bus Address**
0	0	0	1000	000
0	0	1	1000	001
0	0	Z	1000	010
0	1	0	1000	100
0	1	1	1000	101
0	1	Z	1000	110
0	Z	X	1000	011
1	0	0	1001	000
1	0	1	1001	001
1	0	Z	1001	010
1	1	0	1001	100
1	1	1	1001	101
1	1	Z	1001	110
1	Z	X	1001	011
Z	0	0	1010	000
Z	0	1	1010	001
Z	0	Z	1010	010
Z	1	0	1010	100
Z	1	1	1010	101
Z	1	Z	1010	110
Z	Z	X	1010	011

Table 2 – Example device addresses allowed by the SMM153.

I²C PROGRAMMING INFORMATION (CONTINUED)

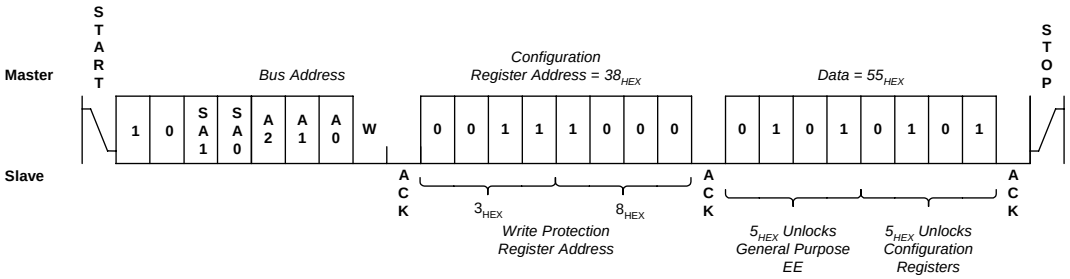


Figure 6 – Write Protection Register Write

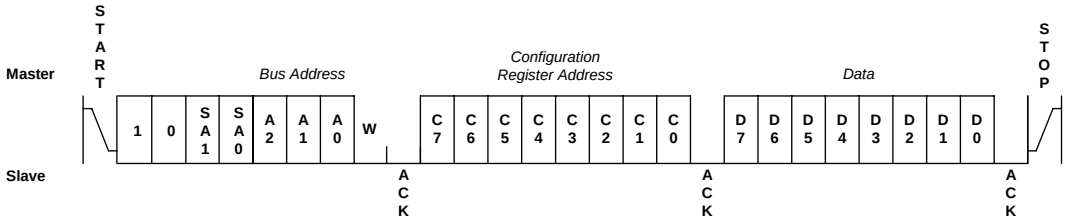


Figure 7 – Configuration Register Byte Write

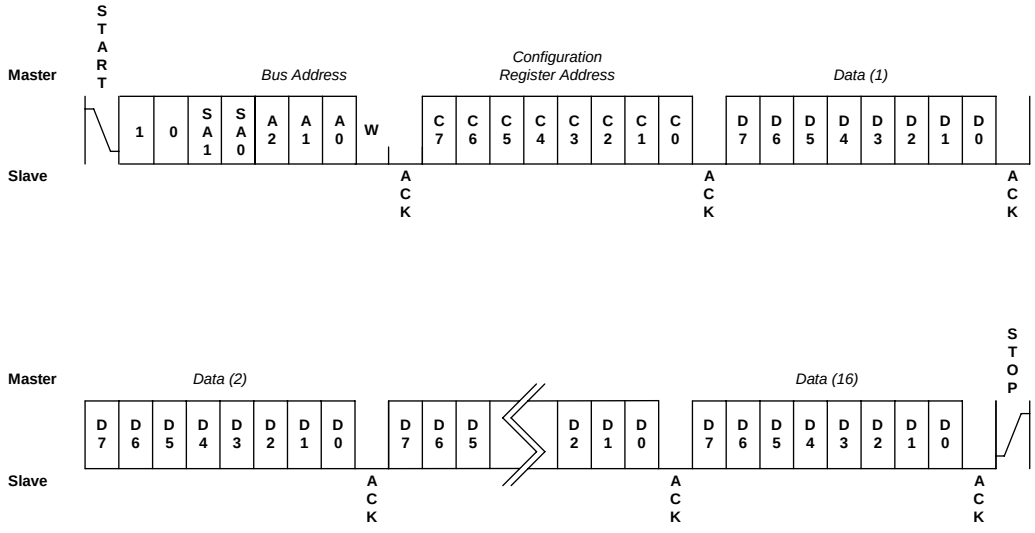


Figure 8 – Configuration Register Page Write

I²C PROGRAMMING INFORMATION (CONTINUED)

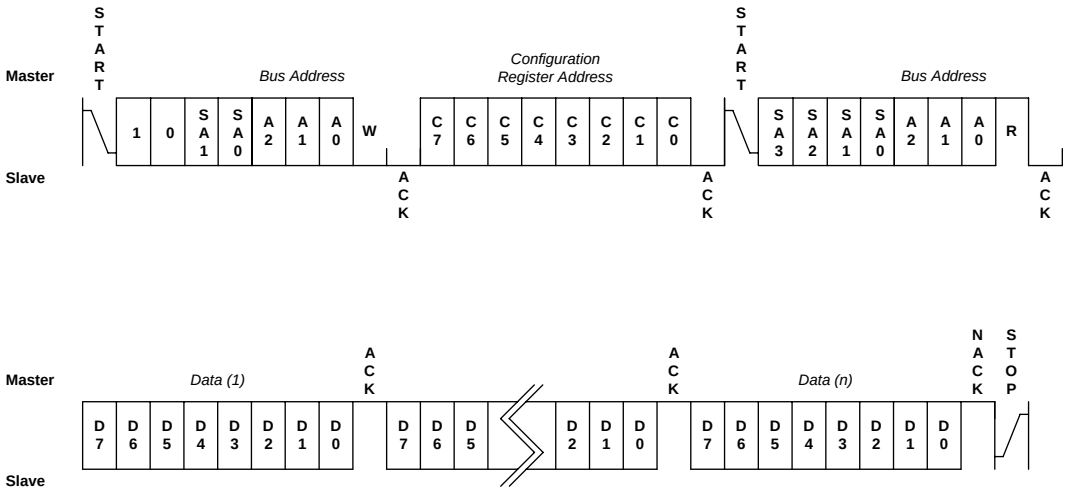


Figure 9 - Configuration Register Read

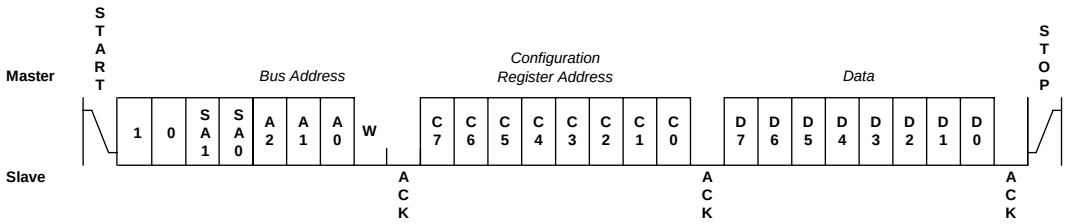


Figure 10 – General Purpose Memory Byte Write

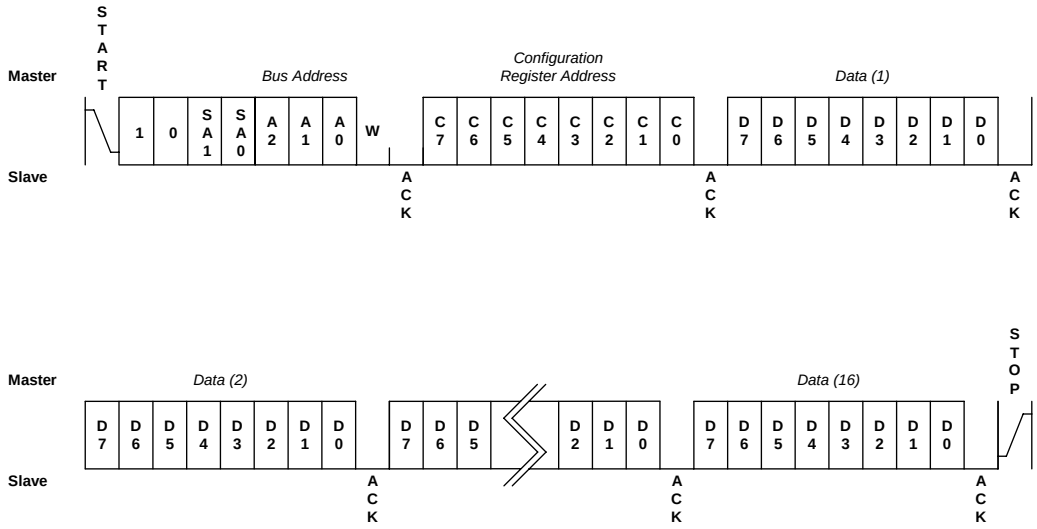


Figure 11 - General Purpose Memory Page Write

I²C PROGRAMMING INFORMATION (CONTINUED)

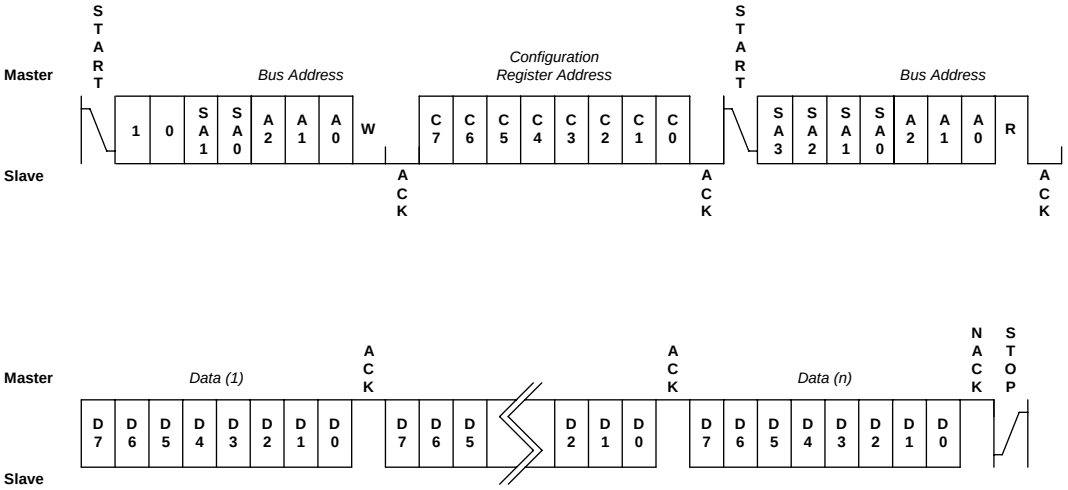


Figure 12 - General Purpose Memory Read

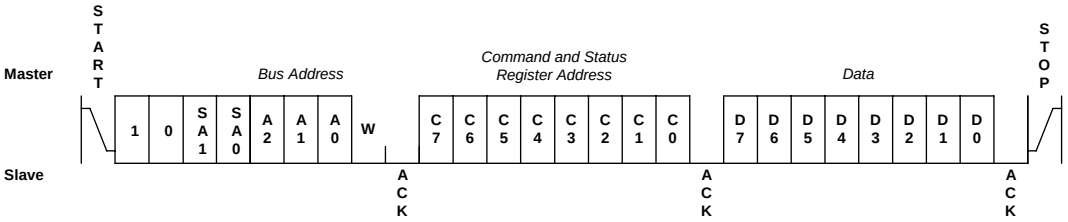


Figure 13 – Command and Status Register Write

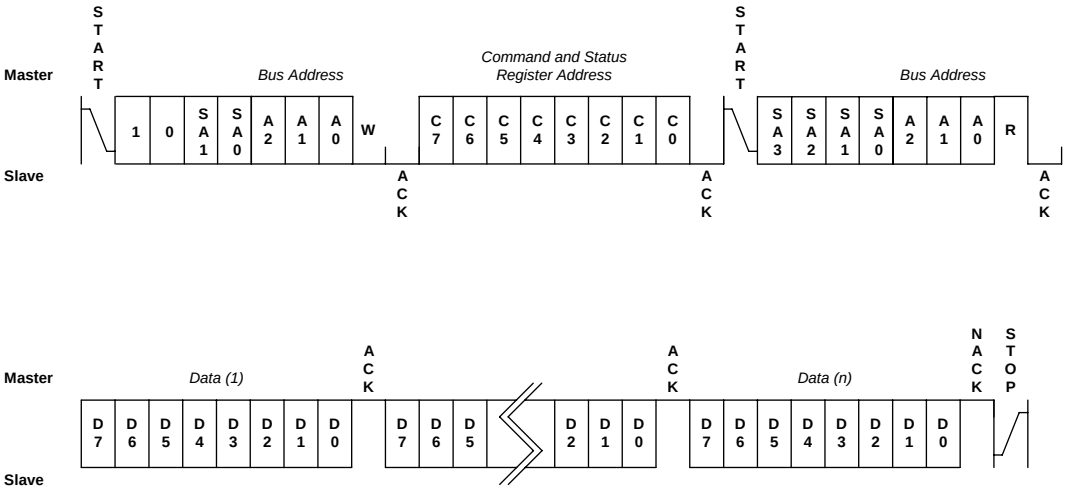
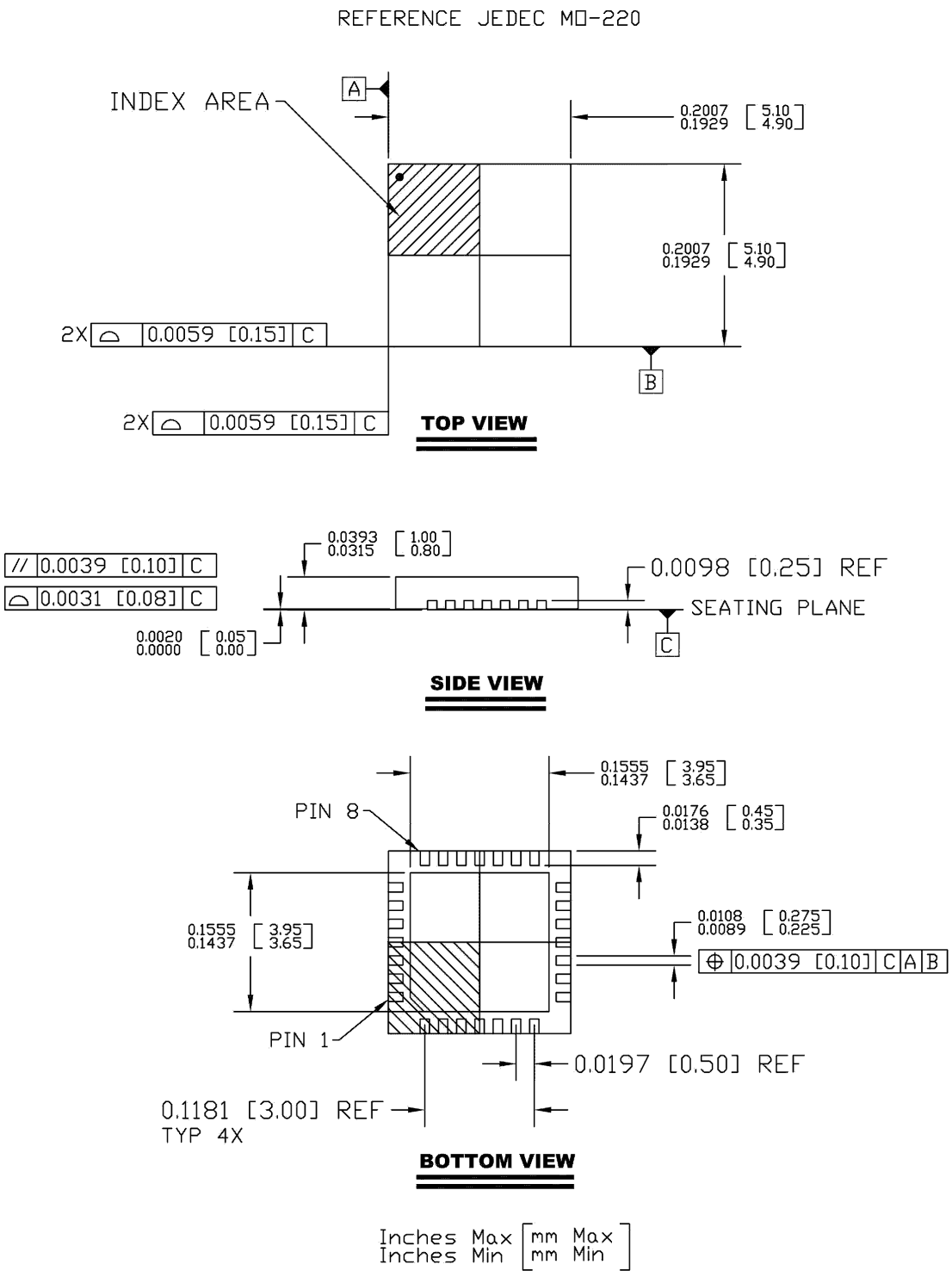


Figure 14 - Command and Status Register Read

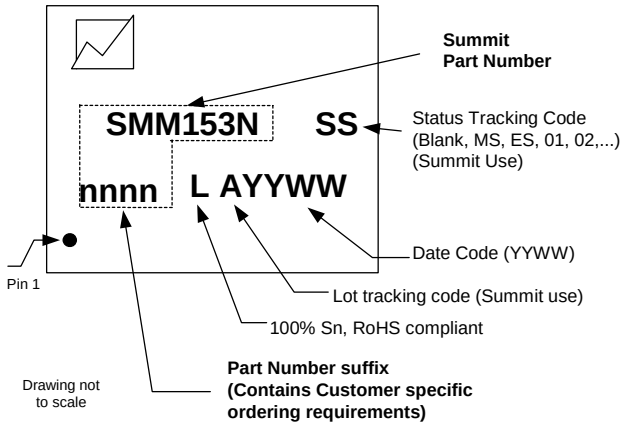
PACKAGE OUTLINES

28-Pad QFN



PART MARKING

Subject to Change



ORDERING INFORMATION

Summit Part Number — **SMM153** **N** **C** **nnnn** **L**

L is the Lead-Free Attribute for the QFN package

Package
N=28-Pad QFN

Temp Range
C=Commercial
Blank=Industrial

Part Number Suffix
Customer specific requirements are contained in the suffix such as Hex code, Hex code revision, etc. (Default: 956)

NOTICE

NOTE 1 - This is a final data sheet that describes a Summit product currently in production.

Revision 3.0 - This document supersedes all previous versions. Please check the Summit Microelectronics Inc. web site at www.summitmicro.com for data sheet updates.