SH3001 MicroBuddy™
Real-Time Clock and Clock Management Support IC for Microcontrollers

SYSTEM MANAGEMENT

Description

The programmable SH3001 MicroBuddy™ (µBuddy™) provides mandatory microcontroller support functions:

- Clock Management System
- Real-Time Support
- Auxiliary functions

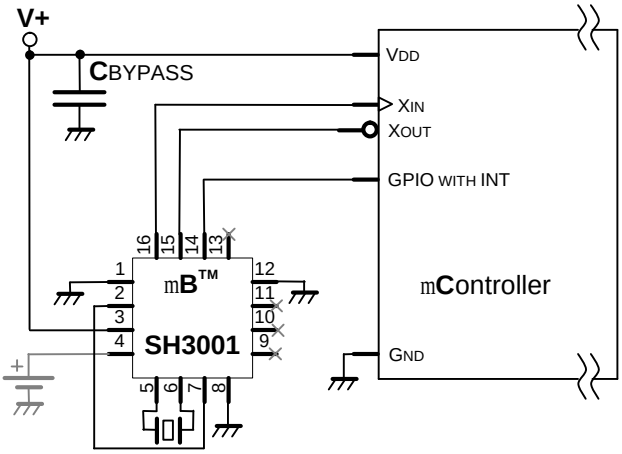
Three components make a complete system: any microcontroller, the SH3001, and a bypass capacitor. This low-cost system would consume very little power and have clock-frequency accuracy of ± 0.5%. A fourth component, a 32.768 kHz crystal, raises the clock frequency accuracy to ± 0.0256% (± 256 ppm).

The SH3001 can operate completely stand-alone, or under control of the microcontroller. A single-wire interface handles bi-directional communications. The SH3001 stores all configuration, calibration, parameters, and status information in a 36-byte bank of control registers. On reset, most of these are reloaded with defaults from the factory-set nonvolatile memory. The microcontroller can change any settings on the fly. If some of the settings must remain fixed, a comprehensive set of write-protect bits is provided for several related groups of registers (with both permanent write-inhibit and lock/unlock capabilities).

A backup power source can also be connected to the SH3001. The IC can directly accommodate 2/3-cell zinc-carbon/alkaline, 2/3-cell mercury, 2/3/4-cell NiCd/NiMH, 1-cell Li/Li+ batteries, or a super cap.

Applications

- Home automation and security
- Consumer products
- Portable/handheld computers
- Industrial equipment
- Any microcontroller-based product

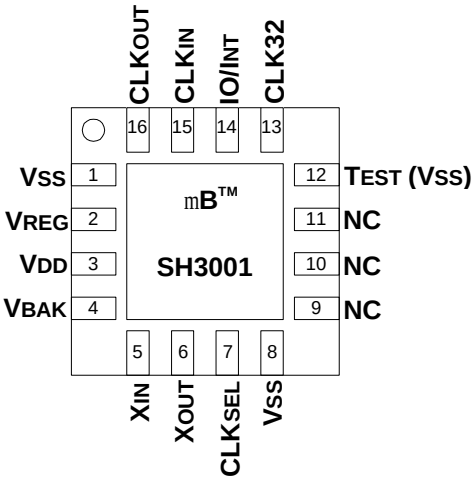


Typical Application Circuit with High Clock Accuracy

Features

- **Highly integrated IC**
  - 3 mm x 3 mm x 0.9 mm 16-lead MLP (QFN) package
- **Clock Management System**
  - Replaces high-frequency (HF) crystal or resonator
  - Programmable clock output from 32.768 kHz to 16 MHz
  - Speed shift between multiple clock frequencies
  - Adjustable spectrum spreading for EMI reduction
  - Directly supports microcontroller STOP function
  - Deep sleep with instantaneous auto-wakeup
- **Real-Time Support**
  - 179-year real-time clock, battery-backup capable
  - Dedicated 32.768 kHz buffered clock output
  - Built-in trim for 32.768 kHz oscillator to ± 4 ppm
  - Programmable periodic interrupt / wakeup timer
- **Operates from 2.3 V to 5.5 V**
- **I_{DD} <850 µA / 2 MHz, <3 mA / 16 MHz, <10 µA / standby**
- **I_{BUP} <2 µA / I_{BSB} <50 nA (battery backup / standby)**

Pin Configuration



3mm MLP (QFN) Package

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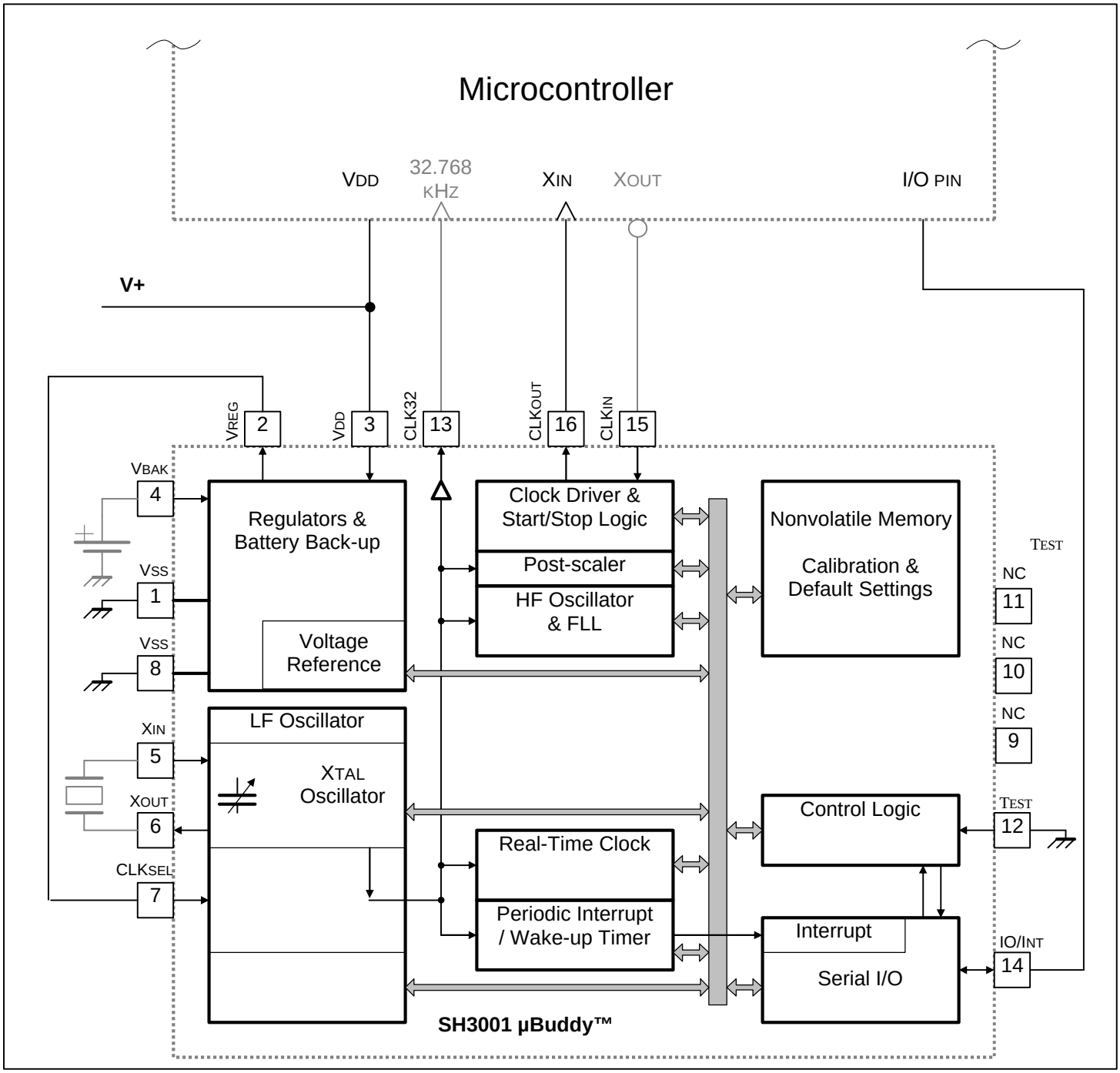
Description

Ordering Information

SH3001IMLTR	IC	MLP 3 x 3 mm, 16 pins, -40° C to +85° C
SH3001IMLTRT	IC	MLP 3 x 3 mm, 16 pins, -40° C to +85° C, Lead Free
EVK-SH3000USB	SH3000 evaluation kit	
SH3000EK.pdf	*SH3000 Evaluation Kit User Guide*	
SH3000UM.pdf	*SH3000 Reference Manual*	

Block Diagram



Pin Descriptions

Pin	Name	Type	Function
1	VSS	Power	Ground, 0 V. All VSS pins and TEST (VSS) pin must be connected together.
2	VREG	Power	Output of internal Voltage Regulator, 2.2 V nominal. This pin can power external loads of <5 mA. If load is "noisy" it requires a bypass capacitor. May be left unconnected or used as a high logic level signal for CLKSEL pin (see below).
3	VDD	Power	Main power supply, +2.3 to +5.5 V.
4	VBAK	Power	Backup power supply for real-time clock, +2.3 to +5.5 V (+1.8 to +5.5 V typical). This voltage can be higher or lower than VDD. Connect a backup battery or backup capacitor (with external recharge circuit). Connect to VDD if not used.
5	XIN	Analog In	Oscillator pins for optional external low frequency crystal, typically 32.768 kHz crystal with nominal 12.5 pF load capacitance. Keep open or connect to VSS if not used.
6	XOUT	Analog Out	
7	CLKSEL	Digital In	Must be tied to VREG
8	VSS	Power	Ground, 0 V. All VSS pins and TEST (VSS) pin must be connected together.
9	NC		Not connected - reserved
10	NC		Not connected - reserved
11	NC		Not connected - reserved
12	TEST (VSS)	Digital In	Factory test enable. All VSS pins and TEST (VSS) pin must be connected together.
13	CLK32	Digital Out	Buffered internal 32.768 kHz clock, derived according to the CLKSEL pin setting. This pin uses backup power for the buffer when VDD is not present. When driving high, this signal is either at VBAK or VDD (if VDD is higher than the reset threshold). When enabled, this signal runs continuously independent of CLKOUT activity. Minimize the external load to reduce power consumption during backup operations. When disabled, this pin is driven to VSS. Keep open if not used.
14	IO/INT	I/O	Serial communications interface and interrupt output pin. This pin is internally weakly pulled to the opposite of the programmed interrupt polarity. For example, if interrupt is programmed to be active low, this pin is weakly pulled to VDD when inactive. Keep open if not used.
15	CLKIN	Digital In	Clock activity sense input. Used to detect when the target microcontroller enters stop mode (which disables its clock). Connect to the microcontroller's clock output or oscillator output pin. Connect to VSS when not used. CLKIN must not be left open.
16	CLKOUT	Digital Out	Programmable high frequency clock output. Connect to the target microcontroller's clock input or oscillator input pin. Keep open if not used.

Functional Description

The SH3001 is a single-chip support system for microcontrollers, microprocessors, DSPs and ASICs. It consists of three major functional blocks, each block having numerous enhancements over alternative solutions.

The major modules are the Clock Management System, the Real-Time Support, and the Auxiliary functions.

The entire chip is controlled by the set of internal registers and accessed via the single-pin serial interface. All of the settings, configuration, and calibration or operating parameters are programmable and re-programmable at any time. All of the parameters required for stand-alone operations are initialized on reset from the built-in factory-programmed Nonvolatile memory. This allows the SH3001 to operate autonomously for most of its supervisory functions. The stand-alone operations do not require the use of the serial interface or any of the initialization and control operation, but without these, the full potential benefit of the SH3001 might not be realized.

In the preferred configuration, where the SH3001 is tightly coupled to the target micro, the SH3001 offers an unprecedented level of design flexibility in clock and power usage management.

The SH3001 is a particularly desirable integration because the built-in features interact and meld to produce more useful system level functions.

The SH3001 offers several ways to minimize system power consumption, such as allowing the target processor to enter deep sleep by stopping its clock completely, and to wake up as often as necessary with no external support. The clock can be programmed to start up at a given frequency, and software can adjust it dynamically to manage power consumption and different operating modes.

Users should consider the interactions of the major functional blocks to gain the maximum advantage from the SH3001.

The individual functional blocks are described in the following sections.

SEMTECH

SYSTEM MANAGEMENT

Clock Management System

The SH3001 provides a flexible tool for creating and managing clocks, a versatile and accurate “any frequency” clock synthesizer (see **Figure 1**).

It is capable of generating any frequency in the range of 62.5 kHz to 16.0 MHz, with worst-case resolution of 0.0256% (256 ppm). The internal 32.768 kHz clock can also be routed to the CLKOUT pin (and HF oscillator stopped for energy savings).

The objectives, features, and behavior of the Clock Management System are aimed towards the systems that utilize a microcontroller, a microprocessor, a DSP or an ASIC.

The SH3001 permits the automatic sensing of the intentions of the host processor, an industry first. The SH3001 shuts down its clock output when it senses that the host processor issued a STOP instruction. Subsequently, the SH3001 idles, consuming less than 10 µA. As soon as the host exits the STOP mode, the SH3001 instantaneously starts to supply a stable clock (<2µs wake-up).

A typical system, constructed with a ceramic resonator or a crystal as the frequency determining element, must wait at least several hundred microseconds (for a resonator), or as much as 100 ms or more (for a HF crystal), to re-start the oscillator. The SH3001 allows the response to and service of an event to finish with a speed previously unattainable for a simple microprocessor. A system with a traditional clock approach can be as much as 100x – 10,000x slower.

Clock Generator Operation

The frequency synthesizer in the SH3001 is constructed from the 2:1 tunable 8.0 –16.0 MHz HF oscillator followed by a programmable “power-of-two” post-divider (see **Figure 1**).

The Clock Source selector and the programmable post-scale divider allow instantaneous switching between the 32.768 kHz internal clock and divided-down HF oscillator output. There is no settling or instability when the switch occurs.

This is a preferred method for clock control in computing systems, when the large ratio between high and low frequency of operations allows for correspondingly large and instantaneous savings in power consumption.

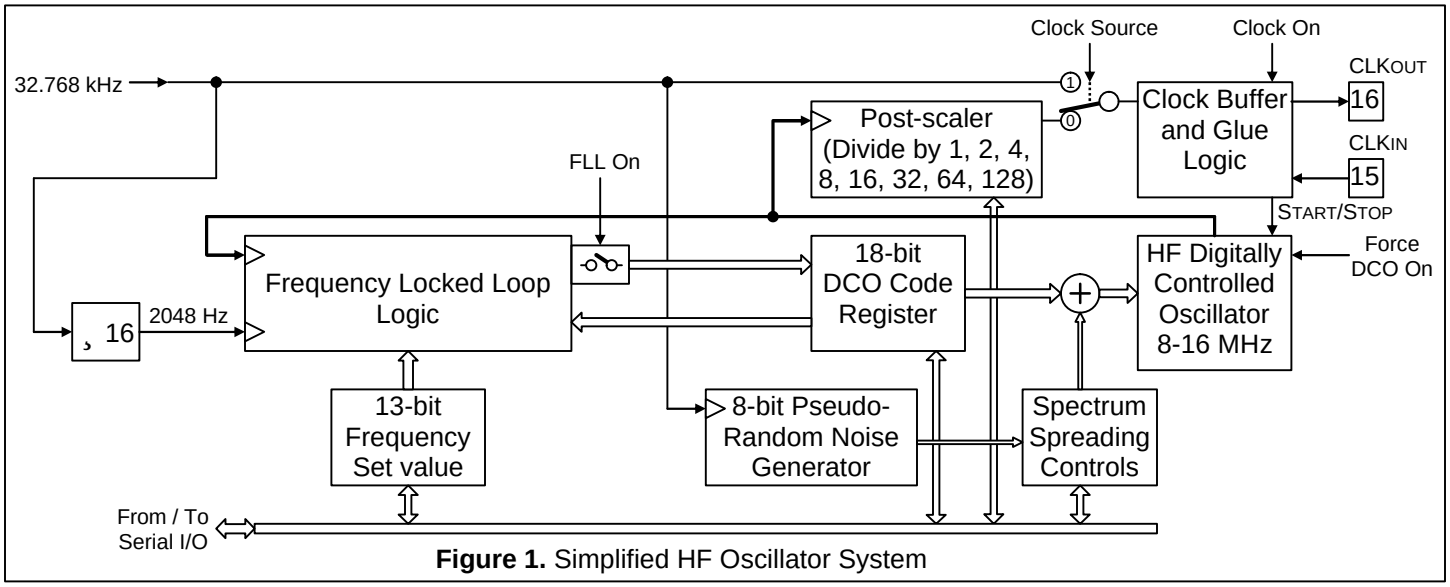


Figure 1. Simplified HF Oscillator System

SYSTEM MANAGEMENT

When the HF oscillator is operating alone, it can set the frequency of the clock on the CLKOUT pin to ± 0.025%, and maintain it to ± 0.5% over temperature. This compares favorable with the typical ± 0.5% initial clock accuracy and ± 0.6% overall temperature stability of ceramic resonators. The SH3001 replaces the typical resonator, using less space and providing better performance and functionality.

The HF oscillator can also be locked to the internal 32.768 kHz signal. The absolute accuracy and stability of the HF clock depends on the quality of the 32.768 kHz internally generated clock; the low-frequency (LF) Oscillator System is described later in this document.

When the Real-Time Clock module of the SH3001 is used for high-accuracy timekeeping, an external 32.768 kHz crystal used as a reference for RTC provides excellent accuracy and stability for the Clock Management System.

The SH3001 employs a Frequency Locked Loop (FLL) to synchronize the HF clock to the 32.768 kHz reference. This architecture has several advantages over the common PLL (Phase Locked Loop) systems, including the ability to stop and re-start without frequency transients or instability, and with instant settling to a correct frequency. The conventional PLL approach invariably includes a Low-Pass Filter that requires a long settling time on re-start.

The primary purpose of the FLL is the maintenance of the correct frequency while the ambient temperature is changing. As the temperature drift of the HF oscillator is quite small, any corrective action from the FLL system is also small and gradual, commensurate with the temperature variation.

The FLL system in the SH3001 is unconditionally stable.

To set a new frequency for the FLL, the host processor writes the 13-bit Frequency Set value. The resulting output frequency is calculated using simple formulas [1] and [2] (reference frequency is 32.768 kHz):

FOSC = 2048 Hz * (Frequency Set value + 1) [1]

FOUT = FOSC / (Post-divider setting) [2]

For example, a post-divider setting of ¸8 and the Frequency Set value of 4000 (0x0FA0) produce an output frequency of 1.024 MHz.

Programmable Spectrum Spreading

Most commercial electronic systems must pass regulatory tests in order to determine the degree of their Electromagnetic Interference (EMI) affecting other electronic devices. In some cases compliance with the EMI standards is costly and complicated.

The SH3001 offers a technique for reducing the EMI. It can be a part of the initial design strategy, or it can be applied in the prototype stage to fix problems identified during compliance testing. This feature of the SH3001 can greatly reduce the requirements for radiofrequency shielding, and permits the use of simple plastic casings in place of expensive RFI-coated or metal casings.

The SH3001 employs Programmable Spectrum Spreading in order to reduce the RF emissions from the processor's clock. There are five (5) possible settings; please see **Table 1** for operating and performance figures in the 8–16 MHz range.

Table 1. EMI reduction with Spectrum Spreading

Setting			Spreading Bandwidth	Peak EMI Reduction (guaranteed)	Peak EMI Reduction (measured)
En	CFG1	CFG0	kHz	db	db
0	X	X	Off	0	0
1	0	0	32	-3	-3
1	0	1	64	-6	-7
1	1	0	128	-9	-10
1	1	1	256	-12	-15

Spectrum Spreading is created by varying the frequency of the HF oscillator with a pseudo-random sequence (with a zero-average DC component). The Maximum-Length Sequence (MLS) 8-bit random number generator, clocked by 32.768 kHz, is used. Only 4, 5, 6, or 7 bits of the generated 8-bit random number are used, according to the configuration setting.

Maximum fluctuations of the frequency depend on the selected frequency range and the position within the range. Selecting the HF oscillator frequency to be near the high end of the range limits the peak variations to ± 0.1%, ± 0.2%, ± 0.4%, or ± 0.8% (corresponding to the configuration setting).

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Special Operating Modes

The SH3001 can operate stand-alone, without connections to the In and Out terminals of the host's oscillator. For example, a bank of SH3001 chips can generate several different frequencies for simultaneous use in the system, all controlled by a single micro (and possibly sharing one 32.768 kHz crystal by chaining the CLK32 pin to XIN pin on the next device). In this case the CLKIN pin should be connected to VSS. The clock output on the CLKOUT pin is continuous; the correct operating mode is automatically recognized by the SH3001.

Real-Time Support

The SH3001 has two support modules that are specifically designed for various real time support functions. They are the Real-Time Clock and the Periodic Interrupt / Wakeup Timer. Both of these units as well as other functions of the SH3001 depend on the internal 32.768 kHz clock for accuracy.

With one external component (a 32.768 kHz crystal), the SH3001 can provide a processor clock accuracy of ± 256 ppm (± 0.0256%) and the accuracy of the real-time system of ± 4 ppm (± 0.0004%).

A microcontroller might not have a STOP command. With the SH3001, this controller can do a "simulated" STOP by issuing an instruction to the SH3001 to stop the clock. This command is accepted only if the Periodic Interrupt / Wakeup Timer has started (otherwise, once the system is put to sleep, it would never wake up again). This mode of operations is only possible if the host processor is capable of correct operations with clock frequency down to zero, and keeps all of the internal RAM alive while the clock is stopped.

Low Frequency (LF) Oscillator System

This module provides the 32.768 kHz clock to all internal circuits and to the dedicated output pin, CLK32.

If enabled, the CLK32 output continues normal operations when VDD is absent and backup power is available.

When the power is first applied to the SH3001, the RC oscillator takes over. It supplies the 32.768 kHz clock for start-up and initialization. Once the crystal has started and stabilized, the internal 32.768 kHz clock switches to the very accurate crystal frequency; see **Figure 2**.

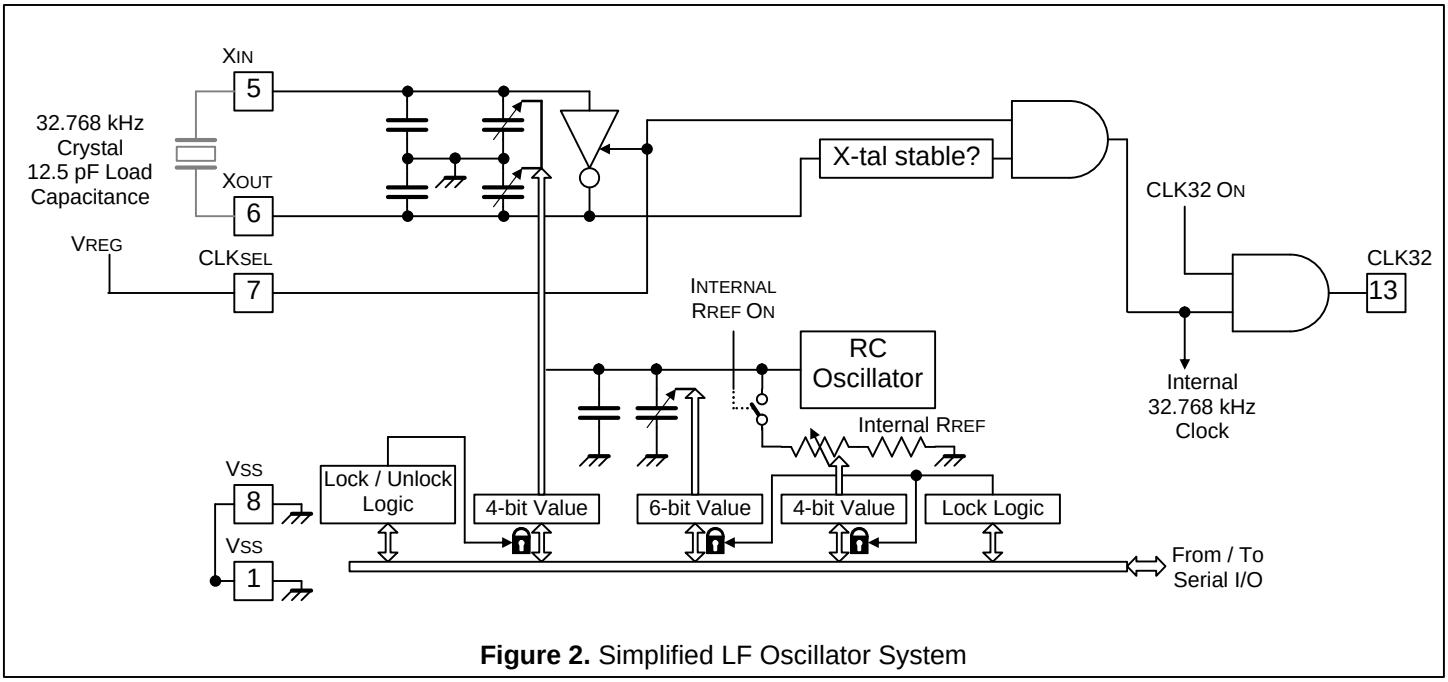

Figure 2. Simplified LF Oscillator System

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The crystal oscillator has the useful feature of adjustable load capacitors. It permits tuning of the circuit for initial tolerance of the crystal (often ± 20 ppm) as well as an adjustment for the required load capacitance (with possible variations from the PCB layout). While the oscillator was designed for a crystal with a nominal load capacitance of 12.5 pF, the circuit accommodates any value from ~7 pF to 22 pF (depending on parasitics of the layout). All of these corrections can be performed when the part is already installed on the PCB, in the actual circuit.

The default value for load capacitance (12.5 pF) loaded on power-up from the factory-programmed Nonvolatile memory can be re-programmed at any time (following a secure process of unlocking the load capacitance value register and immediately writing a new setting), or it can be completely protected from any changes by a permanent write-protect flag.

This adjustment can set the frequency of the crystal oscillator to within ± 4 ppm of the ideal value. As a reference, a typical 32.768 kHz crystal changes its frequency 4 ppm for a 10°C change in temperature. Since the temperature characteristics of crystals are well known and stable, the host processor is free to implement an algorithm for temperature compensation of the crystal oscillator using the adjustable load capacitors, with resulting accuracy of ± 4 ppm over the entire temperature range.

Real-Time Clock

Using the ± 4 ppm, 32.768 kHz clock from the LF oscillator, the Real-Time Clock module keeps time with a maximum error as low as 2 minutes per year. This compares favorably with a conventional error of 2 minutes per month for typical RTC chips.

The hardware of the Real-Time Clock is capable of 179-years of calendar operations (see **Figure 3**).

All counting-chain values are loaded at the same time into corresponding registers when the Fractions register is read. All values from registers are loaded into the counting-chain when the Fractions register is written.

The RTC continues normal operations when V_{DD} is absent, if backup power is available.

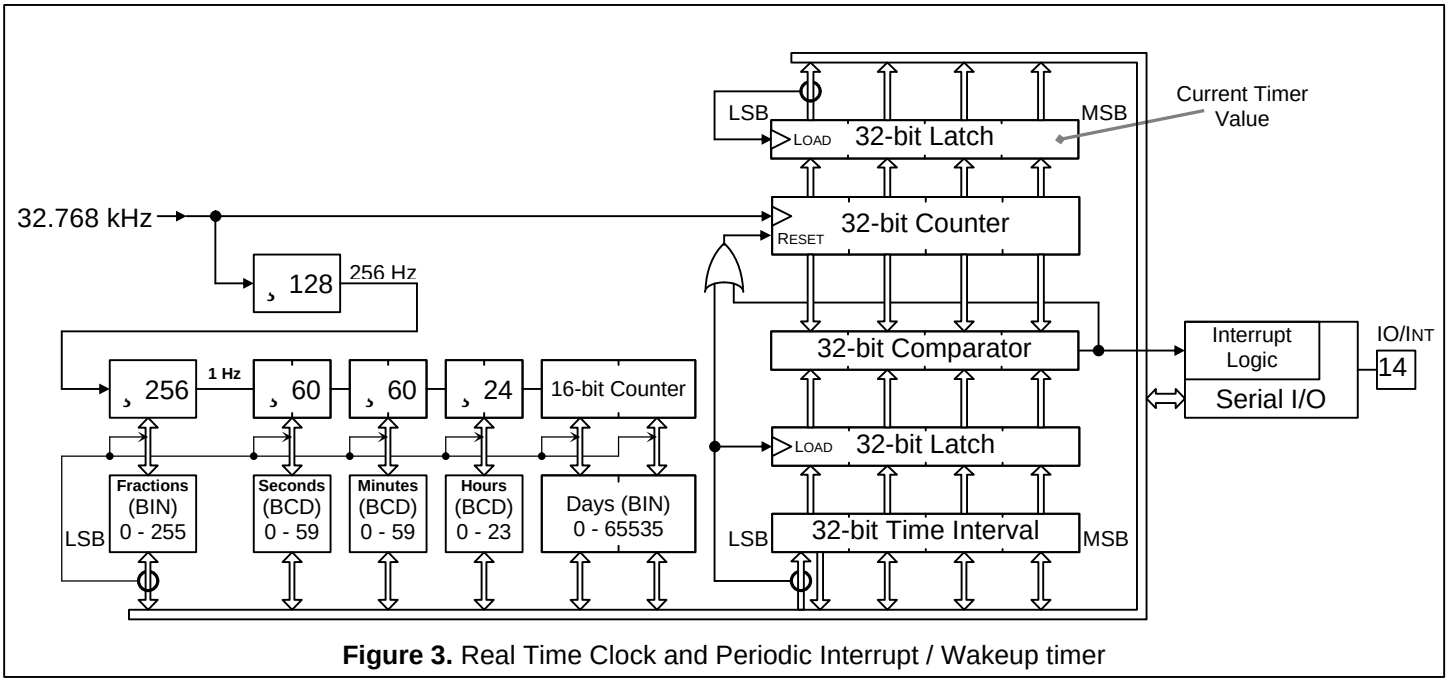

Figure 3. Real Time Clock and Periodic Interrupt / Wakeup timer

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Periodic Interrupt / Wakeup Timer

Simple and versatile, the Periodic Interrupt / Wakeup Timer can be used to create very accurate recurring interrupts for use by the host micro. With some minimal software support from the host processor, it can also be used to create alarms, with practically unlimited duration.

While the timer is running, the host processor can be halted, consuming no energy. The interrupt wakes up the processor, which can perform the requisite task and go back to sleep, until the next periodic interrupt.

This mode of operation can achieve extremely low average power consumption.

A 32-bit counter clocked by 32.768 kHz, producing a minimum interval of 30.5 µs and the maximum interval of 36.4 hours, creates the Timer.

After reset, the Timer is stopped until the new value for the time interval is written into the 4-byte Time Interval register. When the least significant byte (LSB) is written, the whole value is moved to the Time Interval latch, the counter is reset and starts to increment with the 32.768 kHz clock.

When the 32-bit comparator detects a match, an interrupt is generated and the counter is reset and starts the next timing cycle.

Although the counter cannot be written to, the current value from the counter can be read at any time. The whole 32-bit value is loaded into the 32-bit Current Timer Value latch when the least significant byte is read. This prevents errors stemming from the finite time between the readings of individual bytes of the current value.

Auxiliary functions

Voltage Regulator

Pin V_{REG} can be used as a nominal 2.20 V reference voltage or a supply source for small loads (<2 mA). A bypass capacitor might be necessary between this pin and V_{SS}, if the load generates large current transients or a low ripple reference is required.

Interrupt and Serial Interface

A single line is used to convey bi-directional information between the SH3001 and the processor, and as the interrupt line to the processor.

The polarity of the interrupt signal is programmable.

The SH3001 and the host microcontroller communicate using a single wire, bi-directional asynchronous serial interface. The bit rate is automatically determined by the SH3001. . At the fastest possible rate, a read or write access of a single byte from the register bank takes 5 µs.

The SH3001 contains 36 addressable registers located at 0x00–0x1F. Some of these registers are accessed through a page operation. Pin 14, IO/Int, is the serial communications interface and interrupt output pin. This pin is internally weakly pulled to the opposite of the programmed interrupt polarity. For example, if interrupt is programmed to be active low, this pin is weakly pulled to V_{DD} when inactive.

As shown in **Figure 4**, the SH3001 and the host communicate with serial data streams. The host always initiates communication. A data stream consists of the following (in this order):

- 3-bit start field
- 3-bit read/write code
- 5-bit address field
- 1 guard bit
- 8-bit data field
- 2 parity bits

Plus, for write streams only:

- 1 guard bit
- 2 acknowledge (ACK) bits

The 3-bit start field (1,0,1 or 0,1,0, depending on interrupt polarity) uses the middle bit to determine the bit period of the serial data stream.

The 3-bit read/write code consists of 1,1,0 for a read, or 0,1,1 for a write. This protects against early glitches that might otherwise put the interface into an invalid read or write access mode.

The 5-bit address field contains the address of the register.

A single guard bit gives the interface a safe period in which to change data direction. The value of a guard bit does not matter.

The 8-bit data field is written to (read from) the register.

Two parity bits: The first parity bit is high when there are an odd number of bits in the read/write, address and data fields; the second parity bit is the inverse of the first.

For write streams only, a guard bit is appended to the stream (to allow safe turnaround), and then two acknowledge bits, which are a direct copy of the parity bits, are driven back to the host to indicate a successful write access.

Two guard bits are appended to the end of the access stream (read or write). The host can not start the next access before receiving these bits.

The interface is self-timed based on the duration of the start bit field, and communication can take place whenever CLK_{OUT} is active, either at 32.768 kHz or at a higher frequency. If the host microcontroller is running synchronously to the CLK_{OUT} generated by the SH3001 (which should generally be the case), then a minimum of 4 CLK_{OUT} cycles per bit are required to maintain communication integrity. If the host's serial interface is asynchronous to CLK_{OUT}, then a minimum of 52 cycles per bit are necessary. A maximum of 1024 CLK_{OUT} cycles per bit field is supported.

Table 2 displays the minimum and maximum bit periods for the serial communications for CLK_{OUT} frequencies of 16 MHz, 8 MHz, and 2 MHz.

Table 2: Minimum/Maximum Serial Bit Timing

CLK_{OUT} Frequency	**Minimum Bit Period (host synchronous to CLK_{OUT})**	**Minimum Bit Period (host asynchronous to CLK_{OUT})**	**Maximum Bit Period**
16 MHz	250 ns	3.25 µs	63.9 µs
8 MHz	500 ns	6.5 µs	127 µs
2 MHz	2 µs	26 µs	511 µs

Interrupt Interface

The serial communications line to the SH3001 (Pin 14, IO/Int) also serves as the interrupt to the host microcontroller. The polarity of the interrupt is software programmable using the interrupt polarity bit (bit 6) of the IPol_RCtune register (R0x11). This pin is asserted for four cycles of CLK_{OUT}, and then returns to the inactive state.

The interrupt line is used by the Periodic Interrupt/Wake-up Timer to interrupt the host when it reaches its end of count.

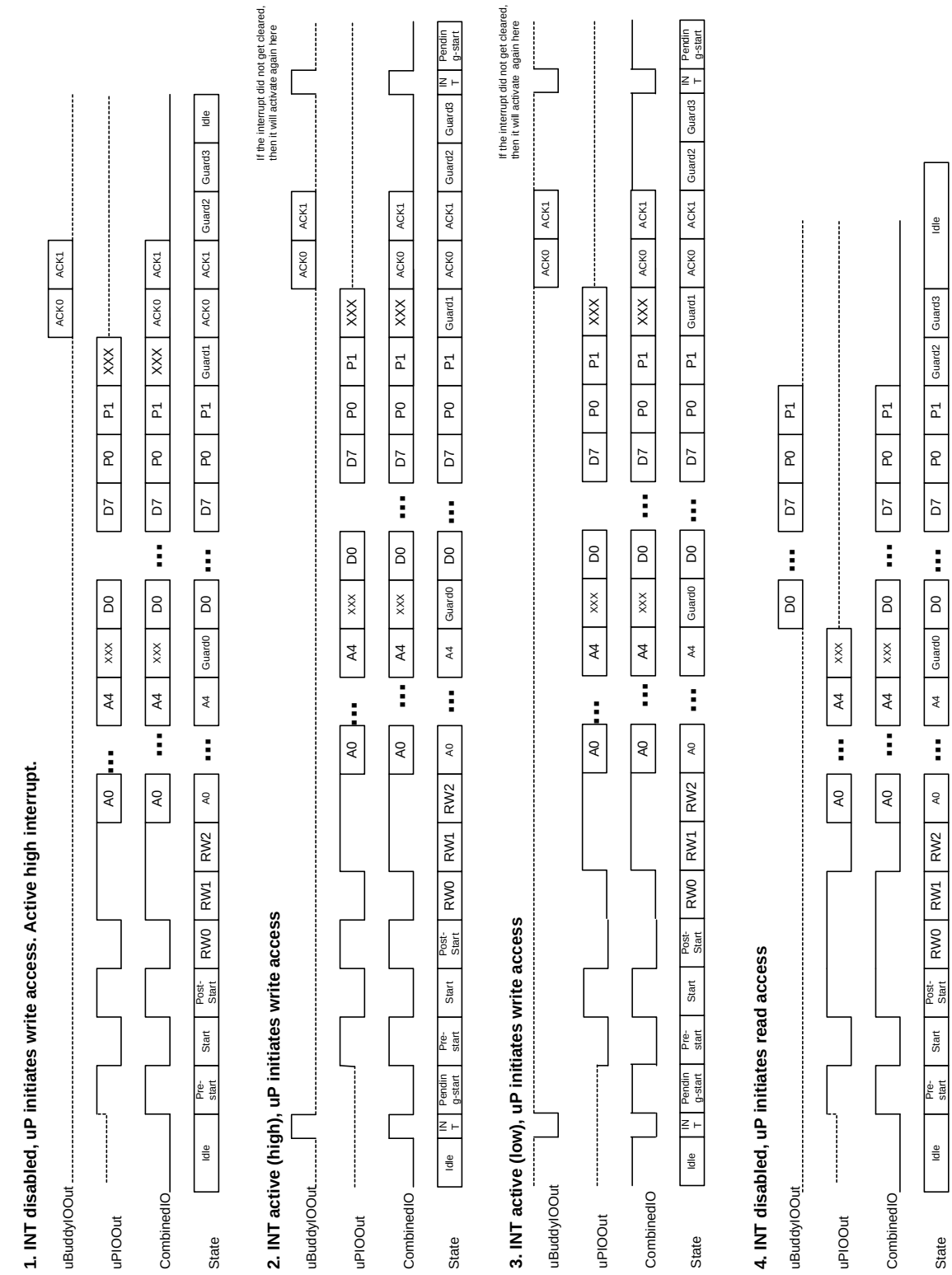


Figure 4: Serial Communication Timing Diagram

Electrical Specifications

Absolute Maximum Ratings

Note: The SH3001 is ESD-sensitive.

Description	Symbol	Min	Max	Units
Supply voltages on V_{DD} or V_{BAK} relative to ground	V_{DD}	-0.5	5.5	V
Input voltage on CLKIN, IO/INT, TEST	V_{IN1}	-0.5	V_{DD} + 0.5	V
Input voltage on CLKSEL	V_{IN2}	-0.5	V_{REG} + 0.5	V
Input current on any pin except V_{REG}	I_{IN1}		10	mA
Input current on V_{REG}	I_{IN2}		150	mA
Ambient operating temperature	T_{OP}	-40	85	ºC
Storage temperature	T_{STG}	-55	160	ºC
IR Reflow temperature, (soldering for 10 seconds, TR Option)	T_{IRRT}		240	ºC
IR Reflow temperature, (soldering for 10 seconds, TRT Option)	T_{IRRT}		260	ºC

Operating Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Notes
Case temperature	T_{OP}	–40		+85	°C	
Supply voltage	V_{DD}	2.3		5.5	V	
Supply current, CLK_{OUT} = 16 MHz*	I_{DD}			3	mA	
Supply current, CLK_{OUT} = 8 MHz*	I_{DD}		1.8		mA	
Supply current, CLK_{OUT} = 2 MHz*	I_{DD}		0.9		mA	
Standby current, 32.768 kHz crystal**	I_{SB}			8	µA	CLK32 disabled
Backup Supply Voltage**	V_{BAK}	2.3		5.5	V	
Backup current, 32.768 kHz crystal**	I_{BUP}			2	µA	CLK32 disabled
Backup standby current**	I_{BSB}			50	nA	$V_{DD} > V_{BO}$

*Note: Assuming load on CLK_{OUT} < 20 pf

**Note: Assuming temperature < 60ºC

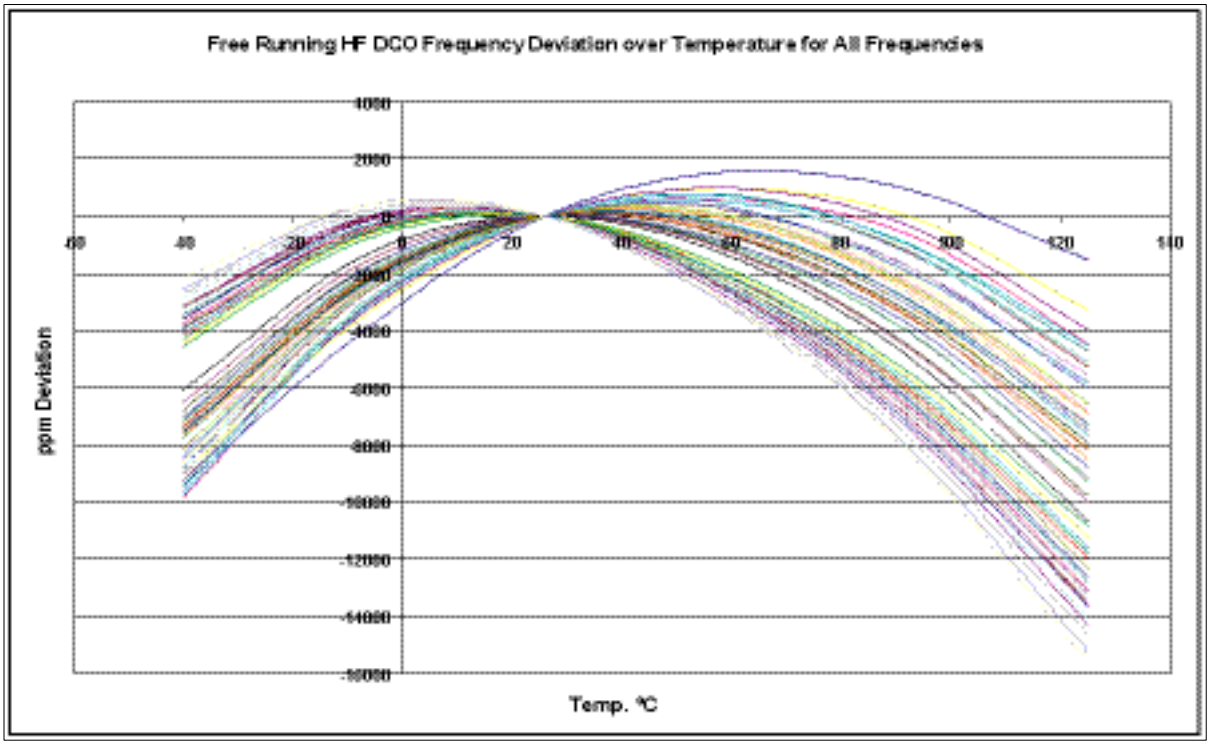
Operating characteristics with crystal oscillator

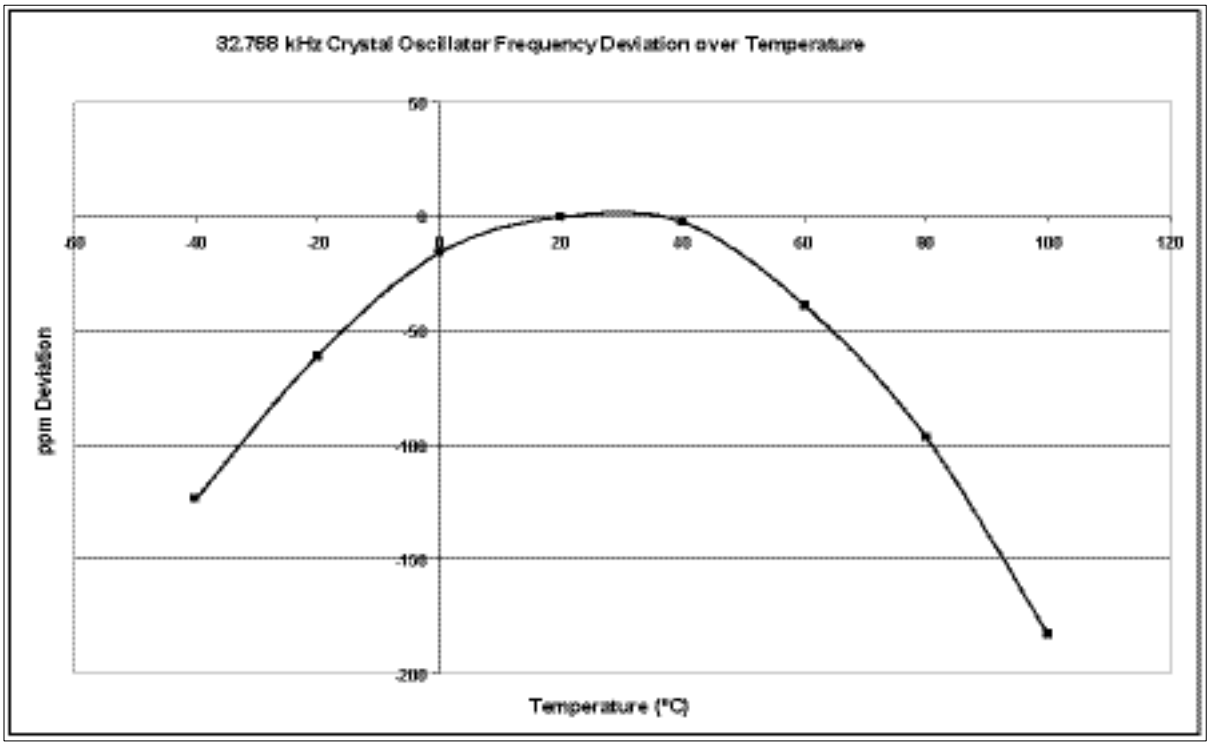
Parameter	Symbol	Min	Typ	Max	Units
Crystal operating frequency	Fop		32.768		kHz
CLK32 duty cycle	DC	25		75	%
Startup time	Tst			3	secs
Minimum XIN/XOUT padding capacitance	Cmin		10		pF
Maximum XIN/XOUT padding capacitance	Cmax		40		pF
Padding capacitance resolution	Cres		2		pF
XIN switching threshold	Vth		0.6		V
XIN to CLK32 delay	Td		0.5		µs
CLK32 frequency stability (crystal-dependent)	Fs		1		ppm/°C
CLK32 cycle to cycle jitter	J		0.05		
CLK32 rise/fall time (10 pF load)	Trf		10		ns
CLK32 logic output low (0.5 mA load)	Vol		0.25	0.5	V
CLK32 logic output high (0.5 mA load)	Voh	-0.5	-0.25		Ref VDD*

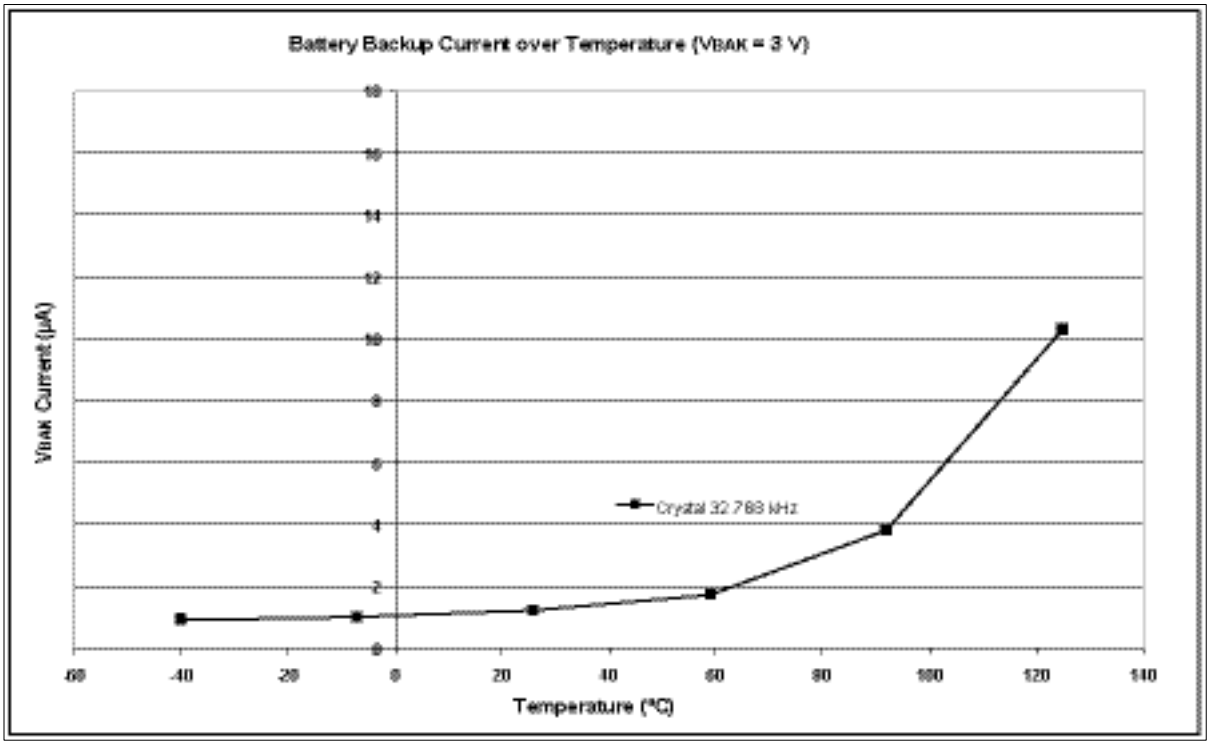
*Note: VDD here is VDD during normal operation and VBAK during battery backup.

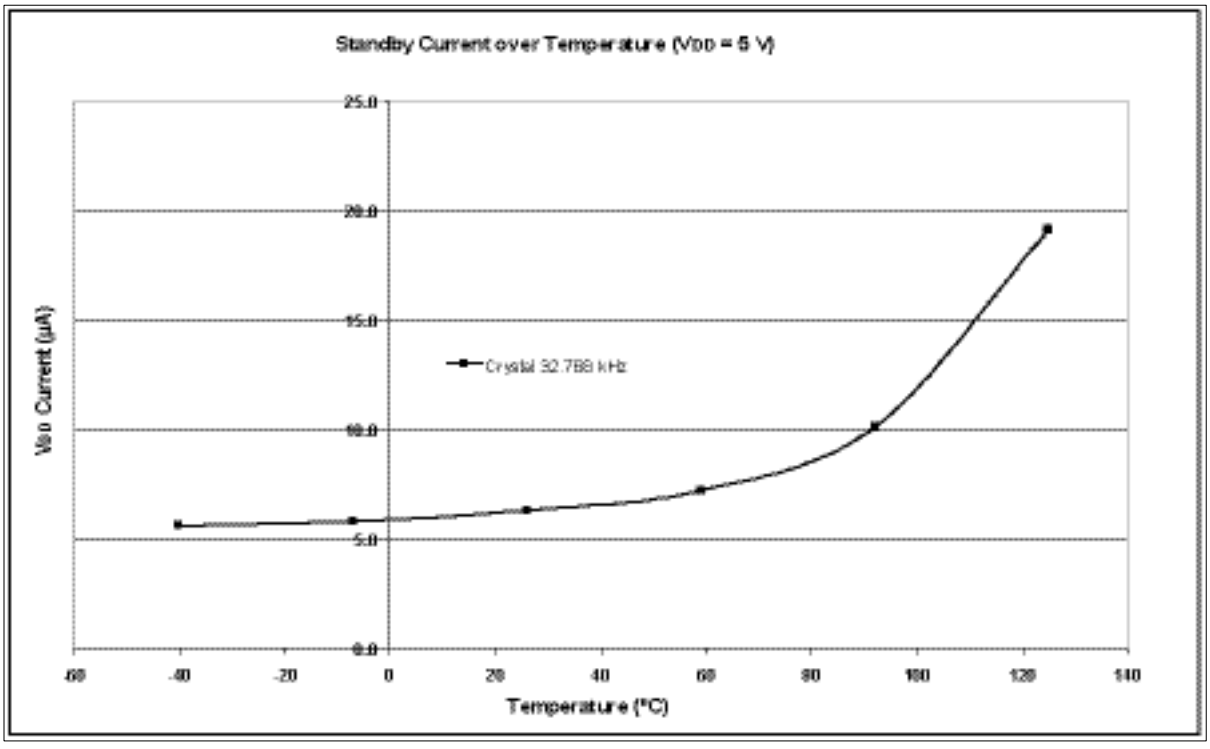
Operating characteristics of the high-frequency oscillator (HFO)

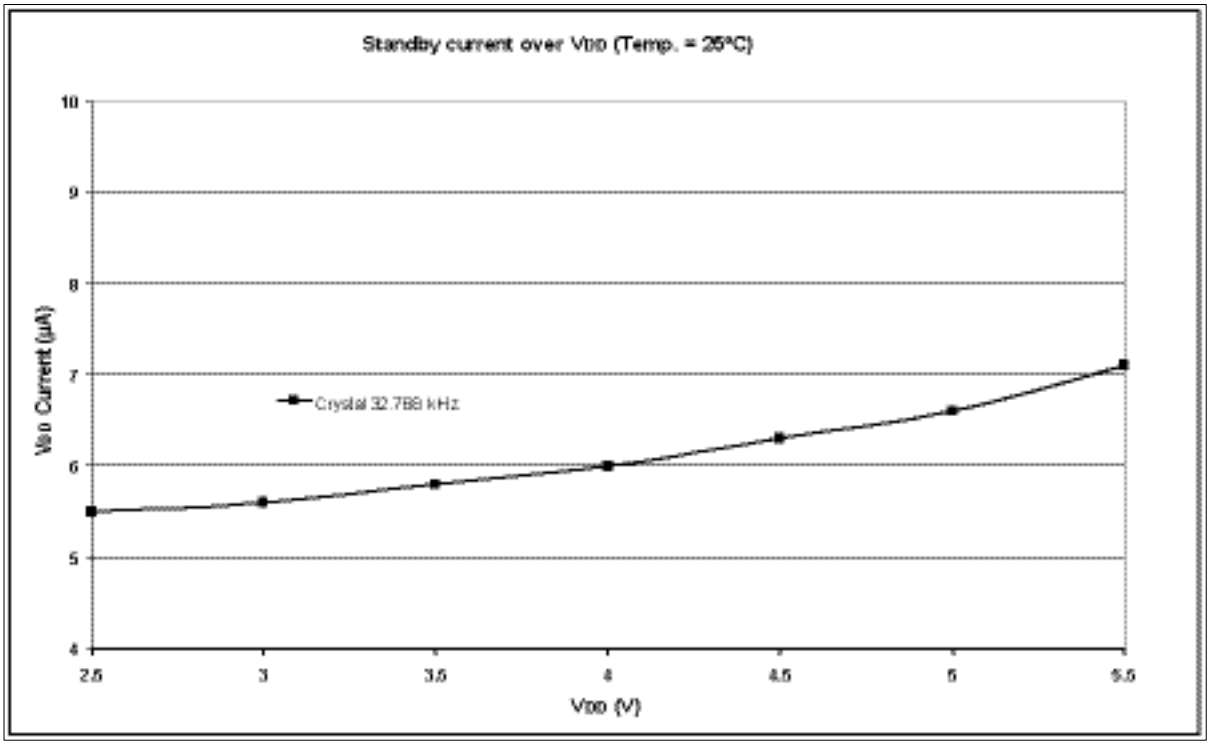
Parameter	Symbol	Min	Typ	Max	Units
Minimum operating frequency (Start-up default = 2 MHz)	Fmin		5.6	8	MHz
Maximum operating frequency	Fmax	16.8	21		MHz
Frequency resolution	Fres		2		kHz
Programmed frequency accuracy at 25°C	Fst	-0.3		+0.3	%
Frequency drift over temperature and supply	Fdrift		±0.5		%
CLKOUT cycle to cycle jitter (spread spectrum off)	J		0.1		%
Startup time from standby	Tstart			2	µs
Settling time to 0.1% after HF digitally-controlled oscillator (DCO) code change	Tsett		10		µs
CLKOUT duty cycle	DC	40		60	%
Frequency temperature stability	Fts		100		ppm/°C
Short term frequency stability	Fs		0.5		%/sec
Minimum spread spectrum range	SSmin		32		kHz
Maximum spread spectrum range	SSmax		256		kHz
CLKOUT rise/fall time (20 pF load)	Trf		3		ns
CLKOUT logic output low (4 mA load)	Vol		0.25	0.4	V
CLKOUT logic output high (4 mA load)	Voh	-0.4	-0.25		Ref VDD

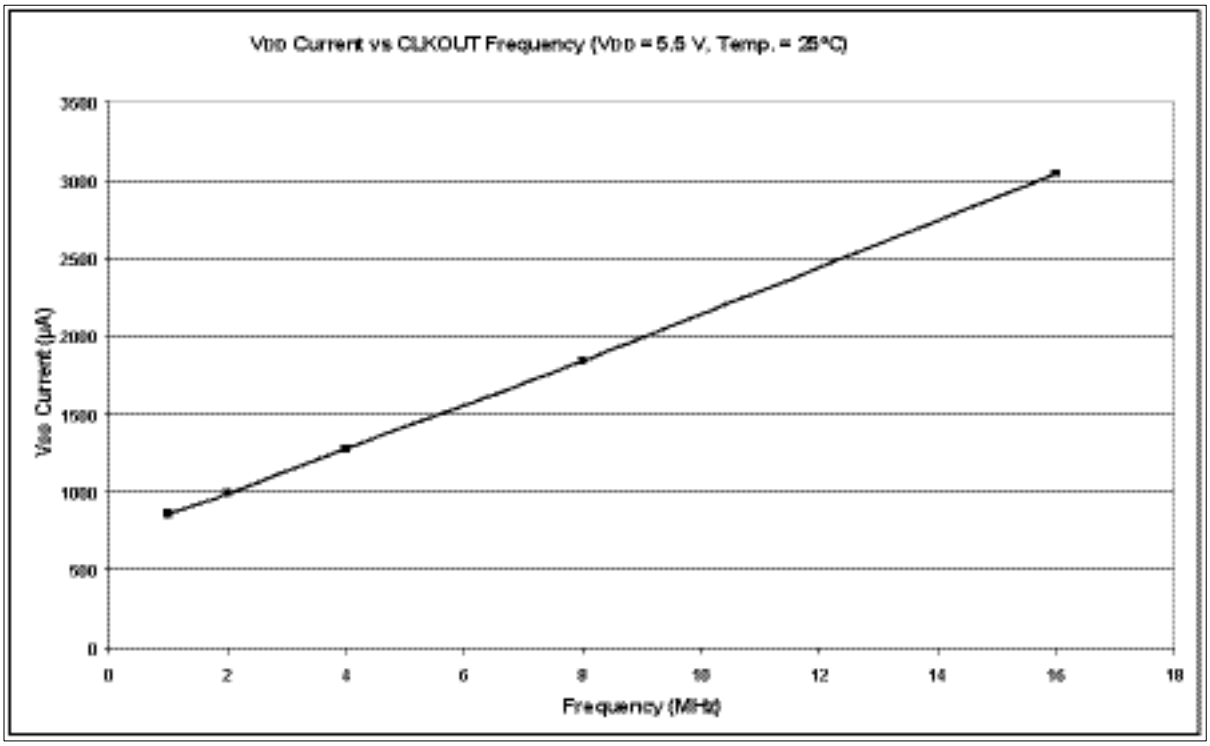


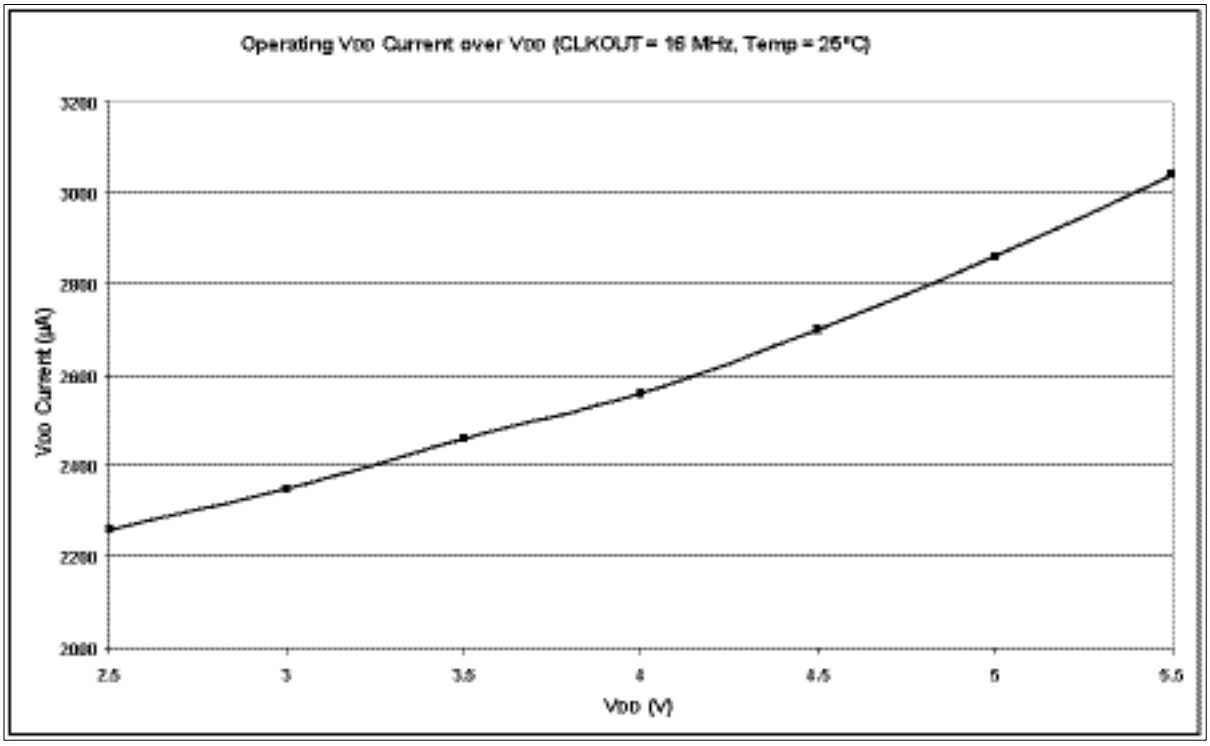


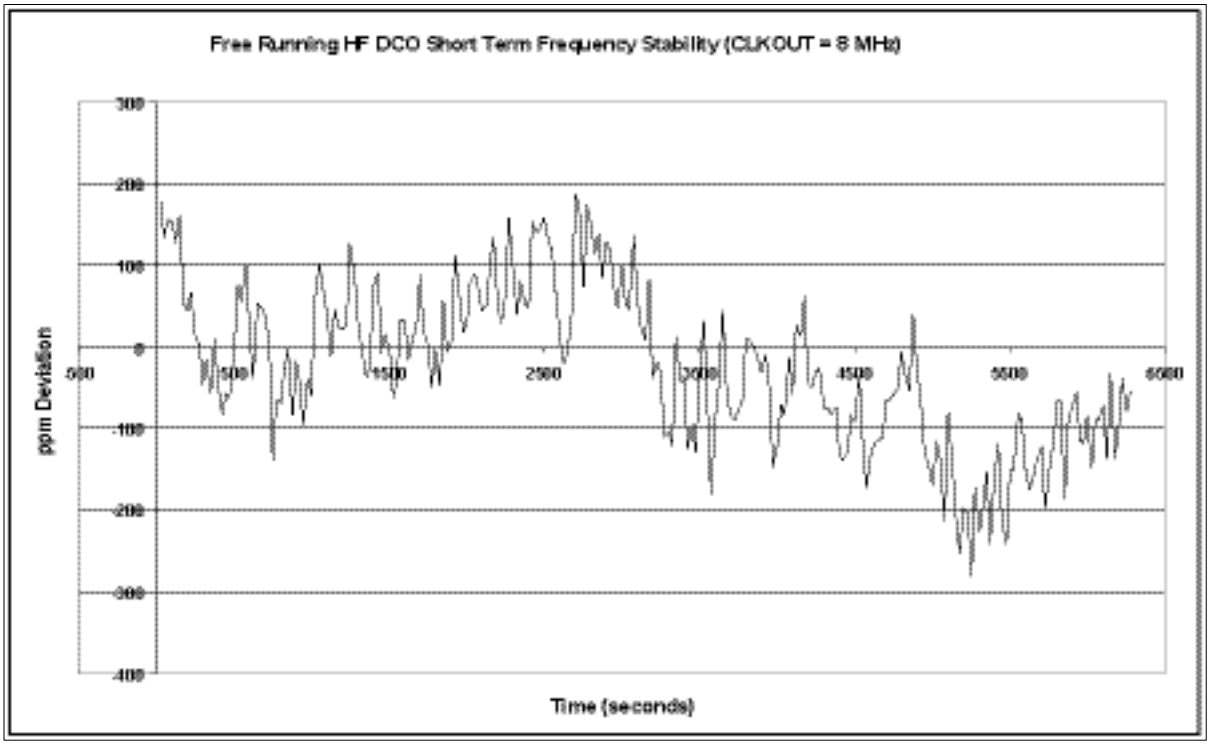


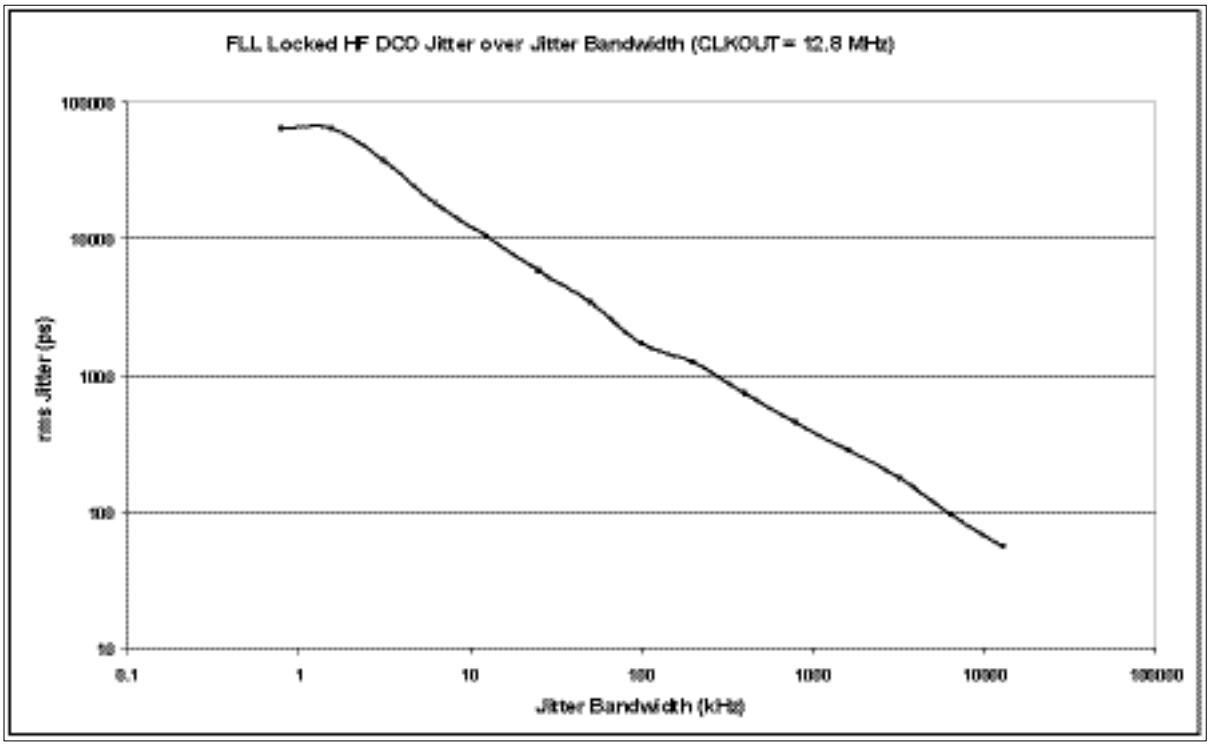




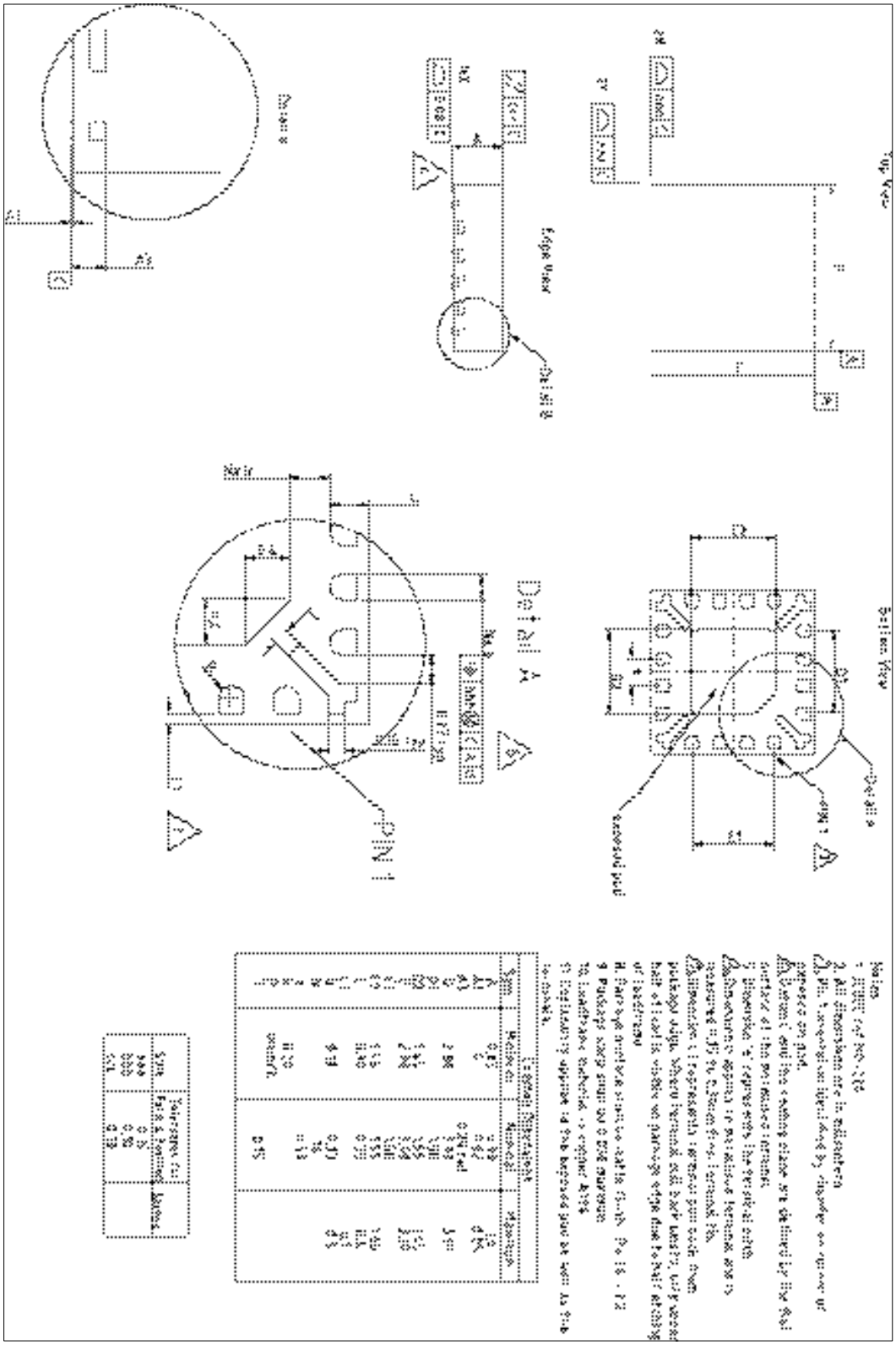








Package Outline Drawing MLP 3 x 3 mm 16 pins



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