SH3002 MicroBuddy™
Reset Management and Clock Management Support IC for Microcontrollers

SYSTEM MANAGEMENT

Description

The programmable SH3002 MicroBuddy™ (µBuddy™) provides mandatory microcontroller support functions:

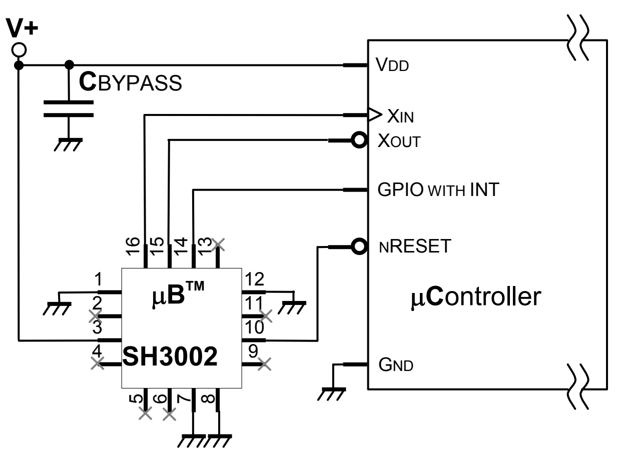
- CPU Supervisor
- Clock Management System
- Auxiliary functions

Three components make a complete system: any microcontroller, the SH3002, and a bypass capacitor. This low-cost system would consume very little power and have clock-frequency accuracy of ± 0.5%.

The SH3002 can operate completely stand-alone, or under control of the microcontroller. A single-wire interface handles both bi-directional communications and the interrupt / wake-up signal from the SH3002. The SH3002 stores all configuration, calibration, parameters, and status information in a 36-byte bank of control registers. On reset, most of these are reloaded with defaults from the factory-set nonvolatile memory. The microcontroller can change any settings on the fly. If some of the settings must remain fixed, a comprehensive set of write-protect bits is provided for several related groups of registers (with both permanent write-inhibit and lock/unlock capabilities).

Applications

- Home automation and security
- Consumer products
- Portable/handheld computers
- Industrial equipment
- Any microcontroller-based product

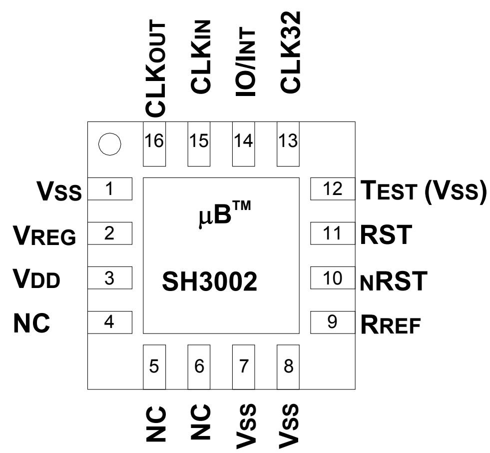


Typical Application Circuit

Features

- **Highly integrated IC**
  - 3 mm x 3 mm x 0.9 mm 16-lead MLP (QFN) package
- **CPU Supervisor**
  - Low VDD reset programmable from 2.3 V to 4.3 V
  - Both active-high and active-low reset outputs
- **Clock Management System**
  - Replaces high-frequency (HF) crystal or resonator
  - Programmable clock output from 32.768 kHz to 16 MHz
  - Speed shift between multiple clock frequencies
  - Adjustable spectrum spreading for EMI reduction
  - Directly supports microcontroller STOP function
  - Deep sleep with instantaneous auto-wakeup
- **Operates from 2.3 V to 5.5 V**
  - Ideal for battery-operated devices
- **IDD <850 µA / 2 MHz, <3 mA / 16 MHz, <10 µA / standby**

Pin Configuration



3mm MLP (QFN) Package

Covered by US Patent No. 6,903,986

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SEMTECH

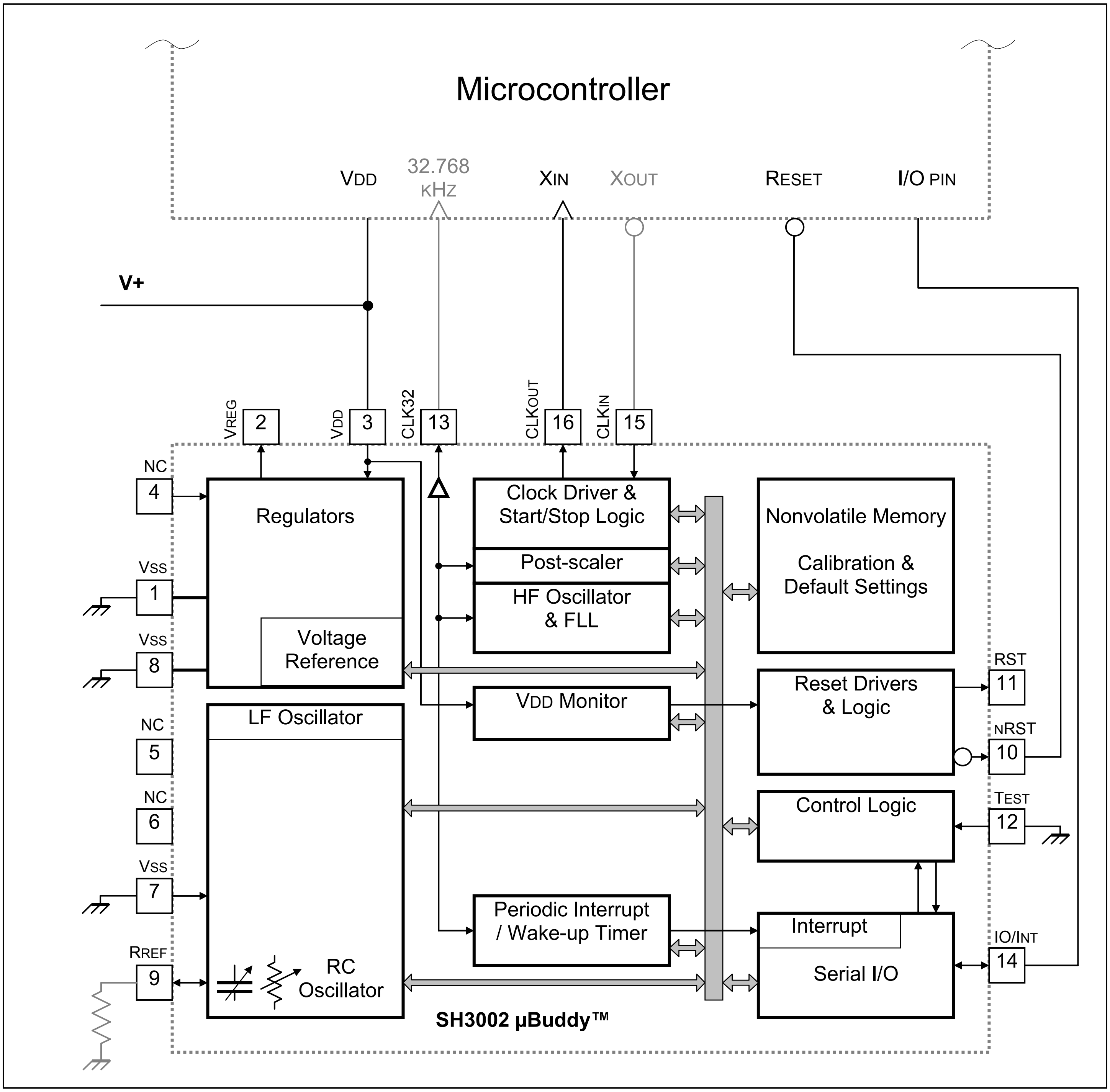
SYSTEM MANAGEMENT

Description

Ordering Information

SH3002IMLTR	IC	MLP 3 x 3 mm, 16 pins, temp. range -40° C to +85° C
EVK-SH3000USB	SH3000 evaluation kit	
SH3000EK.pdf	*SH3000 Evaluation Kit User Guide*	
SH3000UM.pdf	*SH3000 Reference Manual*	

Block Diagram



Pin Descriptions

Pin	Name	Type	Function
1	VSS	Power	Ground, 0 V. All VSS pins and TEST (VSS) pin must be connected together.
2	VREG	Power	Output of internal Voltage Regulator, 2.2 V nominal. This pin can power external loads of <5 mA. If load is "noisy" it requires a bypass capacitor. May be left unconnected or used as a high logic level signal for CLKSEL pin (see below).
3	VDD	Power	Main power supply, +2.3 to +5.5 V.
4	NC		Not connected - reserved
5	NC		Not connected - reserved
6	NC		Not connected - reserved
7	VSS	Power	Ground, 0 V. All VSS pins and TEST (VSS) pin must be connected together.
8	VSS	Power	Ground, 0 V. All VSS pins and TEST (VSS) pin must be connected together.
9	RREF	Analog	Optional 1 MOhm external bias resistor for the internal 32.768 kHz RC oscillator. Can be used to set, trim or modulate the internal RC oscillator. Keep open if not used.
10	nRST	Digital Out	Active low system reset output. Asserted with a strong low state when a reset condition occurs. Weakly pulled to VDD internally when not active. This signal is valid for VDD as low as 1 V. Keep open if not used.
11	RST	Digital Out	Active high system reset output. Asserted with a strong high state when a reset condition occurs. Weakly pulled to VSS internally when not active. This signal is valid for VDD as low as 1 V. Keep open if not used.
12	TEST (VSS)	Digital In	Factory test enable. All VSS pins and TEST (VSS) pin must be connected together.
13	CLK32	Digital Out	Buffered internal 32.768 kHz clock, derived according to the CLKSEL pin setting. This pin uses backup power for the buffer when VDD is not present. When driving high, this signal is either at VBAK or VDD (if VDD is higher than the reset threshold). When enabled, this signal runs continuously independent of CLKOUT activity. Minimize the external load to reduce power consumption during backup operations. When disabled, this pin is driven to VSS. Keep open if not used.
14	IO/INT	I/O	Serial communications interface and interrupt output pin. This pin is internally weakly pulled to the opposite of the programmed interrupt polarity. For example, if interrupt is programmed to be active low, this pin is weakly pulled to VDD when inactive. Keep open if not used.
15	CLKIN	Digital In	Clock activity sense input. Used to detect when the target microcontroller enters stop mode (which disables its clock). Connect to the microcontroller's clock output or oscillator output pin. Connect to VSS when not used. CLKIN must not be left open.
16	CLKOUT	Digital Out	Programmable high frequency clock output. Connect to the target microcontroller's clock input or oscillator input pin. Keep open if not used.

Functional Description

The SH3002 is a single-chip support system for microcontrollers, microprocessors, DSPs and ASICs. It consists of four major functional blocks, each block having numerous enhancements over alternative solutions.

The major modules are the CPU Supervisor, the Clock Management System, and the Auxiliary functions.

The entire chip is controlled by the set of internal registers and accessed via the single-pin serial interface. All of the settings, configuration, and calibration or operating parameters are programmable and re-programmable at any time. All of the parameters required for stand-alone operations are initialized on reset from the built-in factory-programmed nonvolatile memory. This allows the SH3002 to operate autonomously for most of its supervisory functions. The stand-alone operations do not require the use of the serial interface or any of the initialization and control operation, but without these, the full potential benefit of the SH3002 might not be realized.

In the preferred configuration, where the SH3002 is tightly coupled to the target micro, the SH3002 offers an unprecedented level of design flexibility in clock and power usage management.

The SH3002 is a particularly desirable integration because the built-in features interact and meld to produce more useful system level functions.

For example, on power up, the SH3002 can quickly release the reset lines on its CPU Supervisor module because the clock signal from the Clock Management System is guaranteed to be running and stabilized. An ordinary reset circuit must hold reset active for a long time to allow an unknown crystal to start up and stabilize.

The SH3002 offers several ways to minimize system power consumption, such as allowing the target processor to enter deep sleep by stopping its clock completely, and to wake up as often as necessary with no external support. The clock can be programmed to start up at a given frequency, and software can adjust it dynamically to manage power consumption and different operating modes.

Users should consider the interactions of the major functional blocks to gain the maximum advantage from the SH3002.

The individual functional blocks are described in the following sections.

CPU Supervisor

The SH3002 has two supervisory functions that manage the reset of the target processor, a low V_{DD} monitor (Brownout Detector), see **Figure 1**.

Both functions are integrated with the Clock Management System to provide a more complete system solution than stand-alone components.

The SH3002 has both active high and active low reset output pins. Both are driven strong to the active state and weak to the inactive state. This eliminates the need for external pull-ups and allows various reset sources to be connected together in a wire-OR configuration. (This makes it simple to set up a manual reset circuit.)

A set of flags in the register map indicates the source of the reset to the system software.

Low V_{DD} Reset

The SH3002 drives the reset pins active whenever V_{DD} is below the value of V_{BO}, the brownout reset threshold, programmable from 2.3 V to 4.3 V in average steps of 33 mV, see **Table 1**.

Table 1. Programmable V_{BO} Values

Parameter	Min	Typ	Max	Units
VBO for min code (000000)	2.27	2.3	2.33	V
VBO for max code (111111)	4.2	4.3	4.4	V
Step resolution		33		mV

The default V_{BO} value is loaded on power-up from the factory-programmed nonvolatile memory. It can be re-programmed at any time or it can be permanently protected from any changes by setting the V_{BO} Lock flag or a write-protect flag.

On power up both the active-high and active-low reset signals are driven active. These outputs are typically valid for a V_{DD} level of at least 0.5 V, and guaranteed to be valid for a V_{DD} level of 1.0 V.

The reset outputs remain active until V_{DD} rises and stays above the level of (V_{BO} + V_{HYST}), where V_{HYST} is a small fixed amount of hysteresis, nominally 50 mV, added to prevent nuisance reset activations (when V_{DD} slowly changes near the level of V_{BO} and some noise or power glitching is present).

At the level of (V_{BO} + V_{HYST}) the power supply is considered valid. In case of the initial power-up, the reset is then driven inactive once 6 ms of valid power have elapsed. In the case of brownout, the reset is released after a delay of 6 ms (but no less than 12 ms from the beginning of the brownout).

Such a fast reset is possible because the SH3002 provides a fast-starting clock that is free of crystal start-up time requirements. This gives the SH3002 an advantage over most external reset circuits, which must have a long reset pulse duration to accommodate long and unpredictable crystal start-up times.

The SH3002 guarantees that a valid and stable clock is available 2 ms before the reset signals are negated, so that internal synchronous reset and initialization of the target micro can proceed normally.

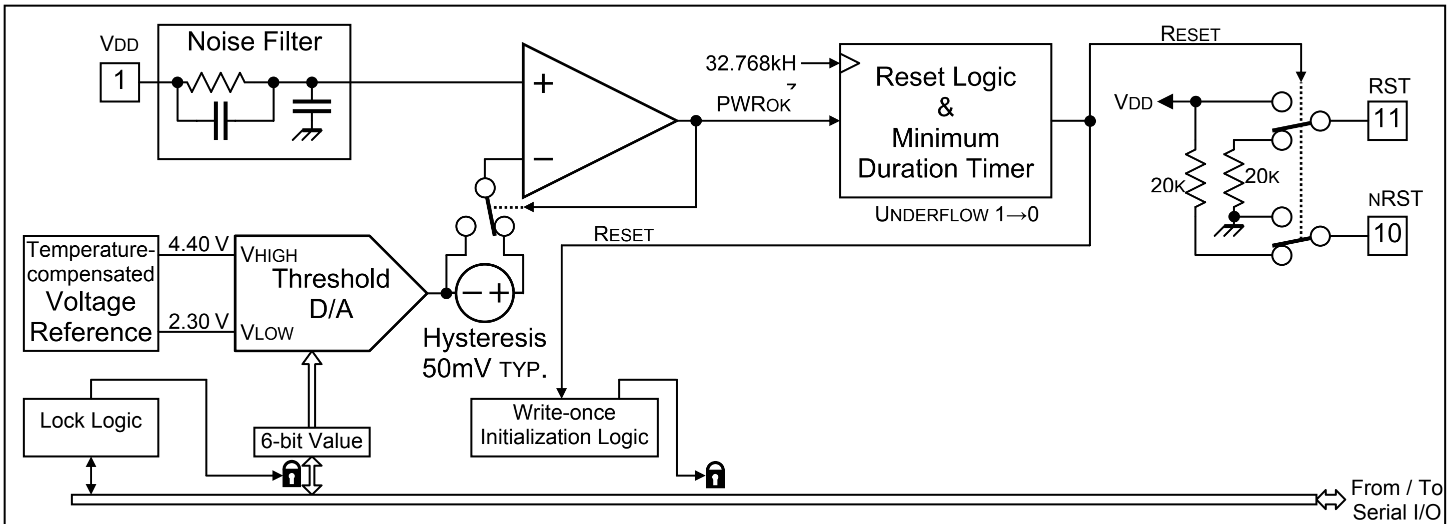


Figure 1. CPU Supervisor --- Low V_{DD} / Brownout Detector, Watchdog, Reset logic & Drivers

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Since the clock is only active for the last 1 or 2 ms of the reset interval, when VDD has already been valid for some time, energy savings are realized and the startup of the whole system is made easier. The commonly used reset approach forces the processor to turn the oscillator on and to run at full speed (thus consuming full power) during the critical time when the (possibly depleted) battery is trying to raise VDD to an acceptable level. In contrast, the SH3002 allows the power source to charge the bypass capacitors and raise the level of VDD with little additional load. Only when power has stabilized is the target micro permitted to start expending energy.

When a brownout event occurs, the SH3002 continues to provide the clock to the target processor, but at a reduced frequency between 500 kHz and 1.0 MHz. After a delay of 2 ms this clock is stopped, automatically lowering the energy consumption of the whole system, see **Figure 2.**

A Noise Filter (see **Figure 1**) prevents reset activations from noise and small power glitches on the VDD line. A typical behavior is shown in **Figure 3** for the VDD level just above VBO and various amplitudes and durations of the negative-going spikes.

When VDD is falling, both reset lines are guaranteed to activate within 5 µs from the time VBO is crossed over.

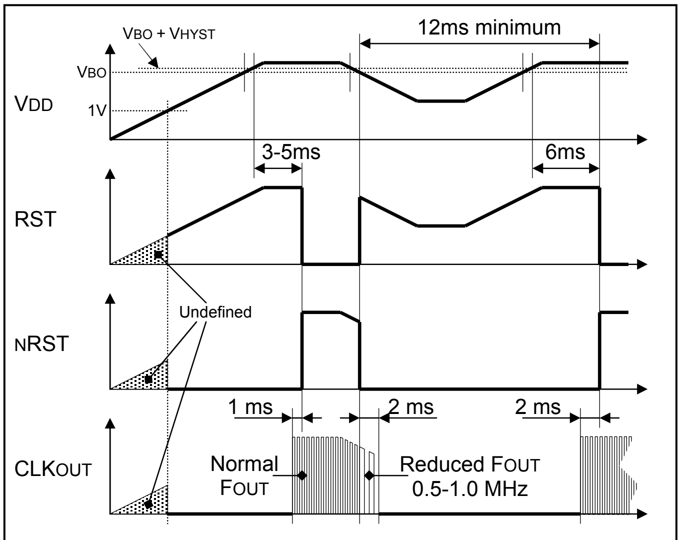


Figure 2. Operations of low VDD / Brownout Detector

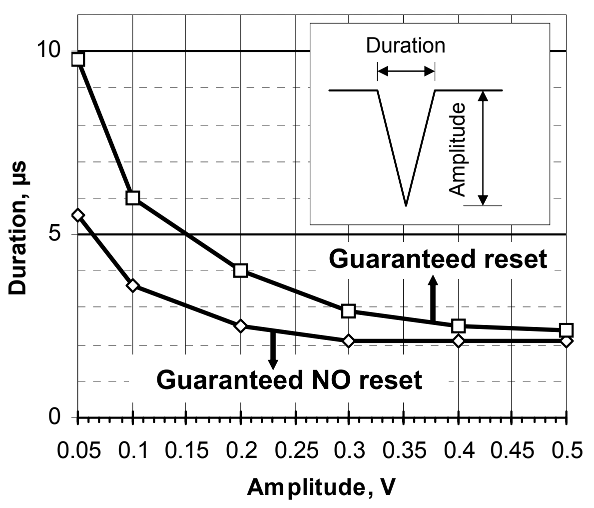


Figure 3. Response to negative voltage spikes

Clock Management System

The SH3002 provides a flexible tool for creating and managing clocks, a versatile and accurate "any frequency" clock synthesizer (see **Figure 4**).

It is capable of generating any frequency in the range of 62.5 kHz to 16.0 MHz, with worst-case resolution of 0.0256% (256 ppm). The internal 32.768 kHz clock can also be routed to the CLKOUT pin (and HF oscillator stopped for energy savings).

The objectives, features, and behavior of the Clock Management System are aimed towards the systems that utilize a microcontroller, a microprocessor, a DSP or an ASIC.

The SH3002 permits the automatic sensing of the intentions of the host processor, an industry first. The SH3002 shuts down its clock output when it senses that the host processor issued a STOP instruction. Subsequently, the SH3002 idles, consuming less than 10 µA. As soon as the host exits the STOP mode, the SH3002 instantaneously starts to supply a stable clock (<2 µs wake-up).

A typical system, constructed with a ceramic resonator or a crystal as the frequency determining element, must wait at least several hundred microseconds (for a resonator), or as much as 100 ms or more (for a HF crystal), to re-start the oscillator. The SH3002 allows the response to and service of an event to finish with a speed previously unattainable for a simple microprocessor. A system with a traditional clock approach can be as much as 100x – 10,000x slower.

Clock Generator Operation

The frequency synthesizer in the SH3002 is constructed from the 2:1 tunable 8.0–16.0 MHz HF oscillator followed by a programmable "power-of-two" post-divider (see **Figure 4**).

The Clock Source selector and the programmable post-scale divider allow instantaneous switching between the 32.768 kHz internal clock and divided-down HF oscillator output. There is no settling or instability when the switch occurs.

This is a preferred method for clock control in computing systems, when the large ratio between high and low frequency of operations allows for correspondingly large and instantaneous savings in power consumption.

When the HF oscillator is operating alone, it can set the frequency of the clock on the CLKOUT pin to ± 0.025%, and maintain it to ± 0.5% over temperature. This compares favorable with the typical ± 0.5% initial clock accuracy and ± 0.6% overall temperature stability of ceramic resonators. The SH3002 replaces the typical resonator, using less space and providing better performance and functionality.

The HF oscillator can also be locked to the internal 32.768 kHz signal. The absolute accuracy and stability of the HF clock depends on the quality of the 32.768 kHz internally generated clock; the low-frequency (LF) Oscillator System is described later in this document.

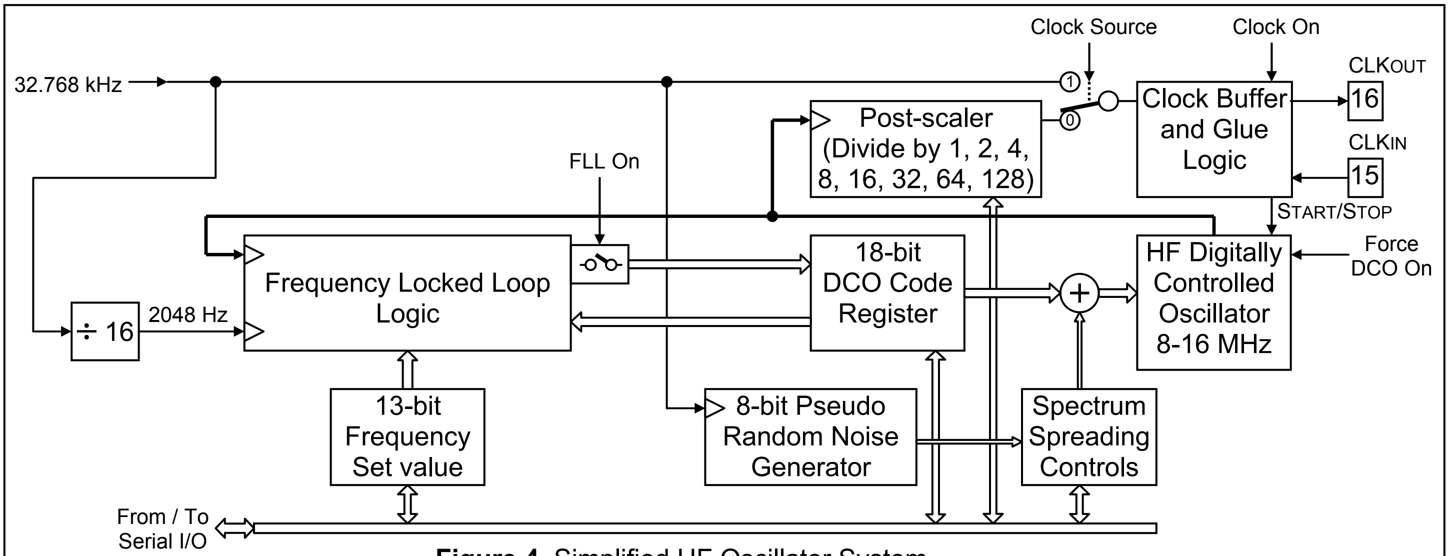


Figure 4. Simplified HF Oscillator System

The SH3002 employs a Frequency Locked Loop (FLL) to synchronize the HF clock to the 32.768 kHz reference. This architecture has several advantages over the common PLL (Phase Locked Loop) systems, including the ability to stop and re-start without frequency transients or instability, and with instant settling to a correct frequency. The conventional PLL approach invariably includes a Low-Pass Filter that requires a long settling time on re-start.

The primary purpose of the FLL is the maintenance of the correct frequency while the ambient temperature is changing. As the temperature drift of the HF oscillator is quite small, any corrective action from the FLL system is also small and gradual, commensurate with the temperature variation.

The FLL system in the SH3002 is unconditionally stable.

To set a new frequency for the FLL, the host processor writes the 13-bit Frequency Set value. The resulting output frequency is calculated using simple formulas [1] and [2] (reference frequency is 32.768 kHz):

Table 2. EMI reduction with Spectrum Spreading

Setting			Spreading Bandwidth kHz	Peak EMI Reduction (guaranteed) db	Peak EMI Reduction (measured) db
En	CFG1	CFG0			
0	X	X	Off	0	0
1	0	0	32	-3	-3
1	0	1	64	-6	-7
1	1	0	128	-9	-10
1	1	1	256	-12	-15

F_{OSC} = 2048 Hz * (Frequency Set value + 1) [1]

F_{OUT} = F_{OSC} / (Post-divider setting) [2]

For example, a post-divider setting of ÷8 and the Frequency Set value of 4000 (0x0FA0) produce an output frequency of 1.024 MHz.

Programmable Spectrum Spreading

Most commercial electronic systems must pass regulatory tests in order to determine the degree of their Electromagnetic Interference (EMI) affecting other electronic devices. In some cases compliance with the EMI standards is costly and complicated.

The SH3002 offers a technique for reducing the EMI. It can be a part of the initial design strategy, or it can be applied in the prototype stage to fix problems identified during compliance testing. This feature of the SH3002 can greatly reduce the requirements for radiofrequency shielding, and permits the use of simple plastic casings in place of expensive RFI-coated or metal casings.

The SH3002 employs Programmable Spectrum Spreading in order to reduce the RF emissions from the processor's clock. There are five (5) possible settings; please see **Table 2** for operating and performance figures in the 8-16 MHz range.

Spectrum Spreading is created by varying the frequency of the HF oscillator with a pseudo-random sequence (with a zero-average DC component). The Maximum-Length Sequence (MLS) 8-bit random number generator, clocked by 32.768 kHz, is used. Only 4, 5, 6, or 7 bits of the generated 8-bit random number are used, according to the configuration setting.

Maximum fluctuations of the frequency depend on the selected frequency range and the position within the range. Selecting the HF oscillator frequency to be near the high end of the range limits the peak variations to ± 0.1%, ± 0.2%, ± 0.4%, or ± 0.8% (corresponding to the configuration setting).

Special Operating Modes

The SH3002 can operate stand-alone, without connections to the In and Out terminals of the host's oscillator. For example, a bank of SH3002 chips can generate several different frequencies for simultaneous use in the system, all controlled by a single micro (and possibly sharing one 32.768 kHz crystal by chaining the CLK32 pin to X_{IN} pin on the next device). In this case the CLK_{IN} pin should be connected to V_{SS}. The clock output on the CLK_{OUT} pin is continuous; the correct operating mode is automatically recognized by the SH3002.

A microcontroller might not have a STOP command. With the SH3002, this controller can do a "simulated" STOP by issuing an instruction to the SH3002 to stop the clock. This command is accepted only if the Periodic Interrupt / Wakeup Timer has started (otherwise, once the system is put to sleep, it would never wake up again). This mode of operations is only possible if the host processor is capable of correct operations with clock frequency down to zero, and keeps all of the internal RAM alive while the clock is stopped.

SYSTEM MANAGEMENT

Low Frequency (LF) Oscillator System

This module provides the 32 kHz clock to all internal circuits and to the dedicated output pin, CLK32.

If enabled, the CLK32 output continues normal operations when VDD is absent and backup power is available.

Just like the VBO value for the Reset circuit, the default calibration values for the RC oscillator are loaded on power-up from the factory-programmed nonvolatile memory. They can be re-programmed at any time or they can be permanently protected from any changes by setting the Lock flag or a write-protect flag. Factory calibration brings the frequency of the RC oscillator within ±3 % of the 32768 Hz for the internal reference resistor, and ± 2% for the external 1 MΩ 1% resistor, over the entire temperature and supply voltage range.

The frequency of the RC oscillator can be tuned or modulated by varying the external reference resistor, which should be located as close as possible to RREF, pin 9.

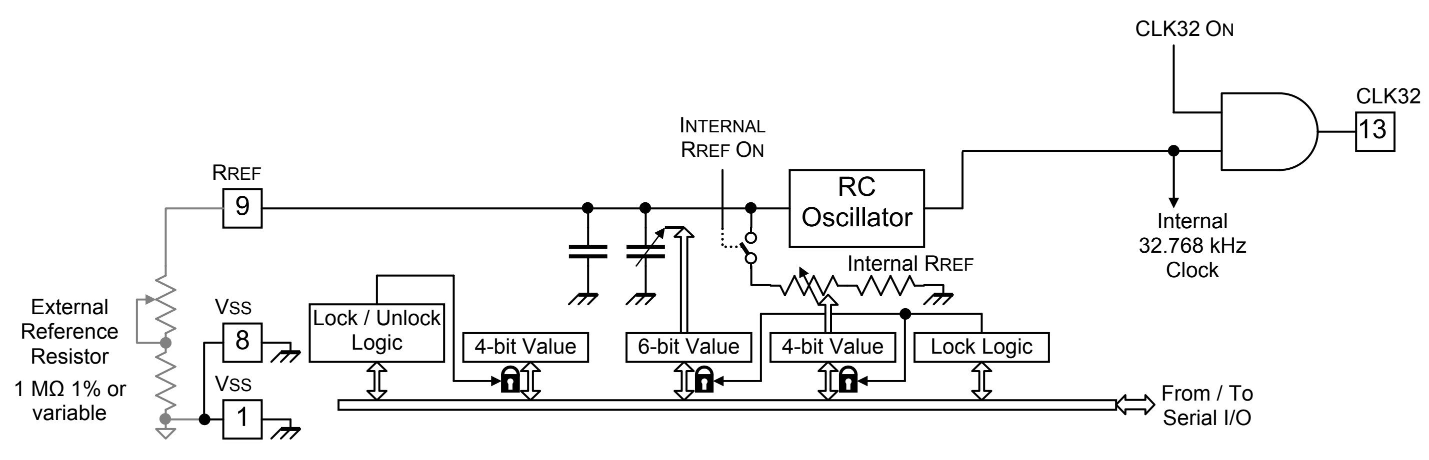


Figure 5. Simplified LF Oscillator System

SYSTEM MANAGEMENT

Periodic Interrupt / Wakeup Timer

Simple and versatile, the Periodic Interrupt / Wakeup Timer can be used to create very accurate recurring interrupts for use by the host micro. With some minimal software support from the host processor, it can also be used to create alarms, with practically unlimited duration.

While the timer is running, the host processor can be halted, consuming no energy. The interrupt wakes up the processor, which can perform the requisite task and go back to sleep, until the next periodic interrupt.

This mode of operation can achieve extremely low average power consumption.

A 32-bit counter clocked by 32.768 kHz, producing a minimum interval of 30.5 µs and the maximum interval of 36.4 hours, creates the Timer.

After reset, the Timer is stopped until the new value for the time interval is written into the 4-byte Time Interval register. When the least significant byte (LSB) is written, the whole value is moved to the Time Interval latch, the counter is reset and starts to increment with the 32.768 kHz clock.

When the 32-bit comparator detects a match, an interrupt is generated and the counter is reset and starts the next timing cycle.

Although the counter cannot be written to, the current value from the counter can be read at any time. The whole 32-bit value is loaded into the 32-bit Current Timer Value latch when the least significant byte is read. This prevents errors stemming from the finite time between the readings of individual bytes of the current value.

Auxiliary functions

Voltage Regulator

Pin VREG can be used as a nominal 2.20 V reference voltage or a supply source for small loads (<2 mA). A bypass capacitor might be necessary between this pin and VSS if the load generates large current transients or a low ripple reference is required.

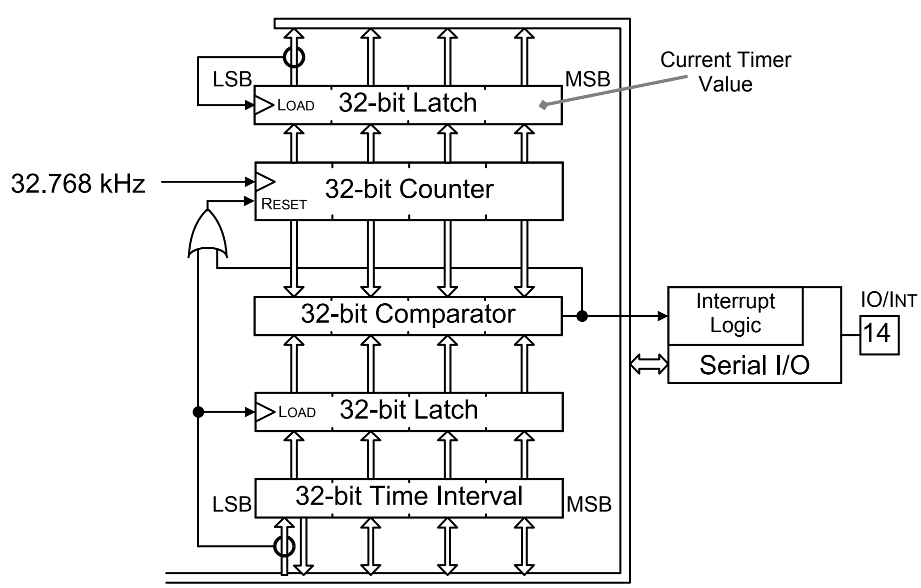


Figure 6. Periodic Interrupt / Wakeup timer

Interrupt and Serial Interface

A single line is used to convey bi-directional information between the SH3002 and the processor, and as the interrupt line to the processor.

The polarity of the interrupt signal is programmable.

The SH3002 and the host microcontroller communicate using a single wire, bi-directional asynchronous serial interface. The bit rate is automatically determined by the SH3002. . At the fastest possible rate, a read or write access of a single byte from the register bank takes 5 µs.

The SH3002 contains 36 addressable registers located at 0x00–0x1F. Some of these registers are accessed through a page operation. Pin 14, IO/Int, is the serial communications interface and interrupt output pin. This pin is internally weakly pulled to the opposite of the programmed interrupt polarity. For example, if interrupt is programmed to be active low, this pin is weakly pulled to VDD when inactive.

As shown in **Figure 7**, the SH3002 and the host communicate with serial data streams. The host always initiates communication. A data stream consists of the following (in this order):

- 3-bit start field
- 3-bit read/write code
- 5-bit address field
- 1 guard bit
- 8-bit data field
- 2 parity bits

Plus, for write streams only:

- 1 guard bit
- 2 acknowledge (ACK) bits

The 3-bit start field (1,0,1 or 0,1,0, depending on interrupt polarity) uses the middle bit to determine the bit period of the serial data stream.

The 3-bit read/write code consists of 1,1,0 for a read, or 0,1,1 for a write. This protects against early glitches that might otherwise put the interface into an invalid read or write access mode.

The 5-bit address field contains the address of the register.

A single guard bit gives the interface a safe period in which to change data direction. The value of a guard bit does not matter.

The 8-bit data field is written to (read from) the register.

Two parity bits: The first parity bit is high when there are an odd number of bits in the read/write, address and data fields; the second parity bit is the inverse of the first.

For write streams only, a guard bit is appended to the stream (to allow safe turnaround), and then two acknowledge bits, which are a direct copy of the parity bits, are driven back to the host to indicate a successful write access.

Two guard bits are appended to the end of the access stream (read or write). The host can not start the next access before receiving these bits.

The interface is self-timed based on the duration of the start bit field, and communication can take place whenever CLKOUT is active, either at 32.768 kHz or at a higher frequency. If the host microcontroller is running synchronously to the CLKOUT generated by the SH3002 (which should generally be the case), then a minimum of 4 CLKOUT cycles per bit are required to maintain communication integrity. If the host's serial interface is asynchronous to CLKOUT, then a minimum of 52 cycles per bit are necessary. A maximum of 1024 CLKOUT cycles per bit field is supported.

Table 3 displays the minimum and maximum bit periods for the serial communications for CLKOUT frequencies of 16 MHz, 8 MHz, and 2 MHz.

Table 3: Minimum/Maximum Serial Bit Timing

CLKOUT Frequency	Minimum Bit Period (host synchronous to CLKOUT)	Minimum Bit Period (host asynchronous to CLKOUT)	Maximum Bit Period
16 MHz	250 ns	3.25 µs	63.9 µs
8 MHz	500 ns	6.5 µs	127 µs
2 MHz	2 µs	26 µs	511 µs

Interrupt Interface

The serial communications line to the SH3002 (Pin 14, IO/Int) also serves as the interrupt to the host microcontroller. The polarity of the interrupt is software programmable using the interrupt polarity bit (bit 6) of the IPol_RCtune register (R0x11). This pin is asserted for four cycles of CLKOUT, and then returns to the inactive state.

The interrupt line is used by the Periodic Interrupt/Wake-up Timer to interrupt the host when it reaches its end of count.

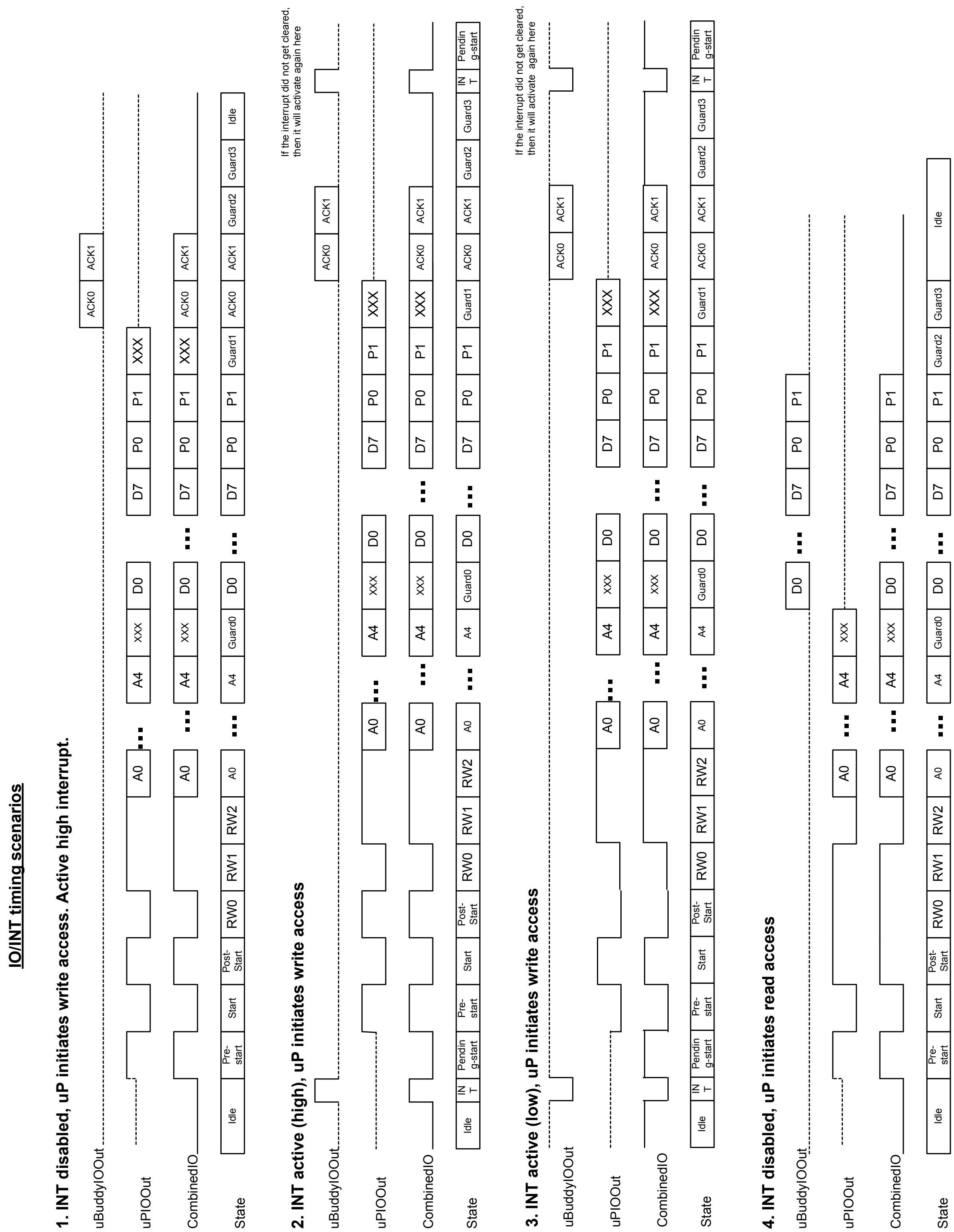


Figure 7: Serial Communication Timing Diagram

Electrical Specifications

Absolute Maximum Ratings

Note: The SH3002 is ESD-sensitive.

Description	Symbol	Min	Max	Units
Supply voltages on VDD relative to ground	VDD	-0.5	5.5	V
Input voltage on CLKIN, IO/INT, TEST	VIN1	-0.5	VDD + 0.5	V
Input voltage on CLKSEL	VIN2	-0.5	VREG + 0.5	V
Input current on any pin except VREG	IIN1		10	mA
Input current on VREG	IIN2		150	mA
Ambient operating temperature	TOP	-40	85	ºC
Storage temperature	TSTG	-55	160	ºC

Operating Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Notes
Case temperature	TOP	–40		+85	°C	
Supply voltage	VDD	2.3		5.5	V	
Supply current, CLKOUT = 16 MHz*	IDD			3	mA	
Supply current, CLKOUT = 8 MHz*	IDD		1.8		mA	
Supply current, CLKOUT = 2 MHz*	IDD		0.9		mA	
Standby current, 32.768 kHz RC oscillator**	ISB			10	µA	CLK32 disabled

*Note: Assuming load on CLKOUT < 20 pf

**Note: Assuming temperature < 60ºC

Operating characteristics of 32.768 kHz RC oscillator

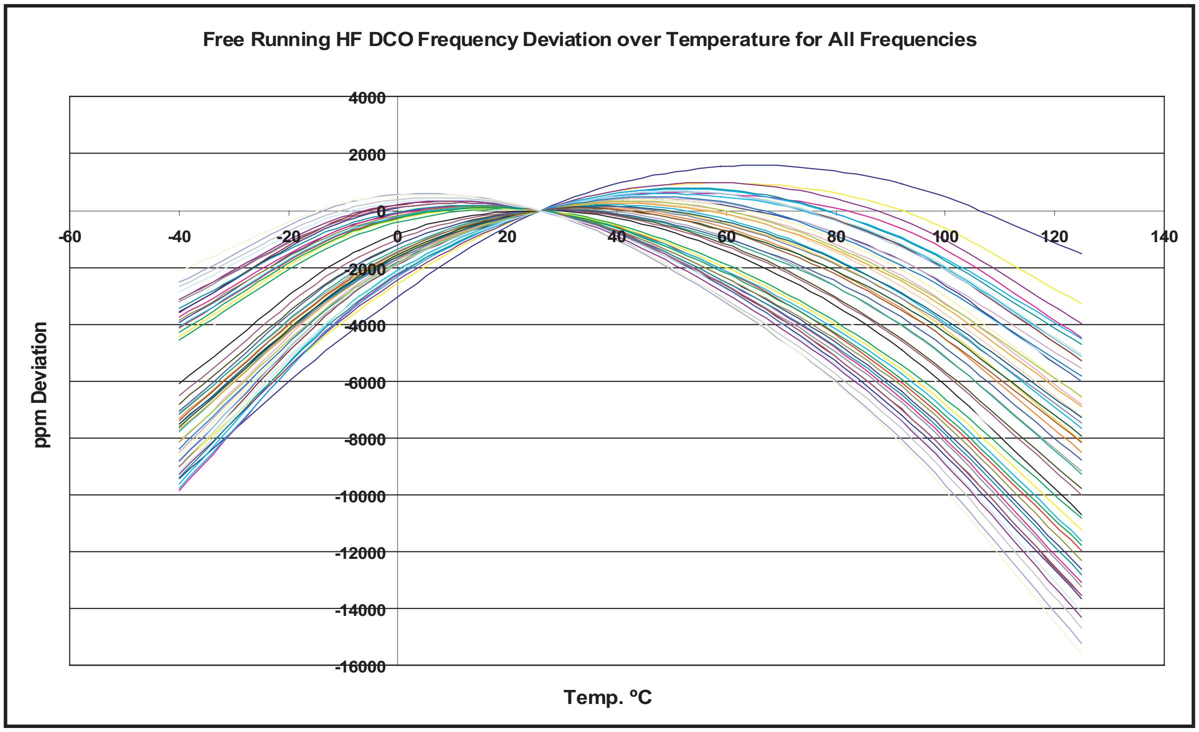
Parameter	Symbol	Min	Typ	Max	Units
External 1 MOhm referenced nominal frequency	Fext		32.768		kHz
Internal 1 MOhm referenced nominal frequency	Fint		32.768		kHz
CLK32 duty cycle	DC	40		60	%
Programmed frequency accuracy at 25°C	Fst	-1.5		+1.5	%
Absolute accuracy over temperature and supply (external 1 MOhm)	Fde		±2		%
Absolute accuracy over temperature and supply (internal 1 MOhm)	Fdi		±3		%
Frequency temperature stability (ext. 1 MOhm)	Fse		100		ppm/°C
Frequency temperature stability (int. 1 MOhm)	Fsi		200		ppm/°C
Power on startup time	Tst		70		µs
CLK32 cycle to cycle jitter	J		0.1		%

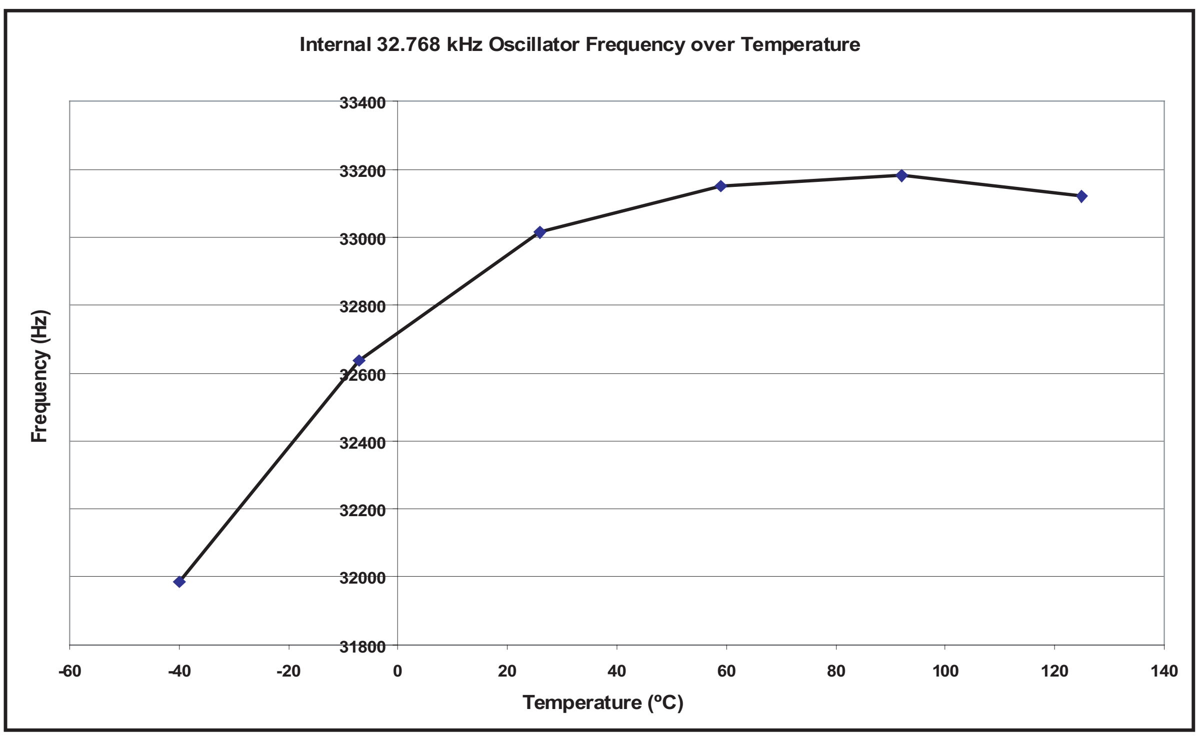
Operating characteristics of programmable reset

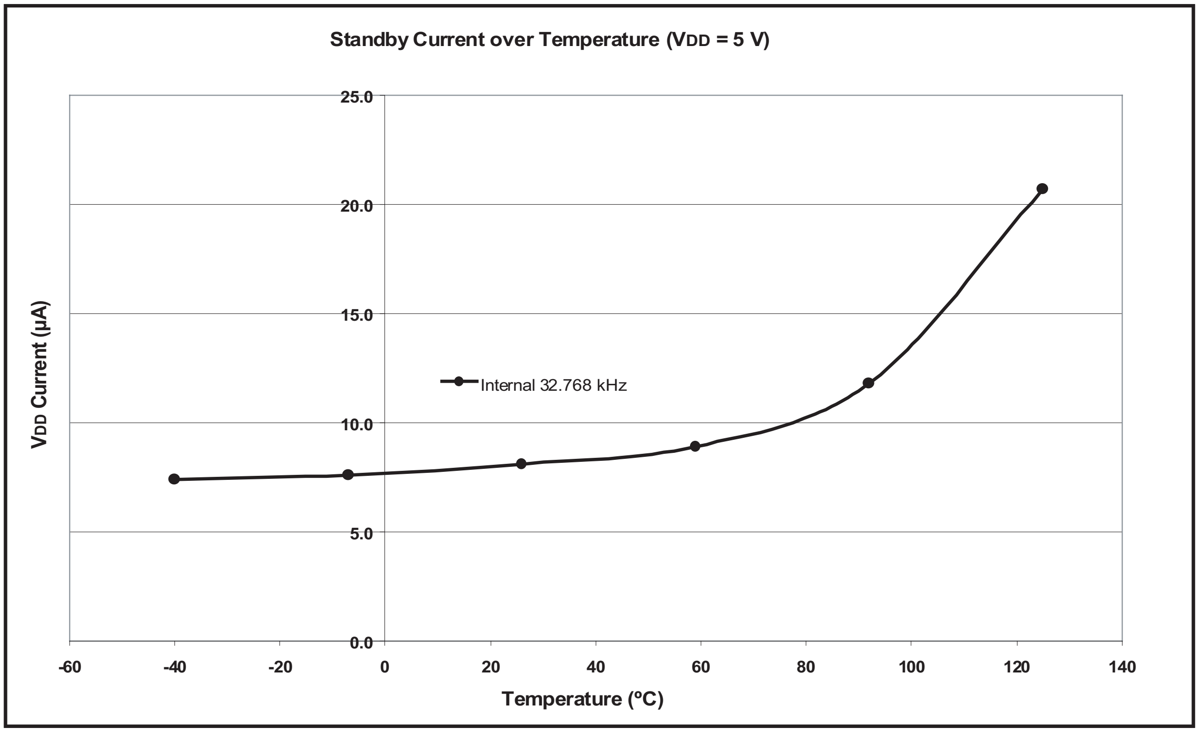
Parameter	Symbol	Min	Typ	Max	Units
V_{DD} switching threshold for Min code (Start-up default = 2.3 V)	Vbo(min)	2.27	2.3	2.33	V
V_{DD} switching threshold for Max code	Vbo(max)	4.2	4.3	4.4	V
V_{DD} threshold resolution	Vres		33		mV
V_{DD} hysteresis	Vhys		50		mV
Falling V_{DD} threshold switch delay	Td		2.5		µs
Threshold digital-analog converter (DAC) settling time	Tdac		4		ms
Minimum V_{DD} for valid nRST	VDDmin			1	V

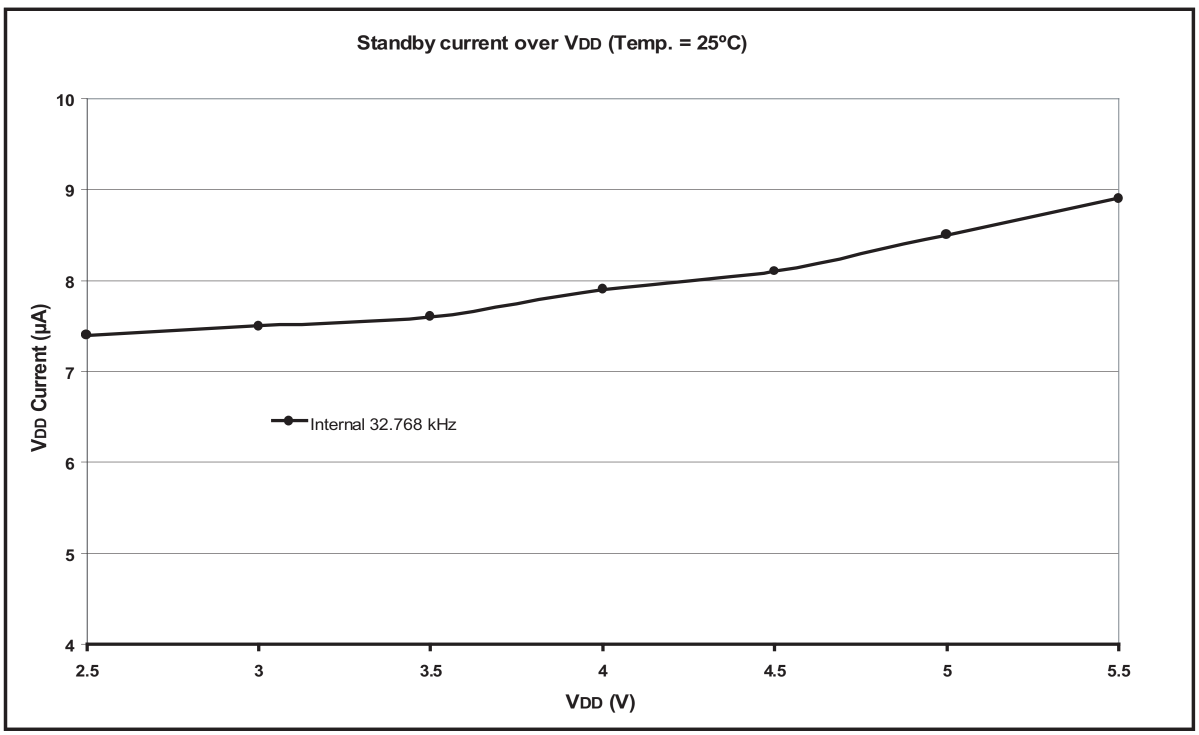
Operating characteristics of the high-frequency oscillator (HFO)

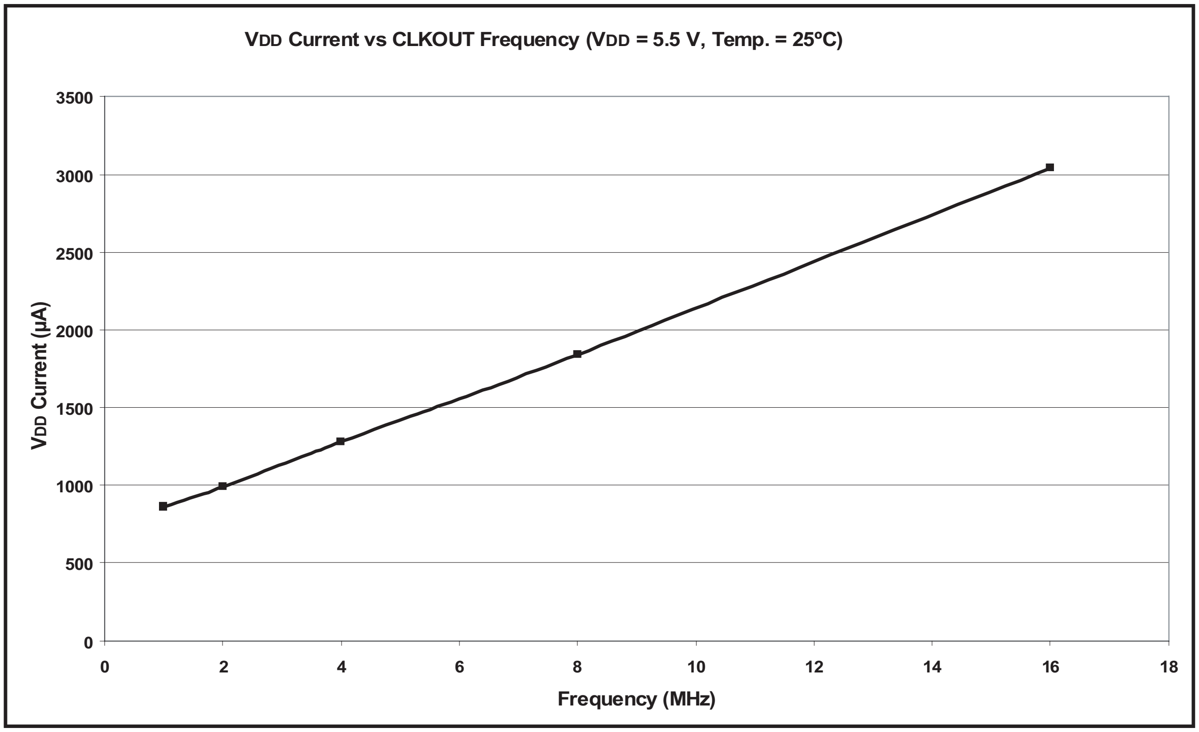
Parameter	Symbol	Min	Typ	Max	Units
Minimum operating frequency (Start-up default = 2 MHz)	Fmin		5.6	8	MHz
Maximum operating frequency	Fmax	16.8	21		MHz
Frequency resolution	Fres		2		kHz
Programmed frequency accuracy at 25°C	Fst	-0.3		+0.3	%
Frequency drift over temperature and supply	Fdrift		±0.5		%
CLKOUT cycle to cycle jitter (spread spectrum off)	J		0.1		%
Startup time from standby	Tstart			2	µs
Settling time to 0.1% after HF digitally-controlled oscillator (DCO) code change	Tsett		10		µs
CLKOUT duty cycle	DC	40		60	%
Frequency temperature stability	Fts		100		ppm/°C
Short term frequency stability	Fs		0.5		%/sec
Minimum spread spectrum range	SSmin		32		kHz
Maximum spread spectrum range	SSmax		256		kHz
CLKOUT rise/fall time (20 pF load)	Trf		3		ns
CLKOUT logic output low (4 mA load)	Vol		0.25	0.4	V
CLKOUT logic output high (4 mA load)	Voh	-0.4	-0.25		Ref VDD

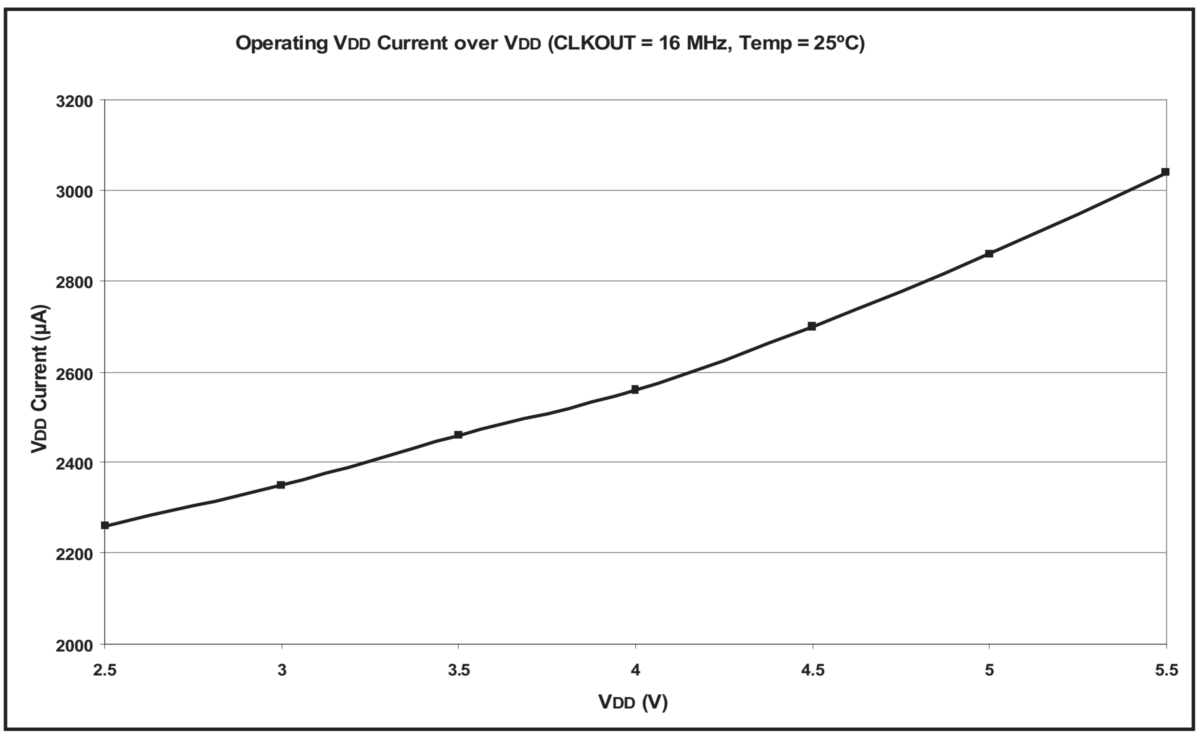

Free Running HF DCO Frequency Deviation over Temperature for All Frequencies
4000
2000
0
-2000
-4000
-6000
-8000
-10000
-12000
-14000
-16000
ppm Deviation
-60
-40
-20
0
20
40
60
80
100
120
140
Temp. °C

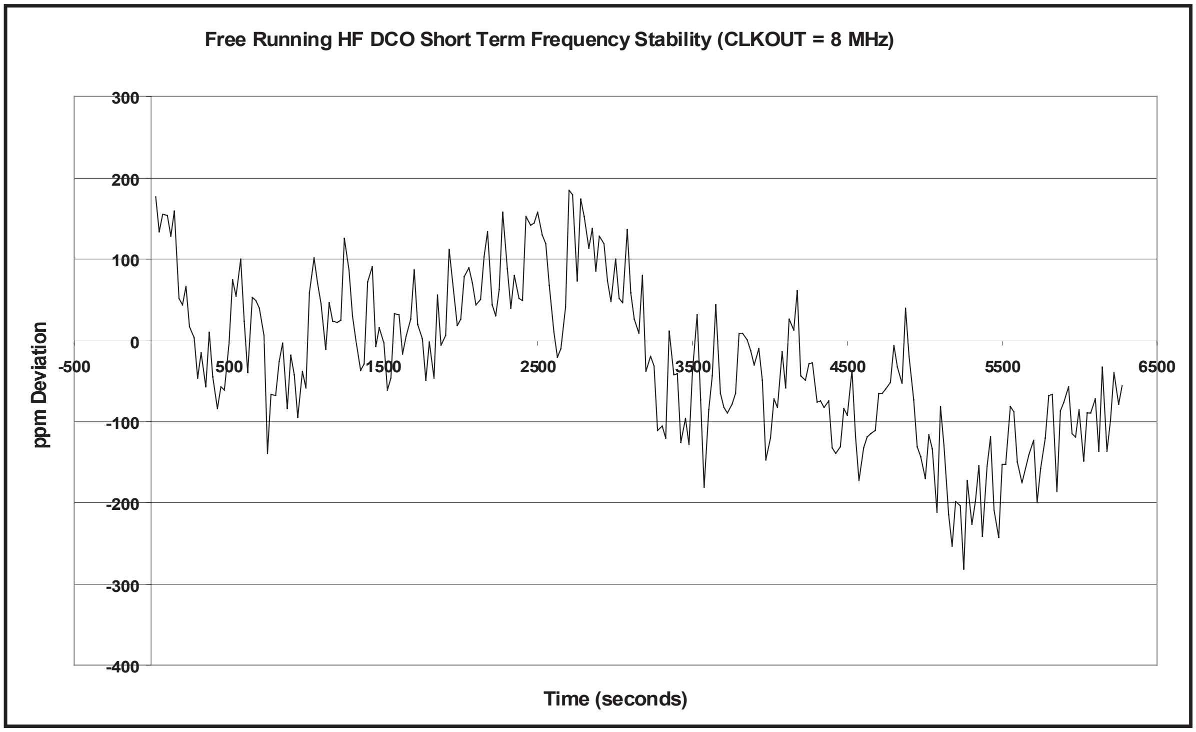

Internal 32.768 kHz Oscillator Frequency over Temperature
33400
33200
33000
32800
32600
32400
32200
32000
31800
Frequency (Hz)
-60
-40
-20
0
20
40
60
80
100
120
140
Temperature (ºC)

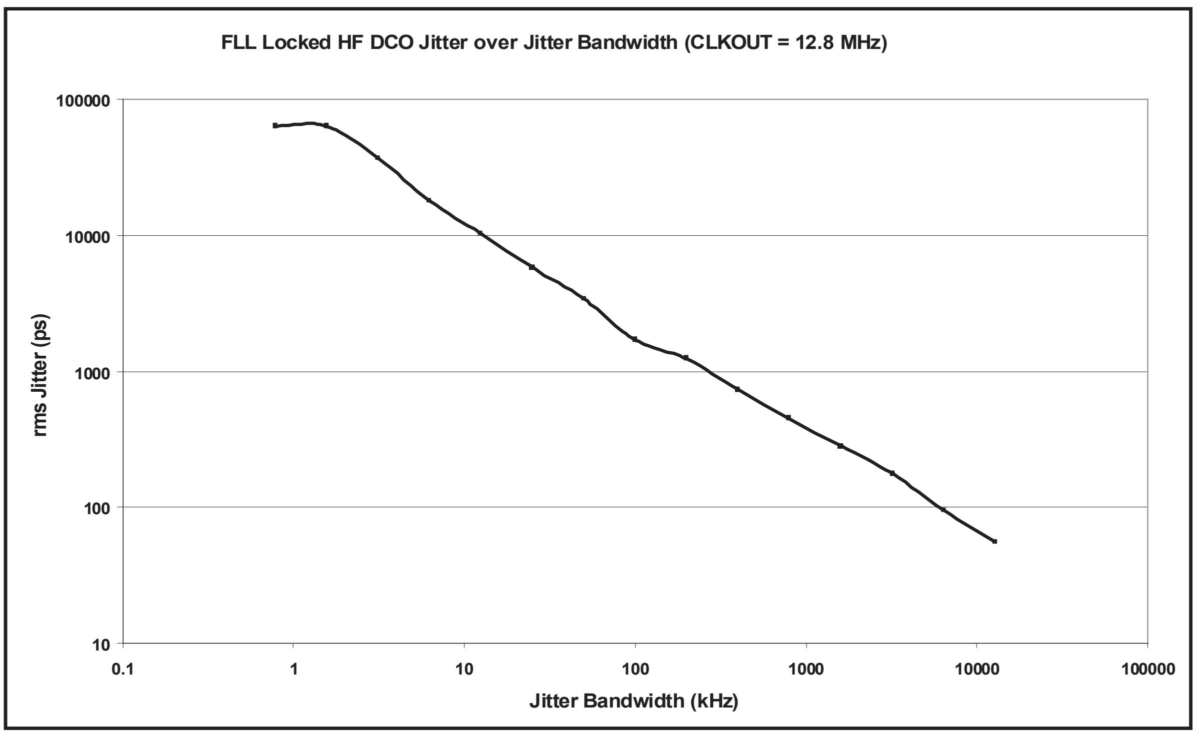

Standby Current over Temperature (VDD = 5 V)
VDD Current (µA)
25.0
20.0
15.0
10.0
5.0
0.0
Internal 32.768 kHz
-60
-40
-20
0
20
40
60
80
100
120
140
Temperature (ºC)


Standby current over VDD (Temp. = 25ºC)
VDD Current (µA)
10
9
8
7
6
5
4
Internal 32.768 kHz
2.5
3
3.5
4
4.5
5
5.5
VDD (V)


VDD Current vs CLKOUT Frequency (VDD = 5.5 V, Temp. = 25ºC)
VDD Current (µA)
3500
3000
2500
2000
1500
1000
500
0
0
2
4
6
8
10
12
14
16
18
Frequency (MHz)


Operating VDD Current over VDD (CLKOUT = 16 MHz, Temp = 25ºC)
VDD Current (µA)
3200
3000
2800
2600
2400
2200
2000
2.5
3
3.5
4
4.5
5
5.5
VDD (V)

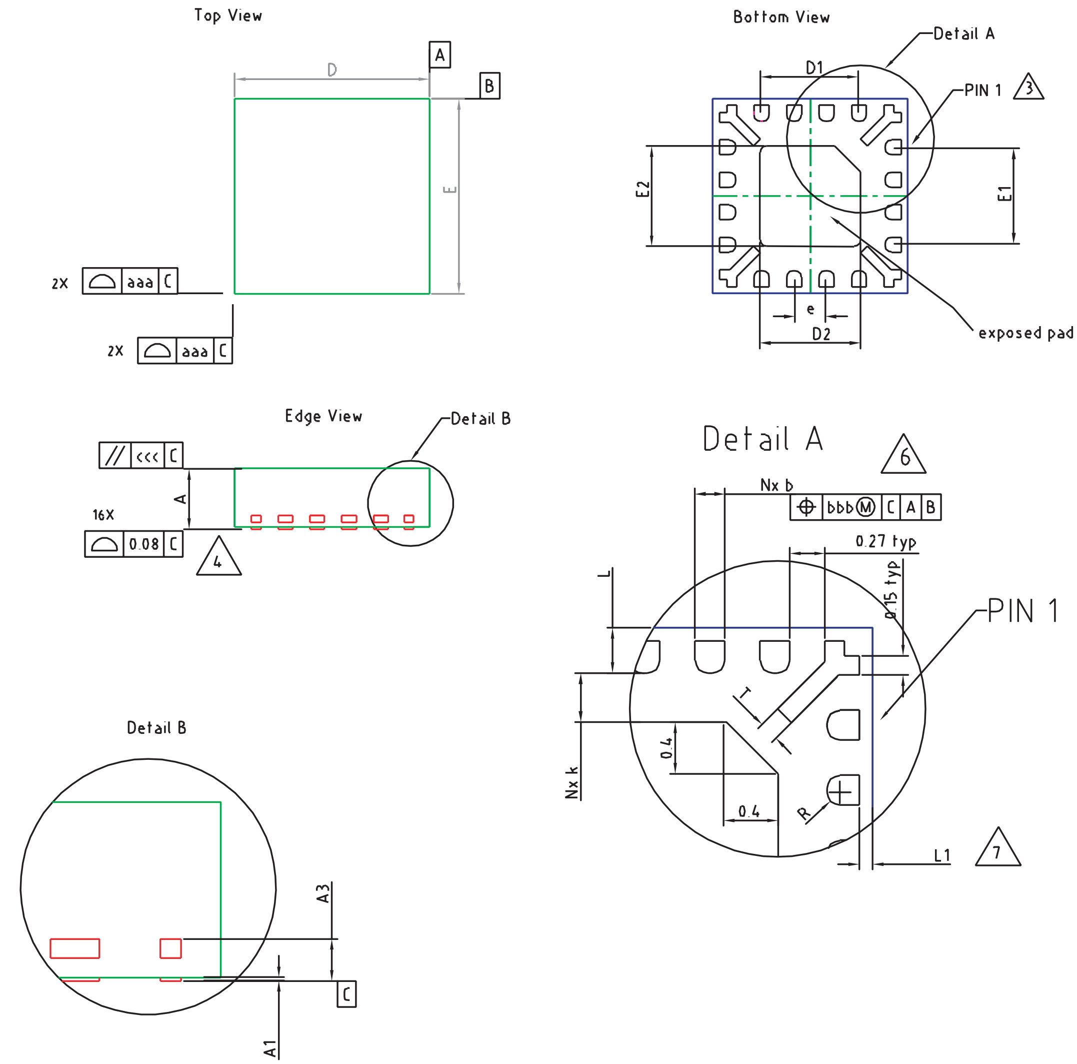

Free Running HF DCO Short Term Frequency Stability (CLKOUT = 8 MHz)
300
200
100
0
-100
-200
-300
-400
-500
500
1500
2500
3500
4500
5500
6500
ppm Deviation
Time (seconds)


FLL Locked HF DCO Jitter over Jitter Bandwidth (CLKOUT = 12.8 MHz)
100000
10000
1000
100
10
0.1
1
10
100
1000
10000
100000
rms Jitter (ps)
Jitter Bandwidth (kHz)

SEMTECH

SYSTEM MANAGEMENT

Package Outline Drawing MLP 3 x 3 mm 16 pins



Notes
1. JEDEC ref MO-220
2. All dimensions are in millimeters
3. Pin 1 orientation identified by chamfer on corner of exposed die pad.
4. Datum C and the seating plane are defined by the flat surface of the metallised terminal
5. Dimension 'e' represents the terminal pitch
6. Dimension b applies to metallised terminal and is measured 0.25 to 0.30mm from terminal tip.
7. Dimension L1 represents terminal pull back from package edge. Where terminal pull back exists, only upper half of lead is visible on package edge due to half etching of leadframe.
8. Package surface shall be matte finish , Ra 1.6 - 2.2
9. Package warp shall be 0.050 maximum
10. Leadframe material is copper A194.
11. Coplanarity applies to the exposed pad as well as the terminals.

Common Dimensions			
Sym.	Minimum	Nominal	Maximum
A	0.85	0.90	1.0
A1	0	0.02	0.05
A3		0.20 ref	
D	2.90	3.00	3.10
D1		1.50	
D2	1.45	1.55	1.65
E	2.90	3.00	3.10
E1		1.50	
E2	1.45	1.55	1.65
L	0.30	0.35	0.4
L1			0.1
b	0.18	0.23	0.3
N		16	
e		0.50	
k	0.20		
R	bmin/2		
T		0.15	

Sym.	Tolerances for Form & Position	Notes
aaa	0.15	
bbb	0.10	
ccc	0.10	

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