

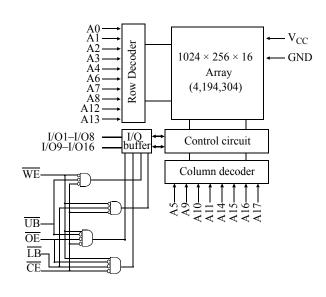
5V/3.3V 256K × 16 CMOS SRAM

Features

- AS7C4098 (5V version)
- AS7C34098 (3.3V version)
- Industrial and commercial temperature
- Organization: 262,144 words × 16 bits
- Center power and ground pins
- High speed
 - 10/12/15/20 ns address access time
 - 5/6/7/8 ns output enable access time
- Low power consumption: ACTIVE
 - 1375 mW (AS7C4098)/max @ 12 ns
 - 576 mW (AS7C34098)/max @ 10 ns

- Low power consumption: STANDBY
- 110 mW (AS7C4098)/max CMOS
- 72 mW (AS7C34098)/max CMOS
- Individual byte read/write controls
- Easy memory expansion with \overline{CE} , \overline{OE} inputs
- TTL- and CMOS-compatible, three-state I/O
- 44-pin JEDEC standard packages
- 400-mil SOJ
- TSOP 2
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 100 mA

Logic block diagram



Pin arrangement for SOJ and TSOP 2

44-pin (400 mil) SOJ TSOP2

A3	3
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Selection guide

		-10	-12	-15	-20	Unit
Maximum address access time		10	12	15	20	ns
Maximum output enable access time		5	6	7	8	ns
Maximum operating current	AS7C4098	_	250	220	180	mA
iviaximum operating current	AS7C34098	160	130	110	100	mA
Maximum CMOS standby current	AS7C4098	_	20	20	20	mA
Waximum Civios standay current	AS7C34098	20	20	20	20	mA



Functional description

The AS7C4098 and AS7C34098 are high-performance CMOS 4,194,304-bit Static Random Access Memory (SRAM) devices organized as 262,144 words × 16 bits. They are designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times (t_{AA}, t_{RC}, t_{WC}) of 10/12/15/20 ns with output enable access times (t_{OE}) of 5/6/7/8 ns are ideal for high-performance applications. The chip enable input \overline{CE} permits easy memory expansion with multiple-bank memory systems.

When $\overline{\text{CE}}$ is High the device enters standby mode. The standard AS7C4098/AS7C34098 is guaranteed not to exceed 110/72mW power consumption in CMOS standby mode. A write cycle is accomplished by asserting write enable ($\overline{\text{WE}}$) and chip enable ($\overline{\text{CE}}$). Data on the input pins I/O1–I/O16 is written on the rising edge of $\overline{\text{WE}}$ (write cycle 1) or $\overline{\text{CE}}$ (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{\text{OE}}$) or write enable ($\overline{\text{WE}}$).

A read cycle is accomplished by asserting output enable (\overline{OE}) and chip enable (\overline{CE}) , with write enable (\overline{WE}) High. The chip drives I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

These devices provide multiple center power and ground pins, and separate byte enable controls, allowing individual bytes to be written and read. \overline{LB} controls the lower bits, I/O1–I/O8, and \overline{UB} controls the higher bits, I/O9–I/O16.

All chip inputs and outputs are TTL- and CMOS-compatible, and operation is from either a single 5V (AS7C4098) or 3.3V (AS7C34098) supply. Both devices are available in the JEDEC standard 400-mL, 44-pin SOJ and TSOP 2 packages.

Absolute maximum ratings

Parameter	Device	Symbol	Min	Max	Unit
Voltage on V _{CC} relative to GND	AS7C4098	V _{t1}	-0.50	+7.0	V
voltage on Ver relative to GND	AS7C34098	V _{t1}	-0.50	+5.0	V
Voltage on any pin relative to GND		V _{t2}	-0.50	V _{CC} +0.50	V
Power dissipation		P_{D}	_	1.5	W
Storage temperature		T _{stg}	-65	+150	°C
Ambient temperature with V _{CC} applied		T _{bias}	-55	+125	°C
DC current into outputs (low)		I _{OUT}	_	±20	mA

Note: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

II dell'edb							
CE	WE	OE	LB	UB	I/O1–I/O8	I/O9-I/O16	Mode
Н	X	X	X	X	High Z	High Z	Standby (I _{SB} , I _{SB1})
L	Н	Н	X	X	High Z	High Z	Output disable (I _{CC})
L	X	X	Н	Н	Iligii Z	IIIgii Z	Output disable (ICC)
			L	Н	D _{OUT}	High Z	
L	Н	L	Н	L	High Z	D _{OUT}	Read (I _{CC})
			L	L	D _{OUT}	D _{OUT}	
			L	Н	D _{IN}	High Z	
L	L	X	Н	L	High Z	D _{IN}	Write (I _{CC})
			L	L	D _{IN}	D _{IN}	

Key: X = Don't care, L = Low, H = High.



Recommended operating conditions

Parameter		Symbol	Min	Typical	Max	Unit	
		AS7C4098	V _{CC} (12/15/20)	4.5	5.0	5.5	V
Supply voltage		AS7C34098	V _{CC} (10)	3.15	3.3	3.6	V
	AS7C34098	V _{CC} (12/15/20)	3.0	3.3	3.6	V	
		AS7C4098	V _{IH}	2.2	_	$V_{CC} + 0.5$	V
Input voltage		AS7C34098	V _{IH}	2.0	_	$V_{CC} + 0.5$	V
			V_{IL}^{I}	-0.5	_	0.8	V
Ambient operating temperature –	commercial		$T_{\mathbf{A}}$	0	_	70	°C
	industrial		T_{A}	-40	_	85	°C

¹ $V_{\rm IL}$ min = -1.0V for pulse width less than 5ns.

DC operating characteristics (over the operating range)¹

					10	_	12	-	15	-2	20	
Parameter	Symbol	Test conditions	Test conditions			Min	Max	Min	Max	Min	Max	Unit
Input leakage current	$ I_{LI} $	$V_{CC} = Max$ $V_{IN} = GND \text{ to } V_{CC}$	AS7C4098/ AS7C34098		1	1	1	_	1	ı	1	μА
Output leakage current	$ I_{LO} $	$\begin{aligned} V_{CC} &= \underbrace{Max} \\ \overline{CE} &= V_{\underline{IH}} \text{ or } \overline{OE} = V_{IH} \\ \text{ or } \overline{WE} &= V_{IL} \\ V_{I/O} &= GND \text{ to } V_{CC} \end{aligned}$	AS7C4098/ AS7C34098	-	1	1	1		1	-	1	μΑ
Operating	т.	$V_{CC} = Max$	AS7C4098	_	_	-	250	_	220		180	mA
power supply current	I_{CC}	$\frac{\text{Min cycle, } 100\% \text{ duty}}{\overline{\text{CE}}} = V_{\text{IL}}, I_{\text{OUT}} = 0\text{mA}$	AS7C34098	_	160	_	130	_	110	_	100	mA
	I_{SB}	$V_{CC} = Max$	AS7C4098	_	_	_	60	_	60	_	60	mA
Standby power	1SB	$\overline{CE} = V_{IH}, f = Max$	AS7C34098	_	60	_	60	_	60	_	60	mA
supply current	_	$V_{CC} = Max$	AS7C4098	_	_	_	20	_	20	_	20	mA
	I_{SB1}	$\label{eq:center_constraints} \begin{split} \overline{CE} &\geq V_{CC} - 0.2V, V_{IN} \geq V_{CC} \\ &- 0.2V \text{ or } V_{IN} \leq 0.2V, f = 0 \end{split}$	AS7C34098	_	20	-	20	_	20	_	20	mA
Output voltage	V _{OL}	$I_{OL} = 8 \text{ mA}, V_{CC} = \text{Min}$	AS7C4098/	_	0.4	_	0.4	_	0.4	_	0.4	V
Output voltage	V _{OH}	$I_{OH} = -4 \text{ mA}, V_{CC} = \text{Min}$	AS7C34098	2.4	_	2.4	_	2.4	_	2.4	_	V

Capacitance (f = 1MHz, $T_a = 25^{\circ} C$, $V_{CC} = NOMINAL)^2$

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C _{IN}	$A, \overline{CE}, \overline{WE}, \overline{OE}, \overline{UB}, \overline{LB}$	$V_{IN} = 0V$	6	pF
I/O capacitance	C _{I/O}	I/O	$V_{IN} = V_{OUT} = 0V$	8	pF



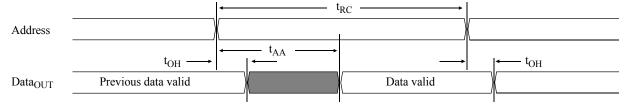
Read cycle (over the operating range) 3,9

		I.	10	-1	12	-	15	-7	20		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Read cycle time	t_{RC}	10	_	12	_	15	_	20	_	ns	
Address access time	t_{AA}	_	10	_	12	_	15	_	20	ns	
Chip enable (\overline{CE}) access time	t _{ACE}	_	10	_	12	_	15	_	20	ns	
Output enable (OE) access time	t _{OE}	_	5	_	6	_	7	_	8	ns	
Output hold from address change	t _{OH}	3	_	3	_	3	_	3	_	ns	5
CE Low to output in low Z	t_{CLZ}	0	_	3	_	0	_	0	_	ns	4, 5
TE High to output in higfch Z	t _{CHZ}	_	5	_	6	_	7	_	9	ns	4, 5
OE Low to output in low Z	$t_{ m OLZ}$	0	_	0	_	0	_	0	_	ns	4, 5
OE High to output in high Z	t _{OHZ}	_	5	_	6	_	7	_	9	ns	4, 5
LB, UB access time	t_{BA}	_	5	_	6	_	7	_	8	ns	
LB, UB Low to output in low Z	$t_{ m BLZ}$	0	_	0	_	0	_	0	_	ns	
LB, UB High to output in high Z	t _{BHZ}		5	_	6	-	7	_	9	ns	
Power up time	t_{PU}	0	_	0	_	0	_	0	_	ns	5
Power down time	t _{PD}	_	10	_	12		15		20	ns	5



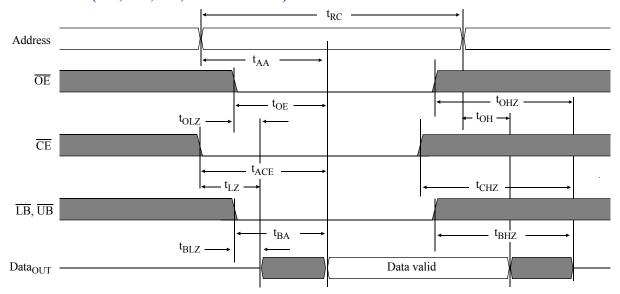
Rising input Falling input Undefined/don't care

Read waveform 1 (address controlled)^{6,7,9}





Read waveform 2 (CE, OE, UB, LB controlled)^{6,8,9}

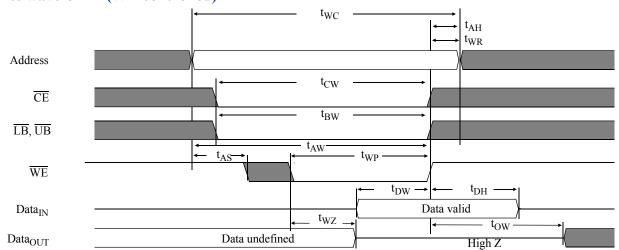


Write cycle (over the operating range)¹¹

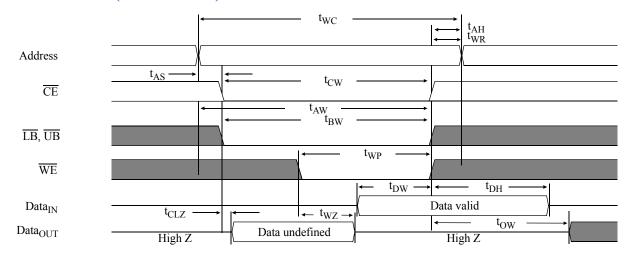
		-	10	-	12	_	15	_	20		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Note
Write cycle time	t _{WC}	10	_	12	_	15	_	20	_	ns	
Chip enable (\overline{CE}) to write end	t_{CW}	7	_	8	_	10	_	12	_	ns	
Address setup to write end	t _{AW}	7	_	8	_	10	_	12	_	ns	
Address setup time	t_{AS}	0	_	0	_	0	_	0	_	ns	
Write pulse width $(\overline{OE} = High)$	t _{WP1}	7	_	8	_	10	_	12	_	ns	
Write pulse width $(\overline{OE} = Low)$	t _{WP2}	10	_	12	_	15	_	20	_	ns	
Write recovery time	t_{WR}	0	_	0	_	0	_	0	_	ns	
Address hold from end of write	t _{AH}	0	_	0	_	0	_	0	_	ns	
Data valid to write end	t_{DW}	5	_	6		7	_	9	_	ns	
Data hold time	t _{DH}	0	_	0	_	0	_	0	_	ns	4, 5
Write enable to output in High-Z	t_{WZ}	0	5	0	6	0	7	0	9	ns	4, 5
Output active from write end	t_{OW}	3	_	3	_	3	_	3	_	ns	4, 5
Byte enable Low to write end	t _{BW}	7	_	8	_	10	_	12	_	ns	4, 5



Write waveform 1(WE controlled)^{10,11}

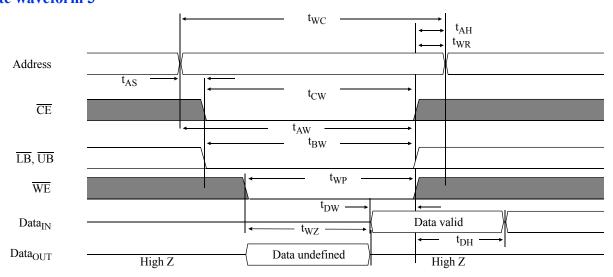


Write waveform 2 ($\overline{\text{CE}}$ controlled)^{10,11}



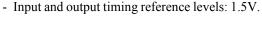


Write waveform 3 10,11



AC test conditions

- Output load: see Figure B or Figure C.
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 2 ns. See Figure A.



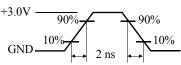
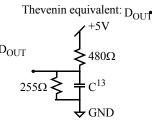
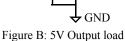


Figure A: Input pulse





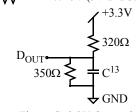


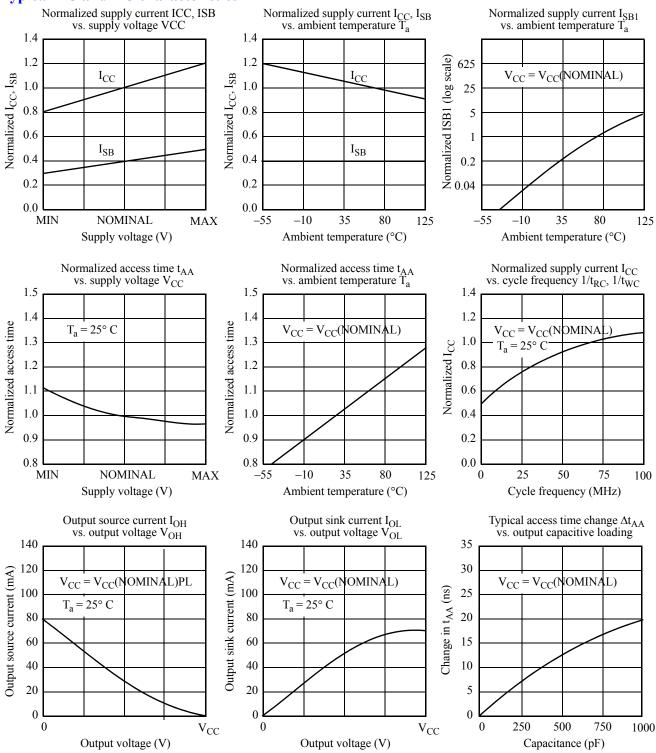
Figure C: 3.3V Output load

Notes

- During V_{CC} power-up, a pull-up resistor to V_{CC} on \overline{CE} is required to meet I_{SB} specification. 1
- This parameter is sampled, but not 100% tested.
- For test conditions, see AC Test Conditions, Figures A, B, C.
- t_{CLZ} and t_{CHZ} are specified with C_L = 5pF as in Figure C. Transition is measured ± 500 mV from steady-state voltage. 4
- This parameter is guaranteed, but not tested. 5
- WE is High for read cycle.
- $\overline{\text{CE}}$ and $\overline{\text{OE}}$ are Low for read cycle.
- Address valid prior to or coincident with \overline{CE} transition Low.
- All read cycle timings are referenced from the last valid address to the first transitioning address.
- 10 $\overline{\text{CE}}$ or $\overline{\text{WE}}$ must be High during address transitions. Either $\overline{\text{CE}}$ or $\overline{\text{WE}}$ asserting high terminates a write cycle.
- All write cycle timings are referenced from the last valid address to the first transitioning address. 11
- 12 Not applicable.
- 13 C = 30pF, except on High Z and Low Z parameters, where C = 5pF.

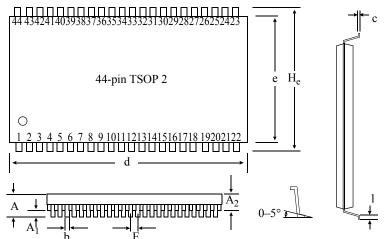


Typical DC and AC characteristics¹²

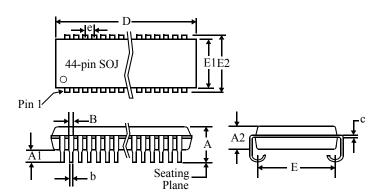




Package dimensions



	44-pin '	TSOP 2					
	Min (mm)	Max (mm)					
A		1.2					
$\mathbf{A_1}$	0.05	0.15					
A ₂	0.95	1.05					
b	0.30	0.45					
c	0.12	0.21					
d	18.31	18.52					
e	10.06	10.26					
H _e	11.68	11.94					
E	0.80 (typical)						
l	0.40	0.60					



	44-pin SO	J 400 mils
	Min(mils)	Max(mils)
A	0.128	0.148
A1	0.025	-
A2	0.105	0.115
В	0.026	0.032
b	0.015	0.020
c	0.007	0.013
D	1.120	1.130
E	0.370	NOM
E1	0.395	0.405
E2	0.435	0.445
e	0.050	NOM



Ordering Codes

Package	Version	10 ns	12 ns	15 ns	20 ns
	5V commercial	NA	AS7C4098-12JC	AS7C4098-15JC	AS7C4098-20JC
SOJ	5V industrial	NA	AS7C4098-12JI	AS7C4098-15JI	AS7C4098-20JI
503	3.3V commercial	AS7C34098-10JC	AS7C34098-12JC	AS7C34098-15JC	AS7C34098-20JC
	3.3V industrial	NA	AS7C34098-12JI	AS7C34098-15JI	AS7C34098-20JI
	5V commercial	NA	AS7C4098-12TC	AS7C4098-15TC	AS7C4098-20TC
TSOP 2	5V industrial	NA	AS7C4098-12TI	AS7C4098-15TI	AS7C4098-20TI
	3.3V commercial	AS7C34098-10TC	AS7C34098-12TC	AS7C34098-15TC	AS7C34098-20TC
	3.3V industrial	NA	AS7C34098-12TI	AS7C34098-15TI	AS7C34098-20TI

Note:

Add suffix "N" to the above part number for lead free devices, Ex. AS7C4098-12JCN

Part numbering system

AS7C	X	4098	-XX	J or T	X	N
SRAM prefix	Voltage: Blank: 5V CMOS 3: 3.3V CMOS	Device number	Access time	Packages: J: SOJ 400 mil T: TSOP 2	Temperature ranges: C: Commercial, 0°C to 70°C I: Industrial, –40°C to 85°C	Lead free device

1/13/05; **v.1.9**

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