CX28342/3/4/6/8

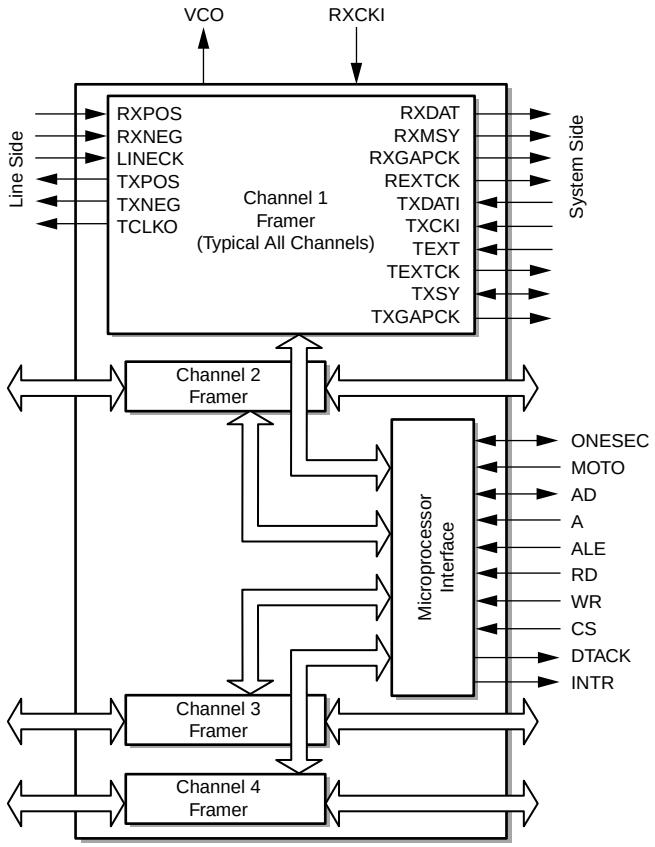
Dual/Triple/Quad/Hex/Octal-Enhanced DS3/E3 Framer

The CX28342/3/4/6/8 provides Dual, Triple, Quad, Hex, and Octal DS3/E3 framers designed to support DS3-M13, DS3-C-bit parity, E3-G.751, and E3-G.832 transmission formats.

The CX28342/3/4/6/8 provides framing recovery for M13, M23, C-bit parity, G.751, and G.832 formatted signals. A FIFO buffer in the receive path can be enabled to reduce jitter on the incoming data. The CX28342/3/4/6/8 devices allow for ease of configuration, while providing maximum flexibility to support the transmission and recovery of industry standard formats. It provides a flexible overhead bit generation method in DS3/E3 modes to source overhead bits on an individual framer.

NOTE: The index letter *i*, appearing in a register's name, represents the channel number, one per channel.

Functional Block Diagram



Distinguishing Features

- Two, three, four, six, eight independent T3/E3 framers in one package
- Line coding supported:
  - T3-B3ZS, NRZ, AMI
  - E3-HDB3, NRZ, AMI
- Framing supported:
  - T3-M13, M23, C-bit parity
  - E3-G.751, G.832
- Inserts and extracts overhead bits
- Full FEAC and TDL channels support
- Full Performance Monitoring support per T1.231
- Integrated Dejitter FIFO
- Glueless interfaces to the following processors:
  - Intel: 8051, 8151, 8031, 8751, 8x251
  - Motorola: 68000, 68020, 68030, 68302
- An asynchronous processor interface
- LIU Interfaces:
  - Glueless interface to Conexant's DS3/E3 LIU (CX2832/3)
  - Option for a definition of LIU's clocks polarity-sampling edge
- Power Supplies and Power Consumption
  - I/O 3.3 V, input 5 V-tolerant, core 2.5 V
  - Requires 3.3 V and 2.5 V power supplies. Optional 5 V supply required for 5 V input tolerance
  - Low power operation (<200 mW per port)

Applications

- Digital Cross-Connect Systems
- Digital PCM Switches
- Access Concentrators
- CSUs
- ATM Switches
- Concentrators
- PBXs
- Routers
- Test Equipment

Testing

- JTAG boundary scan support

Ordering Information

Model Numbe	Number of Frames	Package	Ambient Temperature Range
CX28342	2	144 pin ETQFP	–40 °C to 85 °C
CX28343	3	144 pin ETQFP	–40 °C to 85 °C
CX28344	4	144 pin ETQFP	–40 °C to 85 °C
CX28346	6	27 x 27 mm 318-ball PBGA	–40 °C to 85 °C
CX28348	8	27 x 27 mm 318-ball PBGA	–40 °C to 85 °C

Revision History

Revision	Level	Date	Description
A (Doc # 100542)	Advance	May 2000	Created
A *	—	September 2001	Added details on memory mapping for CX28346 and CX28348 devices. * Document number changed from 100542 to 500064A.
B	Preliminary	November 2001	Added jitter attenuator information.
C	Release	August 2002	Corrected Jitter attenuation information. Rolled up Errata, document #101317A.
A	Release	December 2002	Renumbered document to 28348-DSH-001-A
B	Release	February 2003	Revised section 2.2.5.5

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Tables

1.0 Product Description

1.1 Overview

The CX28342/3/4/6/8 device includes two, three, four, six, and eight identical framers that perform the following functions:

- Signal encoding and decoding
- Frame synchronization and recovery
- Alarm detection and generation
- Far End Alarm Control (FEAC) processing
- Data link processing
- Error and event counting
- Signal and frame generation

Each framer in the CX28342/CX28343/CX28344/CX28346/CX28348 device can be configured individually and is capable of operating at 44.736 Mbps in DS3 mode and 34.368 Mbps in E3 mode. Each framer is composed of a transmitter block and a receiver block. In addition, the CX28342/3/4/6/8 framer includes a microprocessor interface.

Data into the receiver can be in B3ZS/HDB3, AMI, or NRZ format. The B3ZS/HDB3 or AMI data is decoded and the bipolar input is converted to unipolar. The data can then be applied to a First In First Out (FIFO) buffer to reduce jitter on the incoming data. The FIFO buffer provides a Voltage Controlled Oscillator (VCO) control signal to an external clock recovery circuit. A dejittered clock (RXCKI) from the VCO can then be used to read data from the FIFO buffer going to the remaining receiver circuitry.

Each of the receiver blocks provides framing recovery for the M13/M23 DS3, C-bit Parity DS3, E3-G.751, and E3-G.832 formatted signals. The data bits are extracted from the received frame and transferred serially to the system. The transmitter can process serial data from an external pin. In addition, the transmitter can generate AIS/RAI/RDI and IDLE code. The transmitter also transmits the Link Access Direct (LAPD) data link data in HDLC format. The HDLC data is transmitted through a 128-byte FIFO buffer. The microprocessor can use the FIFO status for data transfer. The transmitter can transmit the FEAC channel data in several modes.

The microprocessor interface supports the Intel and Motorola microprocessors. The microprocessor is responsible for configuration, control, and monitoring of the framer. The framers have various event detectors, status indicators, and counters, which are readable by the microprocessor. The microprocessor interface includes (depending on the device) one (CX28342/3/4) or two (CX28346/8) interrupt pins that combine several sources of individually masked interrupts (i.e. the start and end of events, OOF, IDLE, AIS, and RAI/RDI). Status indicators that are available to the microprocessor through status registers are start of a Severely Errored Framing Event (SEF), Yellow Alarm (RAI, RDI), Alarm Indication Signal (AIS), Idle, Out of Frame (OOF), and Loss of Signal (LOS).

1.1.1 DS3 Mode

In DS3 mode, each of the receiver blocks provides framing recovery for DS3 M13/M23 and DS3 C-bit parity formatted signals. The receive signals can be in B3ZS, AMI, or NRZ format. The following events are detected and counted:

- P-bits
- CP-bits (DS3 C-bit parity only)
- FEBE (DS3 C-bit parity only)
- X-bit disagreement
- P-bit disagreement
- Framing Error
- Line Code Violation (LCV)
- Excessive Zeros (EXZ) in rail mode only

The C-bits in DS3 M13/M23 can be provided with the data or through an external pin. Overhead bits can be selectively provided through an external pin or internally generated. The transmitter can generate idle code and other alarm indication codes (AIS and RAI/RDI). In addition, the alarms generated in C-bit parity mode include FEBE and CP for performance monitoring.

Overhead bit can be selected for insertion with the data stream in this mode.

1.1.2 E3 Mode

In E3 mode, each receive block provides framing recovery for E3 G.751 and E3 G.832 formatted signals. The receive signals can be in HDB3, AMI, or NRZ format. The following events are detected and counted:

- BIP (G.832 only)
- REI (G.832)
- Framing Error
- Line Code Violation (LCV)
- Excessive Zeros (EXZ) in rail mode only

The Justification Control bits (Cj) in E3 G.751 can be provided with the data or through an external pin. Overhead bits can be selectively provided through an external pin or internally generated. The transmitter can also generate AIS and RAI/RDI signals. In addition, REI and BIP alarm bits in E3 G.832 format are generated for performance monitoring.

Overhead bit can be selected for insertion with the data stream in this mode. The detailed operation in each mode is described in Chapter 2.

1.2 Pin Descriptions (CX28342/3/4)

Pin descriptions for the CX28342, CX28343, and CX28344 devices are covered in the following paragraphs.

Figure 1-1 illustrates pin assignments for CX28342 dual framer. Figure 1-2 illustrates pin assignments for CX28343 triple framer. Figure 1-4 illustrates pin assignments for CX28344 quad framer.

NOTE: All input pins are 5 V-tolerant. See Table 1-1 for pin type definitions. See Tables 1-2 through 1-8 for pin descriptions.

Figure 1-1. CX28342 Pin Assignments

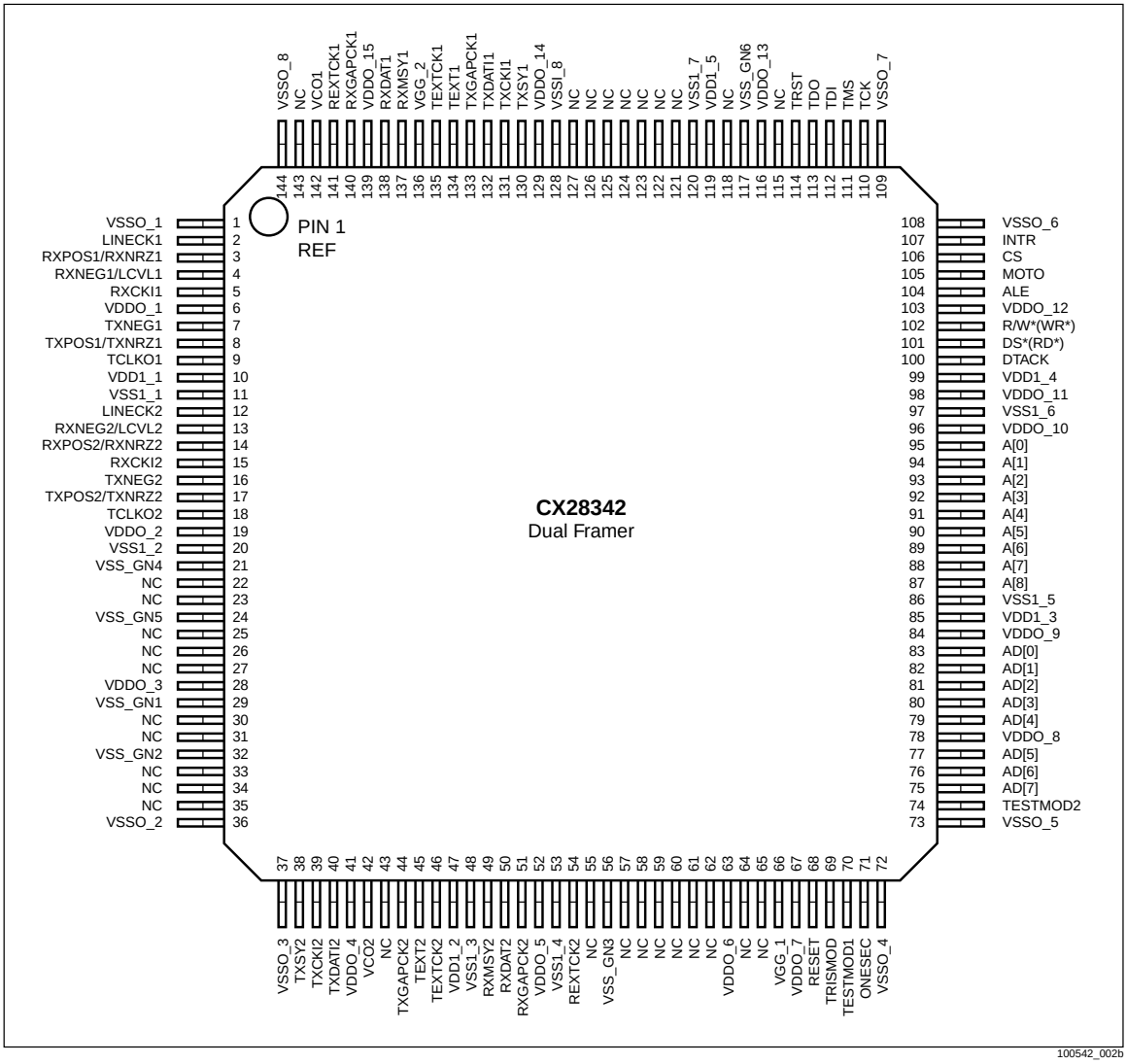


Figure 1-2. CX28343 Pin Assignments

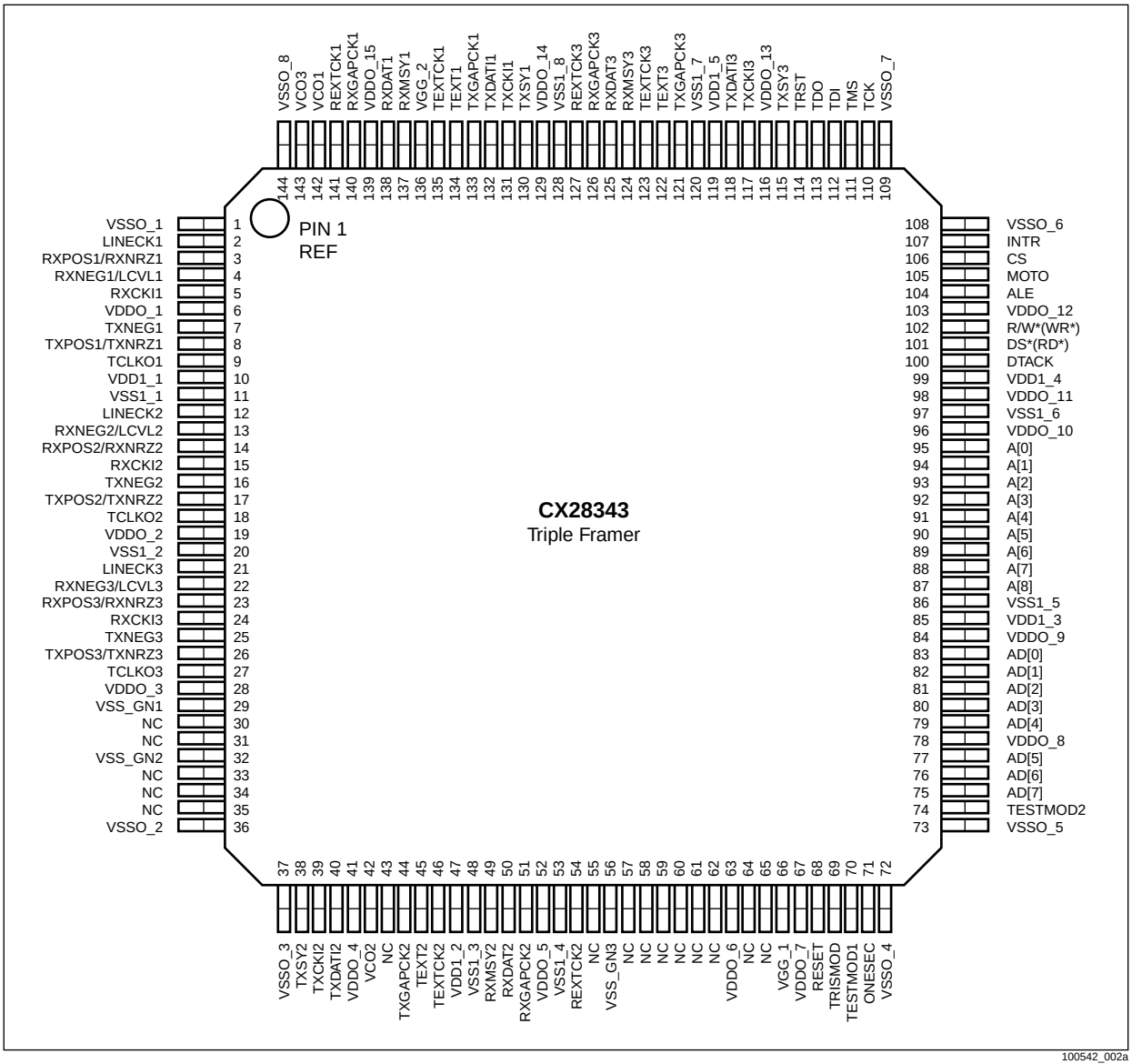


Figure 1-3. CX28344 Pin Assignments

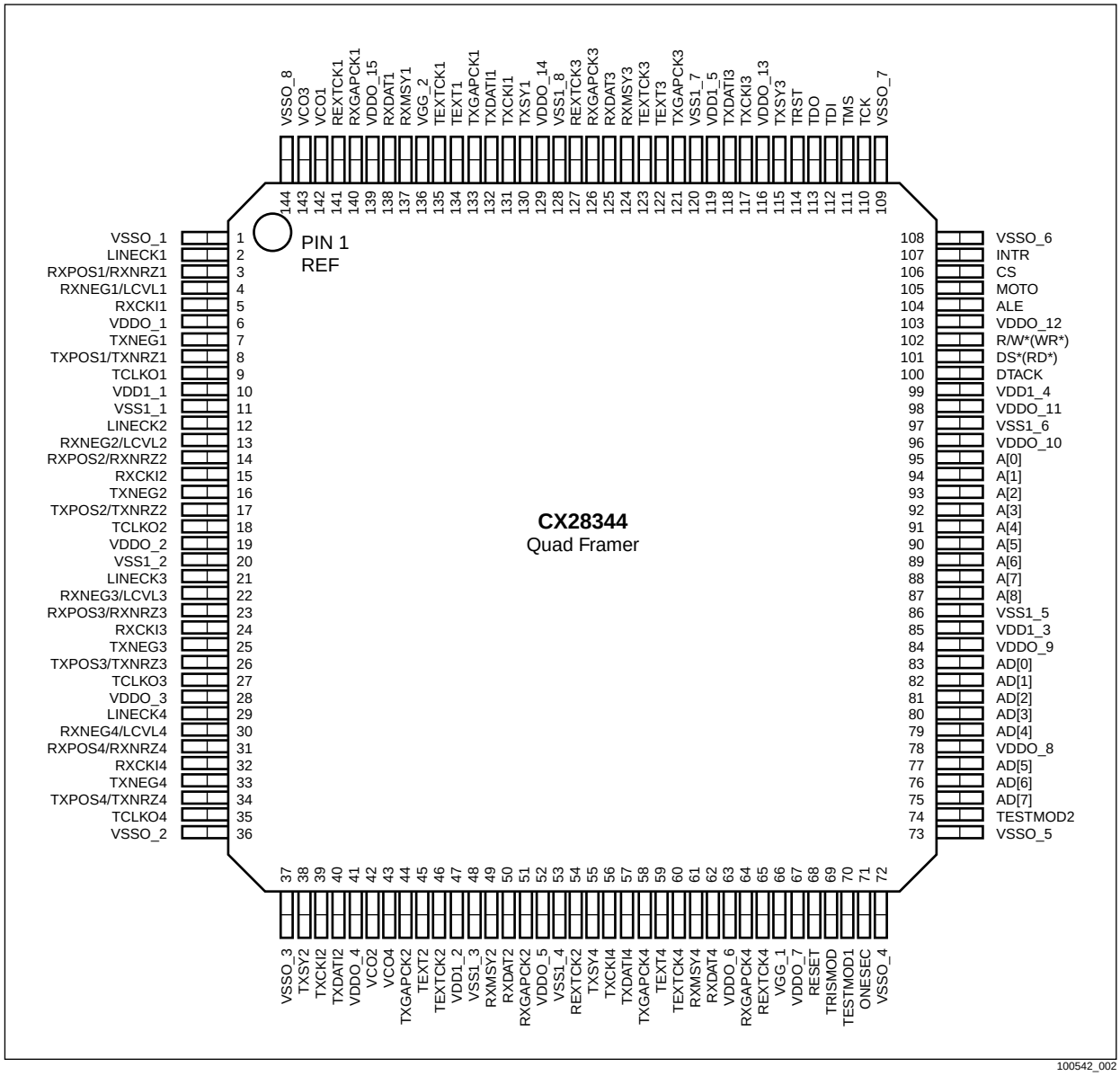


Table 1-1. Pin Type Definitions

Symbol	Name and Function
I	Input pin, CMOS levels, no internal termination
IPU	Input pin, CMOS levels, 75K internal pullup
IPD	Input pin, CMOS levels, 75K internal pulldown
O/Z	Three-state-capable CMOS output pin
IO	CMOS bidirectional pin
IOPD	CMOS programmable pin, 75K internal pulldown
IOZPU	Three-state capable CMOS programmable pin, 75K internal pullup
IOZPD	Three-state capable CMOS programmable pin, 75K internal pulldown
ODO	Open Drain Output, no internal pullup
PC	Digital power pin for core circuits
PI	Digital power pin for I/O pads
GC	Digital ground pin for core circuits
GI	Digital ground pin for I/O pads

Table 1-2. CX28342/3/4 Pins

Pin Label	CX28342 Pin #	CX28343 Pin #	CX28344 Pin #	Signal Name	I/O	Definition
RESET*	68	68	68	General reset	I	Resets all counters and registers to their default values (active low)(1).
VGG[1:2]	66, 136	66, 136	66, 136	Voltage supply	I	These pins must be connected to 5 V if 5 V input tolerance is required; if not, it must be connected to 3.3 V.
VDD1[1:5]	10, 47, 85, 99, 119	10, 47, 85, 99, 119	10, 47, 85, 99, 119	Core Supply Voltage	PC	The core is provided with 2.5 V using these pins. Note: Refer to Section 4, Power Ramp Sequence of VDDx and VDDOx.
VDDO[1:15]	6, 19, 28, 41, 52, 63, 67, 78, 84, 96, 98, 103, 116, 129, 139	6, 19, 28, 41, 52, 63, 67, 78, 84, 96, 98, 103, 116, 129, 139	6, 19, 28, 41, 52, 63, 67, 78, 84, 96, 98, 103, 116, 129, 139	Output Drivers Supply Voltage	PI	These pins must be connected to a 3.3 V power supply. Note: Refer to Section 4, Power Ramp Sequence of VDDx and VDDOx.
VSSO[1:8]	1, 36, 37, 72, 73, 108, 109, 144	1, 36, 37, 72, 73, 108, 109, 144	1, 36, 37, 72, 73, 108, 109, 144	Ground	GI	These are 3.3 V ground pins.
TRISMOD	69	69	69	Three-state Mode	IPD	Setting this pin high forces all the output/ inputs on the device to drive High Z, regardless of the state of the internal state machines, and the frame processing taking place at the same time. Setting this pin low enable the output/inputs to normal driving state.
VSS1[1:8]	11, 20, 48, 53, 86, 97, 120, 128	11, 20, 48, 53, 86, 97, 120, 128	11, 20, 48, 53, 86, 97, 120, 128	Ground	GC	These are 2.5 V ground pins.
VSS_GN[1:6]	21, 24, 29, 32, 56, 117	29, 32, 56	—	Ground	—	Must be connected to ground.
TESTMOD1	70	70	70	Test Mode 1	IPD	For Conexant use only. Must be connected to ground.
TESTMOD2	74	74	74	Test Mode 2	IPD	For Conexant use only. Must be connected to ground.
ONESEC	71	71	71	One-Second Timer	IOZPD	Controls or marks one-second interval used for counter latching. When input, the timer is aligned to ONESEC rising edge. When output, rising edge indicates start of each one-second interval. When output, derived from TXCKI1 clock of the first framer. The ONESEC pulse length is 16 clocks.

FOOTNOTE:
(1) During reset, TXCKI and LINECK (and RXCKI, if Rx dejitter FIFO buffer is to be used) clocks should be supplied for normal operation.

Table 1-3. Transmitter Section Line Side

Pin Label	CX28342 Pin #	CX28343 Pin #	CX28344 Pin #	Signal Name	I/O	Definition
TCLKO1	9	9	9	Framer 1 Transmit Clock Out	O/Z	Used to clock out the TXPOS/ TXNRZ and TXNEG outputs. Data is clocked out on the rising or on the falling edge of TCLKO according to settings of bit LTxCkRis at the Feature2(I) Control register.
TCLKO2	18	18	18	Framer 2 Transmit Clock Out	O/Z	
TCLKO3	—	27	27	Framer 3 Transmit Clock Out	O/Z	
TCLKO4	—	—	35	Framer 4 Transmit Clock Out	O/Z	
TXPOS1/ TXNRZ1	8	8	8	Framers 1 Transmit Positive/NRZ Output	O/Z	In rail mode or AMI mode, B3ZS/HDB3/AMI encoder generates the positive output. In unipolar mode, generates the NRZ output.
TXPOS2/ TXNRZ2	17	17	17	Framers 2 Transmit Positive/NRZ Output	O/Z	
TXPOS3/ TXNRZ3	—	26	26	Framers 3 Transmit Positive/NRZ Output	O/Z	
TXPOS4/ TXNRZ4	—	—	34	Framers 4 Transmit Positive/NRZ Output	O/Z	
TXNEG1	7	7	7	Framers 1 Transmit Negative Output	O/Z	In rail mode or AMI mode, B3ZS/HDB3/AMI encoder generates the negative output. In unipolar mode, not used.
TXNEG2	16	16	16	Framers 2 Transmit Negative Output	O/Z	
TXNEG3	—	25	25	Framers 3 Transmit Negative Output	O/Z	
TXNEG4	—	—	33	Framers 4 Transmit Negative Output	O/Z	

Table 1-4. Transmitter Section System Side (1 of 2)

Pin Label	CX28342 Pin #	CX28343 Pin #	CX28344 Pin #	Signal Name	I/O	Definition
TXDATI1	132	132	132	Framers 1 Transmit Serial Data Input	IPD	TXDATI is serial data input to framer transmitter. The serial data is sampled on the falling edge of TXCKI input clock.
TXDATI2	40	40	40	Framers 2 Transmit Serial Data Input	IPD	
TXDATI3	—	118	118	Framers 3 Transmit Serial Data Input	IPD	
TXDATI4	—	—	57	Framers 4 Transmit Serial Data Input	IPD	
TXSY1	130	130	130	Framers 1 Transmit Sync	IOZPD	Framer transmit frame synchronization indicator. The sync signal can be programmed to be generated internally (the pin used as output) or supplied from external circuit (the pin used as input). After reset, it has a high-Z value.
TXSY2	38	38	38	Framers 2 Transmit Sync	IOZPD	
TXSY3	—	115	115	Framers 3 Transmit Sync	IOZPD	
TXSY4	—	—	55	Framers 4 Transmit Sync	IOZPD	
TXCKI1	131	131	131	Framers 1 Transmit Clock In	I	Used to clock in serial data TXDATI in serial mode. The sync and data inputs are sampled on the falling edge. DS3 Mode Clock = 44.736 MHz E3-G.751/G.832 Mode Clock = 34.368 MHz
TXCKI2	39	39	39	Framers 2 Transmit Clock In	I	
TXCKI3	—	117	117	Framers 3 Transmit Clock In	I	
TXCKI4	—	—	56	Framers 4 Transmit Clock In	I	
TXGAPCK1	133	133	133	Framers 1 Transmit Gapped Clock	O/Z	A gapped clock is derived from the falling edge of TXCKI clock. It is gapped during Overhead bits that are not selected to be inserted with payload on TXDATI. Its polarity is programmable.
TXGAPCK2	44	44	44	Framers 2 Transmit Gapped Clock	O/Z	
TXGAPCK3	—	121	121	Framers 3 Transmit Gapped Clock	O/Z	
TXGAPCK4	—	—	58	Framers 4 Transmit Gapped Clock	O/Z	

Table 1-4. Transmitter Section System Side (2 of 2)

Pin Label	CX28342 Pin #	CX28343 Pin #	CX28344 Pin #	Signal Name	I/O	Definition
TEXT1	134	134	134	Framers 1 Transmit External Overhead Bit In	IPD	Transmit external Overhead bits input. The Overhead bit groups to be inserted through this pin are programmable. The options for each mode of operation are specified in Section 2.1.1
TEXT2	45	45	45	Framers 2 Transmit External Overhead Bit In	IPD	
TEXT3	—	122	122	Framers 3 Transmit External Overhead Bit In	IPD	
TEXT4	—	—	59	Framers 4 Transmit External Overhead Bit In	IPD	
TEXTCK1	135	135	135	Framers 1 Transmit External Overhead Bit Clock	O/Z	Used to indicate to the system when to insert a new Overhead bit on TEXT pin. This output has a clock pulse for each position of Overhead bits (for the specific DS3/E3 mode) that were chosen to be inserted through TEXT pin. Its behavior is specified in Section 2.1.1.
TEXTCK2	46	46	46	Framers 2 Transmit External Overhead Bit Clock	O/Z	
TEXTCK3	—	123	123	Framers 3 Transmit External Overhead Bit Clock	O/Z	
TEXTCK4	—	—	60	Framers 4 Transmit External Overhead Bit Clock	O/Z	

Table 1-5. Receiver Section Line Side (1 of 2)

Pin Label	CX28342 Pin #	CX28343 Pin #	CX28344 Pin #	Signal Name	I/O	Definition
LINECK1	2	2	2	Framers 1 Receive Line Clock In	I	Line clock input should be connected to a 44.736 MHz source in DS3 mode or to a 34.368 MHz source in E3 mode, derived from incoming receive data.
LINECK2	12	12	12	Framers 2 Receive Line Clock In	I	
LINECK3	—	21	21	Framers 3 Receive Line Clock In	I	
LINECK4	—	—	29	Framers 4 Receive Line Clock In	I	
RXPOS1/ RXNRZ1	3	3	3	Framers 1 Receive Positive/NRZ Input	IPD	In rail mode and in AMI mode, it is the positive data input. In unipolar mode it is the NRZ data input. Sampled on the rising/falling (programmable) edge of the receiver input clock (LINECK).
RXPOS2/ RXNRZ2	14	14	14	Framers 2 Receive Positive/NRZ Input	IPD	
RXPOS3/ RXNRZ3	—	23	23	Framers 3 Receive Positive/NRZ Input	IPD	
RXPOS4/ RXNRZ4	—	—	31	Framers 4 Receive Positive/NRZ Input	IPD	
RXNEG1/ LCVI1	4	4	4	Framers 1 Receive Negative/Line Code Violation Input	IPD	In rail mode and in AMI mode, it is the negative data input. In unipolar mode, it is the line code violation input for LCV counting (if unused tie low). Sampled on the rising/falling (programmable) edge of the receiver input clock (LINECK).
RXNEG2/ LCVI2	13	13	13	Framers 2 Receive Negative/Line Code Violation Input	IPD	
RXNEG3/ LCVI3	—	22	22	Framers 3 Receive Negative/Line Code Violation Input	IPD	
RXNEG4/ LCVI4	—	—	30	Framers 4 Receive Negative/Line Code Violation Input	IPD	

Table 1-5. Receiver Section Line Side (2 of 2)

Pin Label	CX28342 Pin #	CX28343 Pin #	CX28344 Pin #	Signal Name	I/O	Definition
RXCKI1	5	5	5	Framers 1 Receive Dejittered Clock In	I	Used to read the received data out of the internal clock dejitter FIFO buffer (if unused, tie to ground).
RXCKI2	15	15	15	Framers 2 Receive Dejittered Clock In	I	
RXCKI3	—	24	24	Framers 3 Receive Dejittered Clock In	I	
RXCKI4	—	—	32	Framers 4 Receive Dejittered Clock In	I	
VCO1	142	142	142	Framers 1 Phase Detector Output	O/Z	Used as the phase detector for the clock recovery circuit that generates dejittered clock, RXCKI. Valid only when framer dejitter FIFO buffer is enabled.
VCO2	42	42	42	Framers 1 Phase Detector Output	O/Z	
VCO3	—	143	143	Framers 1 Phase Detector Output	O/Z	
VCO4	—	—	43	Framers 1 Phase Detector Output	O/Z	

Table 1-6. Receiver Section System Side (1 of 2)

Pin Label	CX28342 Pin #	CX28343 Pin #	CX28344 Pin #	Signal Name	I/O	Definition
RXMSY1	137	137	137	Framers 1 Receive Sync	O/Z	The frame synchronization output of framer recovered from the incoming serial data stream.
RXMSY2	49	49	49	Framers 2 Receive Sync	O/Z	
RXMSY3	—	124	124	Framers 3 Receive Sync	O/Z	
RXMSY4	—	—	61	Framers 4 Receive Sync	O/Z	
RXGAPCK1	140	140	140	Framers 1 Receive Gapped Clock	O/Z	It is a gapped clock signal output that is used to indicate RXDAT serial data output. RXGAPCK clock polarity and behavior are programmable and have several options (see Section 2.2).
RXGAPCK2	51	51	51	Framers 2 Receive Gapped Clock	O/Z	
RXGAPCK3	—	126	126	Framers 3 Receive Gapped Clock	O/Z	
RXGAPCK4	—	—	64	Framers 4 Receive Gapped Clock	O/Z	
REXTCK1	141	141	141	Framer 1 Receive Overhead Clock Output	O/Z	Used to indicate chosen Overhead bits that output on RXDAT. This output has a clock pulse for each position of the chosen group of Overhead bits for the specific DS3/E3 mode. Its polarity is programmable.
REXTCK2	54	54	54	Framer 2 Receive Overhead Clock Output	O/Z	
REXTCK3	—	127	127	Framer 3 Receive Overhead Clock Output	O/Z	
REXTCK4	—	—	65	Framer 4 Receive Overhead Clock Output	O/Z	

Table 1-6. Receiver Section System Side (2 of 2)

Pin Label	CX28342 Pin #	CX28343 Pin #	CX28344 Pin #	Signal Name	I/O	Definition
RXDAT1	138	138	138	Framers 1 Receive Serial Data Output	O/Z	This pin is the serial data bit stream of framer. Data is clocked out on the rising edge of receive internal clock.
RXDAT2	50	50	50	Framers 2 Receive Serial Data Output	O/Z	
RXDAT3	—	125	125	Framers 3 Receive Serial Data Output	O/Z	
RXDAT4	—	—	62	Framers 4 Receive Serial Data Output	O/Z	

Table 1-7. Microprocessor Interface

Pin Label	CX28342 Pin #	CX28343 Pin #	CX28344 Pin #	Signal Name	I/O	Definition
MOTO*	105	105	105	Motorola Bus Mode	I	Selects Intel- or Motorola-style microprocessor interface. DS*, R/W*, A[8:0], and AD[7:0] functions are affected. 0 = Motorola; AD[7:0] is data, A[8:0] is address, DS* is data strobe, and R/W* indicates read (high) or write (low) data direction. 1 = Intel; AD[7:0] is multiplexed address/data, A[7:0] is ignored, A[8] is address, DS* is read strobe (RD*), and R/W* is write strobe (WR*).
A[8:0]	87–95	87–95	87–95	Address Bus	IPD	Address used to identify a register for subsequent read/write data transfer cycle. In Motorola bus mode, all nine address bits (A[8:0]) are valid. In Intel bus mode, only the upper bit (A[8]) is used.
AD[7:0]	75–77, 79-83	75–77, 79-83	75–77, 79-83	Data Bus or Address/Data	IOPD	Multiplexed address/data (Intel) or data only (Motorola). Refer to MOTO* definition.
ALE	104	104	104	Address Strobe	I	For Intel bus mode only, ALE falling edge asynchronously latches address from A[8:0] (Motorola) or A[8]+AD[7:0] (Intel) to identify one register for subsequent read/write data transfer cycle.
CS*	106	106	106	Chip Select	I	Active low enables read/write decoder. Active high ends current read or write cycle and places data bus output in high impedance.
DS*(RD*)	101	101	101	Data Strobe or Read Strobe	I	Active low read data strobe (RD*) for MOTO* = 1, or data strobe (DS*) for MOTO* = 0.
R/W*(WR*)	102	102	102	Read/Write Direction or Write Strobe	I	Active low write data strobe (WR*) for MOTO* = 1, or data select (R/W*) for MOTO* = 0.
INTR*	107	107	107	Interrupt Request	O/Z	Open drain active low output signifies one or more pending interrupt requests. INTR goes to high impedance state.
DTACK*	100	100	100	Data Transfer Acknowledge	O/Z	Open drain active low output signifies in-progress data transfer cycle. Data ready indication for read, transaction end indication for write

Table 1-8. JTAG Interface

Pin Label	CX28342 Pin #	CX28343 Pin #	CX28344 Pin #	Signal Name	I/O	Definition
TRST*	114	114	114	Test Reset	IPU	When this pin is asserted, the internal boundary-scan logic is reset. This pin has a pull-up resistor.
TCK	110	110	110	Test Clock	IPU	Samples the value of TMS and TDI on its rising edge to control the boundary scan operations (input clock).
TMS	111	111	111	Test Mode Select	IPU	Controls the boundary-scan Test Access Port (TAP) controller operation. This pin has a pull-up resistor.
TDI	112	112	112	Test Data Input	IPU	The serial test data input. This pin has a pull-up resistor.
TDO	113	113	113	Test Data Output	O/Z	The serial test data output.
NC	22, 23, 25, 26, 27, 30, 31, 33, 34, 35, 43, 55, 57–62, 64, 65, 115, 118, 121–127, 143	30, 31, 33–35, 43, 55, 57–62, 64, 65	—	No Connect	—	Pins are not internally bonded.

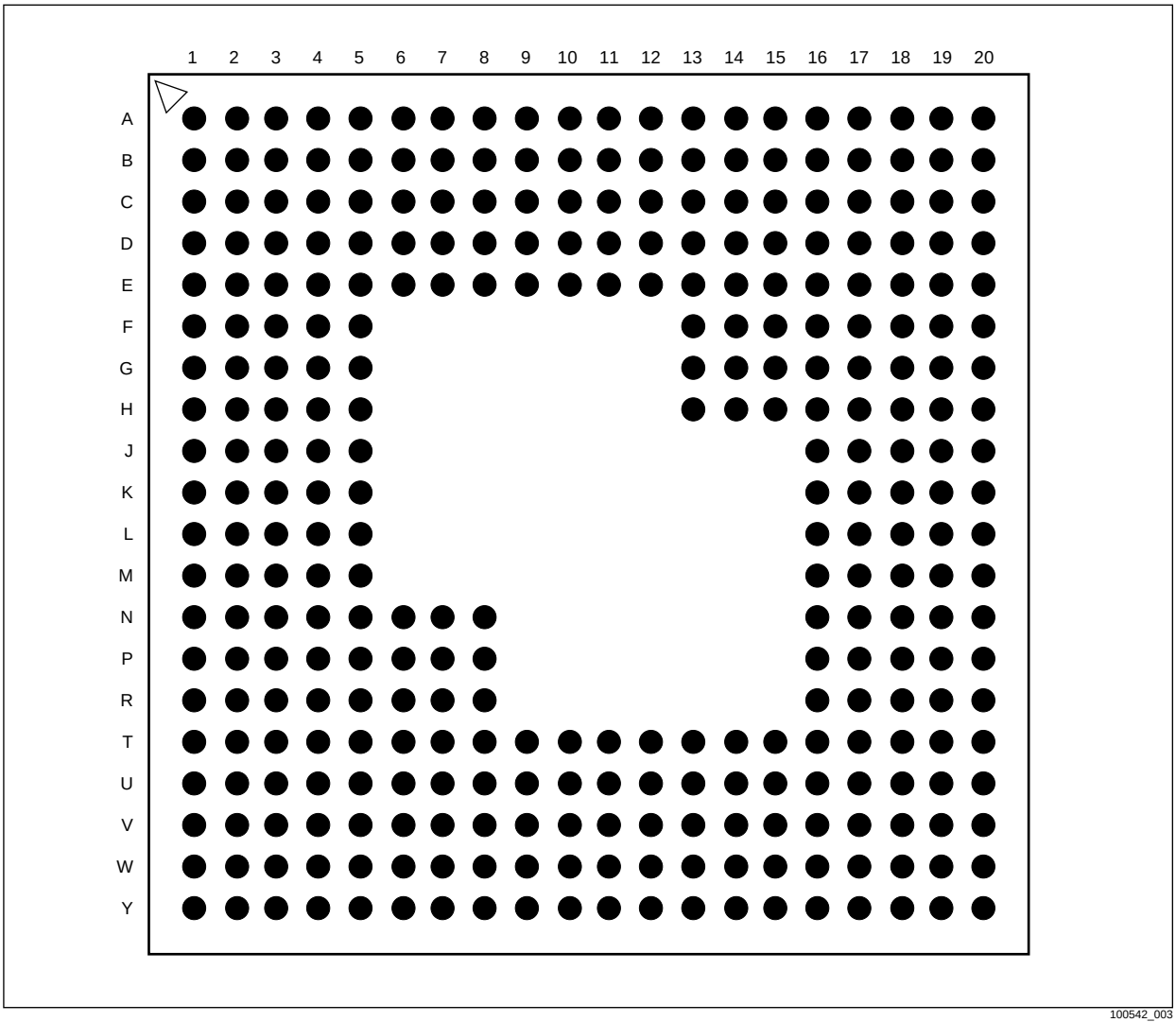
1.3 Pin Descriptions (CX28346/8)

Pin descriptions for the CX28346 (Hex), CX28348 (Octal) devices are covered in the following paragraphs.

Figure 1-4 illustrates pin assignments for the CX28346/CX28348 framer.

NOTE: All inputs are 5 V-tolerant. See Table 1-1 for pin type definitions. See Tables 1-11 through 1-17 for pin descriptions.

Figure 1-4. CX28346/8 Pin Assignments (Top View)



The CX28346 and CX28348 devices are multi-chip modules consisting of two die on a common substrate and distributed as indicated in Table 1-9. Access to the framers is accomplished by the assertion of Chip Selects CS[A]* and CS[B]*.

Table 1-9. Framer Distribution

Framer Distribution		
Device	**A Framers**	**B Framers**
CX28346	1–4	5–6
CX28348	1–4	5–8

In addition to the chip selects, Table 1-10 shows the framer/pin relationship. For a detailed description of the individual pins, see Section 1.3, and Tables 1-11, 1-16, and 1-17.

Table 1-10. Pin Distribution

Pin Distribution			
A Framers		**B Framers**	
Label	**Pin**	**Label**	**Pin**
ONESEC[A]	B5	ONESEC[B]	W16
VGG_[A]	A5	VGG_[B]	Y16
VGG_[A]	M19	VGG_[B]	J2
TRISMOD[A]	B6	TRISMOD[B]	W15
TESTMOD1[RESV_A]	A4	TESTMOD1[RESV_B]	Y17
TESTMOD2[RESV_A]	A3	TESTMOD2[RESV_B}	Y18
CS[A]*	H13	CS[B]*	N8
INTR[A]*	G14	INTR[B]*	P7
TRST[A]*	V20	TRST[B]*	C1
TMS[A]	V17	TMS[B]	C4
TDI[A]	V18	TDI[B]	C3
TDO[A]	V19	TDO[B]	C2
TCK[A]	V16	TCK[B]	C5

Table 1-11. CX28346 and CX28348 General Pins (1 of 2)

Pin Label	CX28346 Pin # Hex Ball Assign	CX28348 Pin # Octal Ball Assign	I/O	Signal Name	Definition
ONESEC[A]	B5	B5	IOZPD	One Sec Timer	Controls or marks one-second interval used for counter latching. When input, the timer is aligned to ONESEC rising edge. When output, rising edge indicates start of each one-second interval. When output, derived from TXCKI1 clock of the first framer. The ONESEC pulse length is 16 clocks.
ONESEC[B]	W16	W16	IOZPD	—	
VGG_[A]1	A5	A5	PI	Voltage Supply	These pins must be connected to 5 V if 5 V input tolerance is required; if not, it must be connected to 3.3 V.
VGG_[A]2	M19	M19	P I	—	
VGG_[B]1	Y16	Y16	PI	—	
VGG_[B]2	J2	J2	PI	—	
RESET*	E12	E12	I	Reset	Resets all counters and registers to their default values (active low).
TRISMOD[A]	B6	B6	IPD	Tri-State Mod	Setting this pin high forces all the output/inputs on the device to drive High Z, regardless of the state of the internal state machines, and the frame processing taking place at the same time. Setting this pin low enable the output/inputs to normal driving state.
TRISMOD[B]	W15	W15	IPD	—	
TESTMOD1[RESV_A]	A4	A4	IPD	Test Mode Resv	For Conexant use only. Must be connected to ground.
TESTMOD2[RESV_A]	A3	A3	IPD	—	
TESTMOD1[RESV_B]	Y17	Y17	IPD	—	
TESTMOD2[RESV_B]	Y18	Y18	IPD	—	
VDD1_4	C6, C7, C16, F14, H18, N3, T9, V5, V13, V14	C6, C7, C16, F14, H18, N3, T9, V5, V13, V14	PC	Core Supply Voltage	The core is provided with 2.5 V using these pins. Note: Refer to Section 4, Power Ramp Sequence of VDDx and VDDOx.
VDDO_9	B2, B8, B19, C15, D13, E16, F18, J16, J17, M4, M5, R3, T4, U8, V6, V8, V9, W2, W11, W12, W17, W18	B2, B8, B19, C15, D13, E16, F18, J16, J17, M4, M5, R3, T4, U8, V6, V8, V9, W2, W11, W12, W17, W18	PI	Output Drivers Supply	These pins should be connected to a 3.3 V power supply. Note: Refer to Section 4, Power Ramp Sequence of VDDx and VDDOx.

Table 1-11. CX28346 and CX28348 General Pins (2 of 2)

Pin Label	CX28346 Pin # Hex Ball Assign	CX28348 Pin # Octal Ball Assign	I/O	Signal Name	Definition
VSS	A1, A2, A6, A9, A10, B1, B3, B4, B9, B10, C8, C9, C10, C11, C12, C13, C14, D3, D5, D6, D7, D8, D9, D10, D11, D12, D14, D15, D16, E1, E2, E3, E4, E13, E14, E15, E17, F4, F13, F15, F16, G1, G2, G4, G13, G15, H15, H16, J4, K16, L5, M17, N5, N6, P6, P8, P16, P17, P19, P20, R5, R6, R7, R8, R17, T5, T6, T7, T8, T17, T18, T19, T20, U5, U6, U7, U9, U10, U16, U18, V10, V11, V12, V15, W13, W19, W20, Y6, Y11, Y12, Y15, Y19, Y20	A1, A2, A6, A9, A10, B1, B3, B4, B9, B10, C8, C9, C10, C11, C12, C13, C14, D3, D5, D6, D7, D8, D9, D10, D11, D12, D14, D15, D16, E1, E2, E3, E4, E13, E14, E15, E17, F4, F13, F15, F16, G1, G2, G4, G13 G15, H15, H16, J4, K16, L5, M17, N5, N6, P6, P8, P16, P17, P19, P20, R5, R6, R7, R8, R17, T5, T6, T7, T8, T17, T18, T19, T20, U5, U6, U7, U9, U10, U16, U18, V10, V11, V12, V15, W13, W19, W20, Y6, Y11, Y12, Y15, Y19, Y20	I	Ground	Must be connected to ground.

Table 1-12. Transmitter Section Line Side (1 of 2)

Pin Label	CX28346 Pin #	CX28348 Pin #	I/O	Signal Name	Definition
TCLKO1	H17	H17	O/Z	Framer 1 Transmit Clock Out	Used to clock out the TXPOS/ TXNRZ and TXNEG outputs. Data is clocked out on the rising or on the falling edge of TCLKO according to settings of bit LTxCkRis at the Feature2(I) Control register.
TCLKO2	G16	G16	O/Z	Framer 2 Transmit Clock Out	
TCLKO3	E18	E18	O/Z	Framer 3 Transmit Clock Out	
TCLKO4	D17	D17	O/Z	Framer 4 Transmit Clock Out	
TCLKO5	N4	N4	O/Z	Framer 5 Transmit Clock Out	
TCLKO6	P5	P5	O/Z	Framer 6 Transmit Clock Out	
TCLKO7	—	T3	O/Z	Framer 7 Transmit Clock Out	
TCLKO8	—	U4	O/Z	Framer 8 Transmit Clock Out	
TXPOS1/ TXNRZ1	J20	J20	O/Z	Framers 1 Transmit Positive/NRZ Output	In rail mode or AMI mode, B3ZS/ HDB3/AMI encoder generates the positive output. In unipolar mode, generates the NRZ output.
TXPOS2/ TXNRZ2	G18	G18	O/Z	Framers 2 Transmit Positive/NRZ Output	
TXPOS3/ TXNRZ3	E19	E19	O/Z	Framers 3 Transmit Positive/NRZ Output	
TXPOS4/ TXNRZ4	C19	C19	O/Z	Framers 4 Transmit Positive/NRZ Output	
TXPOS5/ TXNRZ5	M1	M1	O/Z	Framers 5 Transmit Positive/NRZ Output	
TXPOS6/ TXNRZ6	P3	P3	O/Z	Framers 6 Transmit Positive/NRZ Output	
TXPOS7/ TXNRZ7	—	T2	O/Z	Framers 7 Transmit Positive/NRZ Output	
TXPOS8/ TXNRZ8	—	V2	O/Z	Framers 8 Transmit Positive/NRZ Output	

Table 1-12. Transmitter Section Line Side (2 of 2)

Pin Label	CX28346 Pin #	CX28348 Pin #	I/O	Signal Name	Definition
TXNEG1	J19	J19	O/Z	Framers 1 Transmit Negative Output	In rail mode or AMI mode, B3ZS/HDB3/AMI encoder generates the negative output. In unipolar mode, not used.
TXNEG2	G17	G17	O/Z	Framers 2 Transmit Negative Output	
TXNEG3	E20	E20	O/Z	Framers 3 Transmit Negative Output	
TXNEG4	B18	B18	O/Z	Framers 4 Transmit Negative Output	
TXNEG5	M2	M2	O/Z	Framers 5 Transmit Negative Output	
TXNEG6	P4	P4	O/Z	Framers 6 Transmit Negative Output	
TXNEG7	—	T1	O/Z	Framers 7 Transmit Negative Output	
TXNEG8	—	W3	O/Z	Framers 8 Transmit Negative Output	

Table 1-13. Transmitter Section System Side (1 of 4)

Pin Label	CX28346 Pin #	CX28348 Pin #	I/O	Signal Name	Definition
TXDATI1	R19	R19	IPD	Framers 1 Transmit Serial Data Input	TXDATI is serial data input to framer transmitter. The serial data is sampled on the falling edge of TXCKI input clock.
TXDATI2	A19	A19	IPD	Framers 2 Transmit Serial Data Input	
TXDATI3	U19	U19	IPD	Framers 3 Transmit Serial Data Input	
TXDATI4	A11	A11	IPD	Framers 4 Transmit Serial Data Input	
TXDATI5	F2	F2	IPD	Framers 5 Transmit Serial Data Input	
TXDATI6	Y2	Y2	IPD	Framers 6 Transmit Serial Data Input	
TXDATI7	—	D2	IPD	Framers 7 Transmit Serial Data Input	
TXDATI8	—	Y10	IPD	Framers 8 Transmit Serial Data Input	
TXSY1	R18	R18	IOZPD	Framers 1 Transmit Sync	Framer transmit frame synchronization indicator. The sync signal can be programmed to be generated internally (the pin used as output) or supplied from external circuit (the pin used as input). After reset, it has a high-Z value.
TXSY2	A20	A20	IOZPD	Framers 2 Transmit Sync	
TXSY3	U17	U17	IOZPD	Framers 3 Transmit Sync	
TXSY4	A12	A12	IOZPD	Framers 4 Transmit Sync	
TXSY5	F3	F3	IOZPD	Framers 5 Transmit Sync	
TXSY6	Y1	Y1	IOZPD	Framers 6 Transmit Sync	
TXSY7	—	D4	IOZPD	Framers 7 Transmit Sync	
TXSY8	—	Y9	IOZPD	Framers 8 Transmit Sync	

Table 1-13. Transmitter Section System Side (2 of 4)

Pin Label	CX28346 Pin #	CX28348 Pin #	I/O	Signal Name	Definition
TXCKI1	L16	L16	I	Framers 1 Transmit Clock In	Used to clock in serial data TXDATI in serial mode. The sync and data inputs are sampled on the falling edge. DS3 Mode Clock = 44.736 MHz E3-G.751/G.832 Mode Clock = 34.368 MHz
TXCKI2	C18	C18	I	Framers 2 Transmit Clock In	
TXCKI3	H14	H14	I	Framers 3 Transmit Clock In	
TXCKI4	B15	B15	I	Framers 4 Transmit Clock In	
TXCKI5	K5	K5	I	Framers 5 Transmit Clock In	
TXCKI6	V3	V3	I	Framers 6 Transmit Clock In	
TXCKI7	—	N7	I	Framers 7 Transmit Clock In	
TXCKI8	—	V7	I	Framers 8 Transmit Clock In	
TXGAPCK1	L17	L17	O/Z	Framers 1 Transmit Gapped Clock	A gapped clock is derived from the falling edge of TXCKI clock. It is gapped during Overhead bits that are not selected to be inserted with payload on TXDATI. Its polarity is programmable.
TXGAPCK2	A17	A17	O/Z	Framers 2 Transmit Gapped Clock	
TXGAPCK3	N16	N16	O/Z	Framers 3 Transmit Gapped Clock	
TXGAPCK4	B14	B14	O/Z	Framers 4 Transmit Gapped Clock	
TXGAPCK5	K4	K4	O/Z	Framers 5 Transmit Gapped Clock	
TXGAPCK6	Y4	Y4	O/Z	Framers 6 Transmit Gapped Clock	
TXGAPCK7	—	H5	O/Z	Framers 7 Transmit Gapped Clock	
TXGAPCK8	—	W7	O/Z	Framers 8 Transmit Gapped Clock	

Table 1-13. Transmitter Section System Side (3 of 4)

Pin Label	CX28346 Pin #	CX28348 Pin #	I/O	Signal Name	Definition
TEXT1	L18	L18	IPD	Framers 1 Transmit External Overhead Bit In	Transmit external Overhead bits input. The Overhead bit groups to be inserted through this pin are programmable. The options for each mode of operation are specified in Section 2.1.1.
TEXT2	B16	B16	IPD	Framers 2 Transmit External Overhead Bit In	
TEXT3	U20	U20	IPD	Framers 3 Transmit External Overhead Bit In	
TEXT4	A8	A8	IPD	Framers 4 Transmit External Overhead Bit In	
TEXT5	K3	K3	IPD	Framers 5 Transmit External Overhead Bit In	
TEXT6	W5	W5	IPD	Framers 6 Transmit External Overhead Bit In	
TEXT7	—	D1	IPD	Framers 7 Transmit External Overhead Bit In	
TEXT8	—	Y13	IPD	Framers 8 Transmit External Overhead Bit In	

Table 1-13. Transmitter Section System Side (4 of 4)

Pin Label	CX28346 Pin #	CX28348 Pin #	I/O	Signal Name	Definition
TEXTCK1	L19	L19	O/Z	Framers 1 Transmit External Overhead Bit Clock	Used to indicate to the system when to insert a new Overhead bit on TEXT pin. This output has a clock pulse for each position of Overhead bits (for the specific DS3/E3 mode) that were chosen to be inserted through TEXT pin. Its behavior is specified in Section 2.1.1.
TEXTCK2	C17	C17	O/Z	Framers 2 Transmit External Overhead Bit Clock	
TEXTCK3	N17	N17	O/Z	Framers 3 Transmit External Overhead Bit Clock	
TEXTCK4	B13	B13	O/Z	Framers 4 Transmit External Overhead Bit Clock	
TEXTCK5	K2	K2	O/Z	Framers 5 Transmit External Overhead Bit Clock	
TEXTCK6	V4	V4	O/Z	Framers 6 Transmit External Overhead Bit Clock	
TEXTCK7	—	H4	O/Z	Framers 7 Transmit External Overhead Bit Clock	
TEXTCK8	—	W8	O/Z	Framers 8 Transmit External Overhead Bit Clock	

Table 1-14. Receiver Section Line Side (1 of 3)

Pin Label	CX28346 Pin #	CX28348 Pin #	I/O	Signal Name	Definition
LINECK1	K18	K18	I	Framer 1 Receive Line Clock In	Line clock input should be connected to a 44.736 MHz source in DS3 mode or to a 34.368 MHz source in E3 mode, derived from incoming receive data.
LINECK2	H19	H19	I	Framer 2 Receive Line Clock In	
LINECK3	F17	F17	I	Framer 3 Receive Line Clock In	
LINECK4	C20	C20	I	Framer 4 Receive Line Clock In	
LINECK5	L3	L3	I	Framer 5 Receive Line Clock In	
LINECK6	N2	N2	I	Framer 6 Receive Line Clock In	
LINECK7	—	R4	I	Framer 7 Receive Line Clock In	
LINECK8	—	V1	I	Framer 8 Receive Line Clock In	
RXPOS1/RXNRZ1	L20	L20	IPD	Framers 1 Receive Positive/NRZ Input	In rail mode and in AMI mode, it is the positive data input. In unipolar mode it is the NRZ data input. Sampled on the rising/falling (programmable) edge of the receiver input clock (LINECK).
RXPOS2/RXNRZ2	G20	G20	IPD	Framers 2 Receive Positive/NRZ Input	
RXPOS3/RXNRZ3	F19	F19	IPD	Framers 3 Receive Positive/NRZ Input	
RXPOS4/RXNRZ4	D19	D19	IPD	Framers 4 Receive Positive/NRZ Input	
RXPOS5/RXNRZ5	K1	K1	IPD	Framers 5 Receive Positive/NRZ Input	
RXPOS6/RXNRZ6	P1	P1	IPD	Framers 6 Receive Positive/NRZ Input	
RXPOS7/RXNRZ7	—	R2	IPD	Framers 7 Receive Positive/NRZ Input	
RXPOS8/RXNRZ8	—	U2	IPD	Framers 8 Receive Positive/NRZ Input	

Table 1-14. Receiver Section Line Side (2 of 3)

Pin Label	CX28346 Pin #	CX28348 Pin #	I/O	Signal Name	Definition
RXNEG1/LCVL1	K20	K20	IPD	Framers 1 Receive Negative/Line Code Violation Input	In rail mode and in AMI mode, it is the negative data input. In unipolar mode, it is the line code violation input for LCV counting (if unused tie low). Sampled on the rising/falling (programmable) edge of the receiver input clock (LINECK).
RXNEG2/LCVL2	H20	H20	IPD	Framers 2 Receive Negative/Line Code Violation Input	
RXNEG3/LCVL3	F20	F20	IPD	Framers 3 Receive Negative/Line Code Violation Input	
RXNEG4/LCVL4	B20	B20	IPD	Framers 4 Receive Negative/Line Code Violation Input	
RXNEG5/LCVL5	L1	L1	IPD	Framers 5 Receive Negative/Line Code Violation Input	
RXNEG6/LCVL6	N1	N1	IPD	Framers 6 Receive Negative/Line Code Violation Input	
RXNEG7/LCVL7	—	R1	IPD	Framers 7 Receive Negative/Line Code Violation Input	
RXNEG8/LCVL8	—	W1	IPD	Framers 8 Receive Negative/Line Code Violation Input	

Table 1-14. Receiver Section Line Side (3 of 3)

Pin Label	CX28346 Pin #	CX28348 Pin #	I/O	Signal Name	Definition
RXCKI1	J18	J18	I	Framers 1 Receive Dejittered Clock In	Used to read the received data out of the internal clock dejitter FIFO buffer (if unused, tie to ground).
RXCKI2	G19	G19	I	Framers 2 Receive Dejittered Clock In	
RXCKI3	D20	D20	I	Framers 3 Receive Dejittered Clock In	
RXCKI4	D18	D18	I	Framers 4 Receive Dejittered Clock In	
RXCKI5	M3	M3	I	Framers 5 Receive Dejittered Clock In	
RXCKI6	P2	P2	I	Framers 6 Receive Dejittered Clock In	
RXCKI7	—	U1	I	Framers 7 Receive Dejittered Clock In	
RXCKI8	—	U3	I	Framers 8 Receive Dejittered Clock In	
VCO1	N20	N20	O/Z	Framers 1 Phase Detector Output	Used as the phase detector for the clock recovery circuit that generates dejittered clock, RXCKI. Valid only when framer dejitter FIFO buffer is enabled.
VCO2	A18	A18	O/Z	Framers 2 Phase Detector Output	
VCO3	M20	M20	O/Z	Framers 3 Phase Detector Output	
VCO4	B17	B17	O/Z	Framers 4 Phase Detector Output	
VCO5	H1	H1	O/Z	Framers 5 Phase Detector Output	
VCO6	Y3	Y3	O/Z	Framers 6 Phase Detector Output	
VCO7	—	J1	O/Z	Framers 7 Phase Detector Output	
VCO8	—	W4	O/Z	Framers 8 Phase Detector Output	

Table 1-15. Reciever Section System Side (1 of 3)

Pin Label	CX28346 Pin #	CX28348 Pin #	I/O	Signal Name	Definition
RXMSY1	N19	N19	O/Z	Framers 1 Receive Sync	The frame synchronization output of framer recovered from the incoming serial data stream.
RXMSY2	A16	A16	O/Z	Framers 2 Receive Sync	
RXMSY3	P18	P18	O/Z	Framers 3 Receive Sync	
RXMSY4	A7	A7	O/Z	Framers 4 Receive Sync	
RXMSY5	H2	H2	O/Z	Framers 5 Receive Sync	
RXMSY6	Y5	Y5	O/Z	Framers 6 Receive Sync	
RXMSY7	—	G3	O/Z	Framers 7 Receive Sync	
RXMSY8	—	Y14	O/Z	Framers 8 Receive Sync	
RXGAPCK1	K17	K17	O/Z	Framers 1 Receive Gapped Clock	It is a gapped clock signal output that is used to indicate RXDAT serial data output. RXGAPCK clock polarity and behavior are programmable and have several options (see Section 2.2).
RXGAPCK2	A15	A15	O/Z	Framers 2 Receive Gapped Clock	
RXGAPCK3	M16	M16	O/Z	Framers 3 Receive Gapped Clock	
RXGAPCK4	B12	B12	O/Z	Framers 4 Receive Gapped Clock	
RXGAPCK5	L4	L4	O/Z	Framers 5 Receive Gapped Clock	
RXGAPCK6	W6	W6	O/Z	Framers 6 Receive Gapped Clock	
RXGAPCK7	—	J5	O/Z	Framers 7 Receive Gapped Clock	
RXGAPCK8	—	W9	O/Z	Framers 8 Receive Gapped Clock	

Table 1-15. Reciever Section System Side (2 of 3)

Pin Label	CX28346 Pin #	CX28348 Pin #	I/O	Signal Name	Definition
REXTCK1	K19	K19	O/Z	Framers 1 Receive Overhead Clock Output	Used to indicate chosen Overhead bits that output on RXDAT. This output has a clock pulse for each position of the chosen group of Overhead bits for the specific DS3/E3 mode. Its polarity is programmable.
REXTCK2	A13	A13	O/Z	Framers 2 Receive Overhead Clock Output	
REXTCK3	M18	M18	O/Z	Framers 3 Receive Overhead Clock Output	
REXTCK4	B11	B11	O/Z	Framers 4 Receive Overhead Clock Output	
REXTCK5	L2	L2	O/Z	Framers 5 Receive Overhead Clock Output	
REXTCK6	Y8	Y8	O/Z	Framers 6 Receive Overhead Clock Output	
REXTCK7	—	J3	O/Z	Framers 7 Receive Overhead Clock Output	
REXTCK8	—	W10	O/Z	Framers 8 Receive Overhead Clock Output	

Table 1-15. Reciever Section System Side (3 of 3)

Pin Label	CX28346 Pin #	CX28348 Pin #	I/O	Signal Name	Definition
RXDAT1	R20	R20	O/Z	Framers 1 Receive Serial Data Output	This pin is the serial data bit stream of framer. Data is clocked out on the rising edge of receive internal clock.
RXDAT2	A14	A14	O/Z	Framers 2 Receive Serial Data Output	
RXDAT3	N18	N18	O/Z	Framers 3 Receive Serial Data Output	
RXDAT4	B7	B7	O/Z	Framers 4 Receive Serial Data Output	
RXDAT5	F1	F1	O/Z	Framers 5 Receive Serial Data Output	
RXDAT6	Y7	Y7	O/Z	Framers 6 Receive Serial Data Output	
RXDAT7	—	H3	O/Z	Framers 7 Receive Serial Data Output	
RXDAT8	—	W14	O/Z	Framers 8 Receive Serial Data Output	

Table 1-16. Microprocessor Interface (1 of 2)

Pin Label	CX28346 Pin #	CX28348 Pin #	I/O	Signal Name	Definition
MOTO*	T12	T12	I	Motorola Bus Mode	Selects Intel- or Motorola-style microprocessor interface. DS*, R/W*, A[8:0], and AD[7:0] functions are affected. 0 = Motorola; AD[7:0] is data, A[8:0] is address, DS* is data strobe, and R/W* indicates read (high) or write (low) data direction. 1 = Intel; AD[7:0] is multiplexed address/data, A[7:0] is ignored, A[8] is address, DS* is read strobe (RD*), and R/W* is write strobe (WR*).
A_0	E11	E11	IPD	Address Bus	Address used to identify a register for subsequent read/write data transfer cycle. In Motorola bus mode, all nine address bits (A[8:0]) are valid. In Intel bus mode, only the upper bit (A[8]) is used.
A_1	E10	E10	IPD	Address Bus	
A_2	E9	E9	IPD	Address Bus	
A_3	E8	E8	IPD	Address Bus	
A_4	E7	E7	IPD	Address Bus	
A_5	G5	G5	IPD	Address Bus	
A_6	F5	F5	IPD	Address Bus	
A_7	E5	E5	IPD	Address Bus	
A_8	E6	E6	IPD	Address Bus	
AD_0	U13	U13	IOPD	Data Bus or Address/ Data	Multiplexed address/data (Intel) or data only (Motorola). Refer to MOTO* definition.
AD_1	T13	T13	IOPD	Data Bus or Address/ Data	
AD_2	U14	U14	IOPD	Data Bus or Address/ Data	
AD_3	T14	T14	IOPD	Data Bus or Address/ Data	
AD_4	U15	U15	IOPD	Data Bus or Address/ Data	
AD_5	T15	T15	IOPD	Data Bus or Address/ Data	
AD_6	T16	T16	IOPD	Data Bus or Address/ Data	
AD_7	R16	R16	IOPD	Data Bus or Address/ Data	

Table 1-16. Microprocessor Interface (2 of 2)

Pin Label	CX28346 Pin #	CX28348 Pin #	I/O	Signal Name	Definition
ALE	U12	U12	I	Address Strobe	For Intel bus mode only, ALE falling edge asynchronously latches address from A[8:0] (Motorola) or A[8]+AD[7:0] (Intel) to identify one register for subsequent read/write data transfer cycle.
CS[A]*	H13	H13	I	Chip Select	Active low enables read/write decoder. Active high ends current read or write cycle and places data bus output in high impedance.
CS[B]*	N8	N8	I		
DTACK*	T10	T10	O/Z	Data Transfer Acknowledge	Open drain active low output signifies in-progress data transfer cycle. Data ready indication for read, transaction end indication for write
INTR[A]*	G14	G14	O/Z	Interrupt Request	Open drain active low output signifies one or more pending interrupt requests. INTR goes to high impedance state.
INTR[B]*	P7	P7	O/Z		
RW* (WR*)	T11	T11	I	Read/Write Direction or Write Strobe	Active low write data strobe (WR*) for MOTO* = 1, or data select (R/W*) for MOTO* = 0.
DS* (RD*)	U11	U11	I	Data Strobe or Read Strobe	Active low read data strobe (RD*) for MOTO* = 1, or data strobe (DS*) for MOTO* = 0.

Table 1-17. JTAG Interface

Pin Label	CX28346 Pin #	CX28348 Pin #	I/O	Signal Name	Definition
TRST[A]*	V20	V20	IPU	Test Reset	When this pin is asserted, the internal boundary-scan logic is reset. This pin has a pull-up resistor.
TRST[B]*	C1	C1	IPU		
TMS[A]	V17	V17	IPU	Test Mode Select	Controls the boundary-scan Test Access Port (TAP) controller operation. This pin has a pull-up resistor.
TMS[B]	C4	C4	IPU		
TDI[A]	V18	V18	IPU	Test Data Input	The serial test data input. This pin has a pull-up resistor.
TDI[B]	C3	C3	IPU		
TDO[A]	V19	V19	O/Z	Test Data Output	The serial test data output.
TDO[B]	C2	C2	O/Z		
TCK[A]	V16	V16	IPU	Test Clock	Samples the value of TMS and TDI on its rising edge to control the boundary scan operations (input clock).
TCK[B]	C5	C5	IPU		
NC	D1, D2, D4, G3, H3, H4, H5, J1, J3, J5, N7, R1, R2, R4, T1, T2, T3, U1, U2, U3, U4, V1, V2, V7, W1, W10, W14, W3, W4, W7, W8, W9, Y10, Y13, Y14 , Y9	—	—	No Connect	—

2.0 Functional Description

The descriptions of the following features are for a single Framer. However, all features are the same for all the channels available in the device.

NOTE: Accessing or using the additional framers and the associated registers within CX28346 and CX28348 requires the use of additional pins as outlined in Chapter 1 and Tables 1-9 and 1-10.

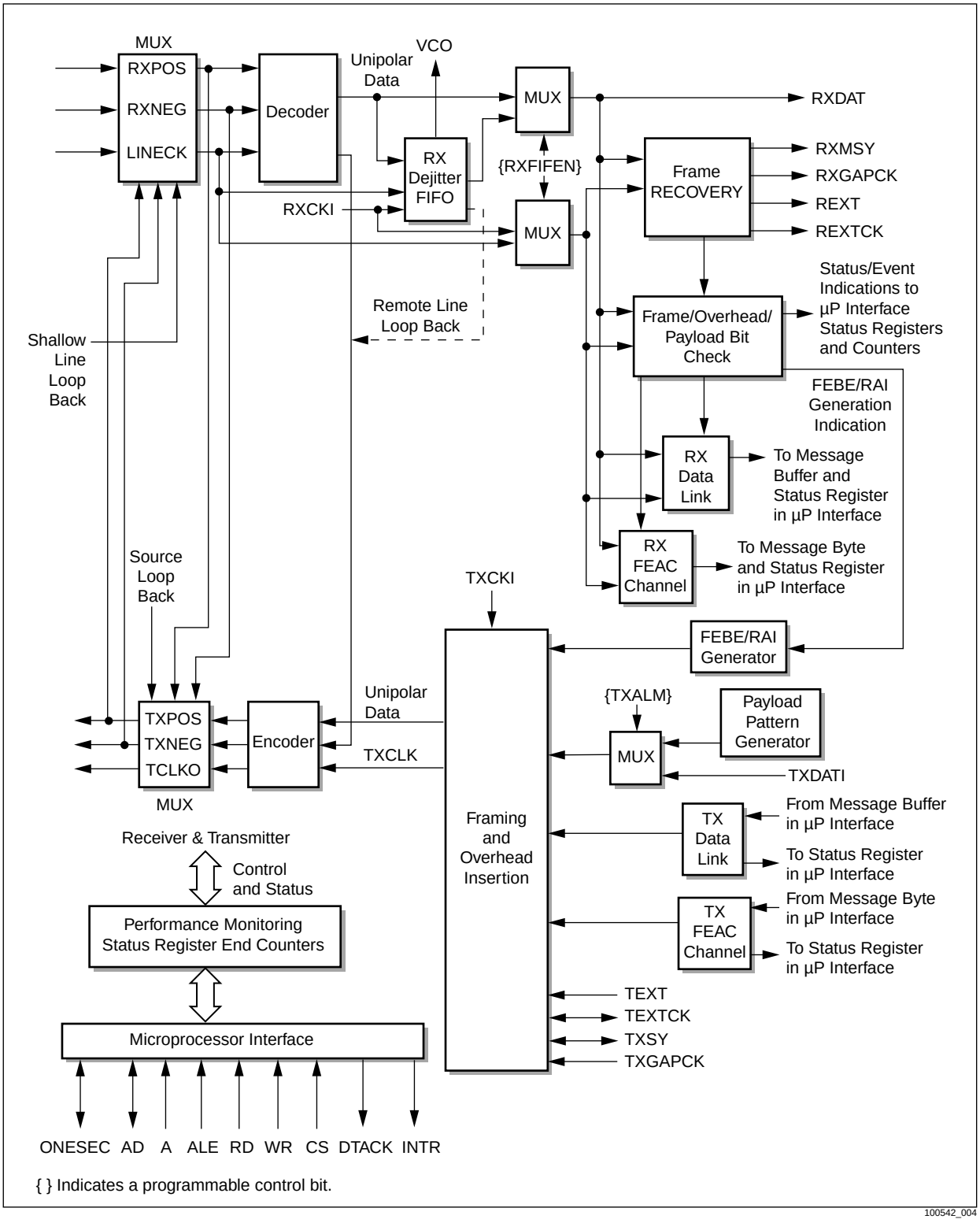
The Functional Description is divided into the following sections:

- Transmitter
- Receiver
- Microprocessor interface
- Miscellaneous (Loopbacks, JTAG, Test equipment, Support)

Each section describes in detail the operation of various features and describes the differences in E3 and DS3 mode.

Figure 2-1 illustrates a single-channel block diagram.

Figure 2-1. Functional Block Diagram of a Channel



2.1 Transmitter Operation

This section describes the transmit operation of the framer.

The transmit line side interface consists of three output pins; TXPOS/TXNRZ, TXNEG, TCLKO.

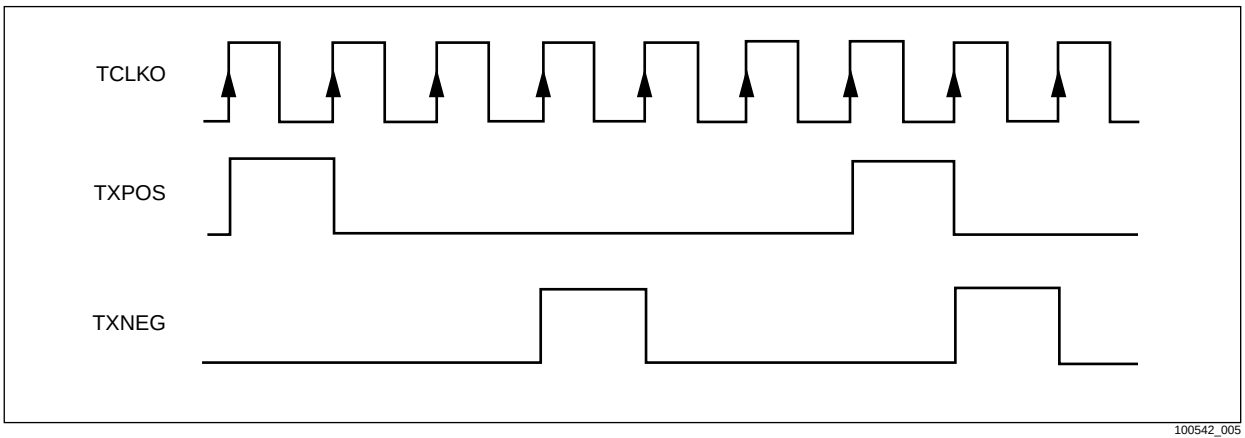
When bipolar mode is enabled, HDB3/B3ZS encoding is performed over all the transmitted data. In this mode, encoded data is transmitted on TXPOS (transmit positive polarity data) and TXNEG (transmit negative polarity data).

When AMI mode is enabled, data is sent in AMI code format without HDB3/B3ZS coding. TXPOS and TXNEG are used to send the positive and negative polarity data.

When NRZ mode is enabled, TXPOS/TXNRZ is used to transmit NRZ data, and TXNEG is unused.

The TCLKO is the clock reference output for TXPOS/TXNRZ and TXNEG output pins. Data outputs are a full-clock period wide in all modes, and can change on positive or negative transition of TCLKO signal. (If the LTxCkRis bit is set to 0, the data changes on the rising edge of TCLKO, or else it changes on the falling edge of TCLKO when bit LTxCkRis is set to 1). Figure 2-2 illustrates TXPOS and TXNEG changing on the rising edge of TCLKO.

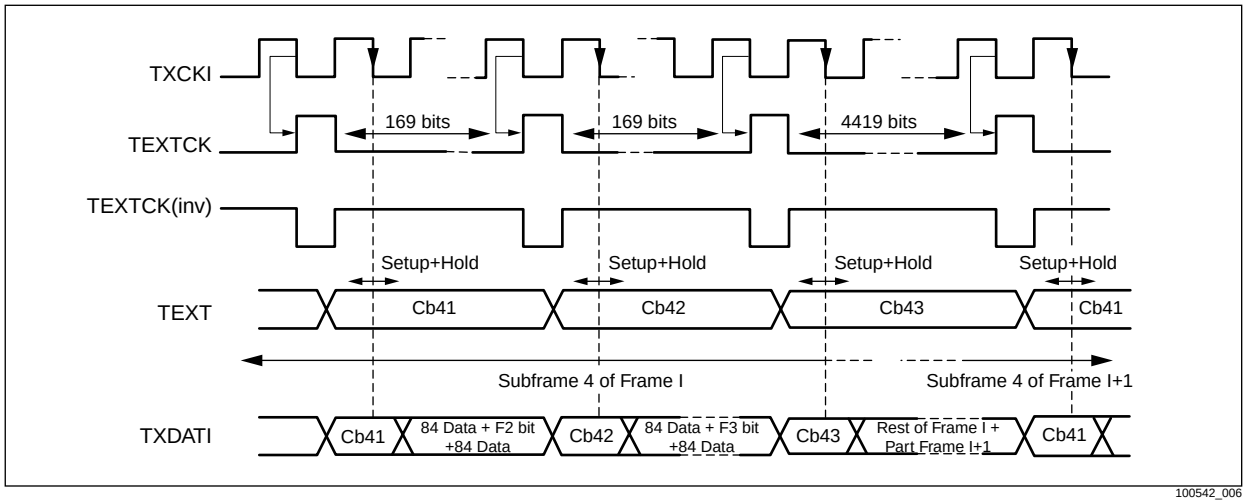
Figure 2-2. Transmitter Line Side Outputs



The transmit system side interface for each framer consists of TXCKI, TXDATI, TXGAPCK, TXSY, TEXT, and TEXTCK signals. Each of these pins is described in the pinout list description.

Figure 2-3 illustrates insertion of FEBE bits through the TEXT pin in DS3 C-bit parity mode. In this example, ExtFEBE/Cj-bit of Transmitter Overhead insertion register is set to 1, and all others are set to 0. In addition to the TEXT overhead input and the TXCKI clock input, the response of TEXTCK clock output is shown for normal (TEXTCK) and inverted ($\overline{\text{TEXTCK}}$) mode of operation. Due to these settings, the TEXTCK clock provides a clock pulse for the three C-bits in subframe 4 (FEBE bits). The FEBE bits are inserted through the TEXT pin and are sampled by the next falling edge of TXCKI clock after the pulse on TEXTCK. This indicates, to the system, that the framer expects a new FEBE bit. The data on TEXT should satisfy setup and hold times around the falling edge of TXCKI clock when it is sampled. TXDATI serial data input is also shown. TEXT and TXDATI have the same timing.

Figure 2-3. Tx System Side External Overhead Insertion (DS3 FEBE-only example)



TXSY

Frame synchronization indicator. Functions either as input or an output pin.

When used as an input pin (TXSYIn is set to 1), it provides the external circuitry with the ability to control frame start synchronization. It is sampled with the falling edge of the TXCKI input clock. After the first TXSY input signal is provided, the transmitter circuitry maintains the last synchronization until the next sync signal is provided on TXSY. Thus, the system has the option of not providing any more sync pulses on TXSY input as long as the old synchronization is valid.

NOTE: If sync signal is provided at an expected place according to the last sync signal (e.g., low-to-high transition over X1-bit in DS3 mode), it does not affect the old synchronization. If a sync signal is provided on TXSY pin not according to old synchronization, new synchronization takes place and incorrect operation (mainly at TXGAPCK and TEXCK) can occur near the sync signal.

The device resynchronizes within one frame time. When set as input, the transmitter expects at least one TXSY input signal. Until the first TXSY input signal is supplied, the framer is not synchronized and does not provide internal synchronization. In this case, TEXTCK and TXGAPCK outputs remain disabled (long gap) until the first TXSY input is provided. When TXSY input is provided, it should have a low-to-high transition from the last bit of the one frame to the first bit of the next frame. The framer watches the transition of TXSY input; when sampled high after it was sampled low, the framer expects the first bit of the new frame to be inserted at TXDATI at the same time. After TXSY input transitioned from low to high, it can be set low again after one or more TXCKI clock. The framer maintains synchronization from the last time TXSY input was provided.

When used as an output pin (by setting bit TXSYOut to 1), it has two modes of operation. Setting TxOvhMrk bit in the Feature 2 Control register controls these modes. It can function as a frame start synchronization signal or as an overhead indication signal. In both cases, it is sampled out with the rising edge of TXCKI clock.

When bit TxOvhMrk is set to 0, TXSY output functions as a frame start synchronization signal. The frame data bits provided to the transmitter on TXDATI are expected to be synchronized to the TXSY indication of frame start. After enabling the framer in this mode, the sync signal is automatically provided on TXSY output. In this mode the sync output signal on TXSY transitions from low to high and from the last bit of the frame to the first bit of the next frame (sampled as high with the first bit of the next frame). When TxOvhMrk bit is set to 1, TXSY output functions as an overhead indication signal. TXSY at this mode is low during all Overhead bits (including during Justification Control bits and Stuff Opportunity bits) and is high during all payload bits.

If the system does not require TXSY for its operation, it should set it as an output where automatic synchronization is provided all the time.

NOTE: After reset, this pin has a high-Z value until it is set to be used as an input or an output.

Transmit Operation in DS3 Mode

In DS3 mode, TXCKI is connected to a 44.736 MHz clock.

If the TXSY signal is provided externally, it should have a low-to-high transition from the last bit of the M-frame to the first bit of the next frame. If the TXSY is provided internally and used as a frame start synchronization signal (bit TxOvhMrk is set to 0 at Feature 2 Control register), it has a low-to-high transition from the last bit of the M-frame to the next bit of the next frame. The TXSY output returns to low after M3 bit of subframe 7. If the TXSY signal is used as an overhead indication output signal (bit TxOvhMrk is set to 1 at Feature 2 Control register), TXSY is low during all Overhead bits positions, and high during data bits position regardless of the Overhead bits source.

Figures 2-4 through 2-6 illustrate the transmitter timing for DS3 mode where none of the overheads are inserted with payload.

Figure 2-4 illustrates the behavior of TXSY, when it is used as a frame start synchronization output signal. In this setting the TXSY signal transitions from low to high at the last rising edge of TXCKI clock and before the X1 bit is sampled in on the next falling edge of TXCKI. The TXSY signal goes low again at the rising of TXCKI clock, and after M3 bit of subframe 7 is entered on TXDATI, it remains low during the rest of subframe 7.

Figure 2-4. DS3 System Side Transmission when TXSY is Externally Provided

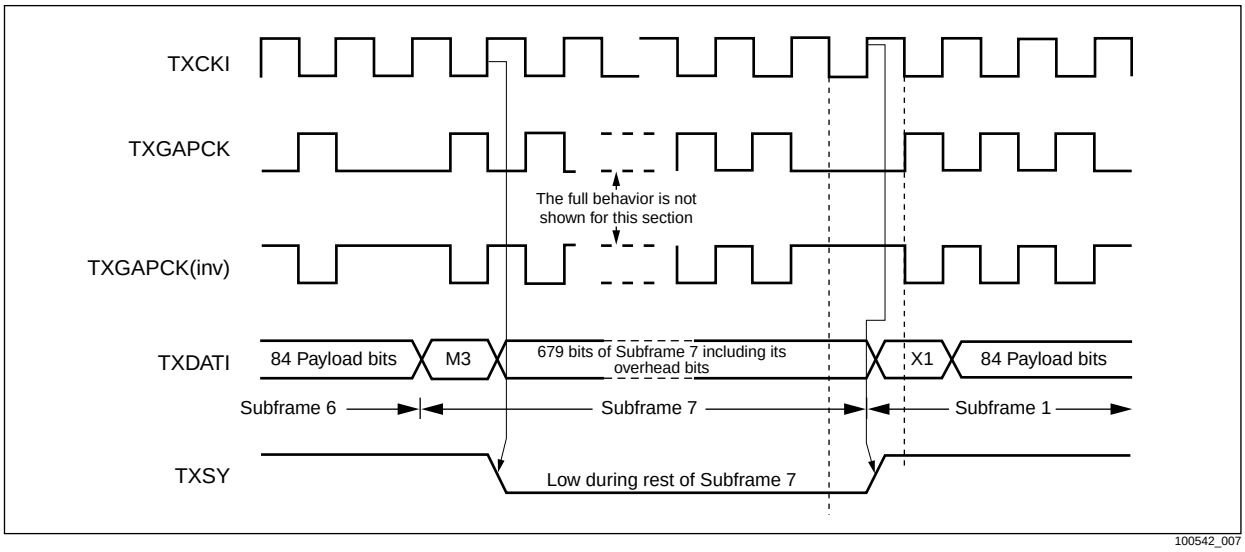


Figure 2-5 illustrates TXSY used as an overhead indication output signal. In this setting, TXSY is low during all Overhead bits position and high during all data bits position.

Figure 2-5. DS3 System Side Transmission Unit when TXSY is Used as an Overhead Indication Bit

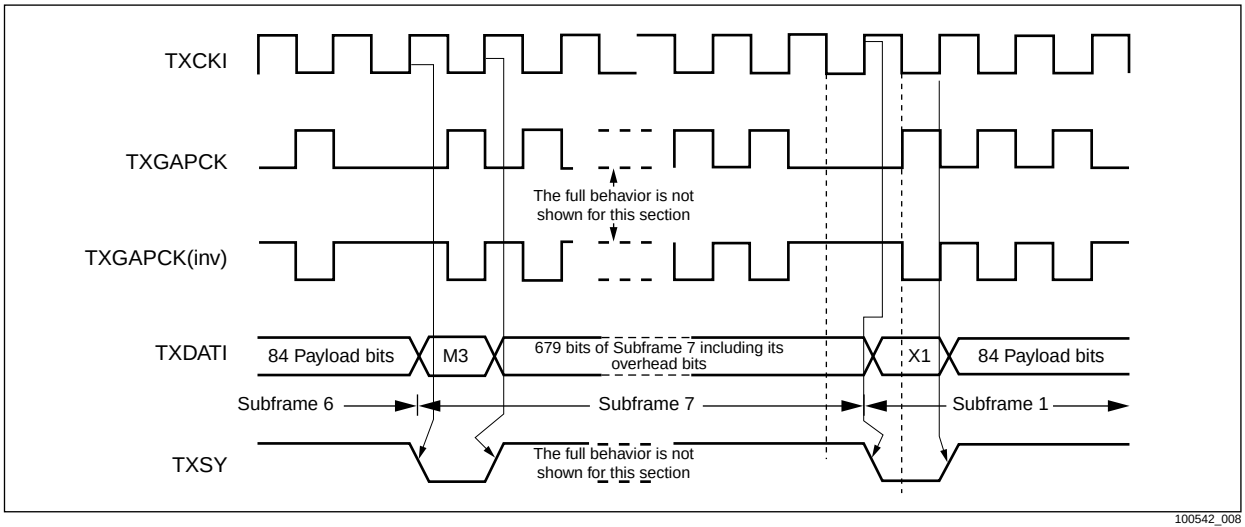
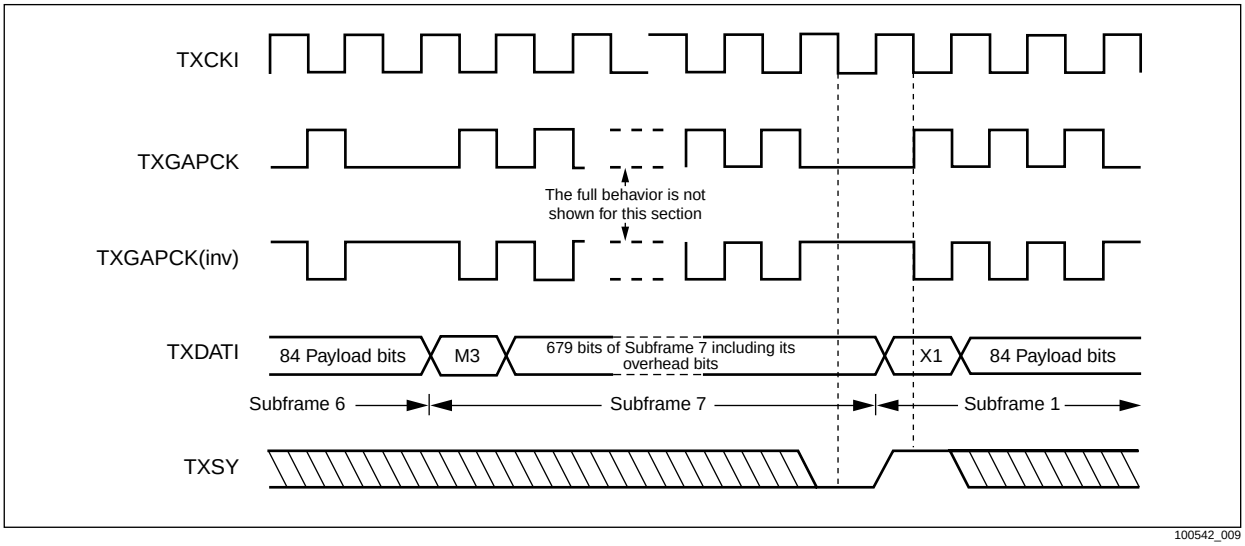


Figure 2-6 illustrates the TXSY signal configured as a frame start synchronization input signal. The signal is sampled on the falling edge of TXCKI clock. The framer also expects the TXSY signal to be low during the last bit of the frame before becoming high during the first of the next frame.

The behavior of TXGAPCK signal is shown both in normal (TXGAPCK) and in inverted mode ($\overline{\text{TXGAPCK}}$). Since none of the overheads are set to be inserted with payload, TXGAPCK is gapped during all Overhead bits illustrated in Figures 2-4 through 2-6.

Figure 2-6. DS3 System Side Transmit when TXSY is Input Signal (Frame Start)



Transmit Operation in E3-G.751 Mode

During E3-G.751 mode of operation, TXCKI pin is connected to a 34.368 MHz clock.

When TXSY signal is provided externally, it should have a low-to-high transition from the last bit of the E3-G.751 frame to the first bit of the next frame.

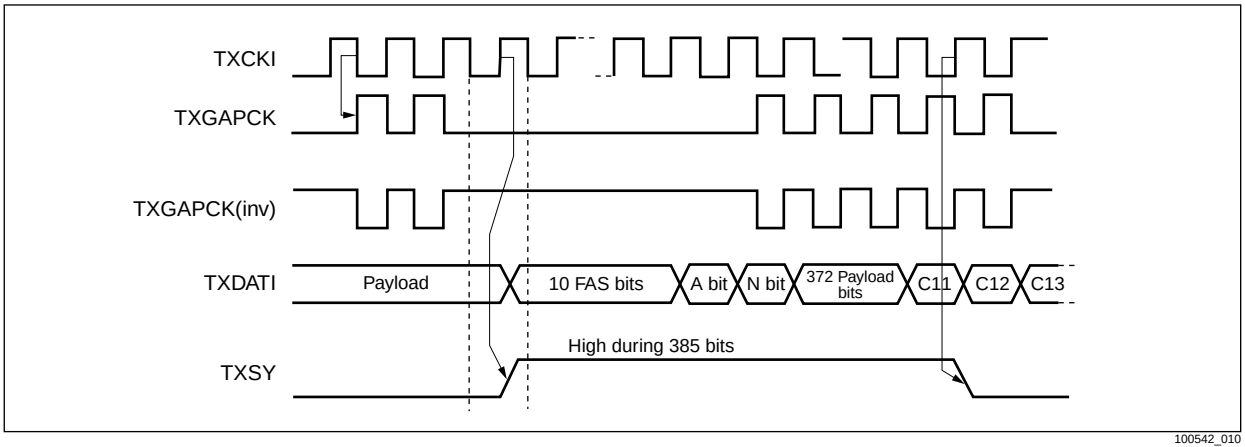
When the TXSY is provided internally and used as a frame start synchronization signal, it has a low-to-high transition at the same place. TXSY output returns to low after the C11 justification bit, as illustrated in Figure 2-7.

If TXSY is used as an overhead indication output signal, TXSY is low during all Overhead bits positions and high during data bits position regardless of Overhead bits source.

Figure 2-7 illustrates the TXGAPCK clock behavior both in normal (TXGAPCK) and in inverted mode ($\overline{\text{TXGAPCK}}$). Identical to the DS3 mode, the signal is sampled from the falling edge of TXCKI. In this figure, Justification Control bits are set to be supplied with the data stream, TXGAPCK is gapped only during FAS, A, N-bits, and Stuff Opportunity bits, and supplies clock pulses during the payload and Justification Control bits (C_j1, C_j2, C_j3 where $_j$ = 1 to 4).

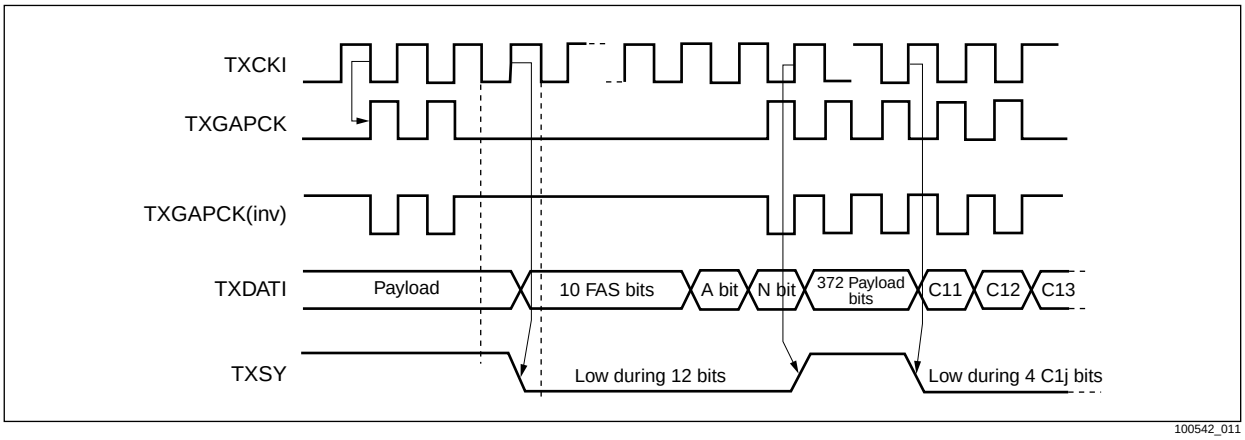
In Figure 2-7, TXSY is an output signal used as the frame start synchronization output signal.

Figure 2-7. E3-G.751 Transmit Mode when TXSY is Frame Start Sync Output Signal



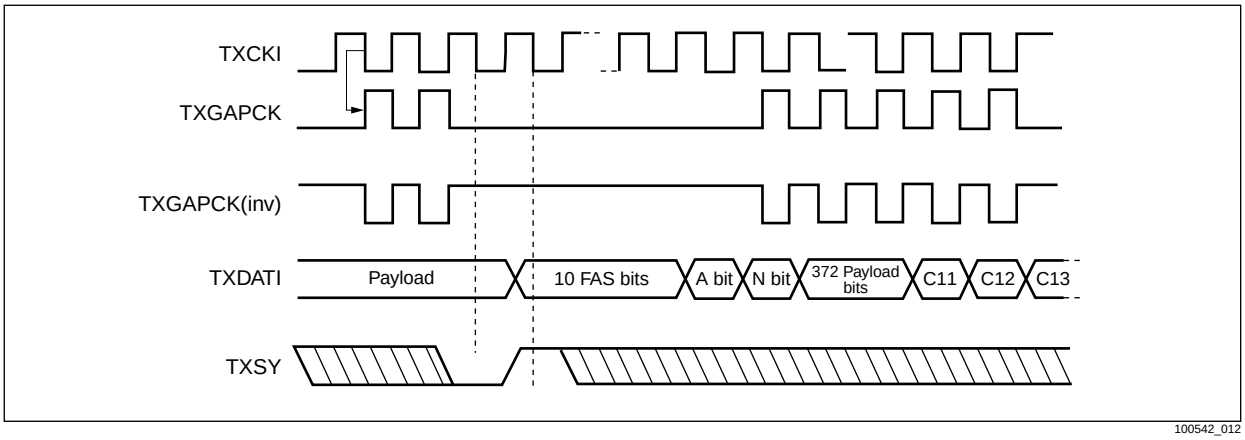
In Figure 2-8, the TXSY signal is used as an overhead indication output signal. Due to this setting, TXSY is low during all Overhead bits position and high during all data bits position.

Figure 2-8. E3-G.751 Transmit Mode where TXSY is an Overhead Indicator Output Signal



In Figure 2-9, the TXSY signal is an input having a low-to-high transition from the last bit of E3-G.751 frame to the first bit of the next frame. In this case, the system can return TXSY to low after at least one TXCKI clock.

Figure 2-9. E3-G751 Mode where TXSY is an Input Signal



Transmit Operation in E3-G.832 Mode

In the E3-G.832 mode of operation, TXCKI pin is connected to a 34.368 MHz clock.

When the TXSY signal is provided externally, it should have a low-to-high transition from the last bit of the E3-G.832 frame to the first bit of the framing alignment octet of the next frame.

When provided internally and used as a frame start synchronization signal, it has a low-to-high transition at the same position. TXSY output returns to low after the last bit of GC field.

If the TXCKI pin is used as an overhead indication output signal, TXSY is low during all Overhead bits positions (i.e., low during FA1, FA2, EM, TR, MA, NR, and GC bytes) and high during data bits position regardless of Overhead bits source.

In Figure 2-10, the TXSY pin is an output signal indicating frame start synchronization.

Figure 2-10. E3-G.832 Mode where TXSY is an Output Signal Indicating Frame Start Sync

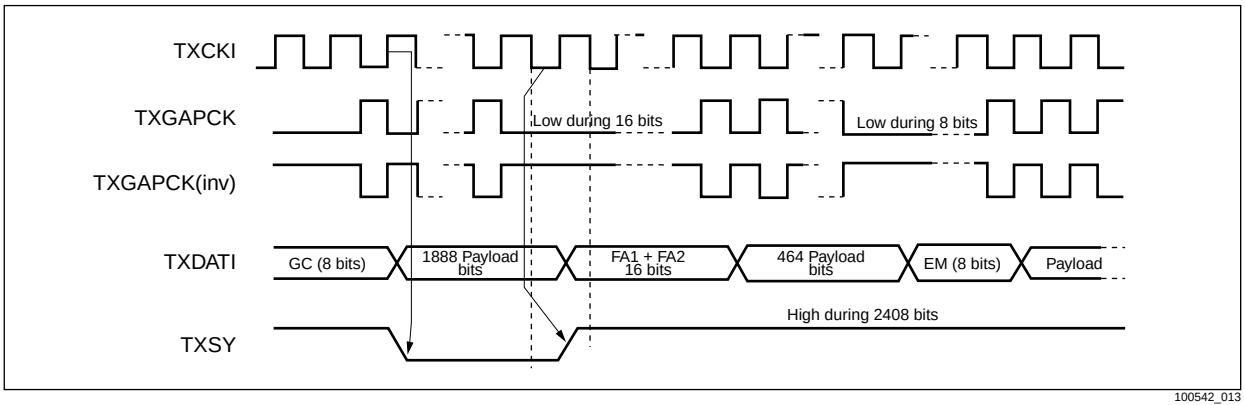
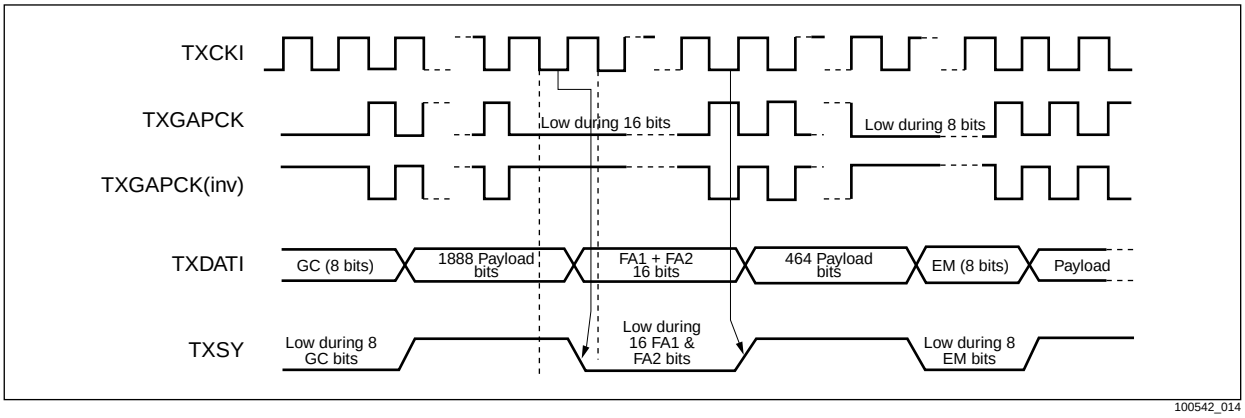


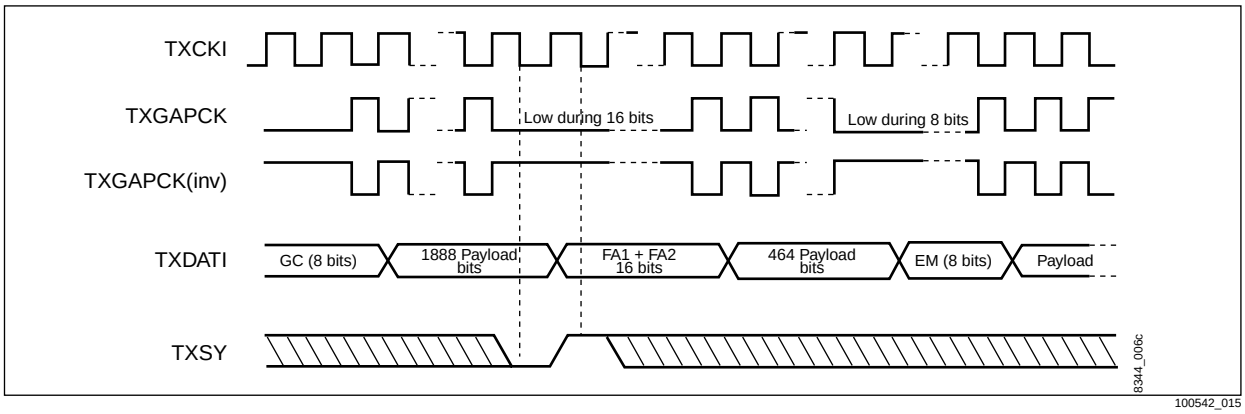
Figure 2-11 illustrates the TXSY pin functioning as an output signal indicating the Overhead bits.

Figure 2-11. TXSY Transmitter System Side Signal (E3-G.832)



In Figure 2-12, the TXSY pin is an input indicating synchronization.

Figure 2-12. TXSY Transmitter System Side Signal (E3-G.832)



2.1.1 Transmitter Overhead Bit Generation

For the DS3 M13/M23, DS3 C-bit parity, E3-G.751, and E3-G.832 modes of operation, the framer can use any of the following four techniques to insert framing and Overhead bits:

- Internal-Auto—Automatically generated by the internal circuitry, either because the value is predetermined and constant (e.g., DS3 F- and M-bits), or as a response to an incoming stimulus (e.g., automatic FEBE/REI).
- Internal-Reg—The Overhead bits value to be transmitted and/or the control over the value transmitted is performed through microprocessor-controlled registers.
- External-Data—Overhead bits to be transmitted can be supplied with the data stream.
- External-Pin—The Overhead bit is input from an external pin (TEXT) based on the gapped clock (TEXTCK) as set in the registers and controlled by the microprocessor.

The allocation of the Overhead bits to one method is done for groups of overheads. The options vary for each one of the four main modes of operation. The Transmit Overhead Insertion1 (i) control register and Transmit Overhead Insertion2 (i) control register controls the allocation. The registers' setting ability changes according to the framer mode of operation. Table 2-1 indicates the availability for the various Overhead bits in various modes.

Table 2-1. Overhead Sourcing Methods (1 of 2)

Mode	Field	Technique			
		Internal-Auto	Internal-Reg	External-Data(1)	External-Pin
DS3	F-bits, M-bits (Frame)	•		•	•
	X-bits (RAI)		•	•	•
	P-bits (Parity)	•		•	•
	7 Stuff Opportunity bits(2)			•	•
	C-bits (Justification Control)(2)			•	•
	Cb11 (AIC)(3)	•		•	
	Cb13 (FEAC)(3)		•	•	•
	Cb3 (Path Parity)(3)	•		•	•
	Cb4 (FEBE)(3)	•		•	•
	Cb5 (DL)(3)	•	•	•	•
	Cb12, Cb2, Cb6-7(3)	•		•	•
E3-G.751	FAS (Frame)	•		•	•
	A-bit (RAI)	•	•	•	•
	N-bit (DL)	•	•	•	•
	C_j-bits (Justification Control)			•	•
	4 Stuff Opportunity bits			•	•

Table 2-1. Overhead Sourcing Methods (2 of 2)

Mode	Field	Technique			
		Internal-Auto	Internal-Reg	External-Data[1]	External-Pin
E3-G.832	FA1, FA2 (Frame)	•		•	•
	EM (BIP-8)	•		•	
	TR (Trail Trace)	•		•	•
	MA RDI	•	•	•	•
	MA REI	•		•	•
	MA PT		•	•	
	MA PD[4]		•	•	•
	MA MI[5]	•		•	•
	MA TM/SSM[6]		•	•	
	NR (DL)	•	•[7]	•	•
	GC (DL)	•	•[7]	•	•

Note(s):
(1) Either all fields enter via data stream, or only Justification Control bits (in DS3 M13/M23 and E3-G.751), or Stuff Opportunity bits, or either justification control and stuff bits value or none.
(2) In M12/M23 mode.
(3) In C-bit Parity mode.
(4) In non-SSM mode.
(5) In SSM mode.
(6) In either SSM or non-SSM mode.
(7) Only one of these Overhead bits should be used at a time to enable the LAPD datalink.

2.1.1.1 DS3 Mode

There are 56 Frame Overhead bits in a DS3 M-frame structure. See Appendix B for details.

The External-Data source option for the DS3 mode provides the ability to insert all the Frame Overhead bits with the data stream. When the framer operates in C-bit parity mode there is an option to either insert *all* the Frame Overhead bits with the data stream or none of them by setting bit ExtDat in the Transmit Overhead Insertion 1 Control register. When the framer operates in M13/M23 mode there are five options (see Table 2-2) concerning the insertion of Overhead bits with the data stream:

1. All Overhead bits can be inserted with the data stream by setting bit ExtDat to 1.
2. Only C-bits (justification control bits) enter with the data stream and the 7 Stuff Opportunity bits are inserted via TEXT by setting bit ExtDat to 0 and ExtFEBE/Cj-bit to 0 and ExtStf to 1.
3. Only 7 Stuff Opportunity bits are inserted with the data stream while Justification Control bits are inserted from TEXT by setting bit ExtDat to 0 and ExtFEBE/Cj-bit to 1 and ExtStf to 0.
4. Both C-bits (justification control bits) and the 7 Stuff Opportunity bits are inserted with the data stream by setting bit ExtDat to 0 and ExtFEBE/Cj-bit to 0 and ExtStf to 0.

5. None of the Overhead bits are inserted with data (justification control and Stuff Opportunity bits enter through external pin and other overload bits are internally generated) by setting ExtDat to 0 and ExtFEBE/Cj-bit to 1 and ExtStf to 1.

Table 2-2. Overhead Options

Option	Setting of External Data		
	ExtDat	ExtFEBE/Cj	ExtStf
1	1	0	0
2	0	0	1
3	0	1	0
4	0	0	0
5	0	1	1

When the Frame Overhead bits are not chosen to be inserted via the data stream, the following source options are provided: internally generated, taken from register, or entered through an external pin. For enabling sourcing options, the Frame Overhead bits are divided into groups where each group of overheads has its own sourcing options. Some groups and their source options are different for C-bit parity and M13/M23 mode of operation. The difference is in the C-bits, which are divided to more groups in C-bit parity mode.

C-Bit Parity and M13/M23 Modes of Operation

The following groups of overheads have the same options for both operational modes.

- Framing bits (F-bits and M-bits)—When the External-Data method is disabled, the three M-bits and the 28 F-bits can be either generated internally by the framer (when ExtFrmAl bit is 0) or inserted through TEXT pin (when ExtFrmAl bit is 1).
- X-bits (RAI)—Can be either inserted through the TEXT pin (controlled by bit ExtRAI in the Transmit Overhead Insertion 2 register) or can be generated by an internal register setting (controlled by TxAlm[1:0] bits). When TxAlm[1:0] is set to 01, bits X1 and X2 contain 0s regardless of other X-bits sourcing settings.
- P-bits (parity bits)—Can be either internally calculated or inserted from TEXT pin (controlled by bit ExtP in the Transmit Overhead Insertion 2 register). When set to be calculated internally, the transmitter calculates the parity over 4704 payload bits of each M-frame (even parity calculation is used) and inserts the result into both P1 and P2 bits of the following M-frame.

The C-bits in M13/M23 modes are used as Justification Control bits and are all supplied from the same source. Their options are as follows:

- Either to be inserted with the data stream (with or without the rest of the Overhead bits) by setting ExtDat bit to 1 or ExtFEBE/Cj-bit to 0.
- To be inserted through the TEXT external pin. This option is chosen by setting ExtDat bit to 0 and ExtFEBE/Cj-bit to 1.

C-Bit Parity Mode Only: Overhead Insertion

In the C-bit parity mode of operation, the C-bits are divided into groups with the following source options:

- AIC (Cb11)—Application Identification Channel. It is generated internally. The transmitter inserts 1 to the transmitted data at the C11 place to indicate that the line works with the C-bit parity application (a constant 1 at AIC-bit indicates C-bit parity application).
- FEAC (Cb13)—Far End Alarm Channel. When bit ExtFEAC/PD (Transmit Overhead Insertion 1 Control register) is set to 1, Cb13 value is inserted through the TEXT input pin. When bit ExtFEAC/PD is set to 0, Cb13 is internally generated using the Transmit FEAC Channel Byte register and setting bit FEACSin (single or repetitive mode bit) at the Feature3 Control register.
- Path Parity (Cb3)—The three C-bits at subframe 3 can either be supplied to the transmitter circuit on TEXT external input by setting bit ExtCP/TR in Transmit Overhead Insertion 1 Control register to 1 or internally generated by setting bit ExtCP/TR to 0. When internally generated, the transmitter calculates the parity over 4704 payload bits of each M-frame (even parity calculation is used) and inserts the result to Cb31, Cb32, and Cb33 bits of the next M-frame (they are all set to the same value as the P-bits when no error insertion occurs).
- FEBE (Cb4)—The three C-bits at subframe 4 (FEBE bits) can either be inserted through the TEXT pin (when ExtFEBE/Cj-bit in the Transmit Overhead Insertion 1 Control register is set to 1), or can have an internal-automatic source (when ExtFEBE/Cj-bit is set to 0). The internal-auto sourcing of FEBE in DS3-C-bit parity mode is further described in Section 2..
- DL (Cb5)—The three C-bits in subframe 5 are assigned as a 28.2 Kb terminal-to-terminal path maintenance data link. Their values can be taken from the TEXT input pin when bits DLMod[2] and DLMod[1] are set to 11. The bits can all be automatically set to 1 by setting bit DLMod [2] to 0 (DLMod [1] bit can be set to either 0/1), or they can be chosen internally by registers generated by setting DLMod [2] and DLMod [1] bits to 10. The last option uses an internal FIFO buffer and the HDLC formatting mechanism to implement LAPD data link channel on those bits. For details, see Section 2..
- Cb12, Cb2, and Cb6-7—Cb12 is an Nr bit (network reserved bit). The C-bits in the second, sixth, and seventh M-subframe are reserved bits—all together, they can either be generated internally or provided from an external pin. When bit DLMod [0] is set to 1, those bits are taken from the TEXT pin. When this bit is set to 0, they are all internally generated and transmitted as 1.

2.1.1.2 E3–G.751 Mode

E3-G.751 frame structure has 24 frame Overhead bits, which are divided as follows:

- 10 frame alignment signal (FAS) bits
- Alarm indication to the remote digital multiplex equipment (A-bit) bit
- Bit reserved for national use (N-bit)
- 12 justification service bits (Cj-bits)

The External-Data source option for the E3-G.751 mode provides the following options of framing bits insertion with the data stream:

- All Overhead bits can be inserted with the data stream by setting bit ExtDat to 1.
- Only Cj-bits enter with the data stream and the 4 Stuff Opportunity bits are inserted via TEXT by setting bit ExtDat to 0 and bit ExtFEBE/Cj to 0 and ExtStf = 0. The rest of the Overhead bits (FAS, A, and N) source is set separately.
- Both Cj-bits and the 4 Stuff Opportunity bits are inserted with the data by setting ExtDat=0 and ExtFEBE/Cj = 0 and ExtStf = 0.
- None of the Overhead bits or stuff bits are inserted with data (they are either generated internally or enter through external pin) by setting bits ExtDat and ExtFEBE/Cj to 0, 1 respectively and ExtStf = 1.

When the frame Overhead bits are not chosen to be inserted via the data stream, the following source options are provided for each group of frame Overhead bits:

- FAS—Bits 1 to 10 of set 1 are used as the frame alignment signal. Those bits are generated automatically internally by the transmitter circuit and inserted at the beginning of each E3-G.751 frame transmission. The 10 FAS bits have the sequence: 1111010000 (transmitted from left to right), or they can be inserted through the TEXT pin by setting of bit ExtFrmA1.
- A-bit—Bit 11 of set 1 is the alarm indication to the remote digital multiplex equipment bit (used to send RAI alarm signal). This bit can be automatically internally generated, controlled by a register or inserted through the TEXT pin. Automatic RAI generation is enabled by setting bit AutoRAI in the Transmit Overhead Insertion 1 Control register to 1. In this mode as long as a Loss of Signal (LOS) condition or loss of frame alignment—Out of Frame (OOF) are detected at the RCV, the TRN automatically inserts 1 at the transmitted A-bit. When LOS and OOF conditions are not detected, the TRN sets the transmitted A-bit to 0 (no RAI alarm). When AutoRAI = 0, setting ExtRAI bit at the Transmit Overhead Insertion 2 Control register to 1 causes A-bit insertion through TEXT pin. For as long as TxAlm [1] is set to 1, the A-bit contains 1 regardless of other A-bits sourcing settings.
- N-bit—Bit 12 of set 1 is reserved for national use. Its value can be taken from the TEXT input pin when bits DLMod [2] and DLMod [1] in the Transmit Overhead Insertion 1 Control register are both set to 1. It can be automatically set to 1 by the framer when bit DLMod [2] is set to 0, or it can be chosen internally generated by registers when DLMod [2] and DLMod [1] are set to 10. The last option implements a LAPD data link with HDLC formatting over the N-bit using an internal FIFO buffer. For more details about using the data link FIFO buffer, see Section 2..
- Cj-bits—The justification bits are provided either to the transmitter framer with the data stream, or by the TEXT external overhead input pin (when ExtFEBE/Cj is set to 1) when the option of providing them with the data stream is disabled.

2.1.1.3 E3–G.832 Mode

E3-G.832 frame structure comprises seven octets of Overhead bits. They are divided into the following:

- FA1 and FA2 (2 octets)
- Error Monitoring byte (EM)
- Trail Trace byte (TR)
- Maintenance and Adaptation byte (MA)
- Network operator byte (NR)
- General purpose communication channel byte (GC)

In E3-G.832 mode, the framer provides two options for the insertion of the frame overhead bytes within the data stream: either all frame Overhead bits are inserted with the data stream (by setting bit ExtDat to 1), or none of the Overhead bits are inserted via the data stream (setting bit ExtDat to 0).

When the frame Overhead bits are not chosen to be inserted via the data stream, the following source options are provided for each group of frame Overhead bits:

- FA1 and FA2—The frame alignment bytes that have the value of FA1 = 11110110 (transmitted left to right), FA2 = 00101000 (transmitted left to right) are automatically inserted by the framer's transmitter circuit at the beginning of each frame or inserted from the TEXT pin by setting ExtFrm A1 bit.
- EM—Error monitoring. BIP-8 byte. When not all overheads are inserted via the data stream, this byte is generated automatically by the transmitter circuit. The transmitter calculates a BIP-8 code using even parity. The BIP-8 is calculated over all bits, including the Overhead bits, from the previous frame. The computed BIP-8 is placed in the EM byte of the current transmitted E3-G.832 frame.
- TR—The trail trace byte to be transmitted can be either supplied externally on the TEXT pin (by setting ExtCP/TR bit at the Transmit Overhead Insertion 1 Control register to 1) or disabled and automatically transmitted as all 0s (by setting ExtCP/TR bit to 1).
- MA RDI—Bit 1 of the MA field is the remote defect indicator. This bit value can either be generated automatically, controlled by a register or inserted through TEXT pin, depending on AutoRAI, TxAlm, and ExtRAI bit settings. If AutoRAI = 1, automatic RDI is enabled. In this mode, for as long as Loss of Signal (LOS) or loss of frame alignment—Out of Frame (OOF) conditions are detected at the receiver, the transmitter automatically inserts 1 at the transmitted RDI-bit. Otherwise, the RDI-bit is transmitted as 0. RDI insertion is also controlled by TxAlm [1] bit at the Mode Control register. Normally, the transmitter sends 0 as the RDI-bit. When AutoRAI = 0, setting ExtRAI bit at the Transmit Overhead Insertion 2 Control register to 1 causes RDI-bit insertion through TEXT pin. For as long as TxAlm[1] is set to 1, RDI-bit contains 1, regardless of other RDI-bit sourcing settings.
- MA REI—Bit 2 of the MA field is the remote error indication. It can be either generated internally or supplied on the TEXT pin to the transmitter circuit. If bit ExtFEBE/Cj in Transmit Overhead Insertion 1 Control register is set to 1, REI-bit is inserted to the transmitter via the TEXT pin. If bit ExtFEBE/Cj is set to 0, REI is internally generated automatically. In the internal-automatic mode the REI-bit is set by the transmitter as a reaction to an error detected in a received BIP-8 code (in EM field). In this mode, if the received BIP-8 code at the current frame does not equal the calculated BIP-8 code over the previously received frame, the transmitter inserts 1 at the REI-bit for one frame at the first opportunity. As long as no BIP-8 errors are detected at the received frame, the tra3nsmitter inserts 0 at the transmitted REI-bit.

- MA PT—(payload type) Bits 3 to 5 of the MA byte are the payload type field. The 3-bit payload type pattern, to be transmitted, is contained in bits FEBEC/PT[1:3] at the Feature1 Control register. Writing a new payload type to the register affects the next transmitted frame.
- MA PD/MI—Bits 6 and 7 of the MA byte are the payload dependent/multiframe indicator bits. There are two modes of operation for these bits: SSM mode, and the normal mode. When bit SSMEn in Feature4 (I) Control register is set to 1, SSM mode is enabled. In this mode the MA PD/MI bits act as multiframe indicator bits (MI). They can be supplied by either an external circuit on TEXT bit input or they can be automatically generated internally by setting of bit ExtFEAC/PD (when set to 0, it is automatically generated; when set to 1, it is supplied through the TEXT pin). When multiframe indication bits are supplied automatically, a 2-bit roll-over counter is implemented. The counter is incremented each frame and its value is transmitted on MI bits (The MI counter is reset to 00 when enabling automatic generation of MI bit in SSM mode). When bit SSMEn is set to 0, SSM mode is disabled and the PD/MI bits act as the payload dependent bits. When SSM mode is not set, those bits can be either supplied by external circuitry on the TEXT pin by setting bit ExtFEAC/PD bit in the Transmit Overhead Insertion 1 register to 1, or the value to be transmitted can be taken from bits MAPD [1:2] in register Feature4 (I) Control register by setting bits ExtFEAC/PD and SSMEn to 0.
- MA TM/SSM—Bit 8 of the MA byte is the timing marker/SSM bit. There are two modes of operation for these bits: SSM mode, and the normal mode that is controlled by the settings of bit SSMEn in Feature4 (I) Control register. If bit SSMEn is set to 1, SSM mode is enabled, otherwise SSM mode is disabled. In both SSM and normal mode, the bits to be transmitted are written to the register. When SSM mode is disabled, the TM value to be transmitted is taken from bit SSM [1]/TM in Feature4 Control register. When SSM mode is enabled, the 4-bit SSM message to be transmitted is stored in bits SSM [1]/TM, SSM [2:4] in Feature4 Control register. In this mode, the bit of the SSM message to be transmitted is selected according to the value of MI transmitted bits (supplied through the TEXT pin or automatically generated).

NOTE: There are eight options for setting NR and GC sources using the DLMod [2:0] bits setting at the Transmit Overhead Insertion 1 Control register in a E3-G.832 mode of operation. All are specified in the control register section. *The framer is capable of implementing one LAPD data link using an internal FIFO buffer at a time. In E3-G.832 mode a LAPD data link can either be implemented on GC or NR, but not on both at the same time.*

- **NR (DL)**—The network operator byte source is determined by bits DLMod [2], DLMod [1], and DLMod [0] at the Transmit Overhead Insertion 1 Control register. It can be supplied externally on TEXT. It can be transmitted as all-1s (data link disabled). The framer is also capable of implementing LAPD data link using an internal FIFO buffer, as specified in Section 2.
- **GC (DL)**—The general purpose communication channel bytes source is determined by bits DLMod [2], DLMod [1] and DLMod [0] at the Transmit Overhead Insertion 1 Control register together with the NR byte. It can be supplied externally on the TEXT pin or transmitted as all-1s (data link disabled). The framer is also capable of implementing an LAPD data link using an internal FIFO buffer, as specified in Section 2.

2.1.2 Alarm Signal Generation

Each one of the framers is provided with an alarm signal generation mechanism. Some of the alarms can be either generated automatically as a reaction to receive conditions or initiated by the user (set by bits, inserted via external interface or with the data stream). All alarm signals that are initiated by the user are implemented as an activate/deactivate mechanism in which the user is responsible for activating and deactivating the alarm signal generation bit. The alarms that can be generated are specified for each available mode of operation.

For all DS3/E3 modes of operation bits, TxAlm1 and TxAlm0 in the Mode (i) Control register are responsible for alarm generation.

During alarm generation and transmission, the system interface is not influenced, thus all clocks and signals remain the same.

2.1.2.1 Loss of Signal Generation

For all modes of operation, the transmit mechanism provides the user with a programmable option to transmit LOS to the line side by setting bit TxLOS at the Feature2 Control register. When bit TxLOS is set to 1, the transmit mechanism generates 0 on the line side data interface outputs (TXPOS and TXNEG are transmitted as 0)—regardless of inserted payload and Overhead bit settings.

2.1.2.2 DS3 Mode

In DS3 M13/M23 and C-bit parity modes RAI, AIS, and IDLE alarm signals can be generated on the outgoing DS3 stream by setting the TxAlm1 and TxAlm0 bit pair in the Mode (i) Control register for each framer individually. Table 2-3 summarizes the alarms. In C-bit parity mode, a FEBE alarm is also generated. The various alarms are described in the following paragraphs.

Table 2-3. DS3 Mode Alarm Signal Setting

Bits		Type Alarm
TxAlm0	**TxAlm1**	
0	0	Normal
0	1	RAI (Yellow)
1	0	IDLE
1	1	AIS

RAI (Yellow Alarm)

The yellow alarm is contained in the X1 and X2 bits (by setting them to 0). The Yellow alarm is controlled by TxAlm[1:0] regardless of X-bits sourcing settings. Setting the TxAlm bit pair to 01 sends the Yellow alarm. X1 and X2 bits are sent as 0 as long as TxAlm bit pair is set to 01. The start and termination of RAI occur in the next frame after setting of TxAlm [1:0] bits.

AIS

The AIS signal has a valid M-frame alignment channel, a valid M-subframe alignment channel and valid P-bits, all C-bits are set to 0 regardless of DS3 framing mode (M13/M23 or C-bit parity), both X-bits set to 1, and the payload set to a 1010... pattern starting with 10 after each Overhead bit.

Generation and transmission of the AIS signal is enabled by setting the TxAlm [1,0] bit pair to 11. It continues as long as TxAlm [1,0] bits are set to 11. When TxAlm [1,0] bit pair is set to 11, the transmit line output is replaced with the DS3 AIS pattern. The pattern is generated internally regardless of the inserted data and Overhead bits insertion method from the system side, which is ignored by the framer.

NOTE: When the transmitter starts generating the AIS alarm, it continues keeping the old M-frame's synchronization. The start and termination of AIS generation are frame aligned (AIS transmission initiates with the beginning of the next frame after setting TxAlm [1,0] bit pair to 11 and terminates at the beginning of the next frame after setting TxAlm [1,0] bit pair to other than 11).

IDLE

The DS3 IDLE signal has valid framing and parity. With both X-bits set to 1, the payload is set to a 1100... pattern—starting with 11 after each Overhead bit. The C-bits in M-subframe 3 are set to 0, and the remaining C-bits can individually be a 1 or a 0, and can vary with time.

The transmission of idle code is enabled by setting TxAlm [1,0] bit pair to 10 for each framer individually, and continues as long as those bits are set to 10. The start and termination of IDLE generation are frame aligned (IDLE transmission initiates with the beginning of the next frame after setting TxAlm [1,0] bit pair to 10 and terminates at the beginning of the next frame after setting TxAlm [1,0] bit pair to other than 10).

In both DS3 framing modes (M13/M23 or C-bit parity), when IDLE code generation is enabled, the framers transmitter line output is replaced with the DS3 IDLE pattern. It is internally generated regardless of the inserted data. The C-bits are handled as follows: the C-bits in M-subframe 3 are set to 0 and the remaining C-bits are set according to their method of generation setting (from Internal-Auto, from Internal-Reg, from External-data, or from External-Pin) that are set for each mode, described in Section 2. The rest of the Overhead bits are generated according to IDLE code specifications. When the transmitter starts generating the IDLE alarm, the transmitter keeps the previous M-frame's synchronization.

The handling of the C-bits in IDLE code generation is such to allow full use of the remaining C-bits, e.g., to use terminal data link and transmit FEAC channel in C-bit parity mode during transmission of IDLE code.

FEBE

The FEBE alarm in DS3 is defined for C-bit parity application only. The three C-bits in M-subframe 4 are used as FEBE-bits.

In C-bit parity mode, when the ExtFEBE/Cj-bit in the Transmit Overhead Insertion 1 Control register is set to 0, the FEBE bits are not expected on TEXT input pin. FEBE alarms are automatically generated in the transmitter when the receiver detects either a frame bit error (F or M-bit error) or a path parity error in an M-frame. The 3-bit FEBE pattern that is transmitted is contained in the FEBE Pattern Bit Field (FEBEC/PT[1:3]) of the Feature1 Control register of each framer respectively. When no alarm condition is present, the FEBE channel contains all-1s. To prevent disabling proper FEBE operation during the Internal-Auto method of FEBE, the FEBE field should be written to any combination other than 111.

NOTE: FEBE transmission is performed at the first opportunity after framing error or CP error detection. Automatic FEBE transmission also remains operational (if set) during receiver OOF, LOS, AIS, or IDLE conditions. When FEBE bits are inserted from an external pin or with data, the automatic FEBE insertion is disabled and Pattern Bit Field settings have no meaning—FEBE bits are inserted externally.

2.1.2.3 E3-G.751 Mode

When E3-G.751 mode is set, two alarms can be generated: RAI (yellow alarm) and AIS according to the G.751 standard.

RAI (Yellow Alarm)

Bit 11 set 1 of E3-G.751 frame structure is the A-bit and used to transmit the remote alarm indication (RAI). RAI alarm is defined as transmitting 1 on A-bit.

Each of the framers has an option to insert the A-bit:

- With payload (when the method of overhead insertion is all with the data stream)
- From TEXT pin
- Automatically generate it
- Force RAI alarm sending by a control register

If automatic RAI is enabled (by setting AutoRAI in Transmit Overhead Insertion 1 Control register to 1), as long as LOS condition or OOF are detected at the receiver, the transmitter automatically inserts 1 at the transmitted A-bit (starting and stopping at first opportunity). When LOS and OOF conditions are no longer detected, the transmitter sets the transmitted A-bit to 0 (no RAI alarm). In the automatic RAI mode the transmitter side sends automatic RAI as long as OOFAlm or LOSAlm bits at the Maintenance Status register are set. Detection of LOS and OOF are specified at the alarm detection section.

Forcing a RAI alarm can also be done by setting TxAlm [1] to 1. As long as TxAlm [1] is set to 1, A-bit contains 1, regardless of other A-bits sourcing settings.

AIS

E3 AIS is defined as unframed all-1s.

In E3 mode, transmission of AIS is enabled by setting TxAlm0 high. When AIS is enabled, the framer ignores the inserted data and Overhead bit settings and transmits an all-1s code as long as TxAlm0 bit is set to 1. Start of AIS transmission and termination in E3 is immediate with the setting of TxAlm0.

2.1.2.4 E3-G.832 Mode

In E3-G.832 mode, three alarms are generated: Remote Defect Indicator (RDI), Remote Error Indicator (REI), and Alarm Indication Signal (AIS).

RDI

Bit 1 of MA field at E3-G.832 34.368 Mbps frame structure is used to transmit RDI.

Transmission of RDI in E3-G.832 mode is similar to RAI in E3-G.751 mode. Each of the framers has an option to insert the RDI-bit:

- With payload (when the method of overhead insertion is all with data)
- From TEXT pin
- Automatically generate it
- Force RDI alarm sending by a control register

If automatic RDI is enabled (by setting bit AutoRAI in Transmit Overhead Insertion 1 Control register to 1), as long as LOS or OOF conditions are detected at the receiver, the transmitter automatically inserts 1 at the transmitted RDI-bit. When LOS and OOF conditions are no longer detected, the transmitter sets the transmitted RDI-bit to 0 (no RDI alarm). In the automatic RDI mode the transmitter side sends automatic RDI as long as OOFAlm or LOSAlm bits at the Maintenance Status register are set.

Forcing a RDI alarm can also be done by setting TxAlm [1] to 1. As long as TxAlm [1] is set to 1, RDI-bit contains 1, regardless of other RDI-bits sourcing settings.

NOTE: Automatic RDI transmission does not react to TR mismatch because the framer does not check TR mismatches. When the method of overhead insertion is all with data, setting AutoRAI or ExtRAI has no influence on the transmitted RDI-bit.

REI

REI is transmitted in bit 2 of MA octet at the E3-G.832 34.386 Kb frame structure.

For each framer this bit can be either externally supplied (with the data stream or from an external pin) or internally generated automatically.

If the REI-bit is selected to be generated internally, the transmitter sets this bit to 1 (generate REI signal) if one or more errors are detected by BIP-8 code received in the EM field. The REI-bit is otherwise transmitted as 0 (no BIP-8 errors). During receiver LOS or AIS, automatic REI remains active. During receiver OOF condition, REI is transmitted as 0 in this mode.

AIS

The ability to transmit an all-1s AIS code is also supplied for the E3-G.832 mode (similar to the E3-G.751 mode).

In E3-G.832 mode, transmission of AIS (unframed all 1) is enabled by setting TxAlm0 high. When AIS is enabled, the framer ignores the inserted data and Overhead bit settings and transmit an all-1s code, as long as TxAlm0 bit is set to 1. Start of AIS transmission and termination in E3-G.832 is immediate with the setting of TxAlm0.

2.1.3 Terminal Data Link Transmission

A terminal data link channel can be implemented over the 3 C-bits in subframe 5 in DS3, C-bit parity mode, over the N-bit in E3-G.751 mode, and over GC byte or the NR byte in E3-G.832 mode of operation (either GC or NR not both).

The transmitted data link bits for each mode of operation can be supplied to the transmitter circuit externally via the data stream or on TEXT (external overhead input pin). They can be processed internally using an internal FIFO buffer, which is accessed, via a microprocessor-controlled interface. When the data link is disabled and its bits are not supplied externally, the transmitter circuit automatically inserts a default value to the transmitted data link bits: i.e. in DS3 C-bit parity mode the 3 C-bits in subframe 5 are transmitted as 1, in E3-G.751 mode N-bit is transmitted as 1, and in E3-G.832 when the data link is disabled on NR or GC (or both) those bytes are transmitted as 1.

The following sections describes the transmit side terminal data link implementation using an internal FIFO buffer. Setting bits DLMod [2:0] at the Transmit Overhead Insertion 1 Control register as specified in Section 3.2, Feature Control registers, can enable this mode for each rate.

For this mode of operation, the framer is equipped with a microprocessor written and is controlled internally by a FIFO buffer and LAPD/HDLC formatting circuitry to implement a LAPD/HDLC terminal data link transmission according to ITU-T Q.921 and ISO/IEC 3309 standards.

2.1.3.1 HDLC/LAPD Formatting Circuitry

The HDLC/LAPD formatting circuitry includes the following:

- Automatic generation of FLAG sequences (01111110) when no message is being transmitted and between messages
- Zero insertion mechanism for transparency (a 0 bit is inserted after all sequences of five continuous 1 bits in a message between two FLAGs including the FCS to differ data from FLAG transmission)
- Automatic generation of abort sequence (a sequence of 16 continuous 1 bits)

The formatting circuitry has the capability of calculating the 16-bit Frame Check Sequence (FCS) and transmitting it at the end of the message. Transmitting of FCS is software-selectable by the settings of bit TxFCSEn in Transmit Data Link Control register.

2.1.3.2 FIFO Control Circuitry

The transmit data link side (TDL) of each framer includes a 128-byte FIFO buffer that is additional to a 128-byte receiver side data link FIFO buffer (RDL). The FIFO buffer is filled by the microprocessor with the data bytes to be transmitted for each message and also provides interrupts and status bits to indicate its condition.

Writing to the FIFO

The FIFO buffer is written using the microprocessor interface. Writing a byte each time to the Transmit Data Link Message Byte register (TxDLMsg [7:0] byte) fills the FIFO buffer with a new message. The writing of the message byte adds it to the FIFO buffer.

The Transmit Data Link Message Byte register has two addresses. The low address should be used to write all message bytes except the last byte of the message. The high address is used to write the last byte of the message. The writing to the high address marks the written byte as the end of message byte (EOM). The next byte that is written to the FIFO buffer belongs to a new message.

TDL FIFO Related Interrupts

All TDL FIFO interrupts are maskable individually. Settings in the Transmit Data Link Control register control the enabling and disabling of the interrupts.

The TDL FIFO provides the following interrupts:

- TDL FIFO Near-Empty—(interrupt enabled by setting TxNEIE bit to 1)
  - Turned on when the number of data bytes that remains to be transmitted in the FIFO buffer becomes equal to or falls below the programmable Near-Empty threshold level and the Near-Empty indication is not set.
  - Turned off when the number of data bytes that remained to be transmitted in the FIFO buffer becomes higher than the programmable Near-Empty threshold level.
    The range of Near-Empty threshold settings is 0 to 126, and is set in TxNEThr[6:0] at the Transmit Data Link Threshold Control register. Setting Near-Empty threshold to NE = 0 to 126, means that Near-Empty event is declared when the number of data bytes remaining in the FIFO buffer is equal or less than NE.
- TDL FIFO underrun—(interrupt enabled by setting TxURIE bit to 1)
  - Turned on when the FIFO buffer is empty, if the last message byte that was transmitted did not indicate an end of message byte, and the inner HDLC circuitry requests the FIFO buffer for another byte to transmit.
  - Turned off when the Transmit Data Link FEAC Status register is read.
- TDL message transmitted —(interrupt enabled by setting TxMsgIE bit to 1)
  - Turned on when the last bit of the closing FLAG of a message is transmitted.
  - Turned off when the TxMsg status bit at the Transmit Data Link FEAC Status register is read.

TDL FIFO Related Status Bits

The TDL FIFO status indications are available at the Transmit Data Link FEAC Status register to be read by the microprocessor. They are as follows:

- TDL FIFO Near-Empty—(set and cleared with the interrupt) (indicated by TxNE bit)
- TDL FIFO empty—This status indicates that the FIFO buffer is empty and has no message bytes written to it (indicated by TxEmpty bit).
- TDL FIFO underrun – (set and cleared with interrupt) (indicated by TxUR bit)
- TDL message transmitted—(set and cleared with interrupt). This status indicates that a full message was transmitted including its closing FLAG (indicated by TxMsg bit).
- TDL FIFO full—An indication bit that is set and stays set as long as the FIFO buffer is full—128 bytes are stored inside the FIFO buffer. The FIFO full status can be used in polling mode to check if the FIFO buffer is full and there is no point in writing to it (indicated by TxFull bit).

2.1.3.3 Initial Setup of Transmit Data Link

The TDL is disabled on reset, with no interrupts active. Bits DLMod [2:0] in the Transmit Overhead Insertion 1 Control register control TDL enabling for each mode. The desired interrupt settings, for the Near-Empty FIFO threshold, and the TDL-related options should be set to the desired values through the Transmit Data Link and the Transmit Data Link Threshold Control registers. The insertion of the FCS is software-selectable by setting the TxFCSEn field of the Transmit Data Link Control register.

When only the Data Link is disabled, the FIFO buffer is cleared, and the Near-Empty and Empty status bits are read. If the Near-Empty interrupt is enabled, a Near-Empty interrupt is generated. Before disabling the Data Link, the user should mask its interrupts. If the channel is enabled when disabling the Data Link a repetitive 1s signal is sent. While the Data Link is disabled, the FIFO buffer can still be written.

When both the Data Link and the channel are enabled, if the FIFO buffer is not reset and is not empty, a new message starts after sending two FLAG sequences. If the FIFO buffer is empty, FLAG sequences are automatically transmitted until a new message byte is written to the FIFO buffer.

When the entire channel is enabled after reset or disabled (while data link is enabled), the FIFO buffer is cleared, the Near-Empty and Empty status bits are led and if the Near-Empty interrupt is enabled a Near-Empty interrupt is generated.

When the whole channel is disabled, the following occurs:

- Data Link activities are terminated.
- Data link control settings at the Transmit Data Link and the Transmit Data Link Threshold Control registers are not affected (interrupt enables, Near-Empty threshold, FCS transmission, etc.).
- The channel's old status at the Transmit Data Link FEAC Status register is maintained (status bits maintain their old values and so do interrupts if not disabled earlier).
- The FIFO buffer is not emptied.

2.1.3.4 Sending Message Using the FIFO—Normal Operation

In normal operation when the TDL FIFO buffer is empty, the TDL circuitry generates IDLE flags. When the system has a message to transmit on the data link, it should write it to the FIFO buffer, one byte each time, by writing all data bytes (except the last message byte) to the low address of the Transmit Data Link Message Byte register (TxDLMsg [7:0]). The last byte of the message should be written to the high address of the Transmit Data Link Message Byte register indicating to the TDL circuit that it is the last byte of the message (EOM byte). After EOM, if the FIFO buffer is not FULL, another message can be written following the last EOM byte.

There is no limit to the length of each message, and the FIFO buffer can contain more than one message written to it at a time.

EMPTY and FULL status bits are provided to help the system evaluate FIFO's content and message transmission status, Near-Empty Threshold and Status, Transmitted Message Status indication and interrupt. With the help of these data bits, the system can control its accesses to optimally use the TDL FIFO buffer with minimum accesses.

The internal logic terminates sending FLAG messages as soon as a new message byte is written to the FIFO buffer. The new message is sent until an EOM byte is encountered, which is followed by sending FCS (if enabled) and two FLAG sequences. After sending the closing FLAG of each message, an indication of transmitted message and an interrupt (if enabled) is provided. The next message immediately starts if the FIFO buffer is not empty. If the last transmitted octet was an EOM, FLAG sequences continue to be generated and transmitted.

From the system point of view there are two TDL modes, Interrupt Driven mode and Polling mode.

Interrupt Driven Mode

Unmasking at least one FIFO-related interrupt (Near-Empty, Underrun, or Message Transmitted) enables interrupt driven mode.

Once an interrupt occurs, the microprocessor should read the Source Channel Status register to identify which framer is the interrupt's originator, then read the framer's Interrupt Source (i) Status register to identify which block raised the interrupt at the particular framer (TDL in this case—bit TxDLFEACItr is high). It then reads the Transmit Data Link FEAC Status register to identify the type of interrupt (Underrun, Near-Empty, or Message Transmitted).

There are many available settings and methods handling of interrupts. The proposed handling for normal operation is to read the Transmit Data Link FEAC Status register as the interrupt occurs. If the TDL Near-Empty indication is set, a new block of data bytes are written and transmitted (maximum 128 Near-Empty threshold bytes to safely fill the FIFO buffer). After servicing this interrupt, the system waits for another interrupt.

Polling Mode

Polling mode is effective when TDL function interrupts are masked. In Polling mode, the service routine are executed based on timers. Here, after writing a message byte or a message block of several bytes, the service routine shall wait for N milliseconds (based on the data link rate and the block size written) and poll or sample the Transmit Data Link FEAC Status register to check whether the FIFO buffer is empty or near empty, and if so, write another block. In this mode, TDL status is read before writing to the FIFO buffer.

2.1.3.5 FIFO Special Events

End of Message Event

The system indicates End of Message (EOM) by writing the last byte of the message to the high address of the Transmit Data Link Message Byte register. When the TDL circuitry encounters the EOM indication set for a byte in the FIFO buffer, and after transmitting the last byte, it checks whether FCS sequence sending is set (bit TxFCSEn is set to 1 in Transmit Data Link Control register). If set, FCS bytes are sent, followed by at least two FLAG sequences before starting transition of the next message in the FIFO buffer (if there is one).

If the EOM byte is the last byte in the FIFO buffer, the TDL circuitry continues transmitting FLAG sequences (after transmitting the last byte and FCS, if enabled) until a new message byte is written to the FIFO buffer.

Near-Empty Event

The Near-Empty event is declared when the number of bytes remaining in the TDL FIFO buffer is less than or equal to the number programmed at the Near-Empty threshold the value of which can be set to 0 to 126. The Near-Empty event results in an interrupt, if enabled. It is used to help the system to control and use the FIFO buffer

FIFO Underrun

A FIFO underrun condition is caused when the internal transmit logic has emptied the FIFO buffer without encountering an end of message and the transmit logic request for the next byte to be transmitted. This causes an Abort sequence (16 consecutive 1s) to be transmitted followed by at least two FLAG sequences. After an ABORT + two FLAG sequences, the transmit internal circuitry is ready to start transmitting a new message as soon as it is written to the FIFO buffer and writing to the FIFO buffer is allowed.

As soon as an underrun condition is declared internally, an interrupt is issued (if enabled) and the FIFO buffer prevents additional data bytes to be written to it. The underrun interrupt is cleared upon reading the Transmit Data Link FEAC Status register. Writing to the FIFO buffer is enabled again only after the interrupt is cleared.

The system checks the amount of data bytes that may have been written and lost between the time the first underrun interrupt occurred and the system reads the FIFO status register and senses a underrun condition.

Writing to FIFO when FIFO is Full

When the FIFO buffer is FULL, writing to the FIFO buffer by the microprocessor is ignored by the circuit, and no indication for ignoring written data during FIFO Full condition is supplied. Neither data bytes and pointers of the FIFO buffer, nor the HDLC formatting and message providing mechanisms are not affected by writing into the FIFO during FIFO FULL condition.

FLAG Transmission

The TDL machine generates and transmits flag sequence (01111110) automatically in the following cases:

1. After enabling the data link, FLAG sequences are transmitted automatically until a new message starts. At least two FLAG sequences are transmitted before the new message begins.
2. Between two consecutive transmitted messages, two FLAG sequences are automatically inserted. In case the FIFO buffer contains more than one message (after FCS sequence is transmitted, if FCS transmission is enabled), the transmitter sends two FLAG sequences after the last byte of the previous message is sent before starting transmission of the first byte of the new message (the next byte to be transmitted at the FIFO buffer after an EOM byte).
3. If the current message is the last message in the FIFO buffer (FIFO is empty, and the last byte is indicated as an end of message byte), the transmitter sends FLAG sequences continuously after the end of the message and as long as the FIFO buffer is empty.
4. After sending one abort sequence (sixteen 1s in underrun condition) the transmitter automatically starts transmitting FLAG sequences for as long as the FIFO buffer is empty (at least two FLAG sequences are transmitted before starting a new message).

Abort Message Transmission

Abort is defined in ISO-3309 as a sequence of seven or more continuous 1s.

The abort message that is generated by the transmit circuitry is a sequence of 16 continuous 1s. It is generated automatically as a result of an underrun condition. When underrun occurs, the transmit generates only one abort sequence followed by at least two FLAG sequences before transmitting the next message.

For the system to intentionally send an ABORT sequence during a message transmission without damaging other messages stored in the TDL FIFO buffer, the system should stop writing new data bytes to the FIFO buffer. In addition, the system should not write an EOM data byte, and wait until the FIFO buffer is emptied. When the FIFO buffer is emptied, an underrun occurs which results in sending the desired Abort sequence.

2.1.4 FEAC Channel Transmission

A description of a FEAC channel is applicable to each framer on the device.

There are three sources available for transmission of FEAC bits in DS3 C-bit parity mode that are set at the Transmit Overhead Insertion 1 Control register by bits ExtDat and ExtFEAC/PD for each framer individually: from data, from an external pin, or generated internally using the Transmit FEAC Channel Byte register and the microprocessor. When TxFEAC bits source is from data (ExtDat = 1) or from an external pin (ExtFEAC/PD = 1 and ExtDat = 0), no operation is done by the framer except inserting TxFEAC bits to the transmitter data stream at the proper time (when TxFEAC bits are inserted from an external pin). When TxFEAC is internally generated (ExtFEAC/PD = 0 and ExtDat = 0), the code word to be transmitted at the TxFEAC is taken from the Transmit FEAC Channel Byte register.

When TxFEAC is generated internally, the Transmit FEAC Channel Byte register controls the byte to be transmitted on the TxFEAC channel. All messages transmitted on this channel are in the form 0xxxmmm011111111. The right-most bit of this sequence is the first bit transmitted on the channel. Only the 0xxxmmm0 byte of the 16-bit message is written to the Transmit FEAC Channel Byte register; the eight consecutive 1s of the FEAC message are transmitted automatically.

The transmitter FEAC mechanism provides the microprocessor with an interrupt and a status bit indicating that the interrupt's source is the TxFEAC (transmit FEAC channel Interrupt bit [TxFEACltr] at the Transmit Data Link FEAC Status register). The setting of bit TxFEACIE at the Feature3 Control register can mask the interrupt. The transmitter FEAC interrupt indicates that the last message was sent and a new message byte can be written to the Transmit FEAC Channel Byte register.

A reset or returning to enable after a disable clears the TxFEAC interrupt (if it was issued). A new interrupt is not issued until a new FEAC message is written and sent, and until then, repetitive 1s are sent.

Activating transmission of AIS in C-bit parity mode in the middle of a FEAC message transmission terminates the FEAC message. The FEAC state machine returns to IDLE state, and no transmitter FEAC interrupt is issued. When AIS transmission is deactivated, the transmitter sends IDLE sequence (repetitive 1s) on the FEAC channel until a new message byte is written to Transmit FEAC Channel Byte register controls.

Transmission of yellow alarm or DS3 IDLE code in C-bit parity mode has no effect on TxFEAC channel transmission.

Two modes of transmitting a FEAC message available using the Transmit FEAC Channel Byte register are the Single code-word mode and the repetitive code-word mode. These are set by bit FEACSin in the Feature3 Control register.

2.1.4.1 Single Code-Word Mode

In this mode, to initiate transmission of a message byte in the TxFEAC channel, the desired byte, in the form 0mmmxxx0 is written into the Transmit FEAC Channel Byte register (TxFEAC [7:0]).

Each time a FEAC written message is sent (eight consecutive 1s, followed by TxFEAC written byte), an interrupt is issued on the INTR* output pin (if interrupt is enabled) to indicate that the last message was sent and to request a new byte from the processor. The transmit FEAC channel Interrupt bit (TxFEACltr) at the Transmit Data Link FEAC Status register is set high. The Transmit Data Link FEAC Status register must be read to clear the interrupt. After sending a written message, if a new message byte is not written to Transmit FEAC Channel Byte register, the old message is continuously, issuing an interrupt for each time the message is sent. Interrupts from the TxFEAC channel occur at a rate of approximately one interrupt per 1.7 ms. If a 1 is written in either the MSB or LSB position of the TxFEAC field, then continuous transmission of idle flags (repetitive 1s) is enabled (starting after the current message transmission is complete). No interrupts are issued until a byte of the proper format is written to the Transmit FEAC Channel Byte register. Interrupts from the TxFEAC channel transmitter are indicated by appearing on Transmit FEAC Channel Interrupt bit of the framer that generated it (TxFEACltr bit).

2.1.4.2 Repetitive Code-Word Mode

In this mode, each new code word that is written to the Transmit FEAC Channel Byte register is transmitted repetitively (eight consecutive 1s, followed by TxFEAC written byte). Every 10 repetitive times the message is transmitted, an interrupt is issued on the INTR* output pin (if transmitter FEAC interrupt is enabled) to request a new byte from the processor. TxFEACltr bit at the Transmit Data Link FEAC Status register is high. The interrupt is cleared with the reading of the Transmit Data Link FEAC Status register. If a new byte is not written to the Transmit FEAC Channel Byte register after an interrupt was issued, the old message is transmitted continuously (it is transmitted for another 10 times until the Transmit FEAC circuitry checks again whether a new message byte was written to Transmit FEAC Channel Byte register). If a new message byte is written the transmitter first finish sending the old message and then start sending the new written message. If a 1 is written in either the MSB or LSB position of the TxFEAC field, continuous transmission of idle flags (repetitive 1s) is enabled (after transmitting the last message 10 times). Interrupts are not issued until a byte of the proper format is written to the Transmit FEAC Channel Byte register.

NOTE: There is no TxFEAC channel transmission in either E3 mode or DS3 M13/M23 modes

2.1.5 Test Equipment—Error Insertion

The CX28342/3/4/6/8 framer provides the ability to insert errors intentionally in the transmitted data stream (for each framer individually) by using the Error Insertion Control registers. The Error Insertion register contains a control bit for each available error. Setting the relevant bit at the Error Insertion Control registers causes insertion of one requested error at the next valid opportunity for each error. Once the error is inserted, the relevant control bit is automatically cleared. Several different error insertions can be set at the same time by setting more than one error control bit; each error selection is cleared when the appropriate error is inserted. Before setting the control bits for another error insertion, they must be polled and the relevant control bits, for the desired errors, should be checked for zero. Writing zero to the control bits does not affect their settings.

The errors that can be inserted, and their effect on the transmitted data, are specified for each basic mode of operation.

2.1.5.1 DS3 Mode

In DS3 mode (both in M13/M23 and in C-bit parity mode), errors listed in Table 2-4 can be transmitted by setting bits at the Error Insertion1 Control register.

Table 2-4. Setting the Error Insertion1 Control Register in DS3 Mode (1 of 2)

Error	Bit	Set to	Description
Framing F	FrmErrF	1	A single F-bit error is inserted by inverting the next transmitted F-bit (only one bit).
Framing M	FrmErrM	1	A single M-bit error is inserted by inverting the next transmitted M-bit (one M-bit).
P-bit Parity	ParErr	1	Transmission of incorrect value in the two P-bits (i.e., incorrect parity calculation over the previous frame). In this case, the next two P-bits of a single frame to be transmitted are inverted.
P-bit parity disagreement	ParDgrErr	1	Transmission of unequal P-bits at the next opportunity (performed by inverting the next transmitted P-bit).
CP bit error (path parity)(1)	CPErr	1	Transmission of an incorrect value in the three CP bits in an M-frame. It is performed by inverting the three CP bits of a single M-frame at the next opportunity.
RAI	YelErr	1	Transmission of the opposite value of the M-frame X-bits than the expected/set value. This is performed by inverting the two X-bits transmitted of a single M-frame at next opportunity. Thus, if RAI is set to be transmitted, the X-bits are set to 1 (instead of 0). If RAI alarm is not set to be transmitted, both X-bits are transmitted as 0 (instead of 1).
X-bit disagreement	XdgrErr	1	Transmission of opposite values of both X-bits in an M-frame. The setting of XdgrErr to 1 causes the two X-bits of a single M to be transmitted with opposite values by inverting the next X-bit to be transmitted.

Table 2-4. Setting the Error Insertion1 Control Register in DS3 Mode (2 of 2)

Error	Bit	Set to	Description
FEBE(2)	FEBEErr	1	Transmission of opposite of the expected code in FEBE bits (the three C-bits in Subframe 4). When FEBE bits are set to be internally-automatically generated, setting a FEBE error insertion results in transmission of a 111 code (no error code) in FEBE bits of a single M-frame (at the next opportunity) if a frame error or a C-bit parity error is detected. Otherwise, it transmits the value stored in FEBEC/PT[1:3] in the Feature1 Control register.

FOOTNOTE:
(1) In DS3 C-bit parity mode.
(2) Active in C-bit parity only.

2.1.5.2 E3-G.751 Mode

In the E3-G.751 mode of operation, setting bits at the Error Insertion1 Control register can generate the errors listed in Table 2-5.

Table 2-5. Setting the Error Insertion1 Control Register in E3-G.751 Mode

Error	Bit	Set to	Description
FAS	FrmErrF	1	Causes one bit of the next FAS sequence to be inverted.
RAI	YelErr	1	Transmission of the opposite value of A-bit than expected or set. In this case the next transmitted A-bit is cleared to 0 if an RAI should be transmitted, and set to 1 if RAI is not expected (done by inverting the next A-bit before transmission).

2.1.5.3 E3-G.832 Mode

In the E3-G.832 mode of operation, setting bits at the Error Insertion1 Control register can generate errors listed in

Table 2-6. Setting the Error Insertion1 Control Register in E3-G.832 Mode

Error	Bit	Set to	Description
Framing Error (FA error)	FrmErrF	1	Transmission of one framing bit error. This causes one bit of the next FA sequence to be inverted.
BIP-8 parity	ParErr	1	Transmission of a single incorrect bit in the next BIP-8 sequence by inverting it before transmission.
RDI	YelErr	1	Transmission of the opposite value of RDI-bit than expected or set. The next transmitted RDI-bit is cleared to 0 if an RDI should be transmitted, and set to 1 if RDI is not expected (done by inverting the next RDI-bit before transmission).
REI (FEBE)	FEBEErr	1	Transmission of the opposite value to the expected one (by automatic generation or its inserted value from external pin or with payload) at the next MA REI-bit position. This is done by inverting the next transmitted MA REI-bit.

NOTE: Error insertion can be performed by the system only on Overhead bits that are set to be automatically generated or taken from a register. Setting error insertion on Overhead bits where the source is set to be from TEXT pin, or inserted with payload, produces undefined results.

2.1.5.4 Line Coding Errors

In all basic modes of operation, line code errors can be forced when the transmitter line side is operating in AMI or rail (HDB3/B3ZS encoding) mode.

In AMI or rail mode, a bipolar violation (BPV) can be inserted by setting the LCVBPV bit in Error Insertion2 Control register. The next 11 arriving after the bit is set is changed to 1V (this restriction, rather than just reversing the next 1, prevents inadvertently creating a zero-substitution sequence). Then, the encoding circuitry adjusts itself to the reversed signal, causing the following output to be opposite the one that would have been produced had this error not been introduced; otherwise each error insertion would result in two consecutive BPVs. Figure 2-13 illustrates an example.

In rail mode, an illegal substitution (IllSub) can be inserted by setting the LCVIllSub bit in Error Insertion2 Control register. The next 000 (in DS3) or 0000 (in E3) arriving after the bit is set, is reversed (00V to 10V or vice versa in DS3; 000V to 100V or vice versa in E3). Then the encoding circuitry adjusts itself to the reversed signal, causing the following output to be the reverse of the one that would have been produced had this error not been introduced; otherwise each error insertion would also result in a BPV.

Figure 2-13 illustrates the possible bipolar outputs (in DS3 B3ZS) resulting from a given unipolar input (assumes ideal conditions where there is no delay between the error insertion request and its execution):

Line 1—Unipolar input (from transmitter circuitry to encoder) of 13 bits, marked A to M

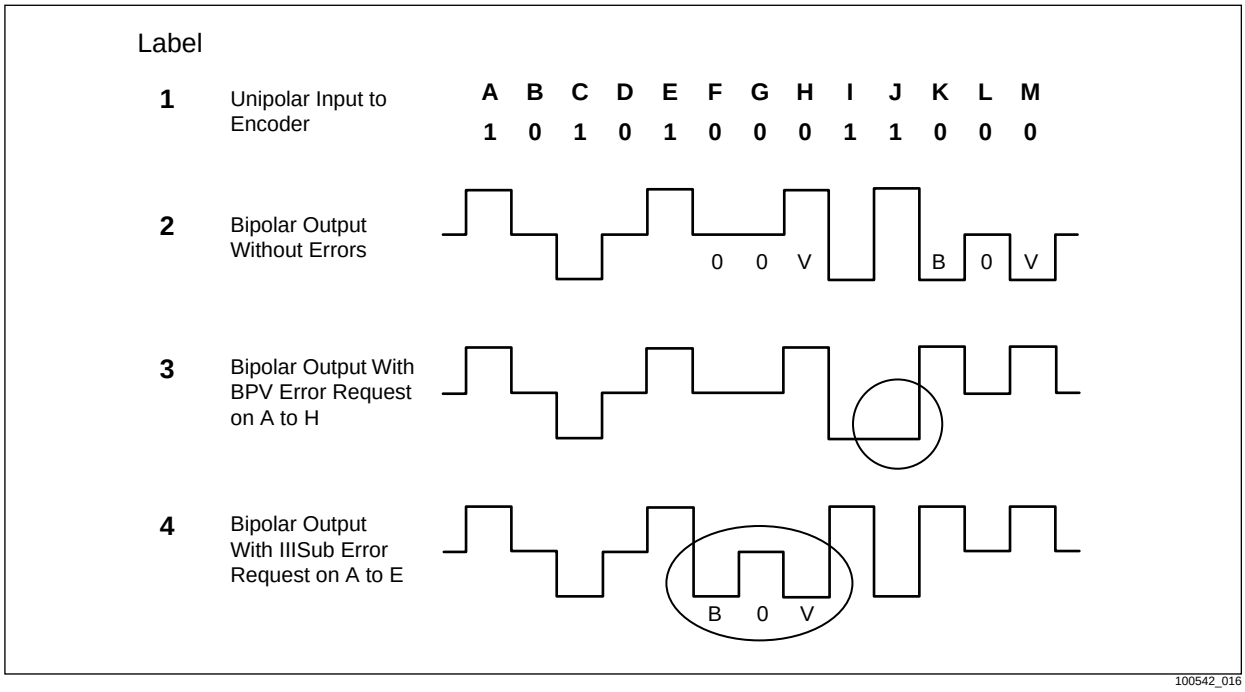
Line 2—Bipolar output (from encoder to line) without errors

Line 3—Bipolar output with BPV error insertion requested on bits A to H

Line 4—Bipolar output with IllSub error insertion requested on bits A to E

The actual erroneous bits are circled in the Figure 2-13. Bits following an error insertion are reversed compared to the original line 2 (i.e., bits K–M in line 3, and I–M in line 4).

Figure 2-13. Line Coding Error Insertion



2.2 Receiver Operation

This section describes the receiver operation of the CX28342/3/4/6/8 device.

2.2.1 Line-Side Interface

The line-side receive interface of CX28342/3/4/6/8 consists of four input signals:

LINECK—Raw clock derived from incoming data (44.736/34.368 MHz)

RXCKI—Dejittered version of LINECK

RXPOS/RXNRZ—In rail/AMI-mode, carry positive polarity data. In unipolar-mode, carry NRZ data

RXNEG/LCVI—In rail/AMI-mode, carry negative polarity data. In unipolar-mode, report an LCV (or tied to ground)

The line-side interface can be placed in one of three different modes by setting the NRZMod and RxAMI fields of the Feature1 Control register. Table 2-7 describes the modes.

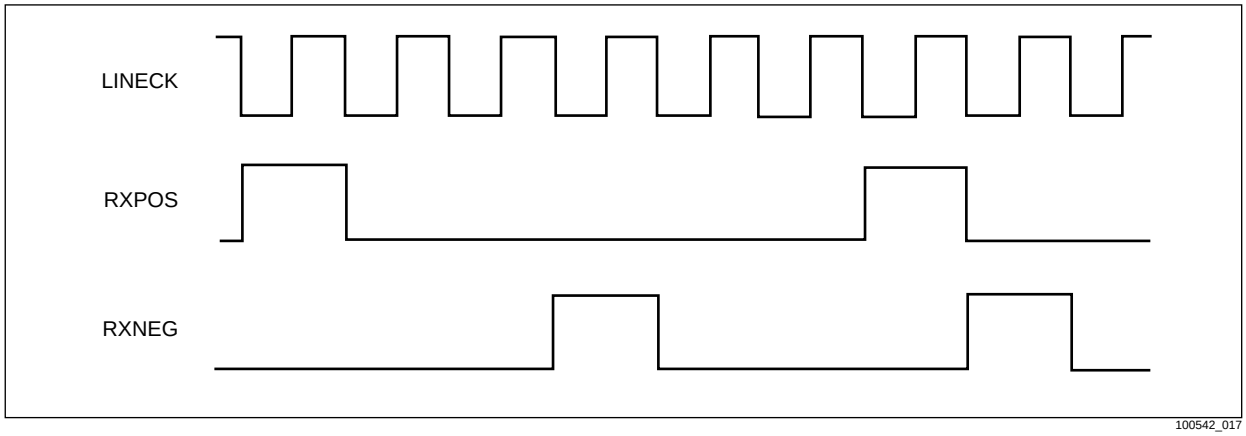
Table 2-7. Line-side Interface Modes

Mode	Description
Rail	2 data pins, B3ZS line code for DS3, HDB3 line code for E3
AMI	2 data pins, AMI line code
Unipolar	1 data pin, NRZ line code

The data stream is sampled from the data (RXPOS and RXNEG, or RXNRZ and LCVI) pins on either the rising or the falling edge of LINECK (based on the value in the LRxCkRis field of the Feature5 Control register). The data should be one full clock period wide. Figure 2-14 illustrates the relation between data (100100110) and clock assuming data is sampled on the rising edge of the clock.

The CX28342/3/4/6/8 decoder converts the bipolar signal to a unipolar stream based on AMI/B3ZS/HDB3 line code and detects LCV, if any. The decoder is bypassed in NRZ (unipolar) mode.

Figure 2-14. Receiver Line Side Inputs



Decoding per ITU-T G.701 AMI line code involves substituting 1 for RXPOS or RXNEG high, and 0 for RXPOS and RXNEG low (an RXPOS or RXNEG high appearing on the same pin as the previous high [a bipolar code violation; marked as V below] is still converted to 1).

Decoding per ITU-T G.703 B3ZS line code, involves AMI-style decoding coupled with substitution of a 100V or 110V sequence with a 1000 sequence (a 100V sequence appearing where a 110V is expected, or vice versa, is still converted to 1000).

Decoding per ITU-T G.703 HDB3 line code, involves AMI-style decoding coupled with substitution of a 1000V or 1100V sequence with a 10000 sequence (a 1000V sequence appearing where a 1100V is expected, or vice versa, is still converted to 10000).

If the clock dejitter FIFO buffer is enabled, LINECK clocks data from the line, through the decode logic (unless bypassed), and into the dejitter FIFO buffer. The data stream is clocked out of the FIFO buffer and through the rest of the receive logic using RXCKI. If the clock dejitter FIFO buffer is disabled, LINECK clocks data through the entire receiver logic, and RXCKI should be tied low.

2.2.2 System-Side Interface

The system-side receive interface consists of four output signals:

RXGAPCK—Data clock, gapped over user-defined bits

RXDAT—Data (all payload and overhead)

REXTC—Receive supplementary clock, software-adjustable (see Section 2.)

RXMSY—Frame synchronization signal

Either RXCKI or LINECK clocks the internal circuits (see Section 2.), from which both output clocks (RXGAPCK and REXTCK) are derived. Output signals (RXDAT and RXMSY) change on the rising edge of the internal clock. This is equivalent to changing on either the rising edge or the falling edge of the output clocks (depending on whether the output clocks are set to be non-inverted or inverted, as defined in the RxInvClk field of the Feature5 Control register). The signals are clocked into the system's circuit with the opposite edge of the output clock.

RXGAPCK functionality is software-selectable to one of five modes:

1. Ungapped (tick on every payload and Overhead bit)
2. Overhead gapped (tick on every payload bit)
3. Non-Cj gapped (tick on every payload and Justification Control bit)
4. Non-stuff gapped (tick on every payload and Stuff Opportunity bit)
5. Non-Cj and stuff gapped (tick on every payload, Justification Control bit and Stuff Opportunity bit)

The RXMSY signal has two modes based on the selection of the RxOvhMrk field of the Feature5 register:

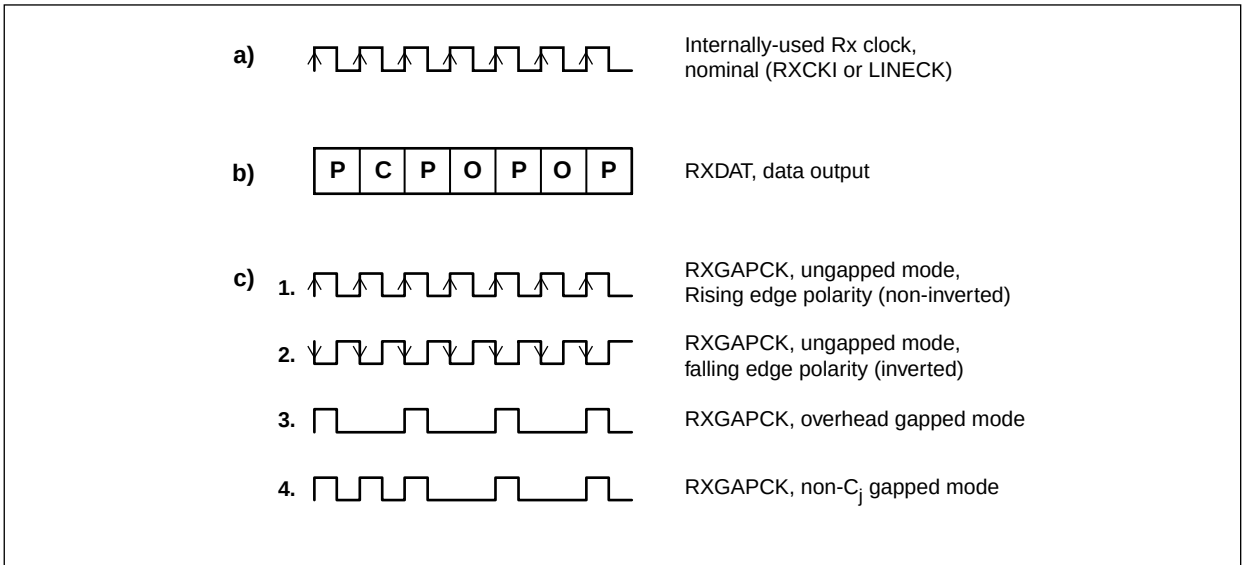
- As a frame synchronization signal, it rises from low to high on the first bit of each frame. It returns to low after the third M-bit in DS3 mode. It returns to low after the first Cj-bit in E3-G.751 mode, and it returns to low after the last bit of the GC byte in E3-G.832 mode.
- As an overhead marker signal, it is low on all Overhead bits and high on all payload bits.

NOTE: Justification control and Stuff Opportunity bits are viewed as Overhead bits.

Figure 2-15 illustrates the ideal behavior of system-side outputs, in several modes, for a general data stream that represents seven bits (bits 1, 3, 5, and 7: payload [*P*]; bit 2: C_j overhead [*C*]; bits 4 and 6: non-C_j overhead [*O*]; bit 3 is the last bit of one frame, bit 4 is the first bit of next frame).

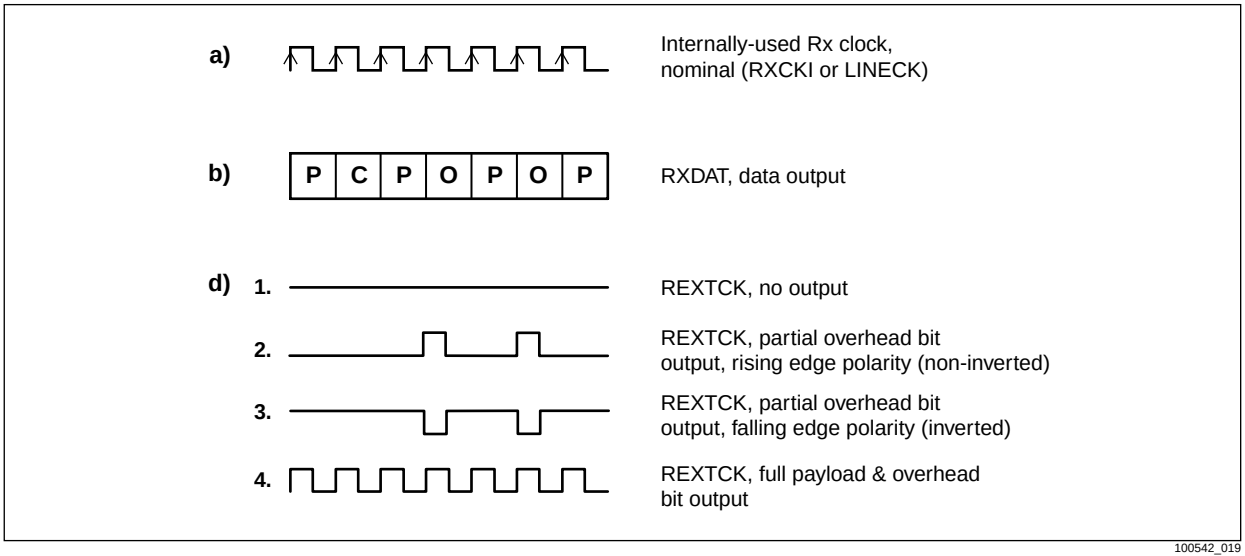
a. Internally-used receiver clock (RXCKI or LINECK).
b. RXDAT, data output.
c. RXGAPCK, in three of the five modes (ungapped, overhead gapped, non-C_j gapped), each available at either rising or falling edge polarity (only showed for ungapped, but valid for all five modes).

Figure 2-15. Receiver System Side Outputs [RXGAPCK]



d. REXTCK, in three representative selections (no output, partial Overhead bit output, and full payload and Overhead bit output). Each is available at either rising or falling edge. Figure 2-16 illustrates partial Overhead bit output, but it is valid for all selections.

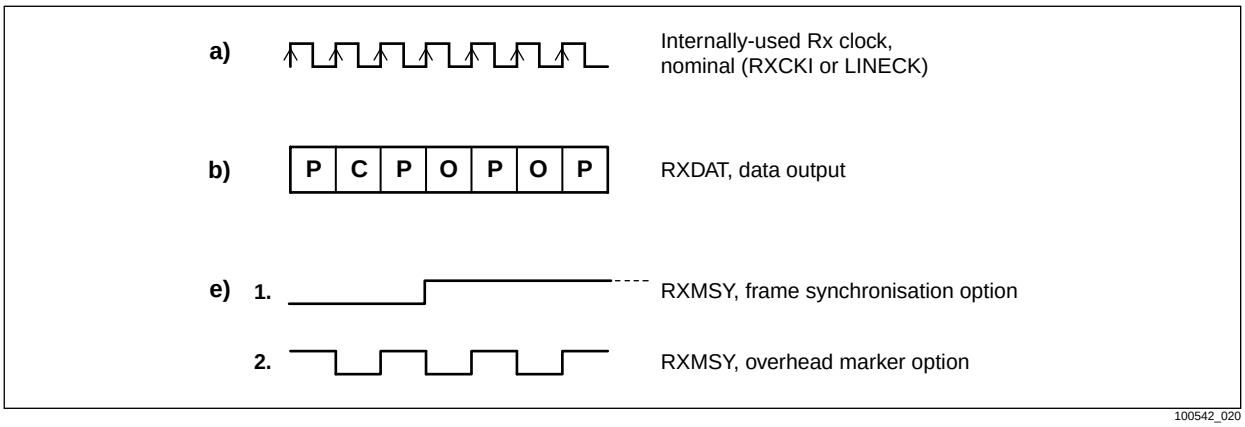
Figure 2-16. Receiver System Side Outputs [REXTCK]



e. Figure 2-17 illustrates two options of RXMSY signal, frame synchronization signal, and overhead marker signal.

In cases where the system may find this useful, options are available (via the RxAll1 and RxAIS fields of the Feature5 Control register) to produce either an all-1s or an AIS output, respectively, on the RXDAT pin, completely masking the received input. In addition, an automatic assertion of an all-1s stream is available (via the RxAutoAll1 mode control bit in Feature5 Control register). When the automatic mode is on, detection in the receiver of one or more of the following events produces an all-1s sequence. The events are LOS, OOF, AIS, Idle in DS3 mode, and LOS, OOF, AIS in E3 mode. Termination of all these events, terminates the all-1s stream assertion. Notice, however, that the data stream arriving from the line is otherwise normally handled and results in all the expected indications relating to internal-processing and performance-monitoring, without regard for these options.

Figure 2-17. Receiver System Side Outputs



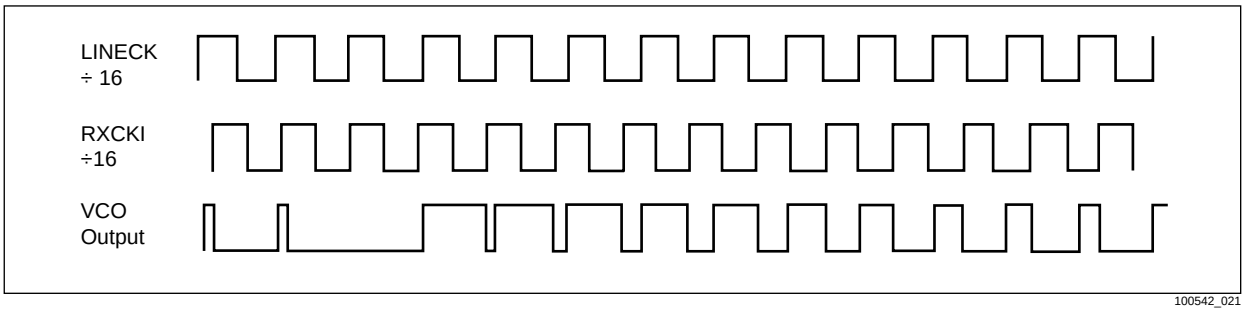
NOTE: During an OOF condition, the system-side interface continues to function relative to the previous framing position (the RXMSY, RXGAPCK, and REXTCK signals are relative to the previous framing position.) until a new framing template is located, and the OOF condition is turned off.

2.2.3 Clock Dejitter FIFO

The receiver circuit contains a 16-bit FIFO buffer immediately following the bipolar-to-unipolar decoding logic (or the unipolar input in unipolar-mode) to provide jitter elasticity up to ± 5 line clock cycles. The data stream is clocked into the FIFO buffer with the incoming LINECK clock. The data stream is clocked out of the FIFO buffer and into the remaining receiver circuitry by RXCKI, which is a dejittered version of LINECK. The FIFO circuit provides a Voltage-Controlled Oscillator (VCO) control signal to indicate the phase relationship of FIFO input and output clocks. Both clocks are divided by 16 internally to derive the VCO output, as illustrated in Figure 2-18. This signal can be used to control the clock recovery circuit producing the smoothed RXCKI.

NOTE: The VCO signal is active all the time, even during channel disable and reset.

Figure 2-18. VCO Output Signal Timing



The FIFO circuit is bypassed, and all receiver circuitry is clocked with LINECK if the RxFIFEn field of the Feature5 Control register is cleared; in this case RXCKI should be tied to ground.

See Appendix A for analysis and reference design.

2.2.4 Overhead Bit Recovery

The bit stream arriving from the line-side is functionally divided into two categories, payload and overhead. See Appendix B.

2.2.4.1 Processing of Overhead Bits

The Overhead bits are processed in several ways, they are as follows:

External-Data—All overhead and payload bits exit on the RXDAT pin; a gapped clock is supplied for skipping Overhead bits, RXGAPCK (see Figure 2-15). This clock's gaps come in one of five types: all Overhead bits, all Overhead bits except Justification Control bits, all Overhead bits except Stuff Opportunity bits, all Overhead bits except justification control and Stuff Opportunity bits, or none are gapped (software-selectable by setting the AllOVHDat and RxCjDat fields of the Receive Overhead Control register).

Internal—Several fields are internally evaluated for alarm and status detection (framing bits, RAI/RDI, FEBE/REI, parity, and path parity bits) or supplied to the system via microprocessor-side buffers or registers (DL, FEAC, PT, PD/MI, TM/SSM, and AIC), described in Section 2..

External-Extended—All overhead and payload bits exit on the RXDAT pin; a clock is supplied for marking various sets of overhead and payload bits (REXTCK) (see Figure 2-16). The output is based on the settings of REXTCK Control register fields:

- In DS3 C-bit Parity, the eight independently-selectable field combinations are as follows:
  - F-bits + M-bits + X-bits + P-bits
  - Cb11 (AIC)
  - Cb13 (FEAC)
  - Cb3 (Path Parity)
  - Cb4 (FEBE)
  - Cb5 (Data Link)
  - Cb12 + Cb2 + Cb6 + Cb7 (Reserved)
  - All Overhead bits + all the payload (effectively a full serial stream)
- In DS3 M13/M23, the four independently-selectable field combinations are as follows:
  - F-bits + M-bits + X-bits + P-bits
  - C-bits
  - Stuff bits
  - All Overhead bits + all the payload (effectively a full serial stream)
- In E3-G.751, the six independently-selectable field combinations are as follows:
  - FAS
  - A-bit
  - N-bit
  - C_j-bits
  - Stuff bits
  - All Overhead bits + all the payload (effectively a full serial stream)

- In E3-G.832, the eight independently-selectable field combinations are as follows:
  - FA + EM + RDI + PT
  - TR
  - REI
  - PD/MI
  - TM/SSM
  - NR
  - GC
  - All Overhead bits + all the payload (effectively a full serial stream)

NOTE: These modes are ***not*** mutually exclusive, i.e., the modes set for REXTCK and RXGAPCK do not interfere in any way with each other or with the internal processing of overheads).

2.2.4.2 Internal Processing of Overhead Bits

The internal logic is responsible for continuously identifying and monitoring the framing bits (i.e., F-bits, M-bits, FAS, and FA) to recover, maintain, and identify loss of frame alignment. The analysis of these bits governs identification of the Framing Bit Error (FBE), Out of Frame (OOF), and Severely Errored Frame (SEF) indications. DS3's maximum average reframe time is less than 1.5 ms, and E3's maximum average reframe time is less than 1 ms.

Control over the frame-search mechanism is available through the RefrmStp bit in the Feature5 Control register:

- When this bit is set, no frame-search is conducted (regardless of OOF status)
- When this bit has been cleared, frame-search resumes, shifted forward by one bit from the current frame position, until a new framing is located
- When this bit is clear, searching occurs in response to an OOF status

To produce a forced reframe, the microprocessor usually needs two write cycles, the first to write a 1 to the bit, the next to write a 0 to it. Activating this forced reframe does *not* transfer the receiver into OOF. The receiver circuit actually moves its framing template due to forced reframe only after the criteria for in frame have been met for the new position. The status of the frame-search mechanism is open to inspection through the ReFrm bit of the Maintenance Status register.

RAI/RDI bits (i.e., X-bits, A-bit, and RDI) are continuously monitored and their value mirrored through the RAI/RDI indication. Similarly, FEBE/REI bits (i.e., Cb4 and REI) are monitored and their value mirrored through the FEBE/REI indication. In case of X-bits, any disagreement between the two bits is also noted through the X-bit disagreement indication.

For each frame, parity is calculated according to the definitions for that frame type, and is compared to that found in the parity/path-parity bits (i.e., P-bits, Cb3, and EM). Any discrepancy is flagged through the parity error and path-parity error indications. In case of P-bits, any disagreement between the two bits is noted via the P-bit disagreement indication.

The AIC bit (Cb11) in DS3 C-bit parity is always 1; while the same bit in DS3 M13/M23, being a justification bit, is either 0 or 1. An 8-bit register (ReceiveAICByte Status register) containing the AIC bits from eight consecutive frames is provided for polling and system verification of the bit.

Internal processing of the terminal data link bits (i.e., Cb5, N-bit, NR, and GC) as HDLC/LAPD channels makes their contents available to the system through an internal 128-byte FIFO buffer; this mechanism is fully described in Section 2. It is not possible to use this internal mechanism for non-HDLC channels.

Messages flowing on the FEAC (Cb13) channel are supplied to the system via a dedicated register.

Non-alarm fields of the MA byte (i.e., PT, PD/MI, and TM/SSM) are available for inspection through the microprocessor interface. Their contents (three bits for PT, two bits for PD/MI, one bit for TM, and four bits for SSM) are saved on every E3-G.832 frame in dedicated registers (RxMAPT, RxMAPD, and RxMATM fields of the E3-G.832 MAFields Status register; RxSSM field of the E3-G.832 SSMField Status register). The host processes poll these fields to detect changes in their values. The RxSSM field, on a multiframe boundary (i.e., when MI is 11), stores the 4-bit SSM field, spread over a four-framed multiframe based on the MI field. Selection of whether the framer functions in TM or SSM mode is through the SSMEn field of the Feature4 Control register.

There is no internal processing of justification control, stuff opportunity, reserved, and TR fields.

2.2.5 Performance Monitoring

Performance monitoring function is available through event indicators, counters, and interrupts. An event indicator represents an event, such as parity error, or a change of status, such as out-of-frame. These event indicators can be the cause for an interrupt or the increment of a event counter. The event indicators are BPV, EXZ, LCV, FBE, PER, PBD, PPER, XBD, FEBE/REI, LOS, OOF, SEF, AIS, IDLE, and RAI/RDI.

These event indicators are externally identifiable through interrupts, counters or the status registers they affect. All the counters used to count the events are 16 bits long except the LCV counter, which is 24 bits long. If these counters are read once per second, the size of the counters guarantees non-saturation in normal conditions (assuming a BER of less than or equal to 1E3).

Depending on the settings of the Counter Interrupt Control register, the counters function either in saturation mode or roll-over mode.

If the interrupt associated with a specific counter is masked, the counter operates in the saturation mode. In this mode, the counter counts up to the highest possible value and turns on a saturation indication bit in the Counter Interrupt Status register. The counter and the indication bits are cleared when read.

If the interrupt associated with a specific counter is unmasked, the counter operates in the roll-over mode. In this mode, the counter resumes counting from zero after counting up to the highest value. An interrupt is generated, and an interrupt identification bit is set in the Counter Interrupt Status register. The counter and the status register are cleared when read.

NOTE: In reading 16-bit/24-bit counters, software should read the low byte first and then the high byte/bytes. The counters do not miss or double count any errors during the microprocessor reads. At reset all counters are cleared.

When the INTR* pin is active, an appropriate interrupt identification bit is active or set. Unless otherwise qualified, the interrupt is associated with the identification bit, and both are cleared when the identification bit is read. The status indication bits often parallel the interrupts and can be used for applications preferring polling to interrupts. Once an interrupt occurs the microprocessor should read the SrcChnl1-SrcChnl4 fields of the Source Channel Status register to identify the interrupt originating channel. Once the channel is identified then read the Interrupt Source Status register to identify which sub-block initiated the interrupt. Finally read the interrupt identification fields of the Status Indication register for that sub-block to identify the type of interrupt. All interrupts are masked on reset. They are unmasked or made active by setting the appropriate fields in the AlarmStartInterrupt and AlarmEndInterrupt registers.

NOTE: The presence of one event indicator does not inhibit the other events from occurring nor inhibit the other data channels (Data Link or FEAC). For example, FBE is still active in OOF, and internal datalink processing is still active in AIS.

The following sections describe the various event indicators encountered in DS3/E3.

2.2.5.1 Bipolar Violation (BPV), Excessive Zeros (EXZ), and Line Code Violation (LCV)

A BPV is defined as the occurrence of a signal of same polarity as the previous one in an AMI mode or rail mode pulse sequence. An EXZ is defined as the occurrence in rail mode of more than two DS3 or three E3 consecutive 0s, regardless of the length of the zero string.

A LCV is defined as the occurrence of either EXZ or BPV, excluding those that are part of the zero substitution code in DS3 mode. In E3 mode, the LCV is defined as the occurrence of two consecutive BPVs of the same polarity.

In rail mode (B3ZS/HDB3), LCV and EXZ events are counted. In AMI mode BPV events are used to increment the LCV counter. In unipolar mode, only LCV is valid, and the LCV (defined as a pulse on RXNEG/LCVI pin) counter is updated.

2.2.5.2 Loss of Signal (LOS)

In DS3, LOS is declared when there are no signal pulses of either polarity over a period of 100 contiguous pulse intervals in rail mode. The LOS event is terminated when the pulse density equals or exceeds 33% over a period of 100 contiguous pulse intervals. The same definition is true in AMI mode.

In E3 mode, LOS is declared when there are no signal pulses of either polarity over a period of 100 contiguous pulse intervals in rail mode. The LOS event is terminated when the pulse density equals or exceeds 25% over a period of 100 contiguous pulse intervals. The same definition is true in AMI mode. In unipolar mode, LOS event is undefined.

When a LOS is initiated, it generates a LOSStrt interrupt indication and sets the LOS status indication bit (the LOSAlm field of the Maintenance Status register). Upon the termination of the LOS event, the LOS event generates a LOSEnd interrupt indication and clears the LOS status indication bit.

In the presence of LOS in the E3 and DS3 modes, if the Auto RAI field is set in the Transmit Overhead Insertion 1 Control register, RAI/RDI is transmitted on the transmit stream.

In the presence of LOS in the E3 and DS3 modes, if the RxAutoAll1 field is set in the Feature5 Control register, an all-1s sequence is transmitted on RXDAT towards the receive system side.

2.2.5.3 Framing Bit Error (FBE)

In E3, an FBE event occurs when a framing bit (FAS, F, M, or FA) in the receive stream is different from the expected value. The FBE event increments a FBE counter.

In DS3 C-bit parity mode, an FBE event is valid and counted. If internal FEBE generation is programmed for the transmitter by clearing the ExtFEBE/Cj-bit in the TransmitOverheadInsertion1 Control register, the detection of a framing bit error in the receiver causes transmission of FEBE error code by the transmitter.

2.2.5.4 Out of Frame (OOF)

In DS3 mode, an OOF event is declared, if in the receive data stream if there are three or more F-bit framing bit errors in sixteen consecutive F-bits or one or more M-bit FBEs per frame in two or more of four consecutive frames. The OOF is terminated upon the non-occurrence of FBEs in three consecutive frames. The checking of F-bits is done in batches of 16 F-bits and not as a sliding window.

In E3-G.751 mode, an OOF event is declared, if in the receive data stream, there is one or more FBEs per frame in four consecutive frames. The OOF is terminated if there are no FBEs in three consecutive frames.

In E3-G.832 mode, an OOF event is declared, if in the receive data stream, there is one or more FBEs per frame in four consecutive frames. An OOF event is also declared if there are PER in 986 or more frames in a block of 1000 frames. The OOF is terminated if there are no FBEs in three consecutive frames.

The OOF event generates an OOFStrt interrupt indication and sets the OOF status indication bit in the OOFAlm field of the Maintenance Status register. Terminating the OOF event generates an OOFEnd Interrupt and clears the OOF status indication bit.

NOTE: While the framer is searching for a new framing template, the old one is maintained for ongoing performance monitoring (e.g., FBE) and output signaling (e.g., RXMSY).

In E3 mode, in the presence of OOF, RAI/RDI is transmitted on the transmit stream if the AutoRAI field in the TransmitOverheadInsertion 1 Control register is set.

In both E3 and DS3 modes, in the presence of OOF, an all-1s sequence is transmitted on the RXDAT toward the receive system side if the RxAutoAll1 field in Feature5 Control register is set.

2.2.5.5 Severely Errored Frame (SEF)

In DS3, an SEF event is declared when there are three or more F-bit FBEs in sixteen consecutive F-bits. This is terminated when the framer is in frame (i.e., OOF end). This is not specified in E3 mode.

The SEF event generates a SEFStrt interrupt indication. Since the termination criteria for SEF is identical to OOF, there is no SEF-end interrupt indication.

NOTE: SEF detection employs a fixed-window algorithm. Two counters are maintained - one for the number of F-bits encountered, and one for the number of errors encountered. When an F-bit is encountered (once every 170 bits in the DS3 data stream) it is checked to see if it has the value specified in the DS3 standard for its position in the DS3 frame. If not, the error counter is incremented, and if it reaches a value of 3, SEF condition is declared. Regardless of whether the F-bit value was correct or in error, the F-bit counter is also incremented (after the value check), and if it reaches a value of 16, both counters are reset and a new window of 16 F-bits is started. Therefore, if one selects an arbitrary set of 16 F-bits and toggles the first bit, the 16th bit and one bit in between, there is 1 in 16 chance that this set matches the Framer's fixed-window set. This is therefore the chance of detection for a single such occurrence.

2.2.5.6 Alarm Indication Signal (AIS)

In DS3, AIS event is declared when the receiver recognizes the AIS pattern (i.e., payload set to a 1010. . . sequence, with C-bits set to 0, X-bits set to 1, and F-, M-, and P- bits all valid) for two consecutive frames with ten or less deviations per frame and when OOF is off. The AIS event is terminated, if in the receive data stream, there are eleven or more deviations per frame for two consecutive frames or OOF is on.

An E3-G.751 AIS event is declared when four or fewer 0s are received by the receiver per frame period for two consecutive frame periods regardless of OOF. If OOF is off, no more than two 0s can be present in the FAS bits in order to differentiate framed and unframed all-1s. The AIS event is terminated if the receiver sees five or more 0s for two consecutive frame periods.

In E3-G.832, AIS event is declared when nine or fewer 0s are received per frame period, for two consecutive frame periods regardless of OOF. If OOF is off no more than two 0s can be present in the FA bytes in order to differentiate framed and unframed all-1s. The AIS event is terminated if the receiver sees ten or more 0s per frame period for two consecutive frames periods.

The AIS event generates a AISStrt interrupt indication and sets the AIS status indication bit (AISDet) in the Maintenance Status register. When the AIS event terminates, AISEnd interrupt indication is generated, and the AIS status indication bit is cleared.

In the presence of AIS event, (in both DS3 and E3) an all-1s sequence is transmitted on the RXDAT pin if the RxAutoAll1 filed in the Feature5 Control register is set.

2.2.5.7 Idle Signal (IDLE)

In DS3, an IDLE event is declared when the receiver recognizes the IDLE pattern (i.e., payload set to a 11001100 . . . sequence, with Cb3 bits set to 0, X-bits set to 1, and F-, M- and P-bits all valid) for two consecutive frames with ten or fewer deviations per frame when OOF is off. The IDLE event is terminated if the receiver has eleven or more deviations from the expected IDLE patter per frame for two consecutive frames or OOF is on.

The IDLE event generates a Idlestrt interrupt indication and sets the IDLE status indication bit in the Maintenance Status register. When the IDLE event terminates, IdleEnd interrupt indication is generated and the IDLE status indication bit is cleared.

In the presence of IDLE event (only in DS3), an all-1s sequence is transmitted on the RXDAT pin if the RxAutoAll1 field in the Feature5 Control register is set.

2.2.5.8 Parity Error (PER) and P-Bit Disagreement (PBD)

In DS3, as per ANSI T1.231-1997, the PER event is declared when at least one of the two P-bits differs in value from the expected value as calculated from the previous frame. The PBD event is declared when the receive data has two p-bits which are not equal.

Similarly in E3-G.832, PER event is declared if in the receive data, at least one of the eight EM bits differs from the expected value calculated on the previous frame and OOF is off. PBD is not defined in E3-G.832. Both PER and PBD are undefined in E3-G.751. The PER event increments the PER counter and PBD event increments the PBD counter.

If the ExtFEBE/Cj field in the TransmitOverheadInsertion1 Control register is enabled, REI gets transmitted on the transmit stream upon a PER event in E3-G.832 mode.

2.2.5.9 Path Parity Error (PPER)

In DS3 C-bit parity mode, the PPER event is declared when at least two of the three Cb3 bits differ in value from the expected value as calculated from the previous frame. The PPER event increments the PPER counter.

If the ExtFEBE/Cj field of the TransmitOverheadInsertion 1 Control register is enabled, FEBE gets transmitted on the transmit stream upon a PPER event.

2.2.5.10 Remote Alarm/Defect Indication (RAI/RDI), X-bit disagreement (XBD)

In DS3, an RAI/RDI event is declared when both X-bits of a receive frame are 0. The RAI/RDI event is terminated when both X-bits are 1. The XBD event is declared when the two X-bits are not equal.

In E3, an RAI/RDI event is declared when two consecutive receive frames have an A/RDI bit with the value 1. The RAI/RDI event is terminated when two consecutive frames have an A/RDI bit with the value 0. The XBD event is not defined.

The RAI/RDI even generates a YelStrt interrupt indication and sets the YelDet status indication bit in the Maintenance Status register. Upon terminating, the RAI/RDI event generates a YelEnd interrupt indication and clears the YelDet status indication bit. The XBD event increments the XBD counter.

2.2.5.11 Far-End Block Error/Remote Error Indication (FEBE/REI)

The FEBE/REI event is defined only in DS3 C-bit parity mode and E3-G.832 mode. In DS3 C-bit parity mode, it is declared when at least one of the three Cb4 bits is 0. In E3-G.832 mode, it is declared when the REI-bit is 1. The FEBE/REI event increments the FEBE/REI counter.

2.2.6 One-Second Counter Latching

A special mode simplifies reading counters every second. Setting the OneSecMod field in the General2 register, activates this mode. On every second in this mode, the values in the performance monitoring counters latch into shadow counters (upon the rising edge of the OneSec trigger), and the original counters reset to 0. This is accompanied by the setting of the OneSecItr field in source channel and, if the 1SecTimIE field in General2 Control register is set, by an interrupt. When counters are read in this mode, the value returned is always from the shadow counters.

The one-second trigger for latching is one of two ways:

1. If the ONESEC pin is set to output (via the OneSecOut field in the General2 register), it is based on a one-second counter (OneSecCtr) incremented by channel 1's TXCKI, (the value to count is determined by software) and is accompanied by an outgoing 16-clock-long pulse on the ONESEC pin
2. If the ONESEC pin is set to input (via the OneSecIn field in the General2 register), it is based on an incoming pulse on the ONESEC pin.

NOTE: Writing to the counters does ***not*** trigger latching. To function properly, the counters must be set to saturating mode by clearing all counter interrupt enable bits in the Counter Interrupt Control register. While the channel is disabled, the one second latching operation is also disabled. When counters are read while the mode is on and channel is disabled, the value returned is the one latched prior to disabling the channel.

2.2.7 Terminal Data Link Reception

The terminal data link channel (DL) resides on the C5 bits of DS3 C-bit Parity frames, which is approximately 28.195 Kbps (3/4760 bits at 44.736 Mbps). On the N-bit of E3-G.751 frames, it is approximately 22.375 Kbps (1/1536 bits at 34.368 Mbps). On the NR or GC (*but not both*) bytes of E3-G.832 frames, it is approximately 64 Kbps (1/537 bytes at 34.368 Mbps). The DL contents are generally available via one or more of three routes, the data stream (marked with other overheads by RXGAPCK), marked by REXTCK, or through a FIFO-buffered microprocessor interface; the first two are specified in Section 2. this section describes the details of the third mode.

The internal circuitry [Receive Data Link (RDL) block] provides logic and FIFO for implementing LAPD/HDLC terminal data link reception according to ITU-T Q.921 and ISO/IEC 3309 standards. The logic is responsible for flag and abort sequence detection, 16-bit frame check sequence (FCS) checking and transparency zero removal, and managing the internal FIFO. Each of the channels contains a 128-byte Receive Data Link FIFO buffer, distinct from the Transmit Data Link FIFO buffer, to reduce the amount of intervention required from the system in accessing the data link contents. FIFO buffer contents are accessed via the microprocessor interface either in interrupt-driven mode, using maskable interrupts to synchronize data flow into and out of the FIFO buffer, or in status-polling mode.

The RDL FIFO buffer contains two types of information, data bytes and status bytes. Data bytes are the actual data extracted from the DL channel (all flag-bounded bytes except flag and abort sequences and zeros for transparency). Status bytes contain additional information qualifying the data bytes following them.

A data block within the FIFO buffer is one status byte followed by 0 to 127 data bytes.

When a new block starts, the RDL reserves one byte for status and then fills data bytes, as required, until the end of the block. At the end, status information is written into the reserved byte and a new block is started.

A block terminates and a new one starts in conjunction with one of the following:

- A FIFO near-full interrupt
- A message received interrupt
- A FIFO overrun interrupt

Before the status byte is read from the RxMsgByte Status register, the user must read the RDL Status register and get the RxGoodBlk field value. This bit defines the type of the status byte to be read from the RxMsgByte Status register.

For type (a1, a2) the RxGoodBlk is set, and for type (b) it is cleared. Refer to Table 2-8.

Table 2-8. Status Byte Description

RxGoodBlk field value	MSB	Type	Description	Additional Information (Bits 0-6)
Set	Set	(a1)	End of message (detection of flag sequence) with correct FCS	Number of data bytes in block (range = 0 to 127)
—	Cleared	(a2)	Partially-received message, FIFO near-full, message data continue in next block	—
Cleared	Undefined	(b)	Errored block cases: end of message with incorrect FCS, or end of message with number of bits indivisible by 8 (alignment error), or aborted message (detection of abort sequence), or overrun error. Priority of error type is: bad FCS, align error, abort, overrun (from low to high). Only one type of error can be indicated.	—
Note(s): In (b), the number of data bytes in the block is always 0, as the data bytes are of no significance and therefore discarded by the RDL. Also, if one or more (a2) blocks is followed by a (b) block, the microprocessor should discard all the data bytes of the previously-read (a2) blocks, as they belong to the same erroneous/aborted message.				

The available RDL-related interrupt events are as follows:

- FIFO near-full:
  - Turned on when the number of bytes in the FIFO buffer is equal to or more than the programmable Near-Full FIFO threshold (range = 2 to 127) [a type (a2) block ends when this interrupt is turned on, and another block of this type is not be produced until the interrupt is turned off]
  - Turned off when there are no more unread complete blocks left in the FIFO buffer, i.e., when the last byte of the last complete data block has been read (if after reading all pending complete blocks from the FIFO buffer, the number of bytes in the remaining incomplete block is again equal to or more than the threshold, a new interrupt is generated and another type, a2, block terminated)
- Message received:
  - Turned on when an end-of-message flag sequence or an abort sequence is detected. A type (a1) or (b) block ends when this interrupt is turned on.
  - Turned off when the message received status indication is read (unless these interrupts are promptly and consistently read and cleared, this interrupt means that one *or more* message received events have occurred since the last read)
- FIFO overrun:
  - Turned on when the FIFO buffer is full and another byte has to be written to it. A type (b) block (with overrun error-type) ends when this interrupt is turned on, and another block of this type is not produced until the interrupt is turned off.
  - Turned off when there are no more unread complete blocks left in the FIFO buffer, i.e., when the last byte of the last complete data block has been read (since all input is discarded by the RDL until the overrun is cleared, this is the status byte of the incoming message within whose data the overrun error has occurred).

These interrupts are independently enabled by setting the RxNFIE, RxMsgIE, and RxOVRIE fields in the Receive Data Link Control register, and are differentiated by reading the Status Indication register (Receive Data Link Status register).

The RDL-related status indications available are as follows:

- FIFO near-full (set and cleared with the interrupt)
- Message received (set and cleared with the interrupt)
- FIFO overrun (set and cleared with the interrupt)
- Data block in FIFO (set if there is ≥1 complete data block in the FIFO, otherwise cleared)
- Type of next FIFO byte (set if status, cleared if data; undefined if the Data block in FIFO indication is not set)

These indications are detected by examining RxNF, RxMsg, RxOVR, RxBlk, and StatByte fields (respectively) of the Receive Data Link Status register.

2.2.7.1 Initial Setup

On reset, the RDL is disabled, with no interrupts active. Prior to enabling the RDL, the desired interrupt enables the Near-Full FIFO threshold, and the RDL related options should be set to the desired values through the Receive Data Link and the Receive Data Link Threshold Control registers. Checking the 16-bit FCS is software-selectable by setting the RxFCSEn field of the Receive Data Link Control register. If the channel is functioning in E3-G.832 mode, the NRDL field of the Receive Data Link Control register should be set to identify which of the two possible overhead bytes (NR or GC) is processed by the RDL.

Setting the RxDLEn field of the Receive Data link Control register activates the RDL. Once active, the HDLC related functionality (flag and abort detection, zero removal) of the RDL is automatically executed on all DL data flowing through the FIFO buffer. Once the RDL is enabled, it assumes the channel is idle and starts looking for HDLC flag sequences.

To modify the basic settings of the RDL (i.e., Near-Full FIFO threshold, FCS checking, E3-G.832 NR/GC source), the system should first disable the RDL (by clearing the RxDLEn field of the Receive Data Link Control register).

After disabling the RDL, when accompanied by an immediate termination of all its activities, the following enable causes discard of all the FIFO contents and update of the status indications to represent a new status (i.e., all interrupt indications clear, no data blocks in the FIFO buffer).

2.2.7.2 Writing Messages into the FIFO

Data arriving on the data link channel is automatically written into the FIFO buffer by the RDL. Type (a1, a2, and b) block description references found below are explained in Table 2-8.

Normal Message

A new data block starts filling up when the RDL detects a transition from flag sequence (01111110) to stuffed-zero data (≤ 5 consecutive 1s). Each octet of message data (i.e., between flag sequences), following stuffed-zero removal (i.e., discarding a 0 directly following five contiguous 1s), is stored in a FIFO byte. A transition from zero-stuffed data back to flag sequence marks the end of the message and results in an interrupt with the indication message received.

NOTE: For each message, all the octets between the initial and terminal flags—not including the flags but including the FCS—are placed in the FIFO buffer.

If the number of data bits collected is not divisible by eight, or if FCS checking is enabled and the FCS is incorrect, a type (b) block is marked in the block type field of the data block's status byte (the first byte of the block), the error type is noted in the same byte, all the data bytes are discarded, and a new block is started on the byte following the current status byte. Otherwise, a type (a1) block is marked, the block length in the status byte is set to the number of data octets stored, and a new block is started on the byte following the last data byte stored.

Since consecutive messages can share the flag between them, the next message can start as soon as new zero-stuffed data is detected, regardless of the number of flags between the messages.

NOTE: Two flags with a shared zero between them are treated as two valid flags.

A sequence of five 1s not followed by 0 (i.e., 01111101111110) is faulty and produces a type (b) block (with alignment error-type).

Aborted Message

A transition from zero-stuffed data to abort sequence (≥7 consecutive 1s) marks an aborted message and results in an interrupt with the indication message received. A type (b) block is marked in the block type field, the error type is noted in the same byte, all the data bytes are discarded, and a new block is started on the byte following the current status byte. The next message starts only after at least one flag sequence is located and new zero-stuffed data follows.

Near-Full FIFO Event

A Near-Full FIFO event occurs when the number of bytes in the FIFO buffer is equal to or more than the Near-Full FIFO threshold *and* the FIFO near-full interrupt is off (the byte whose writing leads to this event is referred to as the threshold byte). This results in an interrupt with the indication FIFO near-full. A type (a2) block is marked in the block type field, block length is set to the number of data octets stored and a new block is started on the byte following the last data byte stored.

If the first octet to arrive after the threshold byte is a flag sequence (i.e., the threshold byte was the last byte of the FCS), the new block is a type (a1) block with a length of 0 or a type (b) block. If the first octet to arrive after the threshold byte is an abort sequence, the new block is a type (b) block. Otherwise, the new block contains the upcoming bytes of the same message.

If the last octet to arrive before the threshold byte is a flag or abort sequence (i.e., the threshold byte is the status byte of an upcoming message), the type (a2) block has a length of 0, and the new block contains the actual data of the new message; i.e., the system receives a message received interrupt (on the byte before the threshold byte) and shortly afterwards a FIFO near-full interrupt (on the threshold byte).

FIFO Overrun

If the FIFO buffer is full when another byte has to be written to it *and* the FIFO overrun interrupt is off, an overrun error occurs, resulting in an interrupt with the indication FIFO overrun. If the new byte is a *data* byte, it is lost (i.e., data bytes already present in the FIFO buffer are not overwritten), and the data block is immediately terminated and marked as a (b) block. If the new byte is a *status* byte, its writing to the FIFO buffer is postponed until at least one byte has been read from the FIFO buffer, and it is guaranteed to be a type (b) status byte.

While the RDL is in overrun state (i.e., until the indication is turned off), all incoming data bytes are discarded and nothing is written to the FIFO buffer except the status byte of the message where the overrun error occurred. New data is written to the FIFO buffer only upon detection of a transition from flag sequence to zero-stuffed data *following* the clearing of the interrupt.

2.2.7.3 Reading Messages from the FIFO

The system reads the contents of the FIFO buffer by accessing the Receive Data Link Message Byte Status register; each access returns the next byte from the FIFO buffer.

The Receive Data Link(i) Status register is read before a new status is read.

This is done to make sure that there are data blocks in the FIFO buffer (RxBlk) and that the type of the next status byte (a1, a2), or type (b) are fetched from RxGoodBlk.

The FIFO buffer contains zero or more complete data blocks at any time, plus zero or more bytes of the current incomplete block.

At no time are the bytes of the current incomplete block accessible by the system. After reading the Receive Data Link(i) Status register, the status itself is read and understood according to the RxGoodBlk field value.

The data block in FIFO status indication bit (the RxBlk field in the Receive Data Link Status register) is cleared if there are zero complete blocks, otherwise it is set. Attempting to read the FIFO buffer when this bit is not set returns an undefined value, but the FIFO read pointer is not incremented.

Although there is a bit in the Status Indication register (Receive Data Link Status register), which can be queried to inform the system if the next byte to be read from the FIFO buffer is a status or a data byte (StatByte field), the bit in the Status Indication register is not strictly needed for reading from the FIFO buffer. The first byte read from the FIFO buffer after the RDL is enabled is a status byte, which indicates the number of data bytes following it, 0 for (b) blocks, additional information field for (a1) and (a2) blocks. After this, another status byte is again guaranteed, and so forth. The next FIFO byte type bit is supplied only for systems that do not want to maintain a count of data bytes after reading each status byte, and would rather query this bit before reading every single byte in the FIFO buffer.

Interrupt-Driven Mode

The interrupt-driven FIFO buffer reading mode is enabled by unmasking at least one of the two functional interrupts related to the RDL (FIFO near-full and message received). The third interrupt (FIFO overrun) is useful for error condition monitoring. Once an interrupt occurs, the microprocessor reads the SrcChnl1 to SrcChnl4 fields of the Source Channel Status register to identify which channel is the interrupt's originator. It then reads that channel's Interrupt Source Status register to identify which part of the chip raised the interrupt (RDL in this case, namely RxDLItr field). It then reads the interrupt identification fields of the Status Indication register for this channel's RDL (the RxNF, RxMsg, and RxOVR fields of the Receive Data Link Status register) to identify the type of interrupt.

Before reading a status byte from the FIFO buffer, the RDL Status Indication register (Receive Data Link Status register) is read; the first time after an interrupt to identify the interrupt's source, every other time to make sure there are data blocks in the FIFO buffer still left to read.

Beyond this, options of handling the interrupt are numerous, but one would expect the microprocessor to read one or more data blocks and/or one or more bytes from the FIFO buffer. What follows is a possible routine:

- The E3-G.832 framer in question has all its RDL interrupts set to active, with the near-full threshold set to 32 bytes.
- After identifying the source and type of interrupt, if the interrupt type is
  - Message received**:** If the microprocessor is busy, do nothing but return; if it is not busy, read one entire block from the FIFO buffer, then check if the "data block in FIFO" indication is set; if not return, otherwise repeat
  - FIFO near-full: Read one entire block from the FIFO buffer, check if the data block in FIFO indication is set; if not return, otherwise repeat
  - FIFO overrun: Inform the network management that the system was unable to cope with the data link throughput, then act as per FIFO near-full

NOTE: In this example, from the time a FIFO near-full. interrupt occurs until the FIFO buffer fills up, a minimum period of 12 ms (96 bytes at 8 KB) passes.

Polling Mode

Polling mode is effective when both the RDL functional interrupts have been masked. Polling mode differs from interrupt-driven mode only in that the entry into the service routine is timer-dependent rather than interrupt-driven. The rest of the handling is much the same as it is under interrupt-driven mode.

2.2.8 Far-End Alarm and Control Channel Reception

The FEAC channel resides on the C13 bit of DS3 C-bit Parity frames. There are three ways to access FEAC contents: through the data stream (marked with other overheads by RXGAPCK), through the data stream marked by REXTCK, or through a register-based microprocessor interface. Section 2. discusses the first two. This section describes the details of the third.

FEAC messages are in the form of 16-bit code words, with a pattern of 0xxxxxx011111111 (right-to-left). The code word overhead are the 10 fixed bits. The code word proper are the six x bits. The entire 16 bits are represented as the complete code word pattern. When no alarm or control signal is present, the channel carries an all-1s (idle) pattern. Internal circuitry (Receive FEAC [RFEAC] block) provides logic and a register for implementing FEAC message identification. As this channel is undefined in DS3 M13/M23 and E3 modes, the RFEAC is automatically disabled in these modes.

The RFEAC comes in two modes (selectable through the FEACSin field of the Feature3 Control register), single code word detection (makes no assumptions about FEAC messages repetitions) and multiple code word detection (assumes each FEAC message is repeated at least 10 times).

In single code word detection, a valid code word is detected when one complete code word pattern is located.

In multiple code word detection, a valid code word is detected when nine complete code word patterns with the same code word proper are located, using the following algorithm F:

F1. [Initiation] Locate a complete code word pattern, store its code word proper (cp1) in a 6-bit register (termed the tentative code word), set a 4-bit counter to 1, and go to step F2

F2. [Tentative] Locate another complete code word pattern and compare its code word proper (cp2) with the tentative code word:
   a. if identical, add 1 to the counter, and go to step F5
   b. if not, store cp2 in another 6-bit register (termed the alternative code word) and go to step F3.

F3. [Tentative and Alternative] Locate another complete code word pattern and compare its code word proper (cp3) with the tentative code word:
   a. if identical, add 2 to the counter (for cp2 and cp3), and go to step F5
   b. if not, go to step F4

F4. [Alternative] Compare cp3 with the alternative code word:
   a. if identical, store the alternative code word in the tentative code word register, set the counter to 2 (for cp2 and cp3) and return to step F2
   b. if not, store the alternative code word in the tentative code word register, set the counter to 1, store cp3 in the alternative code word register, and return to step F3

F5. [Possible Termination] if counter ≥9 declare a valid code word and end algorithm, if not go to step F2

NOTE: When comparing code word propers, the number of bits differing between the two is of no importance, just their identity or lack of identity.

In both modes, no allowance is made for bit errors in the code overhead. Complete code word patterns can be separated from one another by any amount of data (whether all-1s or not), which are ignored by the RFEAC logic.

In both detection schemes, a valid idle signal is detected when 16 consecutive 1s are located.

The RFEAC is always in one of two internal states, namely idle state (the initial state) or message state:

- In idle state, the RFEAC scans for a valid code word (according to one of the two definitions given above). Once this is found, the valid code word proper (plus the two 0s) is written to the Receive FEAC Byte Status register, and a new FEAC message interrupt (with the RxFEACItr indication of the Receive Data Link FEAC Status register) is generated (it is cleared once the code word proper is read from Receive FEAC Byte Status register). This moves the RFEAC to message state.
- In message state, the RFEAC scans for either a valid code word or a valid idle signal. If a valid code word is found, processing is the same as in idle state. If a valid idle signal is detected instead, a reversion to idle interrupt (with the RxFEAC Idle indication of the Receive Data Link FEAC Status register) is generated (it is cleared once the interrupt indication is read); this moves the RFEAC back to idle state.

As a FEAC message takes 16 DS3 frames, new FEAC message interrupts arrive at a maximal rate of 1 per 1.7 ms for single code word detection, and at a maximal rate of 1 per 17 ms for multiple code word detection.

NOTE: There is no buffering of messages; if the system fails to read the code word proper from the Receive FEAC Byte Status register before a new one is located, the old code word is overwritten.

There is no facility for disabling the RFEAC circuitry; systems that do not need to receive this information should not enable the two RFEAC interrupts. Similarly, systems that work by polling should also mask the interrupts and poll the interrupt identification bits. Masking and unmasking is performed by setting the RxFEACIE and RxFEAC IdleIE fields of the Feature3 Control register.

In addition to the interrupt based FEAC mechanism described above, a three-stage FIFO buffer (called “FEAC stack”) for FEAC messages is provided to allow for a more relaxed and flexible FEAC channel processing.

The FEAC stack mechanism provides a register (Receive FEAC Stack byte) for the stacks’ FEAC message with two extra bits. One extra bit signaling that the data is valid and has not been read and another bit signaling that there are more valid messages in the stack. If the valid bit is off, it forces the more bit to zero and the six FEAC message bits are set to undefined.

If the more bit is off, it means there are no more valid messages. An indication that the stack is not empty is provided by and implemented in the FEAC Status register bit RxFEACSNE. When this status bit is set, an interrupt is generated unless the interrupt has been masked. (the RxFEACSNEIE bit in the Feature3 Control register is off.) The stack has no alert on under run and over run. A word shifted into a full stack can overrun an old word that has not been read yet. Reading an empty stack results in reading an undefined code word except for valid bit and more bit which are zero.

2.2.8.1 Writing into the FEAC Stack

A code word is shifted in to the stack for one of the following reasons:

- If the code word is different from the previous code word.
- If the stack was empty (either after reset or after channel enable).
- When the FEAC channel comes out of Idle state (all-1s in the FEAC channel).

Writing a new word into the FEAC stack causes shifting of old code words, possibly overrunning the oldest code word.

2.2.8.2 Reading from the FEAC Stack

The messages are read from the FEAC stack in FIFO style. Reading FEAC stack can be done by either polling or interrupt modes.

The sequence of operation in interrupt mode is as follows:

1. Wait for an interrupt, read the RxFEACSNE before the first read.
2. Read the FEAC stack message only if RxFEACSNE is on.
3. If the more bit in the read word is off, go to step 1 (wait for the next interrupt) or else go to step 2.

The sequence of operation in polling mode is as follows:

1. Read the FEAC FIFO register. The word read is valid only if the valid bit is on.
2. If the more bit is on, the next word read is also valid.

The FEAC stack logic cannot be disabled. Host systems using the interrupt mode to read the FEAC messages should not enable the FEAC stack interrupts. The masking is performed by setting the RxFEACSNEIE in Feature3 Control register. Systems using the polling mode should not read the FEAC Stack register.

2.3 Microprocessor Interface

The Microprocessor Interface (MPU), provides the capability of configuring the CX28342/3/4/6/8, reading status registers and counters, and responding to interrupts. The interface supports Intel 8051, 8151, 8251 and Motorola 68000, 68020, 68030 processors. The Motorola mode is a SRAM like interface. EBUS is also supported for Intel type glueless, and for Motorola types with external address latching. In the Intel mode, the address and data are multiplexed, while in the Motorola mode, the address and data are separate pins. Only asynchronous read and write mode is supported. The asynchronous mode runs internally at channel 1 transmitter clock frequency.

The microprocessor interface is made up of the following pins: MOTO*, CS*, ALE, DS*/RD*, R/W*/WR*, DTACK*, AD[7:0], A[8:0], INTR*, RESET*. A detailed description of the MPU pins is provided in the pin list table.

NOTE: Accessing or using the additional framers and the associated registers within CX28346 and CX28348 requires the use of additional pins as outlined in Chapter 1 and Tables 1-9 and 1-10.

2.3.1 Address/Data Bus

In the Non-Multiplexed Address Mode, A[8:0] provides the address for register access. In the Multiplexed Address Mode, A[8] and AD[7:0] provides the address. In both modes, data bytes flow over the shared bidirectional, byte-wide bus, AD[7:0].

2.3.2 Control Signals

Four signals control the operation of the interface port: ALE, CS*, DS*/RD*, and R/W*(WR*). An additional pin, MOTO*, selects whether the interface signals are a Motorola or Intel type.

When MOTO* is low, indicating a Motorola-style interface, CS*, R/W*, and DS* signals are expected. When MOTO* is high, indicating an Intel-style interface, CS*, ALE, RD*, and WR* signals are expected.

When MOTO* is high, address lines are multiplexed with data. This pin is tied high for Intel devices and tied low for Motorola devices.

2.3.3 Interrupt Requests

The INTR* output pin is an active-low, open-drain type output, that provides a common interrupt request for all four channels.

Each channel includes interrupt status registers and interrupt enable registers or interrupt enable bits combined in control registers. Events, such as alarm status changes, latch in status registers until read by the microprocessor or until another action is taken. Most of the status bits have a corresponding interrupt enable bit to enable or disable interrupt generation. If the specific interrupt is enabled and interrupts from this channel are enabled, INTR* goes low or active.

Status bits from each channel are gated with the corresponding enable bits in the control registers. They go to the Source Channel Status register providing information

about which channel is responsible for interrupt generation. The General1 Control register enables masking the complete set of interrupts of a channel by clearing one bit.

Using these registers, the microprocessor processes interrupts as follows:

1. Read Source Channel Status register to determine which channels caused the interrupt.
2. For each interrupting channel, read Interrupt Source Status register to determines which status registers contain the interrupt events.
3. Read the status registers to determine which events caused the interrupt.
4. Enter the appropriate service routine.

The only exception in the Source Channel Status register is OneSecItr Status bit. This bit always reflects the status of OneSec Counter regardless of the state of its mask. INTR*, however, becomes active due to the OneSec Counter roll-over only if the interrupt is enabled (by One SecIE bit).

NOTE: In exceptional cases, the microprocessor can identify an interrupt, and due to a delay and other actions taken prior to reading the relevant status register, the status bit indicating the interrupt source is already cleared. In such cases, the source of the interrupt might be unknown.

2.3.4 Hardware Reset

Assertion of the hardware reset (RESET*) places internal registers into their default power-up state. Asserting RESET* is required because there is no other way to put the device into reset state. RESET* is used as a level signal. During RESET*, the system and line clocks are supplied for at least 30 cycles, to put the registers into their default values. LINECK and TXCKI must always be supplied in RESET*. RXCKI is supplied if the receive dejitter FIFO buffer is used in the future. During RESET* the system side outputs (besides VCO) are High-Z. The transmitter line side interface is as follows: TCLKO is active and reflects TXCKI; TXPOS and TXNEG are forced to be zero. During RESET* VCO output is active.

After RESET* all the channels are disabled and the control registers set to their default values (the defaults are described in Chapter 3). After hardware RESET*, the microprocessor must initialize the control registers to the desired state and enable the channels that are to be operational.

2.3.5 Software Reset

Assertion of software reset affects the device in the same way as hardware reset. Setting SWRst bit in General2 Control register activates a software reset. The bit is cleared automatically by the device when all internal circuits are reset and when internal registers are at their default values.

During software reset, system interface pins (besides VCO) continue to be active, and when control registers are set to their default values, the pins behave accordingly. Transmitter line side interface and VCO outputs behave similarly to hardware reset.

2.3.6 Initialization Guidelines

The following device status is true after reset:

1. All the channels are disabled.
2. The control registers, status registers, and the counters are at their default values.
3. The default mode after reset is DS3-M13/M23.
4. All the interrupts are disabled.
5. FEAC channel and the data link FIFOs are disabled.
6. The Overhead bits are programmed to be generated internally.
7. The system side pins are inactive and have a value according to their control bits default configuration (TXGAPCK, TEXTCK, RXGAPCK, REXTCK, and RXMSY are zero; RXDAT is undefined; TXSY is High Z until configured.
8. VCO output is active all the time.
9. On the line side, TCLKO is active and reflects TXCKI. TXPOS and TXNEG are forced to zero.

NOTE: Before enabling the channels to be operational, the control registers should be programmed to the desired operating mode. TXSY direction must be set to enable correct operation of the transmitter.

The order of programming does not matter as long as the Chnl(i)E (Channel Enable) bits and Chnl(i)IE (Channel Interrupt Enable) in the General Control register are kept low, i.e., the channels are disabled and the interrupts are globally masked. After the desired modes, features, interrupt masks, overhead control bits, and data link channels are set and enabled, the General1 Control register should be written to enable the desired channels and interrupts.

When a channel is enabled after reset, and if TXSYIn is set, the transmitter waits for the first synchronization pulse to start functioning. Until this pulse is sensed, the transmitter system side signals are inactive, i.e., TXGAPCK and TEXTCK are low or high (according to TxInvClk bit), and data is not sampled from TXDATI and TEXT pins. TXPOS and TXNEG on the line side are also held low until the first synchronization pulse is generated.

If TXSYOut is set, the transmitter starts working immediately after the channel is enabled; it generates a synchronization pulse and drives the clocks and signals as programmed.

The receiver system interface starts to work immediately after enabling the channel. When enabled after reset, the receiver starts in an out-of-frame state. It starts an internal frame counting and searches for framing pattern alignment in the received data stream. The system side signals of the receiver start functioning immediately.

NOTE: Some of the control registers can be changed dynamically, i.e., while the channel is enabled and working (interrupt's mask or message byte, for example). Some of the control registers are limited to be changed only when the channel is disabled (frame format, for example).

Disabling of a channel is done by clearing its Chnl(i)E bit in the General1 Control register. When a channel is disabled after being operational, the control registers are unaffected, and the status bits and counters maintain their value (to enable

debugging). Unless the Chnl(i)IE bits are cleared (hence, globally masking the interrupts), interrupts that were asserted continue to be active. Therefore, the disabled channel's interrupts should be masked in parallel with disabling the channel (by clearing Chnl(i)IE bit).

While a channel is disabled, the system side pins of the transmitter and receiver are frozen in their last state and are inactive until the channel is enabled. RXGAPCK, REXTCK, TXGAPCK, and TEXTCK can change their output polarity when the channel is disabled if the corresponding Control bits are changed at that time. TXSY also can change from output to input and vice versa if the Control bits are changed. On the line side, TXPOS and TXNEG are forced to zero while the channel is disabled.

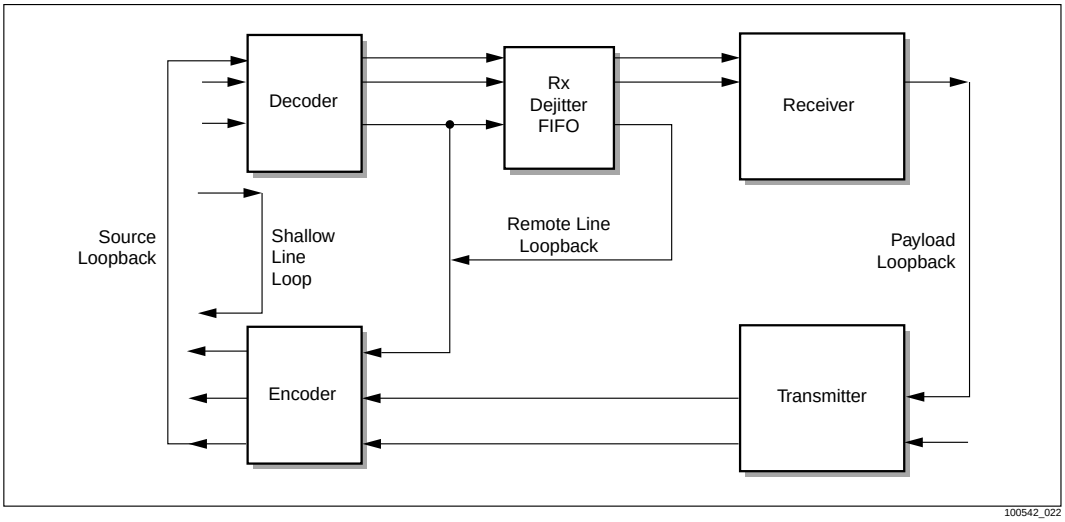
After disabling the channel, the desired modes and functions should be changed. Then, the channel and its global interrupt mask should be enabled again. Some of the status registers and the counters are affected by enabling the channel according to the new mode set, or due to an old event's end. The data link FIFO buffers are flushed. The FEAC channel bytes are not relevant, and their operation starts as it would after reset and enable. The transmitter and the receiver act as they would when enabled after reset.

To enable programming of the control registers and reading of the counters and status registers while the channel is disabled, the system (TXCKI) and line (LINECK and optionally RXCKI) clocks must be supplied. The clocks can be disabled only when a channel is completely shut down and is not going to be used.

2.4 Loopbacks

The Framer provides a complete set of loopbacks for diagnostics, maintenance, and troubleshooting of each channel. All loopbacks perform clock and data switching, if necessary. The activation and deactivation of a specific loopback are done through programmable control bits. Since activation and deactivation of a loopback cause internal circuits to switch between clocks, after writing to a loopback control bit, the microprocessor should not access any of the device registers (read or write) for the 20 slowest clock cycles.

Figure 2-19. Loopback Types



2.4.1 Shallow Line Loopback

The shallow line loopback loops the receiver inputs before B3ZS/HDB3 decoding back to the line through the transmitter outputs. The shallow line loopback provides LCV transparency, i.e., LCVs are transmitted exactly as received. The receiver data path is not affected by activation of this loopback and the received data is still present on RXDAT pin (it can be replaced by an all-1s or AIS stream by programming RxAll1 or RxAIS bits in Feature5 Control register).

The entire transmitter circuit works with the receiver clock (LINECK); therefore, the system interface clock outputs (TXGAPCK and TEXTCK) cannot be related to TXCKI in this mode and are inactive. TXSY is also inactive. If TXSY is programmed as an input, it is ignored by the transmitter. If TXSY is programmed as an output, it is blocked by the transmitter. Error insertion on the looped frame is not valid.

When TxLOS bit in Feature2 Control register is set, an all-0s signal is output on the transmitter and overrides the content of the frame looped from the receiver.

Activation of this loopback is done by setting LineLp bit in the Mode Control register.

When the receiver and the transmitter are programmed to be in shallow line loopback, and the line code is set to unipolar (NRZMod bit in Feature Control register is set), TXNEG output pin is forced to 0. Therefore, TXNEG does not reflect RXNEG in unipolar mode.

NOTE: The Shallow line loopback and source loopback cannot be operated simultaneously.

2.4.2 Remote Line Loopback

The remote line loopback loops receive data after B3ZS/HDB3 decoding and before frame recovery back to the line. If the receiver FIFO buffer is disabled, decoder output is connected to transmitter B3ZS/HDB3 encoder input. If the receiver FIFO buffer is enabled, the FIFO output is connected to transmitter B3ZS/HDB3 encoder input. The remote line loopback provides some LCV error correction due to the path through the decoder and the encoder. Activation of this loopback does not affect the receiver data path. The received data is still present on RXDAT pin (it can be replaced by an all-1s or AIS stream by programming RxAll1 or RxAIS bits in Feature5 Control register). Error insertion on the looped frame is not valid.

The whole transmitter circuit works with the receiver clock (either LINECK or RXCKI). System interface clock outputs (TXGAPCK and TEXTCK) cannot be related to TXCKI in this mode and are inactive. TXSY is also inactive. If TXSY is programmed as an input, it is ignored by the transmitter. If TXSY is programmed as an output, it is blocked by the transmitter.

Overwriting the looped frame by an AIS pattern and transmission of AIS to the line is enabled by programming TxAlm bits in Mode Control register. However, the generated pattern is not aligned to the looped frame boundaries and is initiated and terminated once TxAlm bits change. Idle pattern and RAI transmission due to TxAlm bits are not enabled during this loopback.

When TxLos bit in Feature2 Control register is set, an all-0s signal is output to the transmitter and overrides the content of the frame looped from the receiver.

This loopback is activated by setting RlineLp bit in the Feature3 Control register.

2.4.3 Payload Loopback

The payload loopback loops the received frame from the frame recovery circuit output through the transmitter frame generation circuit input back to the line. The transmitter *must* be programmed through Transmit Overhead Insertion1&2 registers to an internal generation of the Overhead bits, i.e., nothing is inserted via TXDATI or TEXT pins. The only exception is that justification control and Stuff Opportunity bits should be selected to be driven with the data stream, enabling the transmitter to receive them from the receiver with the payload. The entire transmitter circuit works with the receiver clock (either LINECK or RXCKI). The system interface clock outputs (TXGAPCK and TEXTCK) cannot be related to TXCKI in this mode and are inactive. The transmitter circuit gets the frame alignment signal from the receiver with the data that is looped. TXSY is inactive; if TXSY is programmed as an input, it is ignored by the transmitter. If TXSY is programmed as an output, it is blocked by the transmitter.

The payload loopback provides framing bits and some LCV error correction due to the path through the decoder, frame recovery, frame generation, and encoder. Activation of this loopback does not affect the receiver data path. The received data is present on RXDAT pin (it can be replaced by an all-1s or AIS stream by programming RxAll1 or RxAIS bits in Feature5 Control register). Error insertion on the looped frame is valid in this mode. Overwriting the looped frame by an AIS pattern and transmission of AIS to the line is enabled by programming TxAlm bits in Mode Control register. The generated pattern is aligned to the looped frame boundaries, and initiated and terminated similarly to normal operation (i.e., when not

in loopback). Idle pattern and RAI transmission due to TxAlm bits are also valid during this loopback.

NOTE: The transmitter does not generate an AIS or Idle pattern independently due to AIS or Idle detection in the receiver during this loopback. The microprocessor must program the transmitter to generate an AIS/Idle according to the receiver detection.

When TxLOS bit in Feature2 Control register is set, an all-0s signal is output on the transmitter and overrides the content of the frame looped from the receiver.

This loopback is activated by setting PayldLp bit in the Feature3 Control register.

2.4.4 Source Loopback

The source loopback loops the transmitter encoder outputs back to the system through the receiver decoder inputs. The receiver dejitter FIFO is meaningless in this mode, since there is only one clock looped back from the transmitter circuit, TCLKO clock.

The transmitter data path is not affected by activation of this loopback and the transmitted data is still present on TXPOS and TXNEG pins. The transmitted frame can be overwritten by an AIS pattern by setting TxAlm bits in Mode Control register to AIS control state. Doing this affects only TXPOS and TXNEG and not the looped frame. Therefore, there is no way to generate an AIS pattern on the looped frame by the transmitter. The same behavior applies to TxLOS bit. I.e., when TxLOS is set during source loopback only TXPOS and TXNEG are forced to zero, the looped frame is unaffected. When an AIS or LOS pattern is generated error insertion is invalid. Idle pattern and RAI are not supported in this mode like AIS; i.e., they can overwrite the looped frame by setting TxAlm bits as in normal operation.

Setting SourceLp bit in the Mode Control register activates this loopback.

NOTE: The shallow line loopback and source loopback cannot be operated simultaneously.

2.5 Joint Test Access Group (JTAG) Interface

The CX28344 incorporates printed circuit board testability circuits in compliance with *IEEE Std. P1149.1a–1993, IEEE Standard Test Access Port and Boundary–Scan Architecture*, commonly known as JTAG (Joint Test Action Group).

The JTAG includes a Test Access Port (TAP) and several data registers. The TAP provides a standard interface through which instructions and test data are communicated. A Boundary Scan Description Language (BSDL) file for the CX28344 is available from Conexant upon request.

The test access port consists of TDI, TCK, TMS, TDO, and TRST* pins. The TRST* control bit must be manually operated by the microprocessor to take the device in and out of reset.

2.5.1 Instructions

In addition to the required BYPASS, SAMPLE/PRELOAD, and EXTEST instructions, IDCODE and HIGHZ instructions are supported. Table 2-9 lists the JTAG instructions along with their codes.

Table 2-9. JTAG Instruction Codes

Instruction	Code
EXTEST	000
SAMPLE/PRELOAD	001
BYPASS	111
IDCODE	010
HIGHZ	100

3.0 Registers

3.1 Register Address Map

The registers in this device are classified into three types: Control, Status, and Counter registers. The Control registers configure the specific channels into their desired working mode, enable or disable interrupts and miscellaneous features in the devices. The Status registers report the occurrence of different events or triggers and performance errors. If a Status register is combined with an interrupt that is enabled, setting that Status registers to a logic 1 causes that interrupt to appear on the INTR* pin.

NOTE: The CX28346/8 devices have two interrupt pins, INTR[A]* and INTR[B]*

Clearing that Status register deactivates that related interrupt. The Counters count events and performance errors in the received signal and data path. The Counters are combined with an interrupt, which if enabled, is asserted once a counter rolls over. The Counters are cleared when the counters are individually read. A special additional counter is the One-Second Timer (GCtr00), which is discussed in more detailed later in the document.

The descriptions following this paragraph describe one register. Depending on the device, the same group is multiplied (i) channel times and functions the same way for every (i) channel. The General registers are the exception. With the CX28342/3/4 devices, there are only one set of general registers. For the CX28346/8, there are two sets of general registers, one associated with each chip select, CS[A]* and CS[B]*. These registers include the Source Channel Status, Part Number/Hardware Version, and the One-Second Timer. The full address map for all channels can be found in Section 3.6.

Some Control registers can be modified, whether the channel is either disabled or enabled or currently operating (*dynamic modification*). Some Control registers can only be modified when the channel is disabled (*static modification*). Specifications regarding each register are found in the following paragraphs. When a register with mixed bits (both *dynamic* and *static* bits in the same register) is modified while channel is enabled, the software must modify the dynamic bits, but leave the static bits unchanged.

A third variant of modification is available in relation to the datalink channel and is termed datalink static (*DL-static*). These bits can be modified dynamically only if the internal datalink mechanism is disabled:

- Rx bits: when the RxDLEn field in the Receive Data Link Control register is cleared
- Tx bits: when the DLMod fields in the Transmit Overhead Insertion Control register is set, so that HDLC and FIFO mechanism is disabled and does not affect the DL channel

The same applies to the OneSecMod-static modification. (These bits can be modified dynamically, but only when the One Second mode is disabled.).

When the channel is disabled via software, the control bits are unchanged to avoid interrupt assertion the channel's interrupts and should be masked via software. To clear a status register while a channel is disabled, the software should read the registers and execute the required operations. Enabling a channel can affect some of the status registers. The values after enable are detailed in the following paragraphs. Some registers are described as unaffected by enabling the channel, because they are not affected directly by the enable bit. However, they may be affected by other registers, which may be affected by the channel's enable bit.

NOTE: In the following paragraphs the term *set* means logic 1, and the term *cleared* means logic 0. Reserved bits with defined values are marked with Rsvd, and their value is 0. Reserved bits with undefined values are marked with - -.

3.2 Register Address Map

Register addresses are 9 bits in length, A[8:0]. The two most significant bits, A[8:7], represent the framer number, and the remaining seven bits, a[6:0], are the specific register offset within the framer's address space. With the CX28342/3/4 devices, there is only one set of registers. For the CX28346/8, there are two sets of registers with this addressing scheme, one associated with each chip select, CS[A]* and CS[B]*.

Therefore, the same registers in different framers share the same offset. General registers shared by framers use the lower offsets of each framer, but are only implemented in Framer 1 address space. In the case of CS28346/8, the General registers are implemented in Framers 1 and 5.

The address space of one channel is illustrated below:

00-01(h)	General Control
02-07(h)	Reserved
08-09(h)	General Status
0A-0F(h)	Reserved
10-13(h)	General Counters
14-1F(h)	Reserved
20-35(h)	Control Registers
36-3F(h)	Reserved
40-52(h)	Status Registers
53-5F(h)	Reserved
60-70(h)	Counters
71-7F(h)	Reserved

For all devices, the base addresses are allocated as follows:

- CX28342/3/4 or CX28346/8—CS[A] (Chip Select A)
  - General registers—00 (b)
  - Framer1—00(b)
  - Framer2—01(b)
  - Framer3—10(b)
  - Framer4—11(b)
- CX28346/8—CS[B] (Chip Select B)
  - General Control registers—00(b)
  - Framer5—00(b)
  - Framer6—01(b)
  - Framer7—10(b) [CX28348 only]
  - Framer8—11(b) [CX28348 only]

The addresses appearing in the following tables are offsets. The Addr column in the following tables relates to the 7-bits offset address, A[6:0].

General Registers

Table 3-1. General Registers

Label	Addr.(h)	Value After Reset.(h)	Name	Dir.	Cross Ref
General Control Registers					
GCR00	00	0x00	General1 Control Register	R/W	page 3-7
GCR01	01	GCR01	General2 Control Register	R/W	page 3-8
General Status Registers					
GSR00	08	GSR00	Source Channel Status Register	R	page 3-29
GSR01	09	GSR01	Part Number/Hardware Version Register	R	page 3-30
GCtr00	10	See Note Below(1)	One Second Timer— first address [7-0]	R/W	page 3-47
GCtr00	11	See Note Below(1)	One Second Timer—second address [15 – 8]	R/W	page 3-47
GCtr00	12	See Note Below(1)	One Second Timer—third address [23 – 16]	R/W	page 3-47
GCtr00	13	See Note Below(1)	One Second Timer—fourth address [31 – 24]	R/W	page 3-47

FOOTNOTE:
(1) Value after Enable: If set to DS3 = 0x02AA9E00, E3 = 0x020C6A00.

Channel (i) Registers

Table 3-2. Channel (i) Registers (1 of 2)

Label	Addr.(h)	Value After Reset.(h)	Name	Dir.	Cross Ref
CR00i	20	0x00	Mode Control Register	R/W	page 3-9
CR01i	21	0x00	Counter Interrupt Control Register	R/W	page 3-10
CR02i	22	0x00	Alarm Start Interrupt(1) Control Register	R/W	page 3-11
CR03i	23	0x00	Alarm End Interrupt(1) Control Register	R/W	page 3-12
CR04i	24	0x07	Feature1 Control Register	R/W	page 3-13
CR05i	25	0x01	Feature2 Control Register	R/W	page 3-14
CR06i	26	0x00	Feature3 Control Register	R/W	page 3-15
CR07i	27	0x00	Feature4 Control Register	R/W	page 3-16
CR08i	28	0x00	Feature5 Control Register	R/W	page 3-17
CR09i	29	0x00	Transmit Overhead Insertion1 Control Register	R/W	page 3-19
CR10i	2A	0x00	Transmit Overhead Insertion2 Control Register	R/W	page 3-21
CR11i	2B	0x00	REXTCK(1) Control Register	R/W	page 3-22
CR12i	2C	0x00	Receive Overhead Control Register	R/W	page 3-23
CR13i	2D	0x00	Transmit Data Link Control Register	R/W	page 3-24
CR14i	2E	0x00	Transmit Data Link Threshold Control Register	R/W	page 3-24
CR15i	2F	Undefined	Transmit Data Link Message Byte—lower address	R/W	page 3-25
CR15i	30	Undefined	Transmit Data Link Message Byte—higher address	R/W	page 3-25
CR16i	31	0x00	Receive Data Link Control Register	R/W	page 3-25
CR17i	32	0x7F	Receive Data Link Threshold Control Register	R/W	page 3-26
CR18i	33	0xFF	Transmit FEAC Channel Byte	R/W	page 3-26
CR19i	34	0x00	Error Insertion1 Control Register	R/W	page 3-27
CR20i	35	0x00	Error Insertion2 Control Register	R/W	page 3-28
SR00i	40	0x81	DS3/E3 Maintenance Status Register	R	page 3-31
SR01i	41	0x00	Interrupt Source Status Register	R	page 3-32
SR02i	42	0x00	Counter Interrupt Status Register	R	page 3-33
SR03i	43	0x00	Alarm Start Interrupt Status Register	R	page 3-34
SR04i	44	0x00	Alarm End Interrupt Status Register	R	page 3-35
SR05i	45	Undefined	Reserved for Mindspeed Use	R	—
SR06i	46	Undefined	E3-G.832 MA Fields Status Register	R	page 3-36
SR07i	47	Undefined	E3-G.832 SSM Field(1) Status Register	R	page 3-36
SR08i	48	0x03	Transmit Data Link FEAC Status Register	R	page 3-37

Table 3-2. Channel (i) Registers (2 of 2)

Label	Addr.(h)	Value After Reset.(h)	Name	Dir.	Cross Ref
SR09i	49	Undefined	Reserved for Mindspeed Use	R/W	—
SR10i	4A	Undefined	Reserved for Mindspeed Use	R/W	—
SR11i	4B	Bit 0,5 = Undef 1-4,6,7 = 0x00	Receive Data Link FEAC(i) Status Register	R	page 3-38
SR12i	4C	Undefined	Receive Data Link Message Byte(1)	R	page 3-39
SR13i	4D	0x01	Reserved for Mindspeed Use	R/W	—
SR14i	4E	Undefined	Reserved for Mindspeed Use	R/W	—
SR15i	4F	Undefined	Receive FEAC Byte	R	page 3-40
SR16i	50	Bits 0-1 =0x00 Bits 2-7 Undef	Receive FEAC Stack Byte	R	page 3-40
SR17i	51	0x00	Receive FEAC Status Register	R	page 3-41
SR18i	52	Undefined	Receive AIC Byte	R	page 3-41
Ctr00i	60	0x00	DS3/E3 Parity Error Counter—lower address	R	page 3-42
Ctr00i	61	0x00	DS3/E3 Parity Error Counter— higher address	R	page 3-42
Ctr01i	62	0x00	DS3 Parity Disagreement Counter—lower address	R	page 3-43
Ctr01i	63	0x00	DS3 Parity Disagreement Counter—higher address	R	page 3-43
Ctr02i	64	0x00	DS3 X Disagreement Counter—lower address	R	page 3-43
Ctr02i	65	0x00	DS3 X Disagreement Counter—higher address	R	page 3-43
Ctr03i	66	0x00	DS3/E3 Frame Error Counter—lower address	R	page 3-44
Ctr03i	67	0x00	DS3/E3 Frame Error Counter—higher address	R	page 3-44
Ctr04i	68	0x00	DS3 Path Parity Error Counter— lower address	R	page 3-44
Ctr04i	69	0x00	DS3 Path Parity Error Counter—higher address	R	page 3-44
Ctr05i	6A	0x00	DS3/E3 FEBE Event Counter— lower address	R	page 3-45
Ctr05i	6B	0x00	DS3/E3 FEBE Event Counter—higher address	R	page 3-45
Ctr06i	6C	0x00	DS3/E3 Excessive Zeros Counter—lower address	R	page 3-45
Ctr06i	6D	0x00	DS3/E3 Excessive Zeros Counter— higher address	R	page 3-45
Ctr07i	6E	0x00	DS3/E3 LCV(1) Counter—lower address	R	page 3-46
Ctr07i	6F	0x00	DS3/E3 LCV(1) Counter— middle address	R	page 3-46
Ctr07i	70	0x00	DS3/E3 LCV(1) Counter—higher address	R	page 3-46

3.3 Control Registers

NOTE: Reserved bits in the Control registers must be set to zero.

General Control Registers

The General Control registers provide for enabling and disabling channels and interrupts.

General1 Control Register (GCR00)

7	6	5	4	3	2	1	0
Chnl4E	Chnl3E	Chnl2E	Chnl1E	Chnl4IntE	Chnl3IntE	Chnl2IntE	Chnl1IntE

Default after reset: 00(h)
Direction: Read/Write
Modification: Dynamic

Chnl4E Channel 4 Enable Control—A general enable control for channel 4. Setting this bit enables channel 4 for normal operation. Clearing this bit disables channel 4.

Chnl3E Channel 3 Enable Control—A general enable control for channel 3. Setting this bit enables channel 3 for normal operation. Clearing this bit disables channel 3.

Chnl2E Channel 2 Enable Control—A general enable control for channel 2. Setting this bit enables channel 2 for normal operation. Clearing this bit disables channel 2.

Chnl1E Channel 1 Enable Control—A general enable control for channel 1. Setting this bit enables channel 1 for normal operation. Clearing this bit disables channel 1.

Chnl4IntE Channel 4 Interrupt Enable Control—A general interrupt enable for Channel 4. When cleared, any interrupt resulting from events in channel 4 are disabled and is not asserted on INTR* pin. When set, interrupts occurring due to events in channel 4 are asserted on INTR* pin, depending on the status of the specific event interrupt enable control bit.

Chnl3IntE Channel 3 Interrupt Enable Control—The same behavior as Chnl4IntE applied to channel 3.

Chnl2IntE Channel 2 Interrupt Enable Control— The same behavior as Chnl4IntE applied to channel 2.

Chnl1IntE Channel 1 Interrupt Enable Control—The same behavior as Chnl4IntE applied to channel 1.

General2 Control Register (GCR01)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	1SecTimIE	OneSecOut	OneSecIn	OneSecMod	SWRst

Default after reset: 00(h)
Direction: Read/Write
Modification: Bits 0, 1, 4: dynamic, bits 2, 3: OneSecMod—static

1SecTimIE One Second Timer Interrupt Enable—A control bit that allows interrupts to appear on the INTR* pin due to the occurrence of a one-second trigger (see Section 2.2.6)

OneSecOut One-Second Pin Output—When set, defines the ONESEC pin as an output pin, setting the triggering mode for one-second latching (see Section 2.2.6). When cleared, ONESEC is either an input or undefined according to the value of the OneSecIn bit in this register. During and after reset, ONESEC drives high Z (neither in Output State nor in input state).

NOTE: OneSecOut and OneSecIn bits should not be both set at the same time.

OneSecIn One-Second Pin Input—When set, defines the ONESEC pin as an input pin, setting the triggering mode for one-second latching (see Section 2.2.6). When cleared, ONESEC is either an output or undefined according to the value of OneSecOut bit in this register. During and after reset, ONESEC drives high Z (neither in output state nor in input state).

NOTE: OneSecOut and OneSecIn bits should not be both set at the same time.

OneSecMod One-Second Latching Mode—When set, the one-second latching mode is in effect (see Section 2.2.6).

SWRst Software Reset—Setting this bit produces a reset identical to that produced via the RESET* pin. Internal circuitry clears this bit once the reset is asserted.

Channel Control Registers

The index letter *i*, appearing in the registers' name, represents the channel number, one per channel.

Mode Control Register (CR00i)

7	6	5	4	3	2	1	0
LineLp	SourceLp	TxAlm1	TxAlm0	Reserved	Reserved	E3Frm	CbitP/832

Default after reset: 00(h)
Direction: Read/Write
Modification: Bits 4–7: dynamic, bits 0–1: static

LineLp Shallow Line Loopback Enable—Set to enable loopback in the external direction (back to network). This loopback connects the received data stream before B3ZS/HDB3 decoding to the transmitter. All data and overhead bits are looped, and Bipolar Code Violations (BPVs) are fully preserved per ANSI standard T1.404. The received data is presented to all receiver blocks, and is present on the receiver output pins.

A dynamic change of this bit can cause loss of data for a few clock cycles, until the channel is internally synchronized. Activation or deactivation of a loopback causes internal circuits to switch between clocks. After writing this bit, the microprocessor should not access any of the device registers (read/write) for 20 slowest clock cycles.

SourceLp Source Loopback Enable—Set to enable the loopback in the internal direction. This loopback connects the encoded transmitter data and clock directly to receiver B3ZS/HDB3 decoder. Transmission of data on the line is not affected by this loopback.

A dynamic change of this bit can cause loss of data for a few clock cycles, until the channel is internally synchronized. Activation or deactivation of a loopback causes internal circuits to switch between clocks, after writing to this bit, the microprocessor should not access any of the device registers (read or write) for 20 slowest clock cycles.

TxAlm1,0 Transmit Alarm Control—Used to control transmission of various alarm signals. In DS3 mode, AIS, idle, and yellow alarm signals on the outgoing DS3 stream are controlled as follows:

TxAlm1	TxAlm0	Alarm Action
0	0	Normal, No Alarms Transmitted
0	1	Yellow Alarm (X-bits low) Transmitted
1	0	Idle Code Transmitted
1	1	AIS Transmitted

In E3-G.751 and E3-G.832 modes, the TxAlm0 bit is set high to transmit the E3 AIS signal. The TxAlm1 bit is set high to transmit the E3 yellow alarm (A-bit or RDI bit high). TxAlm0 bit has precedence in E3 mode.

E3Frm E3 Framing Mode—Enables the E3 mode framing and transmission circuitry. When cleared, DS3 mode is active. The specific framing format is defined according to CbitP/832 bit.

CbitP/832 C-Bit Parity/E3-G.832 Mode—Selects which type of framing is present on the transmitted DS3/E3 signal.

E3Frm	CbitP/832	Framing Mode
0	0	DS3-M13/M23
0	1	DS3-C Bit Parity
1	0	E3-G.751
1	1	E3-G.832

Counter Interrupt Control Register (CR01i)

The Counter Interrupt Control register is provided to enable or disable individual interrupt sources. To enable an interrupt for a particular counter, the control bit corresponding to that counter must be set high in the Interrupt Control register. This enables the interrupt from that source to be asserted on the INTR* output pin. If a counter has its interrupt control bit set low, interrupts from this counter are masked from asserting on INTR*.

7	6	5	4	3	2	1	0
EXZCtrlE	XDgrCtrlE	LCVCtrlE	FEBECtrlE	PthCtrlE	FerrCtrlE	PDgrCtrlE	ParCtrlE

Default after reset: 00(h)
Direction: Read/Write
Modification: Dynamic

EXZCtrlE Excessive Zeros Counter Interrupt Enable—A control bit that allows interrupts from the DS3/E3 EXZ Counter to appear on INTR* pin.

XDgrCtrlE X-bits Disagreement Counter Interrupt Enable—A control bit that allows interrupts from the DS3/Disagreement Counter to appear on INTR* pin.

LCVCtrlE Line Code Violation Counter Interrupt Enable—A control bit that allows interrupts from the DS3/E3LCV Counter to appear on INTR* pin.

FEBECtrlE FEBE Event Counter Interrupt Enable—A control bit that allows interrupts from the DS3 FEBE/E3-G.832 REI Event Counter to appear on INTR* pin.

PthCtrlE Path Parity Error Counter Interrupt Enable—A control bit that allows interrupts from the Path Parity Error Counter to appear on INTR* pin.

FerrCtrlE Frame Error Counter Interrupt Enable—A control bit that allows interrupts from the Frame Error Counter to appear on INTR* pin.

PDgrCtrlE Disagreement Counter Interrupt Enable—A control bit that allows interrupts from the DS3 P Disagreement Counters to appear on the INTR* output pin.

ParCtrlE Parity Error Counter Interrupt Enable—A control bit that allows interrupts from the DS3 Parity/E3-G.832 BIP-8 Error Counter to appear on INTR* pin.

Dual-Edge Interrupt Control Registers

The Dual-Edge Interrupt Control registers enable event detection as the source of an interrupt. The events are of a continuous type. Enabling the dual-edge interrupt causes assertion of an interrupt, due to detection of the event's start or to detection of the event's end. To enable an interrupt's appearance on the INTR* pin due to a particular event's start or end, the control bit corresponding to this event's start or end must be set high in these registers. If an event's start or end has its interrupt control bit set low, then interrupts due to this event's start or end are masked from appearing on INTR*. The reason for the dual-edge interrupt assertion can be viewed in the Dual-Edge Interrupt status registers.

Alarm Start Interrupt Control Register (CR02i)

7	6	5	4	3	2	1	0
Reserved	Reserved	SEFStrtIE	LOSStrtIE	IdleStrtIE	YelStrtIE	AISStrtIE	OOFStrtIE

Default after reset: 00(h)
Direction: Read/Write
Modification: Dynamic

SEFStrtIE Severely Errored Frame Start Interrupt Enable—Set to enable interrupts to be asserted on INTR* pin due to detection of SEF event start in DS3 mode. When the receiver detects an SEF condition start, the interrupt is asserted and the SEFStrt bit in Alarm Start Interrupt Status register is set. When this bit is cleared, detection of SEF start sets the appropriate status bit, however an interrupt is not activated. This bit has no effect in E3-G.751 and E3-G.832 modes.

LOSStrtIE Loss of Signal Start Interrupt Enable—Set to enable interrupts to be asserted on INTR* pin, due to a detection of LOS condition start in all modes. When a LOS condition start is detected, the interrupt is asserted and the LOSStrt bit in Alarm Start Interrupt Status register is set. When this bit is cleared, detection of LOS start sets the appropriate status bit; however, an interrupt is not activated.

IdleStrtIE Idle Interrupt Start Enable—Set to enable interrupts to appear on INTR* due to detection of Idle event start in DS3 mode. When the receiver detects an Idle start, the interrupt is asserted and the IdleStrt bit in Alarm Start Interrupt Status register is set. When this bit is cleared, detection of Idle start sets the appropriate status bit; however, an interrupt is not activated.

This bit has no effect in E3-G.751 and E3-G.832 modes.

YelStrtIE Yellow Alarm Start Interrupt Enable—Set to enable interrupts to be asserted on INTR* due to detection of RAI/RDI event start in all modes. When the receiver detects an RAI/RDI event start, the interrupt is asserted and YelStrt bit in Alarm Start Interrupt Status register is set. When this bit is cleared, detection of RAI/RDI start sets the appropriate status bit; however, an interrupt is not activated.

AISStrtIE Alarm Indication Signal Start Interrupt Enable—Set to enable interrupts to be asserted on INTR* due to detection of AIS event start in all modes. When the receiver detects an AIS event start, the interrupt is asserted and AISStrt bit in Alarm Start Interrupt Status register is set. When this bit is cleared, detection of AIS start sets the appropriate status bit; however, an interrupt is not activated.

OOFStrtIE Out of Frame Start Interrupt Enable—Set to enable interrupts to be asserted on INTR* pin due to detection of OOF condition start in all modes. When the receiver detects an OOF condition

start, the interrupt is asserted and OOFStrt bit in Alarm Start Interrupt Status register is set. When this bit is cleared, detection of OOF start sets the appropriate status bit; however, an interrupt is not activated.

Alarm End Interrupt Control Register (CR03i)

NOTE: Reserved bits in Control registers must be set to zero.

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	LOSEndIE	IdleEndIE	YelEndIE	AISEndIE	OOFEndIE

Default after reset: 00(h)
Direction: Read/Write
Modification: Dynamic

LOSEndIE Loss of Signal End Interrupt Enable—Set to enable interrupts to be asserted on INTR* pin due to detection of LOS condition end in all modes. When a LOS condition end is detected, the interrupt is asserted and LOSEnd bit in Alarm End Interrupt Status register is set. When this bit is cleared, detection of LOS end sets the appropriate status bit; however, an interrupt is not activated.

IdleEndIE Idle Interrupt End Enable—Set to enable interrupts be asserted on INTR* pin due to detection of Idle event end in DS3 mode. When the receiver detects an Idle end, the interrupt is asserted and IdleEnd bit in Alarm End Interrupt Status register is set. When this bit is cleared, detection of Idle end sets the appropriate status bit; however, an interrupt is not activated. This bit has no effect in E3-G.751 and E3-G.832 modes.

YelEndIE Yellow Alarm End Interrupt Enable—Set to enable interrupts to be asserted on INTR* pin due to detection of RAI/RDI event end in all modes. When the receiver detects an RAI/RDI event end, the interrupt is asserted and YelEnd bit in Alarm End Interrupt Status register is set. When this bit is cleared, detection of RAI/RDI end sets the appropriate status bit; however, an interrupt is not activated.

AISEndIE Alarm Indication Signal End Interrupt Enable—Set to enable interrupts to be asserted on INTR* pin due to detection of AIS event end in all modes. When the receiver detects an AIS event end, the interrupt is asserted and AISEnd bit in Alarm End Interrupt Status register is set. When this bit is cleared, detection of AIS end sets the appropriate status bit; however, an interrupt is not activated.

OOFEndIE Out of Frame End Interrupt Enable—Set to enable interrupts be asserted on INTR* pin due to detection of OOF condition end in all modes. When the receiver detects an OOF condition end, the interrupt is asserted and OOFEnd bit in Alarm End Interrupt Status register is set. When this bit is cleared, detection of OOF end sets the appropriate status bit; however, an interrupt is not activated.

3.4 Feature Control Registers

The set of Feature Control registers is provided to enable or disable miscellaneous features in the CX2834i devices.

Feature1 Control Register (CR04i)

7	6	5	4	3	2	1	0
TxAMI	RxAMI	NRZMod	Reserved	Reserved	FEBEC/PT[1]	FEBEC/PT[2]	FEBEC/PT[3]

Default after reset: 07(h)
Direction: Read/Write
Modification: Bits 0–2: dynamic; bits 5–7: static

TxAMI Transmit AMI Mode—Set high to enable AMI line coding on TXPOS and TXNEG (no B3ZS/HDB3 encoding or decoding). When cleared, B3ZS/HDB3 line coding is used on these pins. This bit is effective only when NRZMod bit is cleared.

RxAMI Receive AMI Mode—Set high to enable AMI line coding on RXPOS and RXNEG (no B3ZS/HDB3 encoding or decoding). When cleared, these pins use B3ZS/HDB3 line coding.

NOTE: This bit is effective only when NRZMod bit is cleared.

NRZMod NRZ Mode—Set high to disable bipolar (B3ZS/HDB3 or AMI) encoding or decoding and provide a unipolar NRZ line code on TXPOS/TXNEG and RXPOS/RXNEG. Setting this bit disables and bypasses the encoder and decoder circuits. The unipolar output appears at the TXPOS pin while TXNEG pin is continuously low and the clock is available on TCLKO pin. The unipolar input should appear on RXPOS, while RXNEG can be tied to the LCV output of the LIU and be used as an increment control of the LCV counter.

NRZMod	RxAMI	TxAMI	Description
0	0	X	B3ZS/HDB3 encoded data on RXPOS, RXNEG
0	1	X	AMI encoded data on RXPOS, RXNEG
0	X	0	B3ZS/HDB3 encoded data on TXPOS, TXNEG
0	X	1	AMI encoded data on TXPOS, TXNEG
1	X	X	NRZ data on TXPOS, RXPOS; TXNEG is set to zero; RXNEG is used as an LCV input from the LIU (if unused, should be tied low)

FEBEC/PT[1:3] FEBE Pattern/Payload Type Bit Field—In DS3 mode set to the 3-bit sequence that is sent each time a FEBE indication is transmitted in C-bit parity mode. This pattern is automatically transmitted when the ExtFEBE/Cj bit in the Transmit Overhead Insertion 1 Control register is cleared, and the receiver detects a framing or path parity error. This pattern must not be all-1s to indicate a FEBE to the far end. An all-1s pattern disables FEBE transmission and should not be used for any other purpose. In E3-G.832 mode set to the 3-bit pattern that is transmitted every frame in the payload type field in the MA byte.

In both modes, FEBEC/PT[1] bit is transmitted first and FEBEC/PT[3] bit is transmitted last. In both modes, writing a new value to this byte takes effect only starting from the next

transmitted frame. In DS3-M13/M23 and E3-G.751 modes, this field has no effect.

Feature2 Control Register (CR05i)

7	6	5	4	3	2	1	0
Reserved	Reserved	TxLOS	TxOvhMrk	TXSYOut	TXSYIn	TxInvClk	LtxCkRis

Default after rest: 01(h)
Direction: Read/Write
Modification: Bit 5: dynamic, bits 0-4: static

TxLOS Transmit Loss of Signal—This bit, when set results in the generation of all 0's (LOS) on the transmit line side. Setting this bit overrides any other programmed or inserted payload and overhead pattern with 0s.

TxOvhMrk Transmit Overhead Bits Mark—This bit controls the behavior of TXSY pin when programmed to be driven as an output. When set, TXSY marks the bit positions of all overhead bits. When cleared, TXSY marks the beginning of a new frame.

TXSYOut TXSY Pin Output Control—This bit determines if TXSY pin is an output of the chip. When set, this pin is an output, i.e., the transmitter circuit generates its own frame synchronization mechanism and signals the frame start or the overhead bit positions (according to TxOvhMrk bit) on TXSY pin to the system. When cleared, TXSY can be an input or undefined according to the value of TXSYIn bit in this register. During and after reset, TXSY drives high Z, and is neither in output state nor in input state.

NOTE: TXSYOut and TXSYIn bits should not be set at the same time.

TXSYIn TXSY in Input Control—This bit determines if TXSY pin is an input of the chip. When set, this pin is an input, i.e., the system generates a synchronization pulse and the transmitter circuit acts according to it. When cleared, TXSY can be an output or undefined according to the value of TXSYOut bit in this register. During and after reset, TXSY drives high Z, and is neither in output state nor in input state.

NOTE: TXSYOut and TXSYIn bits should not be set at the same time.

TxInvClk Transmit System Side Inverted Clocks—This bit controls the polarity of TXGAPCK and TEXTCK output clocks. When the bit is cleared, TXGAPCK and TEXTCK rising edges are derived from TXCKI falling edge. In this mode, both clock gaps are active low. When this bit is set, TXGAPCK and TEXTCK are inverted, hence TXGAPCK and TEXTCK falling edges are derived from TXCKI falling edge. In this mode, both clock gaps are active high.

LTxCkRis LIU Transmit Clock Polarity Control—Used to define the TCLKO edge upon which the transmitter output data (on TXPOS, TXNEG pins) is sampled by the LIU. When set, the data is clocked out by the chip on the falling edge of TCLKO. It is sampled by the LIU on the rising edge of TCLKO. When cleared, the data is clocked out by the chip on the rising edge of TCLKO; therefore, it is sampled by the LIU on the falling edge of TCLKO.

Feature3 Control Register (CR06i)

7	6	5	4	3	2	1	0
PayldLp	RlineLp	TxFEACIE	FEACSin	Rsvd	RxFEACSNEIE	RxFEACIdleIE	RxFEACIE

Default after reset: 00(h)
Direction: Read/Write
Modification: Bit 4: static, bits 0–2, 5-7: dynamic

PayldLp Payload Loopback Enable—Set to enable a payload loopback from the receiver circuit through the transmitter circuit back to the network. This loopback connects the received payload (after decoding, frame recovery and overhead extraction) to the transmitter input, where it is framed and encoded again. The received data is still present on the receiver output pins. A dynamic change of this bit can cause loss of data for a few clock cycles, until the channel is internally synchronized. Activation or deactivation of a loopback causes internal circuits to switch between clocks. After writing to this bit the microprocessor should not access any of the device registers (read/write) for 20 slowest clock cycles.

RlineLp Remote Line Loopback Enable—Set to enable loopback after decoding or encoding back to the network. If the receiver FIFO is disabled (RxFIFEn bit in Feature5 register is clear) data output of the B3ZS/HDB3 decoder connects to the transmitter encoder input. If the receiver FIFO is enabled (RxFIFEn bit is set), data output of this FIFO connects to the transmitter encoder input. Line Code Violations (LCV) are not preserved in this loopback. The received data is still presented to all receiver blocks and is present on the receiver outputs.

A dynamic change of this bit can cause loss of data, for a few clock cycles, until the channel is internally synchronized. Activation or deactivation of a loopback causes internal circuits to switch between clocks, after writing to this bit the microprocessor should not access any of the device registers (read or write) for 20 slowest clock cycles.

TxFEACIE Transmit FEAC Interrupt Enable—A control bit that allows interrupts from the FEAC transmitter to be asserted on INTR* pin when in DS3-C Bit Parity mode. When in single mode, the interrupt is asserted after every transmission of the code word written in the Transmit FEAC Channel Byte register. When in repetitive mode, the interrupt is asserted once the code word is transmitted 10 times.

FEACSin FEAC Channel in Single Mode—In DS3-C Bit Parity mode set to enable FEAC channel (in the transmitter and the receiver) in a single mode, i.e., assert an interrupt after a single reception or transmission of a code word. When clear, repetitive mode is enabled, i.e., an interrupt is asserted after completion of 10 repetitions of code word reception or transmission. In DS3-M13/M23, E3-G.751, and E3-G.832 modes this bit has no effect.

RxFEACSNEIE Receive FEAC Stack Not Empty Interrupt Enable—A control bit that allows interrupts to appear on INTR* pin due to detection of the FEAC stack being not empty (i.e., Receive FEAC stack byte is holding valid data). This bit is active both in single and repetitive modes.

RxFEACIdleIE Receive FEAC channel Idle Interrupt Enable—A control bit that allows interrupts to be asserted on INTR* pin due to detection of the start of an idle pattern over FEAC channel by the receiver circuit. This bit is active both in single and repetitive modes.

RxFEACIE Receive FEAC Interrupt Enable—A control bit that allows interrupts from the FEAC receiver to appear on INTR* pin when in DS3-C Bit Parity mode. When a legal code word is detected by the receiver (see Far-end Alarm and Control Channel Reception paragraph) this interrupt is asserted.

Feature4 Control Register (CR07i)

NOTE: This control register has an effect only in E3-G.832 mode. In DS3 and E3-G.751 modes the content of this register is ignored.

7	6	5	4	3	2	1	0
Reserved	SSMEn	SSM[1]/TM	SSM[2]	SSM[3]	SSM[4]	MAPD[1]	MAPD[2]

Default after reset: 00(h)
Direction: Read/Write
Modification: Bits 0–5: dynamic; Bit6: static

SSMEn SSM Mode Enable—Set to enable usage of bit 8 in the MA byte as an SSM field and of bits 6–7 in the MA byte as a multiframe indicator (MI) field. When cleared, bit 8 in the MA byte is the timing marker (TM) field and bits 6–7 in the MA byte are used as payload dependent (PD) field.

SSM[1]/TM SSM MSB/Timing Marker Bit Field—When SSM mode is enabled (SSMEn bit is set), this bit is the MS bit (transmitted first) to be sent in the SSM field (bit 8 in MA byte). When MI field has a value of 00, SSM [1] is inserted in the frame. When SSM mode is disabled (SSMEn bit is cleared), this bit is the timing marker. It is inserted on every frame in bit 8 position in the MA byte.

SSM[2:4] SSM Bit Field—When SSM mode is enabled (SSMEn bit is set), set to the three LS bits pattern to be sent in the SSM field (bit 8 of MA byte) according to the multiframe phase indicated by MI field. When MI field has a value of 01, SSM [2] is inserted in the frame. When MI field has a value of 10, SSM [3] is inserted in the frame. When MI field has a value of 11, SSM [4] is inserted in the frame. When SSM mode is disabled, this field is ignored.

MAPD[1:2] Payload Dependent Field in MA byte—When SSM mode is disabled (SSMEn bit in this register is cleared) and ExtFEAC/PD bit in Transmit Overhead Insertion register 1 clears, this field is sent in every frame in bits 6–7 of the MA byte. MAPD [1] bit transmits first. If SSM mode is enabled or ExtFEAC/PD is set, this field is ignored.

Feature5 Control Register (CR08i)

7	6	5	4	3	2	1	0
RxAutoAll1	RefrmStp	RxAIS	RXAll1	RxOvhMrk	RxFIFEn	RxInvClk	LRxCkRis

Default after rest: 00(h)
Direction: Read/Write
Modification: Bits 4–6: dynamic; Bits 0–3, 7: static

RxAutoAll1 Receive Automatic All 1s—Set to enable automatic generation of an all-1s stream on RXDAT pin in response to a fault detection. When set and a LOS, OOF, AIS, or Idle are detected in DS3 mode or LOS, OOF, or AIS are detected in E3 mode, the data received on RXPOS, RXNEG is presented to the receiver circuit, but is not present on RXDAT pin. It is overwritten by an all 1s stream. The assertion of all 1s continues as long as one or more of these conditions is valid. When clear, all 1s sequence on RXDAT pin occurs due to RxAll1 bit in this register. RxAll1 and RxAIS bits have precedence over the RxAutoAll1 bit.

RefrmStp Reframe Mechanism Stop—This bit controls the behavior of the frame-search mechanism. When this bit is set, no frame-search is conducted (regardless of OOF status) when it has been cleared frame-search resumes shifted forward by one bit from the current frame position, until a new framing is located when it is cleared searching occurs in response to an OOF status.

NOTE: To produce a forced reframe, the microprocessor usually needs two write cycles, the first to write 1 to the bit, and then to write 0 to it.

RxAIS Receive Data Stream AIS—Set to enable driving of an AIS pattern (in all DS3 and E3 modes) on RXDAT pin. When set, data received on RXPOS, RXNEG is presented to the receiver circuit but is not present on RXDAT pin. Detection and the count of errors, alarms, and events continue while this mode operates. When cleared, data received on RXPOS, RXNEG, and processed by the receiver circuit is present on RXDAT pin. If both RxAll1 and RxAIS are active, a data stream of all 1s is generated.

RxAll1 Receive Data Stream is All 1s—Set to enable driving an all-1s stream on RXDAT pin. When set, data received on RXPOS, RXNEG is presented to the receiver circuit, but is not present on RXDAT pin. Detection and the count of errors, alarms, and events continue while this mode operates. When cleared, the data received on RXPOS, RXNEG, and processed by the receiver circuit is present on RXDAT pin. If both RxAll1 and RxAIS are active, data stream of all 1s is generated.

RxOvhMrk Receive Overhead Bits Mark—This bit controls behavior of the RXMSY pin. When set, RXMSY marks the bit positions of all overhead bits. When cleared, RXMSY marks the beginning of a new frame. (See Section 2.2.2).

RxFIFEn Receiver FIFO Enable—Set to enable usage of the receiver FIFO buffer to provide jitter elasticity to the input data stream. When set, data from the B3ZS/HDB3 decoder is sampled into the FIFO buffer using LINECK clock, and is taken out of the FIFO buffer according to RXCKI clock. When cleared, the FIFO buffer is bypassed, data goes from the decoder directly into the frame recovery circuit and the only clock used in the receiver circuitry is LINECK. Activation or deactivation of the FIFO buffer causes internal circuits to switch between clocks after writing to this bit. The microprocessor should not access any of the device registers (read or write) for 20 slowest clock cycles.

RxInvClk Receive System Side Inverted Clocks—This bit controls the polarity of RXGAPCK and REXTCK output clocks. When the bit is cleared, RXGAPCK and REXTCK rising edges are in parallel to the data change on RXDAT pin. In this mode, both clock gaps are active low. When this bit is set, RXGAPCK and REXTCK are inverted. The RXGAPCK and REXTCK falling edges are in parallel to the data change on RXDAT pin. In this mode, both clock gaps are active high.

LRxCkRis LIU Receive Clock Polarity Control—Used to define the LINECK edge upon which the receiver input data (on RXPOS, RXNEG pins) is clocked out by the LIU. When set, data is sampled by the device on the falling edge of LINECK, therefore it is clocked out by the LIU on the rising edge of LINECK. When clear, data is sampled by the chip on the rising edge of LINECK, therefore it is clocked out by the LIU on the falling edge of LINECK.

Transmit Overhead Insertion Control Registers

The Transmit Overhead Insertion Control registers are provided to enable insertion of different overhead fields from different sources listed below:

- Internal automatic generation
- Internal registers programmed by the microprocessor
- The system via the data stream
- The system via TEXT pin

NOTE: Not all the sources are available for every overhead field in every mode. Some of the control bits have no effect in a specific mode. Some of the bits have multiple meanings, it depends on the working mode.

Transmit Overhead Insertion1 Control Register (CR09i)

7	6	5	4	3	2	1	0
DLMod[2]	DLMod[1]	DLMod[0]	AutoRAI	ExtFEBE/Cj	ExtCP/TR	ExtFEAC/PD	ExtDat

Default after reset: 00(h)
Direction: Read/Write
Modification: Bits 0–2, 4: static, bits 6–7: dynamic, bit 5: dynamic for DL (G.832) and static for reserved C-bits (DS3), bit 3: dynamic for Cj and static for FEBE

DLMod[2:0] Data Link Mode—This field is interpreted differently in different working modes. In E3-G.832 mode, it is a three-bit field that determines the source of NR and GC bytes. In E3-G.751, only DLMod [2:1] determines the source of the N-bit, while DLMod [0] has no effect. In DS3-C, Bit Parity mode DLMod [2:1] determines the source of the data link (Cb5), and DLMod [0] determines the source of the reserved C-bits. In DS3-M13/M23, this field has no effect.

NOTE: If the system wants to change the source of the data link (i.e., internal FIFO to TEXT pin), it must first disable the data link and then enable it by setting the appropriate mode. Another example is that when changing the type of byte processed by the internal HDLC circuit (NR to GC or vice versa) in E3-G.832 mode, the data link must be disabled first for both (by writing 0 to all three bits).

Tables 3-3 and 3-4 detail the interpretation of this field in the different modes.

Table 3-3. DS3-C Bit Parity/E3-G.751 Mode Field Interpretation

DLMod[2]	DLMod[1]	Description
0	X	Transmit Data Link circuit is disabled, and the framer automatically sends the all-1s pattern on Cb5 bits/N-bit.
1	0	Data link data is inserted through the Transmit Data Link FIFO buffer and is processed by the internal HDLC circuit.
1	1	Data link data is inserted through the TEXT pin and is unaffected by the internal HDLC circuit.

DS3-C Bit Parity

DLMod [0] controls the reserved C-bits (C12, Cb2, Cb6, and Cb7) generation. When set, these bits are inserted via the TEXT pin. When cleared, these bits are automatically generated as all 1s. In this mode, the bit is static.

Table 3-4. E3-G.832 Mode Field Interpretation

DLMod[2]	DLMod[1]	DLMod[0]	Description
0	0	0	Data link on the NR byte is disabled and the chip automatically generates an FF(h) pattern on these bits. Data link on the GC byte is disabled and the chip automatically generates an FF(h) pattern on these bits.
0	0	1	Data link on the NR byte is disabled, and the chip automatically generates an FF(h) pattern on these bits. GC data is inserted via the TEXT pin and is unaffected by the internal HDLC circuit.
0	1	0	Data link on the NR byte is disabled and the chip automatically generates an FF(h) pattern on these bits. GC data is inserted through the Transmit Data Link FIFO buffer and is processed by the internal HDLC circuit.
0	1	1	NR data is inserted via the TEXT pin, it is unaffected by the internal HDLC circuit. Data link on GC byte is disabled and the chip automatically generates FF(h) pattern on these bits.
1	0	0	NR data is inserted via the TEXT pin; it is unaffected by the internal HDLC circuit. GC data is inserted through the Transmit Data Link FIFO buffer and is processed by the internal HDLC circuit.
1	0	1	NR data is inserted through the Transmit Data Link FIFO buffer and is processed by the internal HDLC circuit. GC data is inserted via the TEXT pin and is unaffected by the internal HDLC circuit.
1	1	0	NR data is inserted through the Transmit Data Link FIFO buffer and is processed by the internal HDLC circuit. Data link on GC byte is disabled and the chip automatically generates an FF(h) pattern on these bits.
1	1	1	Both NR and GC data are inserted via the TEXT pin; they are unaffected by the internal HDLC circuit.

AutoRAI Automatic RAI/RDI Generation Control—Set to enable automatic generation of the RAI or RDI alarm in response to a fault detection. When set, an automatic assertion of the RAI bit in E3-G.751 mode or RDI bit in E3-G.832 mode occurs once the receiver detects a LOS or OOF condition. The automatic assertion continues as long as one or more of these conditions is valid. The TxAlm [1] bit in the Mode Control register still effects RAI/RDI generation in E3 mode while this bit is set. When clear, RAI and RDI generation occurs due to the TxAlm [1] bit in the Mode Control register and there is no automatic generation. This bit has no effect in DS3 mode. Generation of an RAI alarm in DS3 mode is controlled only by TxAlm bits.

ExtFEBE/Cj External FEBE/Justification Control— Set to enable insertion of FEBE or Justification Control bits via the TEXT pin. In DS3-C Bit Parity mode, setting this bit enables insertion of FEBE field via TEXT pin. In DS3-M13/M23 mode, setting this bit enables insertion of all C-bits (used for Justification Control) via TEXT pin. In E3-G.751 mode, setting this bit enables insertion of all Cj bits (used for Justification Control) via TEXT pin. In E3-G.832 mode, setting this bit enables insertion of REI bit in MA byte via TEXT pin. When this bit is cleared, FEBE bits are transmitted automatically upon detection of framing or CP error by the receiver according to the contents of FEBEC/PT field described in the Feature1 Control register, DS3-C Bit Parity mode. In DS3-M13/M23 mode or E3-G.751 mode, Justification Control bits are inserted via the data stream when this bit is cleared. In E3-G.832 mode, the REI bit is set automatically by the transmitter upon detection of BIP-8 error if this bit is cleared.

ExtCP/TR External CP/Trail Trace Control—Set to enable insertion of CP-bits or TR byte via TEXT pin. In DS3-C Bit Parity mode, setting this bit enables insertion of CP field via TEXT pin. In E3-G.832 mode, setting this bit enables insertion of Trail Trace byte via TEXT pin. In E3-G.832, when this bit is cleared, the transmitter automatically transmits 00(h) on TR byte. In DS3-M13/M23 and E3-G.751 modes, this bit has no effect.

ExtFEAC/PD External FEAC/Payload Dependent/Multiframe Indicator Field Control—Set to enable insertion of FEAC channel or payload dependent field via TEXT pin. In DS3-C Bit Parity mode, setting this bit enables insertion of FEAC channel via TEXT pin. In E3-G.832 mode, setting this bit enables insertion of payload dependent, multiframe indicator field in MA byte via TEXT pin. When this bit is cleared, FEAC channel is inserted through a programmable register (Transmit FEAC Channel Byte) in DS3-C Bit Parity mode. In E3-G.832, payload dependent field is inserted through a programmable register (MAPD field in Feature4 control register) when this bit is cleared and SSMEn bit (in Feature4 Control register) is also cleared. If SSMEn is set, i.e., bits 6–7 in MA byte are used as a multiframe indicator, the MI is internally produced cycling through the values 00, 01, 10, and 11 on an arbitrarily-defined, 4-frame multiframe. In DS3-M13/M23 and E3-G.751 modes, this bit has no effect.

ExtDat External Data Control—Set to enable all overhead bits to be inserted via the data stream. When set, this bit overrides the rest of the control bits in this register. It disables internal generation of overhead bits (automatic or through programmable registers) and forces the device to use the overhead bits inserted in the data stream of the Transmit Overhead Insertion2 Control register. When clear, overhead configuration is determined by the rest of the control bits as described above. This bit affects all modes. Setting of TxAlm [1:0] bits is effective even during ExtDat = 1.

Transmit Overhead Insertion2 Control Register (CR10i)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	ExtStf	ExtFrmAl	ExtP	ExtRAI

Default after reset: 00(h)
Direction: Read/Write
Modification: Static

ExtStf External Stuff Bits—Set to enable insertion of Stuff Opportunity bits via TEXT pin in DS3-M13/M23 and E3-G.751 modes. When clear, stuff bits are inserted with the payload. This bit has no affect in DS3-C-bit parity and E3-G.832 modes.

ExtFrmAl External Frame Alignment Bits—Set to enable insertion of F and M-bits (DS3 mode), FAS (E3-G.751), FA1 and FA2 (E3-G.832) bits via TEXT pin. When clear, the frame alignment bits are automatically generated by the internal circuitry.

ExtP External P-Bit Control—Set to enable insertion of P-bits via TEXT pin in DS3-C Bit Parity and DS3-M13/M23 modes. When clear, P-bits are automatically calculated by the internal circuitry. In E3-G.751 and E3-G.832 modes, this bit has no effect.

ExtRAI External X/A/RDI-Bit Control—Set to enable insertion of X-bits (in DS3), A-bit (in E3-G.751), and RDI (in E3-G.832) via TEXT pin. It affects E3 when AutoRAI bit is clear.

REXTCK Control Register (CR11i)

The REXTCK Control register provides enabled marking of different fields through REXTCK pin. Presentation of a field through REXTCK pin does not prevent it from being ticked upon by the RXGAPCK pin or from being processed via the microprocessor interface. Setting a bit in this register does not affect other control bits set in other registers. This enables monitoring of certain fields for testing, in addition to being processed by another mechanism. If a specific field should be presented only through the REXTCK pin, it should be disabled from being presented on RXGAPCK/ microprocessor interface in another control register.

7	6	5	4	3	2	1	0
ExtReserved/ GC	ExtDL/NR	ExtFEBE/A	ExtCP/TM	ExtFEAC/PD/ Stf	ExtAIC/Cj/TR	ExtFrm	AllRxExt

Default after reset: 00(h)
Direction: Read/Write
Modification: Static

ExtReserved/GC External Reserved C-bits/GC Byte—Set to enable presentation of reserved C-bits (C12, C2, C6, C7) in DS3-C Bit Parity mode or presentation of GC byte in E3-G.832 mode through REXTCK pin. In DS3-M13/M23 and E3-G.751 modes, this bit is ignored.

ExtDL/NR External Data Link/NR Byte—Set to enable presentation of data link data through REXTCK pin. The bits are output exactly as they were received (i.e., the HDLC circuit is bypassed). In DS3-C Bit Parity mode, this bit enables presentation of C5 bits through REXTCK pin. In E3-G.751 mode, this bit enables presentation of N-bit through REXTCK pin. In E3-G.832 mode, this bit enables presentation of NR byte through REXTCK pin. In DS3-M13/M23, this bit is ignored.

ExtFEBE/A External FEBE/REI/A-Bit—Set to enable presentation of FEBE field in DS3-C Bit Parity mode or REI bit field in E3-G.832 mode through the REXTCK pin. In E3-G.751 mode, set to enable presentation of A-bit through REXTCK pin. In DS3-M13/M23 mode, this bit is ignored.

ExtCP/TM External Path Parity/Timing Marker/SSM—Set to enable presentation of CP field in DS3-C Bit Parity mode or Timing Marker/SSM bit field in E3-G.832 mode through REXTCK pin. In DS3-M13/M23 and E3-G.751 modes, this bit is ignored.

ExtFEAC/PD/Stf External FEAC/Payload Dependent/Multiframe Indicator/Stuff Opportunity Bits—Set to enable presentation of FEAC channel in DS3-C Bit Parity mode or payload dependent/ multiframe indicator field in E3-G.832 mode or Stuff Opportunity bits in DS3 M13/M23 and in E3-G.751 modes through REXTCK pin.

ExtAIC/Cj/TR External AIC/Justification Control/Trail Trace—In DS3-C Bit Parity mode, set to enable presentation of application identification channel through REXTCK pin. In DS3-M13/M23 and E3-G.751 modes, set to enable presentation of the Justification Control bits through the REXTCK pin. In E3-G.832 mode, set to enable presentation of Trail Trace byte through REXTCK pin.

ExtFrm External Framing Fields—In DS3 modes, set to enable presentation of M, F, X, and P-bits through the REXTCK pin. In E3-G.751 mode, set to enable presentation of FAS field through the REXTCK pin. In E3-G.832 mode, set to enable presentation of FA1, FA2, EM, RDI, and PT fields through REXTCK pin.

AllRxExt All Received Data is External—Set to enable presentation of the complete frame, i.e., payload and overhead bits, through REXTCK pin. This bit is available in all framing modes. When this bit is set, it overrides the rest of the bits in this register. Presentation of overhead bits through the RXGAPCK pin or through the microprocessor interface in parallel to REXTCK is determined by the Receive Overhead Control register and by the RxDLEn bit in Receive Data Link Control register.

Receive Overhead Control Register (CR12i)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	RxStfDat	RxCjDat	AllOVHDat

Default after reset: 00(h)
Direction: Read/Write
Modification: Static

RxStfDat Received Stuff Opportunity Bits in the Data Stream—Set to enable presentation of the Stuff Opportunity bits in the Data Stream over RXDAT pin in DS3-M13/M23 and E3-G.751 modes. When set, RXGAPCK is not gapped over the Stuff Opportunity bit positions. When clear, the Stuff Opportunity bits are not extracted (i.e., RXGAPCK is gapped over their bits positions). When AllOVHDat bit in this register is set, this bit is ignored. In DS3-C Bit Parity and E3-G.832 modes, this bit is ignored.

RxCjDat Received Justification Control Bits in the Data Stream—Set to enable presentation of the Justification Control bits in the data stream over RXDAT pin in DS3-M13/M23 and E3-G.751 modes. When set, RXGAPCK is not gapped over the Justification Control bit positions. When clear, the Justification Control bits are not extracted (i.e., RXGAPCK is gapped over their bit positions). When AllOVHDat bit in this register is set, this bit is ignored. In DS3-C Bit Parity and E3-G.832 modes, this bit is ignored.

AllOVHDat All Overhead Bits Are in the Data Stream—Set to enable presentation of the complete frame in the data stream over RXDAT pin (i.e., RXGAPCK is a nominal clock, it is not gapped). This bit is available in all framing modes. When this bit is set, it overrides RxCjDat and RxStfDat bits in this register. When this bit is cleared, presenting the Justification Control bits on RXDAT (RXGAPCK gapping over Cj bit positions) is determined by RxCjDat bit in this register, and presenting the Stuff Opportunity bits in RXDAT (RXGAPCK gapping over Stuff bits positions) is determined by RxStfDat bit in this register. Other overhead bits are not presented on RXDAT pin when this bit is cleared (i.e., RXGAPCK is gapped accordingly).

The following table details RXGAPCK output behavior in different modes according to these bit settings:

RxStfDat	RxCjDat	AllOVHDat	RXGAPCK Output Behavior
X	X	1	Nominal
0	0	0	Tick on Payload bits only (also not on Stuff Opportunity bits)
0	1	0	Ticks only on Payload bits and on Justification Control bits (in DS3-M13/M23 and in E3-G.751)
1	0	0	Ticks only on Payload bits and on Stuff Opportunity bits (in DS3-M13/M23 and in E3-G.751)
1	1	0	Ticks on Payload, Stuff Opportunity, and Justification Control bits (in DS3-M13/M23 and in E3-G.751)

Transmit Data Link Control Register (CR13i)

The Transmit Data Link Control register (CR13i) enables different modes and interrupts in the Transmit Data Link operation.

NOTE:Reserved bits in Control registers must be set to zero.

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	TxMsgIE	TxURIE	TxNEIE	TxFCSEn

Default after reset: 00(h)
Direction: Read/Write
Modification: Bits 1–3: dynamic, bits –DL: static

TxMsgIE Transmit Data Link Message Transmitted Interrupt Enable—Set to enable interrupt assertion on INTR* pin due to end of transmission of a full message, see Section 2.1.3.

TxURIE Transmit Data Link FIFO Underrun Interrupt Enable—Set to enable interrupt assertion on INTR* pin due to Data Link FIFO underrun error, see Section 2.1.3.

TxNEIE Transmit Data Link FIFO Near-Empty Interrupt Enable—Set to enable interrupt assertion on INTR* pin due to the FIFO buffer being near empty, see Section 2.1.3.

TxFCSEn Transmit Data Link FCS Calculation Enable—Set to enable FCS calculation over the transmitted message and add it to the end of the transmitted message. When cleared, the FCS calculation and addition are executed by the software.

Transmit Data Link Threshold Control Register (CR14i)

7	6	5	4	3	2	1	0
Reserved	TxNEThr[6]	TxNEThr[5]	TxNEThr[4]	TxNEThr[3]	TxNEThr[2]	TxNEThr[1]	TxNEThr[0]

Default after reset: 00(h)
Direction: Read/Write
Modification: DL—static

TxNEThr[6:0] Transmit Data Link FIFO Near Empty Threshold—Set to the threshold value, used to indicate a near-empty FIFO event. The range of values available for this purpose is 0–126, where 00(h) is interpreted as 0, 01(h) is 1 …etc. and 7E(h) is interpreted as 126.

Transmit Data Link Message Byte (CR15i)

7	6	5	4	3	2	1	0
TxDLMsg[7]	TxDLMsg[6]	TxDLMsg[5]	TxDLMsg[4]	TxDLMsg[3]	TxDLMsg[2]	TxDLMsg[1]	TxDLMsg[0]

Default after reset: Undefined
Direction: Read/Write
Modification: Dynamic

TxDLMsg [7:0] Transmit Data Link Message Byte—This byte is loaded with data to be written into the Data Link FIFO buffer, which is later transmitted by the Data Link Transmitter circuit. Two addresses are allocated for this register. During the whole message, excepting the last byte, the lower address is used to access this register. When the last byte of the message is written to this register, the higher address is used. The higher address indicates the end of the message to the transmitter circuit. TxDLMsg [0] bit is transmitted first and TxDLMsg [7] bit is transmitted last. Reading this register causes latching of the content of the FIFO stage pointed by the Transmit Data Link Read pointer into this register.

Receive Data Link Control Register (CR16i)

The Receive Data Link Control register enables operation of the receiver terminal data link circuit, defines the FCS mode, and enables interrupt assertion due to data link events.

NOTE: Reserved bits in control registers must be set to zero.

7	6	5	4	3	2	1	0
Reserved	Reserved	NRDL	RxOVRIE	RxMsgIE	RxNFIE	RxFCSEn	RxDLEn

Default after reset: 00(h)
Direction: Read/Write
Modification: Bits 0, 2–4: dynamic, bits 1, 5: DL-static

NRDL NR Byte Over the Data Link—This bit is effective only in E3-G.832 mode. When set, selects NR byte to be processed by the receiver data link HDLC and FIFO circuits. When cleared, selects GC byte to be processed by the receiver data link HDLC and FIFO circuits.

RxOVRIE Receive Data Link FIFO Overrun Interrupt Enable—Set to enable interrupt assertion due to Data Link FIFO overrun error.

RxMsgIE Receive Data Link Message Interrupt Enable— Set to enable interrupt assertion due to a message received event.

RxNFIE Receive Data Link FIFO Near-Full Interrupt Enable—Set to enable interrupt assertion due to the FIFO near-full event.

RxFCSEn Receive Data Link FCS Check Enable—Set to enable execution of an FCS check on the received message. When cleared, the FCS check is executed by software; therefore, no interrupt or status due to bad FCS appears.

RxDLEn Receive Data Link Enable—Set to enable operation of the Receive Data Link FIFO buffer and HDLC/LAPD circuits over the selected data link channel (Cb5, N-bit, NR, or GC). When cleared, the data link channel data is left unchanged (may be presented on the data stream via the REXTCK and RXGAPCK clocks), and no receive datalink interrupts (enabled in this register) are asserted.

Receive Data Link Threshold Control Register (CR17i)

7	6	5	4	3	2	1	0
Reserved	RxNFThr[6]	RxNFThr[5]	RxNFThr[4]	RxNFThr[3]	RxNFThr[2]	RxNFThr[1]	RxNFThr[0]

Default after reset: 7F(h)
Direction: Read/Write
Modification: DL—static

RxNFThr [6:0] Receive Data Link FIFO Near Full Threshold—Set to the threshold value; used to indicate a near-full FIFO event. The range of values available for this purpose is 2–127, where 02(h) is interpreted as 2 and 7F(h) is interpreted as 127.

Transmit FEAC Channel Byte (CR18i)

7	6	5	4	3	2	1	0
TxFEAC[7]	TxFEAC[6]	TxFEAC[5]	TxFEAC[4]	TxFEAC[3]	TxFEAC[2]	TxFEAC[1]	TxFEAC[0]

Default after reset: FF(h)
Direction: Read/Write
Modification: Dynamic

TxFEAC[7:0] Transmit FEAC Channel Message Byte—If the mode is set to DS3-C Bit Parity, this register is used as the data byte for the transmit FEAC channel transmitter. When this byte is in the form 0xxxxxx0 it is transmitted after every flag. If there is a 1 in either the most significant or least significant bit of this register, an all-1s (idle) is transmitted on FEAC channel. An interrupt is associated with this channel and is enabled by TxFEACIE bit in Feature3 Control register. For interrupt activation, see Section 2.1.4. TxFEAC [0] bit is transmitted first and TxFEAC [7] bit is transmitted last.

Error Insertion Control Registers

Error insertion registers enable single insertion of different errors. Setting the relevant bit causes insertion of the requested error at the next valid opportunity. The relevant control bit clears once the error is inserted. Therefore, the control bits have to be polled before setting them for the next error insertion. Several Error Insertion Control bits can be set at the same time; each one of them is cleared when the appropriate error is inserted.

NOTE: The software can only set the Error Insertion bits. Writing 0 to these bits leaves them unaffected. Some of the bits are valid only in certain modes. When not valid, setting the bits has no effect and they are not cleared. Reserved bits are cleared to 0. Value after enabling Error Insertion Control bits = 0.

Error Insertion1 Control Register (CR19i)

7	6	5	4	3	2	1	0
FEBEErr	XdgrErr	YelErr	CPErr	ParDgrErr	ParErr	FrmErrM	FrmErrF

Default after reset: 00(h)
Direction: Read/Write
Modification: Dynamic

FEBEErr FEBE Error Insertion Control—Causes insertion of a FEBE error at the next opportunity. A FEBE error means transmission of the opposite of the expected code.

In DS3 C-bit Parity mode, a FEBE error is the transmission of 111, when a frame bit error or a C-bit parity is detected, and transmission of the FEBE error code (written in FEBEC/PT field in Feature1 control register) when none of these errors is detected.

In E3-G.832 mode, REI (FEBE) bit is cleared to 0 when a BIP-8 error is detected in the EM byte and set to 1 when the parity check in the EM byte is correct.

XDgrErr X-Bits Disagreement Error Insertion Control—Causes insertion of X-bits disagreement (i.e., the two X-bits in an M-frame are not equal) at the next opportunity. Valid in only DS3 mode.

YelErr Yellow Alarm Error Insertion Control—Causes insertion of RAI/RDI error at the next opportunity. RAI error means transmission opposite of the expected value.

In DS3 mode, the two X-bits are set to 1 if an RAI should be transmitted and cleared to 0 if RAI is not expected.

In E3-G.751 mode, The A-bit is cleared to 0 if an RAI should be transmitted and set to 1 if a RAI is not expected.

In E3-G.832 mode, RDI bit clears to 0 if an RAI should be transmitted, and set to 1 if an RAI is not expected.

CPErr C-Bit Parity Error Insertion Control—Causes insertion of a CP error at the next opportunity. A CP error means transmission of an incorrect value in the three CP-bits. Valid only in DS3 C-Bit Parity mode.

ParDgrErr Parity Bits Disagreement Error Insertion Control—Causes insertion of P-bits disagreement (i.e., the two P-bits in an M-frame are not equal) at the next opportunity. Valid only in DS3 mode.

ParErr Parity Error Insertion Control—Causes insertion of a parity error at the next opportunity.

In DS3 mode, the error means transmission of an incorrect value in the two P-bits.

In E3-G.832 mode, the error means transmission of a single incorrect bit in BIP-8 field (EM byte).

FrmErrM Frame Error in M-Bit Insertion Control—Causes insertion of a single error (inversion) in one M-bit at the next opportunity. Valid only in DS3 mode.

FrmErrF Frame Error in F/FAS/FA Insertion Control—Causes insertion of a single frame error at the next opportunity.

In DS3 mode, causes inversion of a single F-bit.

In E3-G.751 mode, causes inversion of a single bit in the next FAS field.

In E3-G.832 mode, causes inversion of a single bit in the next FA field.

Error Insertion2 Control Register (CR20i)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LCVIIISub	LCVBPV

Default after reset: 00(h)
Direction: Read/Write
Modification: Dynamic

LCVIIISub LCV Illegal Substitution Insertion Control—Causes insertion of an illegal substitution at the next opportunity. Illegal substitution is defined as an opposite polarity substitution at the next B3ZS/HDB3 substitution. This means that a B0V/B00V pattern is replaced with a 00V/000V pattern or vice versa.

LCVBPV LCV Bipolar Violation Error Insertion Control—Causes insertion of a bipolar violation at the next opportunity. A bipolar violation is defined as a second pulse with the same polarity as the previous one.

3.5 Status Registers

General Status Registers

General Status registers provide for general information about interrupt sources and about the device. Status bits gather in common registers and are not spread, according to the channels.

Source Channel Status Register (GSR00)

This is a general status register that indicates which channels or one-second trigger are the sources for an asserted interrupt on INTR* pin. More than one bit can be high at the same time because there can be multiple sources for interrupts. Only *unmasked* interrupts are reflected in the SrcChnl1–SrcChnl4 bits, but the OneSecltr bit is the status bit of the one-second trigger, even if its interrupt is masked.

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	OneSecltr	SrcChnl4	SrcChnl3	SrcChnl2	SrcChnl1

Value after reset: 00(h)
Direction: Read only

OneSecltr One Second Interrupt—Set to indicate that the one second trigger occurred. Cleared when this register is read.

SrcChnl4 Source Channel 4—Set to indicate that a source or one of the sources for interrupt on INTR* pin is in channel 4. This bit is cleared when all the status bits in channel 4 indicating the reasons for the interrupt are low.

SrcChnl3 Source Channel 3—Set to indicate that a source or one of the sources for interrupt on INTR* pin is in channel 3. This bit is cleared when all the status bits in channel 3 indicating the reasons for the interrupt are low.

SrcChnl2 Source Channel 2 —Set to indicate that a source or one of the sources for interrupt on INTR* pin is in channel 2. This bit is cleared when all the status bits in channel 2 indicating the reasons for the interrupt are low.

SrcChnl1 Source Channel 1—Set to indicate that a source or one of the sources for interrupt on INTR* pin is in channel 1. This bit is cleared when all the status bits in channel 1 indicating the reasons for the interrupt are low.

Part Number/Hardware Version Register (GSR01)

The Part Number/Hardware Version register contains a part number in the lower nibble and a version number in the higher nibble. This register is provided to indicate to the processor what version of CX28344 is present. This enables loading of version-specific software, if needed.

The part numbers for the CX2834i framer are 8348 (Octal), 8346 (Hex) 8344 (Quadruple), 8343 (Triple), 8342 (Dual), or 8341 (Single), thus the value of Part [3:0] is 8, 6, 4, 3, 2, or 1, respectively. The version number is incremented with any change in circuitry, starting from 0.

7	6	5	4	3	2	1	0
Ver[3]	Ver[2]	Ver[1]	Ver[0]	Part[3]	Part[2]	Part[1]	Part[0]

Direction: Read only

Channel Status Registers

The index *i* appearing in the register names represents the channel number, one per channel.

DS3/E3 Maintenance Status Register (SR00i)

The DS3/E3 Maintenance Status register contains the major DS3/E3 maintenance indicators. Alarm detection details are in Section 2.2.5.

7	6	5	4	3	2	1	0
ReFrm	Reserved	Reserved	LOSAIm	IdleDet	YelDet	AISDet	OOFAIm

Value after reset: 81(h)
Direction: Read only
Value after enable: If RefrmStp bit is clear—81(h)
If RefrmStp bit is set—01(h)

ReFrm Reframe in Progress—Set while the framing circuit searches for a valid framing pattern in either DS3 or E3 modes.

LOSAIm Loss-of-Signal Alarm—Indicates that the received signal prior to B3ZS/HDB3 decoding has been lost. This signal is set as soon as the receiver detects the loss-of-signal condition and clears when the receiver detects a legal signal.

IdleDet Idle Code Detect—Set if an idle pattern is found. This bit is low in E3 modes, since there is no defined E3 idle signal.

YelDet Yellow Alarm Detect—Set when a RAI/RDI event is detected in the receiver.

AISDet Alarm Indication Signal Detect—Set if the receiver detects an AIS event.

OOFAIm Out of Frame Alarm—Set when an OOF condition is detected by the receiver. This condition initiates a reframe.

Interrupt Source Status Register (SR01i)

This register identifies which of the other status registers reports the reason for the interrupt assertion. This register is read at the beginning of the interrupt service routine, after the source channel was identified.

NOTE: More than one bit can be high at the same time, due to multiple sources for the interrupt.

7	6	5	4	3	2	1	0
Reserved	Reserved	TxDLFEACItr	RxDLItr	RxFEACItrS	AlarmEndItr	AlarmStrtItr	CtrItr

Value after reset: 00(h)
Direction: Read only
Value after enable: Unaffected (affected indirectly by other registers)

TxDLFEACItr Transmit Data Link/FEAC Interrupt Source—Set if one or more of the interrupt-related active status bits in the Transmit Data Link FEAC Status register are high. Cleared when the bits related to interrupt activation in the Transmit Data Link FEAC Status register or their interrupt masks are low.

RxDLItr Receive Data Link Interrupt Source—Set if one or more of the interrupt-related active status bits in the Receive Data Link Status register are high. Cleared when the bits related to interrupt activation in the Receive Data Link Status register or their interrupt masks are low.

RxFEACItrs Receive FEAC Interrupt Source—Set if one or more of the interrupt related active status bits in the Receive FEAC Status register are high. Cleared when the bits related to interrupt activation in the Receive FEAC Status register or their interrupt masks are low.

AlarmEndItr Alarm End Interrupt Source—Set if one or more of the active status bits in the Alarm End Interrupt Status register are high. Cleared when the bits related to interrupt activation in the Alarm End Interrupt Status register or their interrupt masks are low.

AlarmStrtItr Alarm Start Interrupt Source—Set if one or more of the active status bits in the Alarm Start Interrupt Status register are high. Cleared when the bits related to interrupt activation in the Alarm Start Interrupt Status register or their interrupt masks are low.

CtrItr Counter Interrupt Source—Set if one or more of the active status bits in the Counter Interrupt Status register are high. Cleared when the bits related to interrupt activation in the Counter Interrupt Status register or their interrupt masks are low.

Counter Interrupt Status Register (SR02i)

The Counter Interrupt Status register contains status information about active interrupts needing service from the controller. This register needs to be read by the controller upon receiving a counter interrupt to determine the source of the interrupt. The interrupt indications are active high in the register and are available even if they are not enabled to be visible on the INTR* output pin. Servicing clears this interrupt indication as described in Section 2.3. Counter operation is discussed in Section 3.3.

The bits in this register are cleared when the register is read.

7	6	5	4	3	2	1	0
EXZCtrItr	XdgrCtrItr	LCVCtrItr	FEBECtrItr	PthCtrItr	FerrCtrItr	PdgrCtrItr	ParCtrItr

Value after reset: 00(h)
Direction: Read only
Value after enable: 00(h)

EXZCtrItr Excessive Zeros Counter Interrupt—Set high on EXZ error counter roll over or saturation. The EXZ Counter Interrupt Enable bit, EXZCtrlE bit in Counter Interrupt Control register, determines the status of the counter (rollover or saturation).

XdgrCtrItr X-Bits Disagreement Counter Interrupt—Set high if the X-Disagreement counter has either rolled over or is saturated. The X Disagreement Counter Interrupt Enable bit (XDgrCtrIE) determines the status of the counter (roll-over or saturation). In E3-G.751 and E3-G.832 modes, this bit is low because there are no X-bits.

LCVCtrItr LCV Counter Interrupt—Set high on an LCV error counter rollover or saturation. The LCV Counter Interrupt Enable bit (LCVCtrIE) determines the status of the counter (roll over or saturation).

FEBECtrItr FEBE Event Counter Interrupt—Set high if the FEBE event counter has either rolled over or is saturated. The FEBE Event Counter Interrupt Enable bit determines the status of the counter (roll-over or saturation).

In E3-G.751 and DS3-M13/M23 modes, this bit is low because there is no FEBE/REI event defined.

PthCtrItr Path Parity Error Counter Interrupt—In DS3 mode, set high if the Path Parity Error counter has either rolled over or is saturated. The Path Parity Error Counter Interrupt Enable bit determines the status of the counter (roll-over or saturation).

In DS3-M13/M23, E3-G.751, and E3-G.832 modes, this bit is low because there is no path parity check.

FerrCtrItr Frame Error Counter Interrupt—Set high when the frame error counter has either rolled over or is saturated. The Frame Error Counter Interrupt Enable determines the status of the counter (roll-over or saturation).

PdgrCtrItr P-Bits Disagreement Counter Interrupt—Set high if the P disagreement counter has either rolled over or is saturated. The Disagreement Counter Interrupt Enable bit determines the status of the counter (roll over or saturation). In E3-G.751 and E3-G832 modes, this bit is low because there is no parity disagreement event defined.

ParCtrItr Parity Error Counter Interrupt—Set high if the parity error counter has either rolled over or is saturated. The Parity Error Counter Interrupt Enable bit determines the status of the counter (roll over or saturation).

In E3-G.751 mode, this bit is low because there is no parity/BIP-8 check defined.

Dual-Edge Interrupt Status Registers

The Dual-Edge Interrupt Status registers provide indications for starting and ending points of continuous events, to enable monitoring of the events' length. All bits are set due to an event and cleared when the register is read. In addition, every event bit (start or end) is cleared upon setting the channel's enable bit for that event to prevent an immediate interrupt due to an old event.

Alarm Start Interrupt Status Register (SR03i)

7	6	5	4	3	2	1	0
Reserved	Reserved	SEFStrt	LOSStrt	IdleStrt	YelStrt	AISStrt	OOFStrt

Value after reset: 00(h)
Direction: Read only
Value after enable: 00(h)

SEFStrt Severely Errored Frame Event Start—Set when the receiver detects an SEF condition. This bit is cleared when this register is read. This bit is low in E3 modes since there is no defined SEF alarm in these modes.

LOSStrt Loss of Signal Event Start—Set when the signal received prior to B3ZS/HDB3 decoding is detected as lost by the receiver. This bit is cleared when this register is read.

IdleStrt Idle Event Start—Set when the receiver detects the start of an Idle event in DS3 mode. This bit is cleared when this register is read. This is low in E3 modes, because there is no defined E3 idle signal.

YelStrt Yellow Alarm Start—Set when the receiver detects the start of an RAI/RDI alarm. This bit is cleared when this register is read.

AISStrt AIS Alarm Start—Set when the receiver detects the start of an AIS alarm. This bit is cleared when this register is read.

OOFStrt Out of Frame Event Start—Set when the channel gets into an OOF condition. This bit is cleared when this register is read.

Alarm End Interrupt Status Register (SR04i)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	LOSEnd	IdleEnd	YelEnd	AISEnd	OOFEnd

Value after reset: 00(h)
Direction: Read only
Value after enable: 00(h)

LOSEnd Loss of Signal Event End—Set when the received signal, prior to B3ZS/HDB3 decoding, satisfies the criteria of correct signal after being in a loss-of-signal state. This bit is cleared when this register is read.

IdleEnd Idle Event End—Set when the receiver detects an end of an Idle event in DS3 mode. This bit is cleared when this register is read. This bit is low in E3 modes, because there is no defined E3 idle signal.

YelEnd Yellow Alarm End—Set when the receiver detects the end of an RAI/RDI alarm. This bit is cleared when this register is read.

AISEnd AIS Alarm End—Set when the receiver detects the end of an AIS alarm. This bit is cleared when this register is read.

OOFEnd Out of Frame Event End—Set when the channel goes into in-frame state again after being in an OOF state. This bit is cleared when this register is read.

E3-832 MA Fields Registers

The E3-832 MA Fields registers collect data of specific fields from E3-G.832 type frames. In DS3 and E3-G.751 modes, they are ignored.

E3-G.832 MA Fields Status Register (SR06i)

7	6	5	4	3	2	1	0
Reserved	Reserved	RxMAPT[1]	RxMAPT[2]	RxMAPT[3]	RxMAPD[1]	RxMAPD[2]	RxMATM

Value after reset: Undefined
Direction: Read only
Value after enable: Unaffected

RxMAPT[1:3] Received Payload Type Field—These 3 bits store the pattern of the payload-type field in an MA byte (bits 3–5). No interrupt is issued to report any change in the content of this field. RxMAPT [1] is the first bit received from the line.

RxMAPD[1:2] Received Payload Dependent/Multiframe Indicator Field—These 2 bits store the pattern of the payload-dependent/multiframe indicator in MA byte (bits 6–7). No interrupt is issued to report any change in the content of this field. RxMAPD [1] is the first bit received from the line.

RxMATM Received Timing Marker Bit Field—This bit contains the timing marker bit in an MA byte (bit 8) information. It is valid only when SSM mode is disabled, i.e., when SSMEn bit in Feature4 register is low. No interrupt is issued to report any change in the content of this field.

E3-G.832 SSM Field Status Register (SR07i)

The E3-G.832 SSM Field Status register (SR07i) is valid only when SSM mode is enabled, i.e., when SSMEn bit in Feature Control register4 is high.

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	RxSSM[1]	RxSSM[2]	RxSSM[3]	RxSSM[4]

Value after rest: Undefined
Direction: Read only
Value after enable: Unaffected

RxSSM[1:4] Received SSM Field—These 4 bits store the pattern of SSM field in MA byte (bit 8 collected from 4 frames). The SSM bits are collected from 4 consecutive frames and arranged according to the multiframe indicator field (SSM [1] is the MS bit that is received when MI = 00, etc.).

Transmit Data Link FEAC Status Register (SR08i)

7	6	5	4	3	2	1	0
—	Reserved	TxFEACItr	TxFull	TxMsg	TxUR	TxNE	TxEmpty

Value after reset: 03(h)
Direction: Read only
Value after enable: 03(h)
Bit [7] is undefined

TxFEACItr Transmit FEAC Channel Interrupt—In DS3-C Bit Parity mode, set high indicating that the transmitter is ready for a new byte to be written to the Transmit FEAC Channel Byte register. When FEAC single mode, this happens after every code word transmission start. When in FEAC repetitive mode, this happens after the transmitter has started sending the code word 10 consecutive times for the first time. Cleared when this register is read.

In DS3-M13/M23, E3-G.751, and E3-G.832 modes, this bit should be ignored.

TxFull Transmit Data Link FIFO is Full—Set when the transmit FIFO contains 128 bytes. Cleared when there are less than 128 bytes in the transmit FIFO (i.e., this bit is high and the first byte is read). No interrupt is linked to this bit.

TxMsg Transmit Data Link Message Transmitted Event—Set when the final bit of the closing flag of a message is transmitted. Cleared when this register is read.

TxUR Transmit Data Link Underrun Error—Set when the transmit FIFO buffer is empty and the transmit circuit tries to read another byte from it, i.e., the microprocessor does not meet the requirements and does not fill the FIFO buffer properly. Cleared when this register is read.

TxNE Transmit Data Link Near-Empty Event—Set when TxNEThr bytes or less are left in the FIFO. Cleared when the number of bytes in the FIFO is greater than TxNEThr.

TxEmpty Transmit Data Link FIFO is Empty—Set when the FIFO is empty, i.e., the last byte is read from it. Cleared when set and the first write by the microprocessor (after being empty) is done. No interrupt is linked to this bit.

Receive Data Link Status Register (SR11i)

7	6	5	4	3	2	1	0
Reserved	Reserved	RxGoodBlk	RxOVR	RxMsg	RxNF	RxBlk	StatByte

Value after reset: Bit 0, 5: undefined, bits 1–4, 6, 7—00(h)
Direction: Read only
Value after enable: Bit 0, 5: undefined, bits 1–4, 6, 7—00(h)

RxGoodBlk Received Good Block Indication—Defines the type of status byte. Set for status with length type in it (a good block (a1) or a2 blocks)) Cleared for status with error type in it—bad, Errored Block, b block.

RxOVR Receive Data Link Overrun Error—Set when the receive FIFO is full and another byte was received from the line and should be written into the FIFO (and it is not already set). Cleared if it was set and there are no more unread complete blocks left in the FIFO (this is determined by RxBlk bit in this register).

RxMsg Receive Data Link FIF Contains a Message—Set when another status byte of a correct-end-of-message or an incorrect-end-of-message (including aborted message) is written into the FIFO. Cleared when this register is read.

RxNF Receive Data Link Near-Full Event—Set when the number of bytes in the receive FIFO equals or exceeds the programmable threshold written in RxNFThr register (and it is not already set). Cleared if was set and there are no more unread complete blocks left in the FIFO (this is determined by RxBlk bit in this register).

RxBlk Receive Data Link FIFO Contains Complete Blocks—Set when there is one or more complete data blocks in the receive FIFO. Cleared when the last data byte of the last complete block is read from the FIFO.

StatByte Byte Type Indication—Set when the next byte to be read from the receive FIFO is a status byte. Clear when the next byte to be read is a data byte. When there is no complete block in the FIFO, i.e., when RxBlk bit in this register is clear, this bit is undefined.

Receive Data Link Message Byte (SR12i)

7	6	5	4	3	2	1	0
RxDLMsg[7]	RxDLMsg[6]	RxDLMsg[5]	RxDLMsg[4]	RxDLMsg[3]	RxDLMsg[2]	RxDLMsg[1]	RxDLMsg[0]

Value after reset: Undefined
Direction: Read only
Value after enable: Undefined

RxDLMsg[7:0] Receive Data Link Message Byte—This register is used to read the content of the Receive Data Link FIFO. Issuing a receive FIFO read is done by addressing this register, which results in putting the byte read from the FIFO on the microprocessor data bus. The type of this register's content (status or data) is defined by StatByte bit in the Receive Data Link Status register or as described in the Terminal Data Link Reception paragraph.

The receive order of bits from the line is RxDLMsg[0] bit is received first and RxDLMsg[7] bit is received last from the line. When this register contains data it can be any combination of 1s and 0s. When this register contains a status, it defines the status of the following data block, where the 1 MS bits contain the block's type (correct or partial) for a good block, or undefined for errored block. The other 7 bits are used as length field or error indications.

For RxGoodBlk-set the register contains:

RxDLMsg[7]	RxDLMsg[6]	RxDLMsg[5]	RxDLMsg[4]	RxDLMsg[3]	RxDLMsg[2]	RxDLMsg[1]	RxDLMsg[0]
Type Select	Length[6]	Length[5]	Length[4]	Length[3]	Length[2]	Length[1]	Length[0]

RxDLMsg[7]: set for complete, cleared for partial.

For RxGoodBlk cleared, the register contains the following block, illustrating the content of the status register in incorrect-end-of-message state and details the different error indications that can be set.

NOTE: The length of the following block is always considered as 0, and only one indication can be set at a time.

RxDLMsg[7]	RxDLMsg[6]	RxDLMsg[5]	RxDLMsg[4]	RxDLMsg[3]	RxDLMsg[2]	RxDLMsg[1]	RxDLMsg[0]
Undefined	Undefined	Undefined	Undefined	Abort	OVR	AlignErr	BadFCS

The error indications are:

- Abort—When an abort sequence is detected, the message is terminated and the bit set.
- OVR—When an overrun error happens (FIFO buffer is full and a new byte was received), the message is terminated and the bit set.
- AlignErr—When the number of bits in the message is indivisible by 8 (alignment error), the message is terminated and the bit set.
- BadFCS—When there is a mismatch between the calculated and the received FCS, the message is terminated and the bit set.

Only one error type is set according to this priority: OVR, Abort, AlignErr, BadFCS (highest to lowest).

Receive FEAC Byte (SR15i)

7	6	5	4	3	2	1	0
RxFEAC[7]	RxFEAC[6]	RxFEAC[5]	RxFEAC[4]	RxFEAC[3]	RxFEAC[2]	RxFEAC[1]	RxFEAC[0]

Value after reset: Undefined
Direction: Read only
Value after enable: Unaffected

RxFEAC[7:0] Receive FEAC Channel Message Byte—If the incoming format is DS3-C Bit Parity, this register contains the received byte from the bit-oriented Receive FEAC channel. The Receive FEAC channel is only defined in DS3-C Bit Parity format. Receive FEAC message reception is described in Section 2.2.8. RxFEAC[0] is the bit received first and RxFEAC[7] is the last bit received from the line. This byte is meaningless in DS3-M13/M23 and both E3 modes and should be ignored.

Receive FEAC Stack Byte (SR16i)

7	6	5	4	3	2	1	0
RxFEACS[5]	RxFEACS[4]	RxFEACS[3]	RxFEACS[2]	RxFEACS[1]	RxFEACS[0]	RxFEACSV	RxFEACSM

Value after reset: Bits 0–1: 0(h), Bits 2–7: undefined
Direction: Read only
Value after enable: Bits 0–1: 0(h), Bits 2–7: undefined

RxFEACS[5:0] Receive FEAC Channel Stack Message Byte—If the incoming format is DS3-C Bit Parity, this register contains the FEAC stack received byte from the bit-oriented Receive FEAC channel. Receive FEAC message reception is described in Far-End Alarm and Control Channel Reception in the Receiver Operation section of the Functional Description chapter. RxFEACS[D] is the first bit received and RxFEACS[5] is the last bit received from the line. This byte is meaningless in DS3-M13/M23 and both E3 modes and should be ignored.

RxFEACSV Receive FEAC Channel Stack Message Byte is Valid— Set on if RxFEACS [5:0] hold a valid FEAC code word. For a detailed description, refer to Far-End Alarm and Control Channel Reception sections.

RxFEACSM Receive FEAC Channel Stack Has More Data—Set on if the current value of RxFEACS[5:0] is not the last valid code word in the FEAC stack. For a detailed description, refer to Far-End Alarm and Control Channel Reception sections.

Receive FEAC Status Register (SR17i)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	RxFEACSNE	RxFEACIdle	RxFEACItr

Value after reset: 00 (h)
Direction: Read only
Value after enable: 00 (h)

RxFEACSNE Receive FEAC Stack Is Not Empty—Set due to detection of the FEAC stack being not empty (i.e., Receive FEAC Stack byte is holding valid data).

RxFEACIdle Received FEAC Channel Is Idle—In DS3-C Bit Parity mode, set when the FEAC receiver detects the first appearance of an Idle code, after reception of legal code words. This bit is cleared when this register is read. In DS3-M13/M23 and both E3 modes, this bit should be ignored.

RxFEACItr Receive FEAC Channel Interrupt—In DS3-C Bit Parity mode, when working in FEAC single mode, set high when an FEAC message byte has been received and placed in the Receive FEAC Channel Byte register. When working in FEAC repetitive mode, set high when the receiver detects an FEAC message byte (see Far-End Alarm and Control Channel Reception paragraph). Reading the Receive FEAC Channel Byte register clears this interrupt. In DS3-M13/M23, E3-G.751 and E3-G.832 modes, this bit should be ignored.

Receive AIC Byte (SR18i)

7	6	5	4	3	2	1	0
RxAIC[7]	RxAIC[6]	RxAIC[5]	RxAIC[4]	RxAIC[3]	RxAIC[2]	RxAIC[1]	RxAIC[0]

Value after reset: Undefined
Direction: Read only
Value after enable: Unaffected

RxAIC[7:0] Receive AIC Channel Message Byte—If the incoming format is DS3, C-Bit Parity, this register contains 8 AIC (Cb11) bits from 8 consecutive frames. RxAIC[0] is the first bit received and RxAIC[7] is the last bit received from the line. This byte is meaningless in DS3-M13/M23 and both E3 modes and should be ignored.

3.6 Counters

There are eight error counters for DS3/E3 errors. All are 16-bit counters except the LCV counter, which is 24 bits long. If the interrupt for a particular counter is not enabled, the counter saturates at 65,535 (LCV = 16,777,215). When more than 65,535 (LCV = 16,777,215) counts of that error are received, the saturation indication appears in the Counter Interrupt Status register. The saturation indication is cleared when the Counter Interrupt Status register is read. The counter is cleared when the counter is read.

If the interrupt for a particular counter is enabled in the Interrupt Control register, the counter does not saturate but rolls over and continue counting from zero. An interrupt is generated on the INTR* pin and appears in the Counter Interrupt Status register when the counter rolls over to a count of zero. The interrupt is cleared when the Counter Interrupt Status register is read. The counter is cleared when the counter is read. The counters count according to indications set by the receiver circuit. For details, see Section 2.2.5.

All counters are cleared when read by the microprocessor. The interrupt indication for a particular counter is cleared when the Counter Interrupt Status register is read. Software should read the low byte first and then the high byte to prevent any missed counts. All counters are designed so that errors occurring during reads by the microprocessor are not be missed or double-counted.

The OneSec timer is a special counter that does not belong to the family of error and event counters. The microprocessor does not read the general counter because its only function is to count one-second intervals and then roll over and set a status/interrupt. The effect of this counter is fully described in Section 2.2.6.

NOTE:All counters must be in the saturating mode for this mode to function properly.

DS3/E3 Parity Error Counter (Ctr00i)

7	6	5	4	3	2	1	0
ParCtr[7]	ParCtr[6]	ParCtr[5]	ParCtr[4]	ParCtr[3]	ParCtr[2]	ParCtr[1]	ParCtr[0]

15	14	13	12	11	10	9	8
ParCtr[15]	ParCtr[14]	ParCtr[13]	ParCtr[12]	ParCtr[11]	ParCtr[10]	ParCtr[9]	ParCtr[8]

Value after reset: 00(h)
Direction: Read/Write
Value after enable: 0000(h)

ParCtr[15:0] Parity Error Counter—In DS3 mode, increments for each M-frame where the calculated parity of the received data bits of the previous M-frame does not match the received parity bits. If the two parity bits are different, this counter increments. In E3-G.832 mode, it increments for each frame where the calculated BIP-8 pattern of the received data bits of the previous frame do not match the received EM byte. The counter increments are per byte, not bits. In E3-G.751 mode, this counter is not used.

DS3 Parity Disagreement Counter (Ctr01i)

7	6	5	4	3	2	1	0
ParDgrCtr[7]	ParDgrCtr[6]	ParDgrCtr[5]	ParDgrCtr[4]	ParDgrCtr[3]	ParDgrCtr[2]	ParDgrCtr[1]	ParDgrCtr[0]

15	14	13	12	11	10	9	8
ParDgrCtr[15]	ParDgrCtr[14]	ParDgrCtr[13]	ParDgrCtr[12]	ParDgrCtr[11]	ParDgrCtr[10]	ParDgrCtr[9]	ParDgrCtr[8]

Value after reset: 0000(h)
Direction: Read/Write
Value after enable: 0000(h)

ParDgrCtr [15:0] Parity-Bit Disagreement Counter—If the two P-bits in an M-frame are in disagreement (e.g., due to line errors), this counter is incremented.

DS3 X Disagreement Counter (Ctr02i)

7	6	5	4	3	2	1	0
XDgrCtr[7]	XDgrCtr[6]	XDgrCtr[5]	XDgrCtr[4]	XDgrCtr[3]	XDgrCtr[2]	XDgrCtr[1]	XDgrCtr[0]

15	14	13	12	11	10	9	8
XDgrCtr[15]	XDgrCtr[14]	XDgrCtr[13]	XDgrCtr[12]	XDgrCtr[11]	XDgrCtr[10]	XDgrCtr[9]	XDgrCtr[8]

Value after reset: 0000(h)
Direction: Read/Write
Value after enable: 0000(h)

XDgrCtr[15:0] X-Bit Disagreement Counter—If the two X-bits in an M-frame are in disagreement (e.g., due to line errors), this counter is incremented.

DS3/E3 Frame Error Counter (Ctr03i)

7	6	5	4	3	2	1	0
FerrCtr[7]	FerrCtr[6]	FerrCtr[5]	FerrCtr[4]	FerrCtr[3]	FerrCtr[2]	FerrCtr[1]	FerrCtr[0]

15	14	13	12	11	10	9	8
FerrCtr[15]	FerrCtr[14]	FerrCtr[13]	FerrCtr[12]	FerrCtr[11]	FerrCtr[10]	FerrCtr[9]	FerrCtr[8]

Value after reset: 0000(h)
Direction: Read/Write
Value after enable: 0000(h)

FerrCtr[15:0] Frame Error Counter—The counter increments for each error in the M- or F-bit framing pattern in DS3 mode and for each error in the FAS/FA pattern in E3 mode. Errors are still counted during an OOF condition (OOFAlm = 1).

DS3 Path Parity Error Counter (Ctr04i)

7	6	5	4	3	2	1	0
DS3PthCtr[7]	DS3PthCtr[6]	DS3PthCtr[5]	DS3PthCtr[4]	DS3PthCtr[3]	DS3PthCtr[2]	DS3PthCtr[1]	DS3PthCtr[0]

15	14	13	12	11	10	9	8
DS3PthCtr[15]	DS3PthCtr[14]	DS3PthCtr[13]	DS3PthCtr[12]	DS3PthCtr[11]	DS3PthCtr[10]	DS3PthCtr[9]	DS3PthCt[8]

Value after reset: 0000(h)
Direction: Read/Write
Value after enable: 0000(h)

DS3PthCtr[15:0] DS3 Path Parity Error Counter—Increments the count for each M-frame in which the calculated parity of the received data bits of the previous M-frame do not match a majority vote of the three received CP-bits (C-bits in subframe 3).

DS3/E3 FEBE Event Counter (Ctr05i)

7	6	5	4	3	2	1	0
FEBE[7]	FEBE[6]	FEBE[5]	FEBE[4]	FEBE[3]	FEBE[2]	FEBE[1]	FEBE[0]

15	14	13	12	11	10	9	8
FEBE[15]	FEBE[14]	FEBE[13]	FEBE[12]	FEBE[11]	FEBE[10]	FEBE[9]	FEBE[8]

Value after reset: 0000(h)
Direction: Read/Write
Value after enable: 0000(h)

FEBE[15:0] FEBE Event Counter—In DS3-C Bit Parity mode, increments for each M-frame where any C-bit in subframe 4 is 0. In E3-G.832 mode, increments for each frame where REI bit in MA byte is set. In DS3-M13/M23 and E3-G.751, this counter is not used.

DS3/E3 Excessive Zeros Counter (Ctr06i)

7	6	5	4	3	2	1	0
EXZCtr[7]	EXZCtr[6]	EXZCtr[5]	EXZCtr[4]	EXZCtr[3]	EXZCtr[2]	EXZCtr[1]	EXZCtr[0]

15	14	13	12	11	10	9	8
EXZCtr[15]	EXZCtr[14]	EXZCtr[13]	EXZCtr[12]	EXZCtr[11]	EXZCtr[10]	EXZCtr[9]	EXZCtr[8]

Value after reset: 0000(h)
Direction: Read/Write
Value after enable: 0000(h)

EXZCtr[15:0] Excessive Zeros Counter—This counter is enabled only when B3ZS/HDB3 encoding or decoding is used. This counter increments upon excessive 0s-event detection by the receiver circuit.

DS3/E3 LCV Counter (Ctr07i)

7	6	5	4	3	2	1	0
LCVCtr[7]	LCVCtr[6]	LCVCtr[5]	LCVCtr[4]	LCVCtr[3]	LCVCtr[2]	LCVCtr[1]	LCVCtr[0]

15	14	13	12	11	10	9	8
LCVCtr[15]	LCVCtr[14]	LCVCtr[13]	LCVCtr[12]	LCVCtr[11]	LCVCtr[10]	LCVCtr[9]	LCVCtr[8]

23	22	21	20	19	18	17	16
LCVCtr[23]	LCVCtr[22]	LCVCtr[21]	LCVCtr[20]	LCVCtr[19]	LCVCtr[18]	LCVCtr[17]	LCVCtr[16]

Value after reset: 000000(h)
Direction: Read/Write
Value after enable: 000000(h)

LCVCtr[23:0] LCV Counter—This counter is incremented due to LCV events detected by the receiver circuit.

3.7 General Counters

One-Second Timer (GCtr00)

7	6	5	4	3	2	1	0
OneSeCtr[7]	OneSeCtr[6]	OneSeCtr[5]	OneSeCtr[4]	OneSCtr[3]	OneSeCtr[2]	OneCtr[1]	OneSeCtr[0]

15	14	13	12	11	10	9	8
OneSecCtr[15]	OneSecCtr[14]	OneSecCtr[13]	OneSecCtr[12]	OneSecCtr[11]	OneSecCtr[10]	OneSecCtr[9]	OneSecCtr[8]

23	22	21	20	19	18	17	16
OneSecCtr[23]	OneSecCtr[22]	OneSecCtr[21]	OneSecCtr[20]	OneSecCtr[19]	OneSecCtr[18]	OneSecCtr[17]	OneSecCtr[16]

31	30	29	28	27	26	25	24
0	0	0	0	0	0	OneSecCtr[25]	OneSecCtr[24]

Value after reset: 02aa9e00(h)
Direction: Read/Write
Value after enable: The programmed value (02aa9e00(h) if nothing is programmed)
Modification of programmed value: OneSecMod—static

OneSecCtr[25:0] One-Second Counter—Decrements with every clock pulse of Channel 1's transmit clock (TXCKI) and rolls over when it reaches zero. The default value 02aa9e00(h) is equivalent to one second at the DS3 clock rate. When the counter rolls over, the value programmed into this counter is automatically reloaded and the count-down continues. Reading this address provides the current value of the counter itself and not the programmed value written to this address. When programming this register, the One-Second Latching mode is disabled, and the OneSecMod bit is cleared in Register GCR01, the General2 Control register.

If the system is set to internal one-second triggering when the counter rolls over, the OneSecItr bit in Register GSR00, the Source Channel Status register, is set. If, at the same time, the 1SecTimIE bit is also set in GCR01, the General2 Control register, an interrupt on the INTR* pin occurs.

For additional information, see Sections 2.2.6 and 2.3.3.

4.0 Electrical and Mechanical Specifications

4.1 Environmental Conditions

4.1.1 Power Requirements and Temperature Range

Stresses above those listed as absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-1. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Units
V_{DD}	Core Power Supply (measured to GND)	–0.5	3.3	V
V_{DDO}	I/O Power Supply	–0.5	4.6	V
Ts	Storage Temperature	–40	125	°C
T j	Junction Temperature	—	125	°C
Tvsol (ETQFP 144-pin)	Vapor Phase Soldering Temperature (1 minute)	—	220	°C
θ_{jA} (ETQFP 144-pin) *(1)*	Thermal Resistance, Still Air	—	43	°C/W
θ_{jA} (ETQFP 144-pin) *(1)*	Thermal Resistance, Still Air, Socketed	—	49	°C/W
V_i	Constant Voltage on Any Signal	–1.0	V_{DD} + 0.5	V

FOOTNOTE:
(1) Zero linear feet/minute airflow.

4.1.1.1 Recommended Operating Conditions

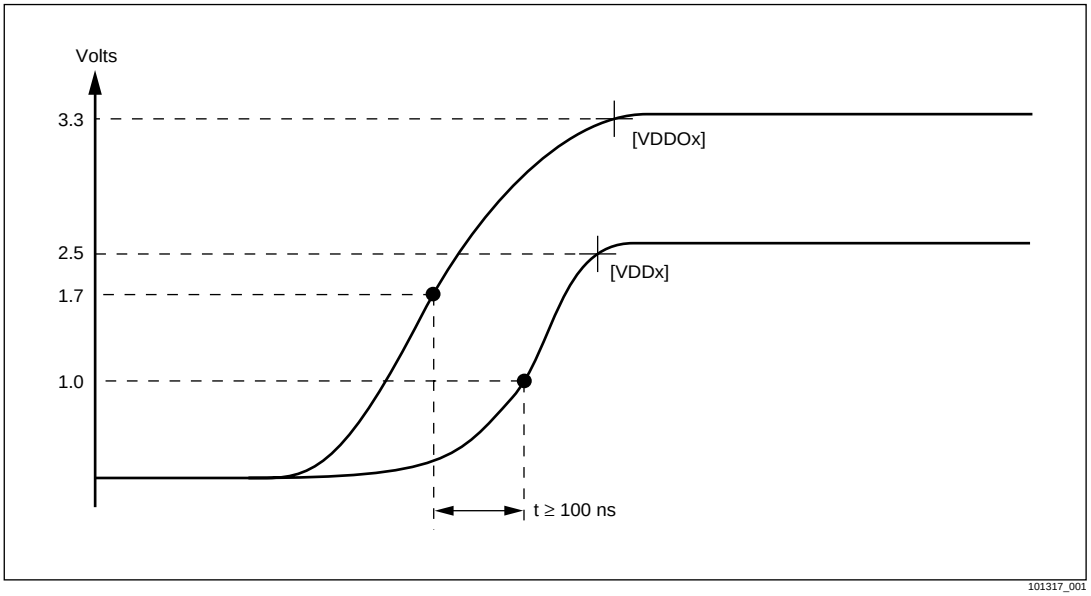
Table 4-2. Recommended Operating Conditions

Symbol	Parameter	Minimum	Maximum	Units
VDD	Core Power Supply	2.375	2.625	V
VDDO	I/O Power Supply	3.135	3.465	V
Tamb	Ambient Operating Temperature EXF Suffix	–40	85	°C
Vih	Input High Voltage	2.0	VDDO + 0.25	V
Vil	Input Low Voltage	–0.25	0.8	V

4.1.1.2 Power Ramp Sequence of VDDx and VDDOx

There is a recommended power ramp sequence for VDDOx (3.3 V I/O) and VDDx (2.5 V core) supplies. A minimum time of ≥100 ns is required from the VDDOx reaching 1.7 V (or greater) until the VDDx supply is allowed to exceed 1.0 V. See Figure 4-1 below for more details.

Figure 4-1. Power Ramp Sequence of VDDx and VDDOx



4.1.2 Electrical Characteristics

4.1.2.1 DC Characteristics

All inputs and bidirectional signals have input thresholds compatible with TTL drive levels. All outputs are CMOS drive levels and can be used with CMOS or TTL logic.

Table 4-3. DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
I_{dd}	8-channel core supply current	—	—	336	mA
I_{dd}	8-channel I/O supply current	—	—	144	mA
I_{dd}	6-channel core supply current	—	—	291	mA
I_{dd}	6-channel I/O supply current	—	—	126	mA
I_{dd}	4-channel core supply current	—	—	180	mA
I_{dd}	4-channel I/O supply current	—	—	85	mA
I_{dd}	3-channel core supply current	—	—	145	mA
I_{dd}	3-channel I/O supply current	—	—	65	mA

Table 4-3. DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
I_{dd}	2-channel core supply current	—	—	104	mA
I_{dd}	2-channel I/O supply current	—	—	49	mA
V_{oh}	Output High Voltage (I_{oh} = –400 µA)	2.4	—	—	V
V_{ol}	Output Low Voltage (I_{ol} = 4 mA)	—	—	0.4	V
I_{il}/I_{ih}	Dig. input leakage current	–200	—	200	nA
I_{il}	Dig. input leakage current 75 kΩ pulldown	–2,000	—	2,000	nA
I_{ih}	Dig. input leakage current 75 kΩ pulldown	–10	—	80	µA
I_{il}	Dig. input leakage current 75 kΩ pullup	–100	—	100	µA
I_{ih}	Dig. input leakage current 75 kΩ pullup	–1,000	—	1,000	nA
I_{il}	Dig. input leakage current 75 kΩ pulldown—I/O	–2,000	—	2,000	nA
I_{ih}	Dig. input leakage current 75 kΩ pulldown—I/O	–10	—	80	µA
Ioz	Dig.output leakage current	–1,000	—	1,000	nA
Ioz	Dig. output leakage current	–1,000	—	1,000	nA

4.2 AC Characteristics

4.2.1 Input Clock Timing

The following illustrates the various clocks applied to the CX28342/CX28343/ CX28344/CX28346/CX28348 device and associated parameters.

Figure 4-2. Input Clock Timing

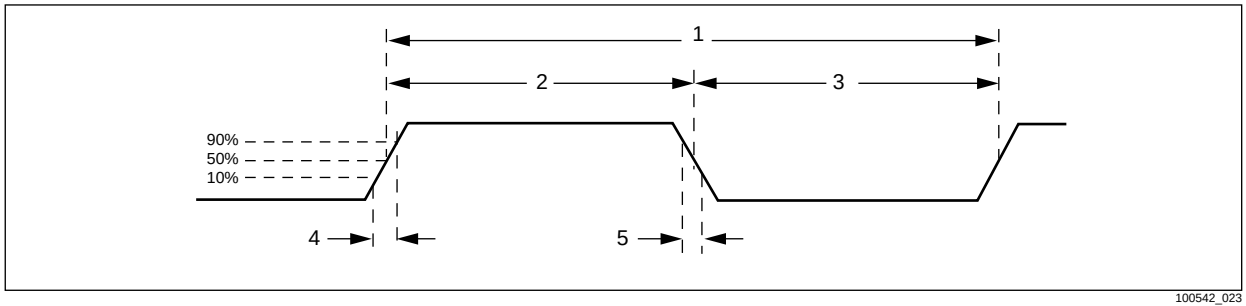


Table 4-4. Input Clock Timing

Symbol	Parameter	Minimum	Maximum	Units
1	TXCKI Frequency *(1)*	E3	DS3	MHz
1	LINECK Frequency *(1)*	E3	DS3	MHz
1	RXCKI Frequency *(1)*	E3	DS3	MHz
2, 3	Clock Width High/Low DS3	8.8	13.2	ns
2, 3	Clock Width High/Low E3	11.6	17.4	ns
4	Clock Rise Time	—	3	ns
5	Clock Fall Time	—	3	ns

GENERAL NOTE: There is a limit of 40%–60% duty cycle to all clocks.

FOOTNOTE:
(1) E3 = 34.368 MHz ±20%; DS3 = 44.736 MHz ±20%

4.2.2 Signal Timing and Clock Output Timings

The clock and data relationships for all output and input signals are illustrated in this section. All signals and clocks listed are for one framer. The timings listed are identical for all framers on-chip. Propagation delays for the output signals are listed below. The output signal timings are relative to the listed edge of the clock. Output and input signals relative to either the rising or the falling edge of the clock (programmable) are listed with the edge as rising/falling. Clock outputs derived from clock inputs are listed with the edge as both. In both cases, this means that the delay number given applies for either edge. Input signals should have setup and hold times with respect to the listed edge of the given input clock.

Figure 4-3. Line Side Receiver Input Data Setup/Hold Timing (1 = tsu [setup time]; 2 = thld [hold time])

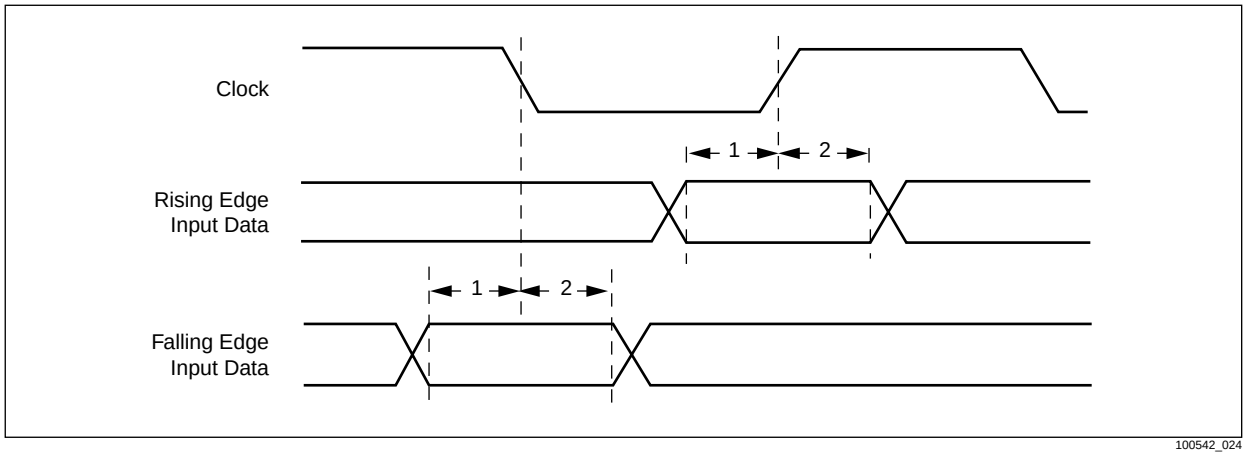


Figure 4-4. Line Side Transmitter Output Data Timing (1 = tpd [propogation delay])

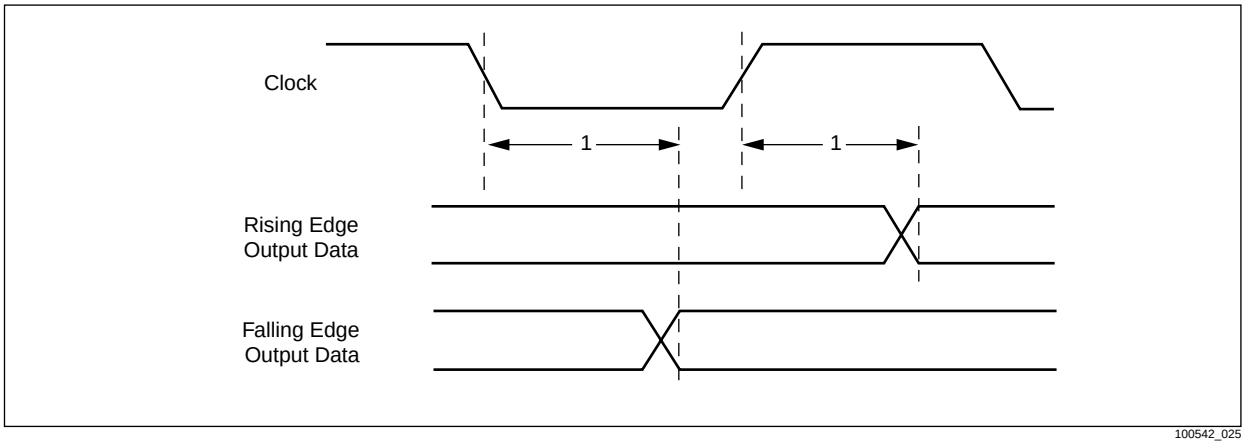


Figure 4-5. System-Side Transmitter Interface Timing

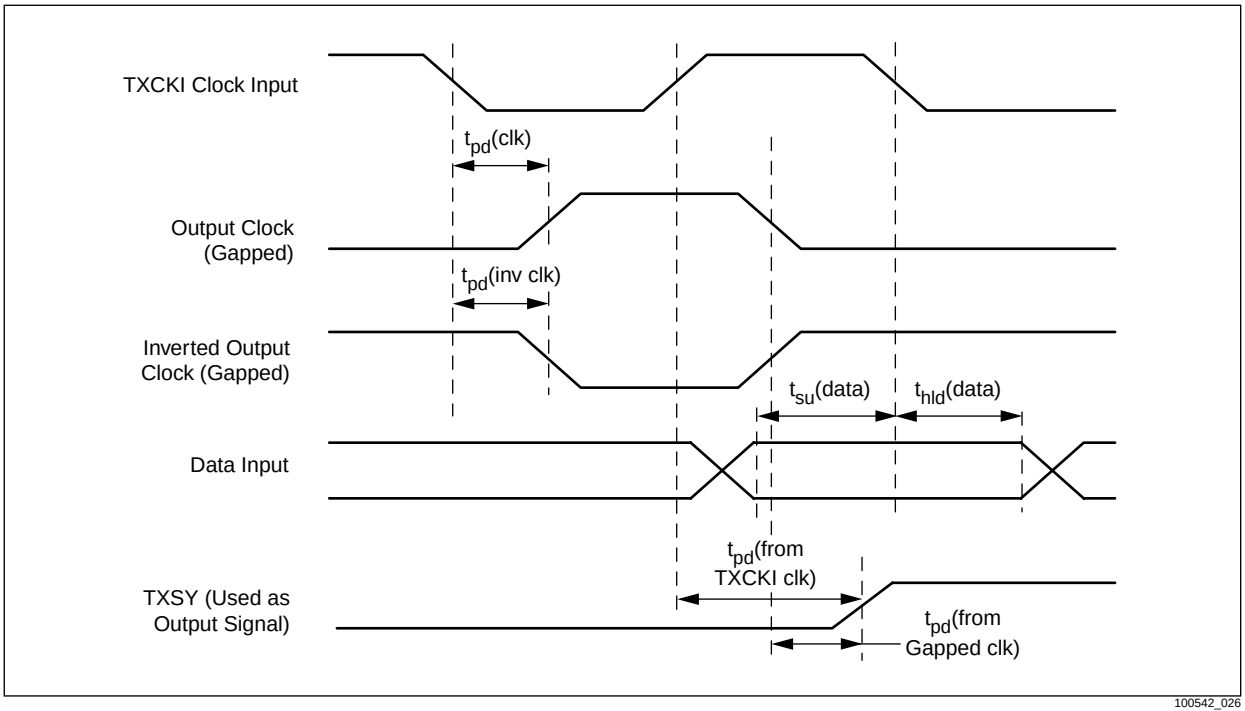


Figure 4-6. System-Side Receiver Interface Timing

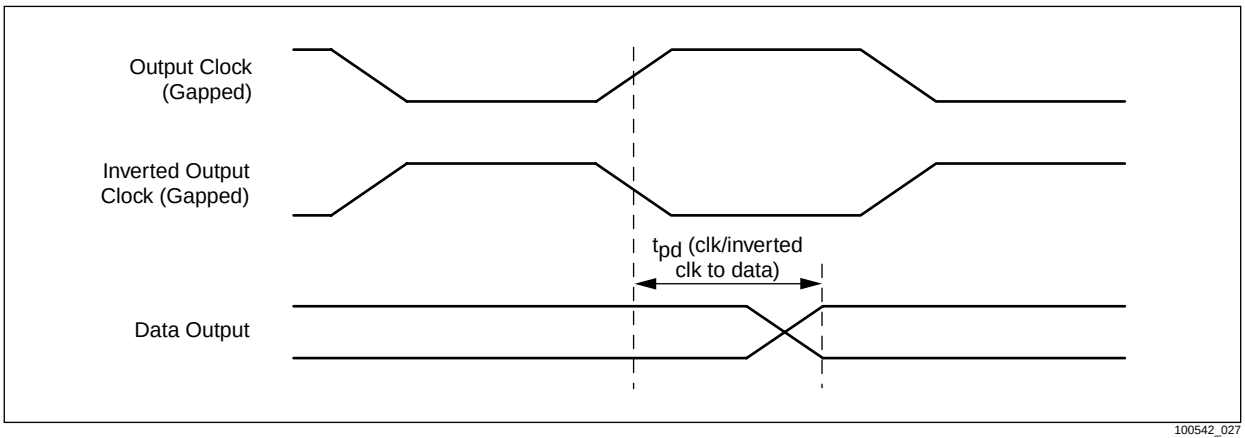


Table 4-5. Output Signal Timing

According To	Output Signal	Clock	tpd Min	tpd Max	Edge	Units
Figure 4-4	TXPOS/TXNRZ	TCLKO	–3	7	Rising/Falling	ns
Figure 4-4	TXNEG	TCLKO	–3	6	Rising/Falling	ns
Figure 4-4	TXSY (when set as an output signal)	Relative timing to TXCKI input clock	1	8	Rising	ns
Figure 4-5	TXSY (when set as an output signal)	Relative timing to TXGAPCK (both inverted and not inverted)	–3	4	Rising/Falling	ns
Figure 4-5	TXGAPCK (when inverted and not inverted)	TXCKI	1	9	Both	ns
Figure 4-5	TEXTCK (when inverted and not inverted)	TXCKI	1	9	Both	ns
Figure 4-6	RXMSY	RXGAPCK	–3	4	Rising/Falling	ns
Figure 4-6	RXDAT	REXTCK	–3	4	Rising/Falling	ns
Figure 4-6	RXDAT	RXGAPCK	–3	4	Rising/Falling	ns

Table 4-6. Input Signal Timing

According To	Input Signal	Clock	tsu Min	thld Min	Edge	Units
Figure 4-5	TXDATI	TXCKI	2	4	Falling	ns
Figure 4-5	TXSY(when set as an input signal)	TXCKI	2	4	Falling	ns
Figure 4-5	TEXT	TXCKI	2	4	Falling	ns
Figure 4-3	RXPOS/RXNRZ	LINECK	4	5	Rising/Falling	ns
Figure 4-3	RXNEG/LCVI	LINECK	4	5	Rising/Falling	ns

4.3 Microprocessor Interface Timing

The interface supports the Intel 8051, 8151, and 8251 and the Motorola 68000, 68020, and 68030 microprocessors. The DTACK* signal is valid only for Motorola. Programmed wait states may have to be used by Intel 8151 and 8251 microprocessors running at 16 MHz and above.

The timing diagrams are provided as Tables 4-7 through 4-10.

NOTE: Test environment—80 pF loading on every output.

Figure 4-7. Intel Asynchronous Read Cycle (MOTO* = 1)

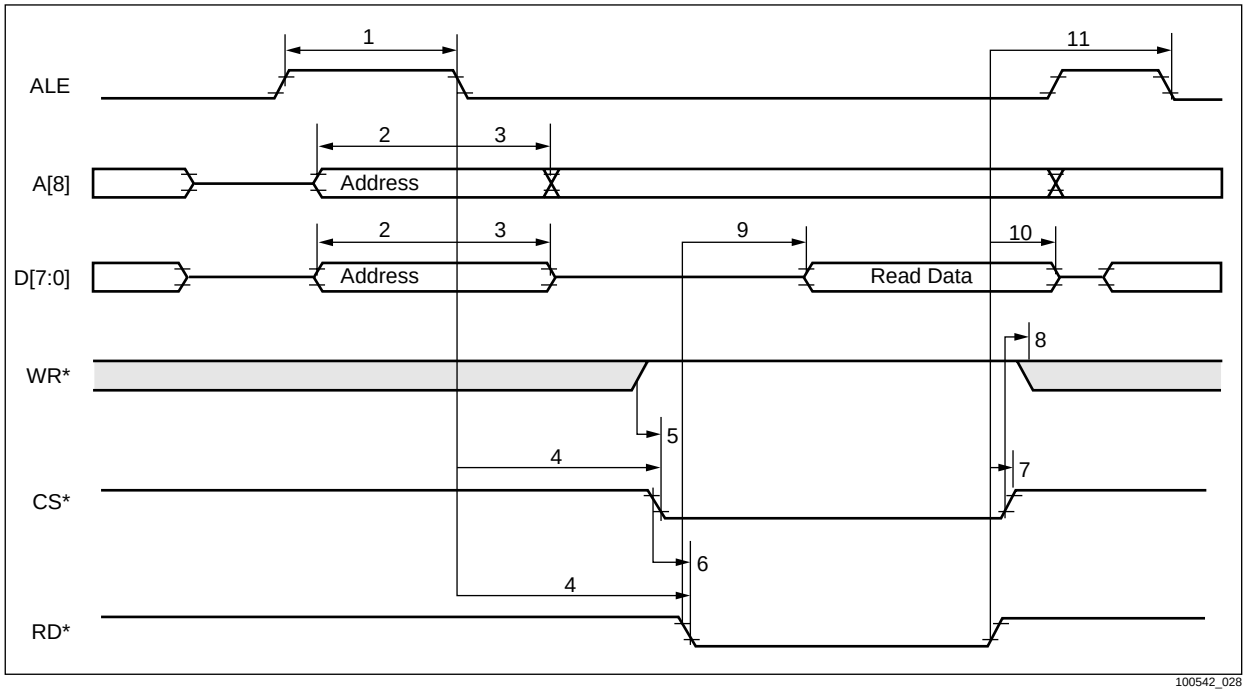


Table 4-7. Intel Asynchronous Read Cycle (MOTO* = 1)

Symbol	Parameter	Minimum	Maximum	Units
1	ALE high pulse width	15	—	ns
2	A[8], AD[7:0] Address setup to ALE low	5	—	ns
3	A[8], AD[7:0] Address hold after ALE low	5	—	ns
4	ALE low to RD* and CS* both low	More than A[8], AD[7:0] hold time	—	ns
5	WR* high to CS* low	3	—	ns
6	CS* low to RD* low	3	—	ns
7	RD* high to CS* high	3	—	ns
8	CS* high to WR* low	3	—	ns
9	RD* low to AD[7:0] valid	—	3 x clk + 20*(1)*	ns
10	RD* high to AD[7:0] invalid or three-state	0	10	ns
11	RD* high to next ALE low	15	—	ns

FOOTNOTE:

(1) Clk is the cycle (ns) of the slowest clock (DS3—22 ns and E3—29 ns).

(2) The transition must be completed, i.e., RD* must rise after AD[7:0] is valid.

(3) CS* can be kept low if only CX28342/CX28343/CX28344/CX28346/CX28348 is in the system, but negative edge of RD* or positive edge of WR* starts a read/write cycle.

Figure 4-8. Intel Asynchronous Write Cycle (MOTO* = 1)

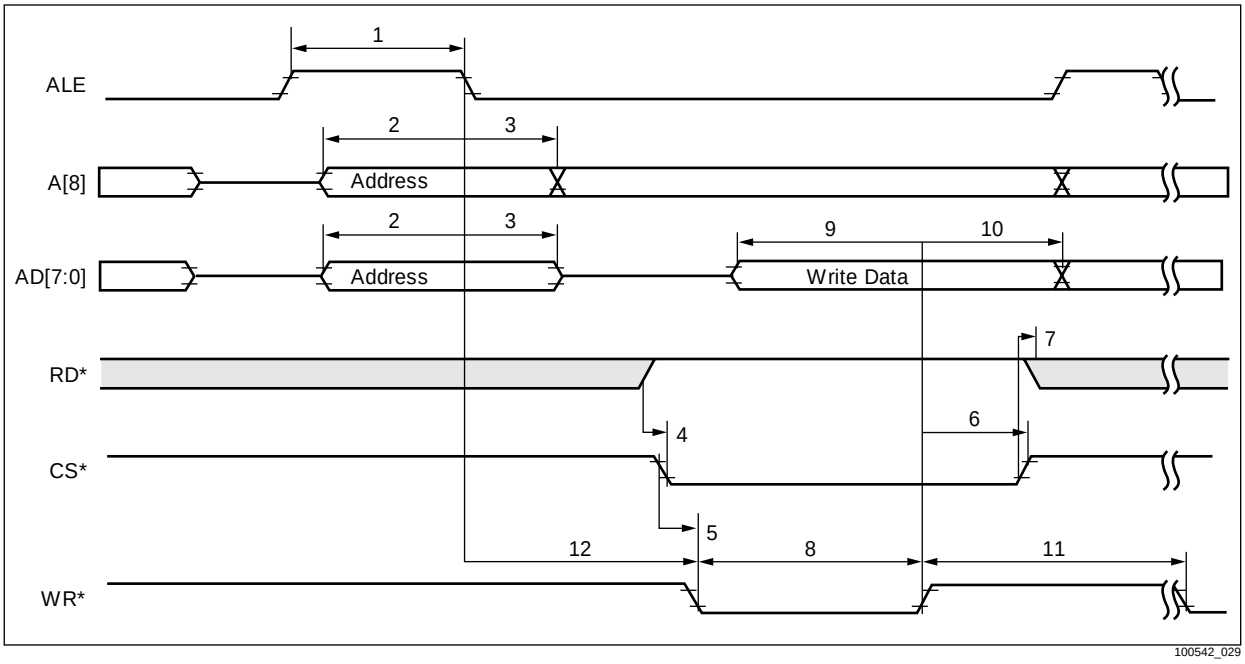


Table 4-8. Intel Asynchronous Write Cycle (MOTO* = 1)

Symbol	Parameter	Minimum	Maximum	Units
1	ALE high pulse width	15	—	ns
2	A[8], AD[7:0] Address setup to ALE low	5	—	ns
3	A[8], AD[7:0] Address hold after ALE low	5	—	ns
4	RD* high to CS* low	3	—	ns
5	CS* low to WR* low	3	—	ns
6	WR* high to CS* high	3	—	ns
7	CS* high to RD* low	3	—	ns
8	WR* pulse width low	15	—	ns
9	AD[7:0] input data setup to WR* high	5	—	ns
10	AD[7:0] input data hold after WR* high	5	—	ns
11	WR* high to next WR* low or RD* low	3 x clk + 15 (1)	—	ns
12	ALE low to WR* low	5	—	ns

FOOTNOTE:

(1) Clk is the cycle (ns) of the slowest clock (DS3—22 ns, E3–29 ns, HSSI—19 ns).

(2) CS* can be kept low if only CX28342/CX28343/CX28344/CX28346/CX28348 device is in the system, otherwise any negative edge of RD* or positive edge of WR* starts a read/write cycle.

Figure 4-9. Motorola Asynchronous Read Cycle (MOTO* = 0)

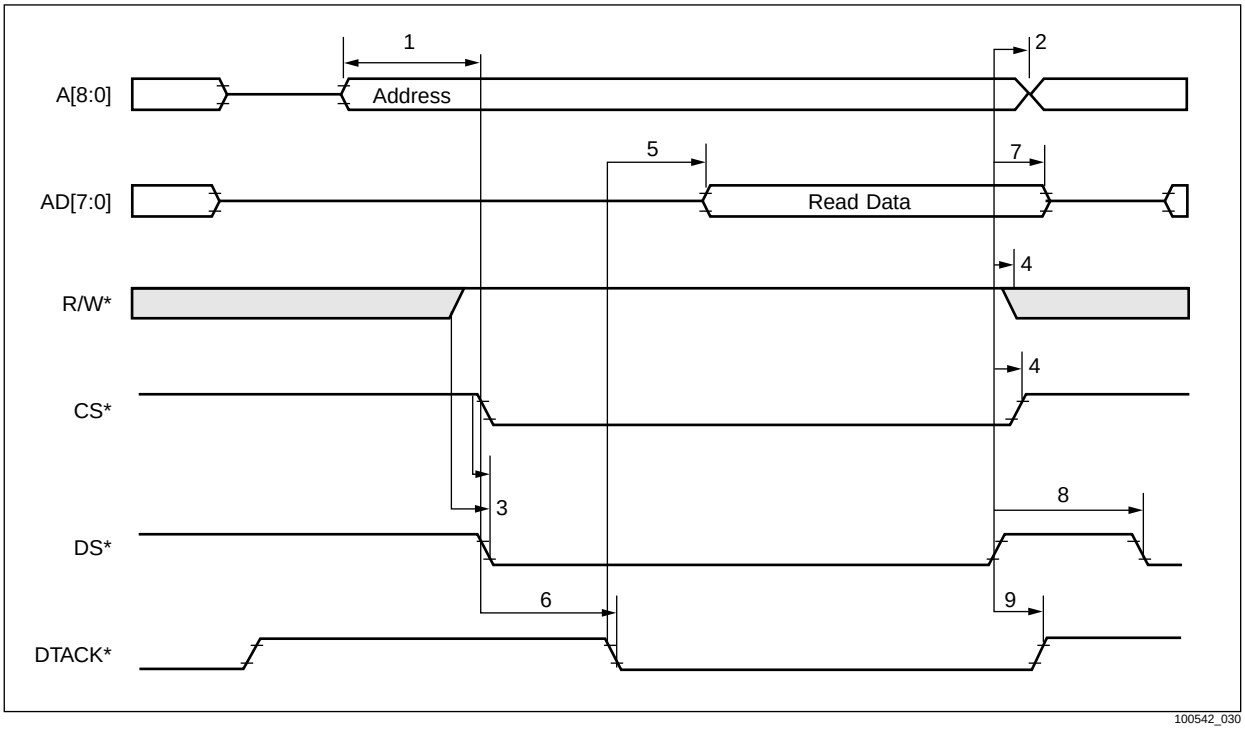


Table 4-9. Motorola Asynchronous Read Cycle (MOTO* = 0)

Symbol	Parameter	Minimum	Maximum	Units
1	A[8:0] Address setup to DS* low	4	—	ns
2	A[8:0] Address hold after DS* high	3	—	ns
3	R/W* high & CS* low to DS* low	3	—	ns
4	DS* high to CS* high and R/W* invalid	3	—	—
5	DTACK* low to AD[7:0] valid	—	13	ns
6	DS* low to DTACK* low	—	3 x clk + 15*(1)*	ns
7	DS* high to AD[7:0] invalid or three-state	—	13	ns
8	DS* high to next DS* low	15	—	ns
9	DS* high to DTACK* highZ	—	19	ns

FOOTNOTE:
(1) Clk is the cycle (ns) of the slowest clock (DS3—22 ns, E3—29 ns).
(2) The transition must be completed, i.e., DS* must rise after DTACK* low.

Figure 4-10. Motorola Asynchronous Write Cycle (MOTO* = 0)

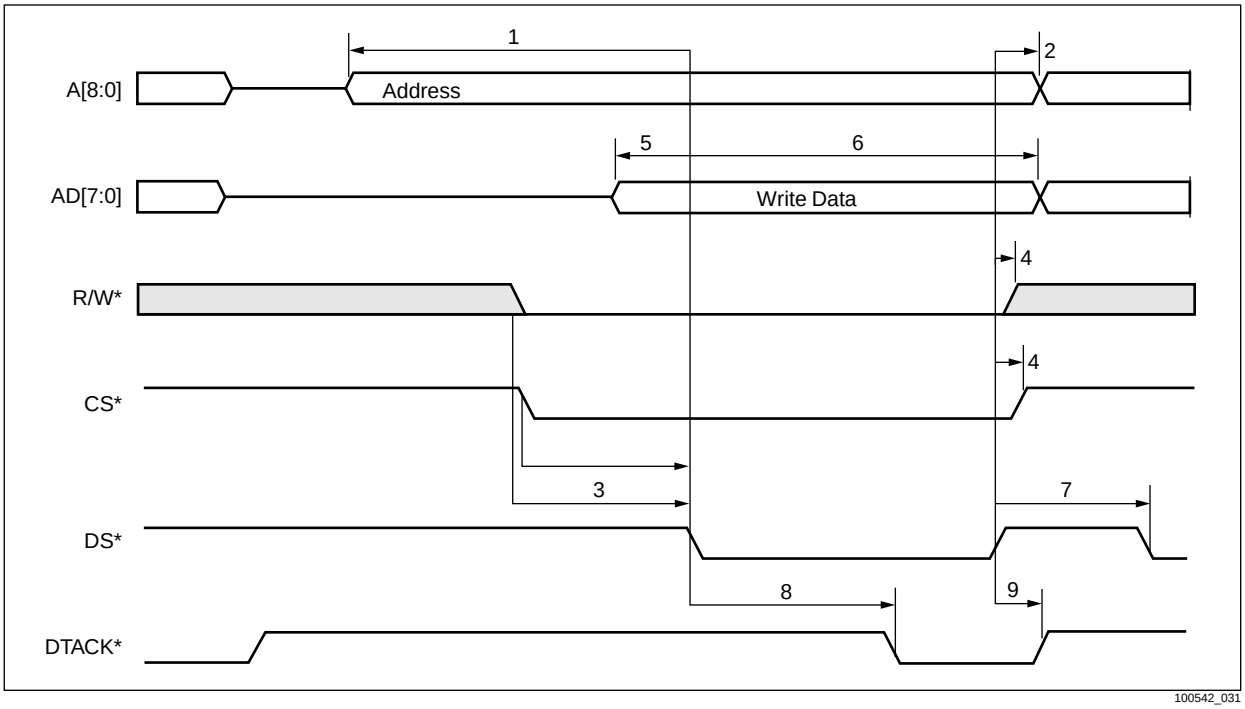


Table 4-10. Motorola Asynchronous Write Cycle (MOTO* = 0)

Symbol	Parameter	Minimum	Maximum	Units
1	A[8:0] Address setup to DS* low	4	—	ns
2	A[8:0] Address hold after DS* high	3	—	ns
3	R/W* low & CS* low to DS* low	3	—	ns
4	DS* high to CS* high & R/W* invalid	3	—	ns
5	AD[7:0] input data setup to DS* low	3	—	ns
6	AD[7:0] input data hold after DS* low	5	—	ns
7	DS* high to next DS* low	15	—	ns
8	DS* low to DTACK* low	—	3 x clk + 15(1)	ns
9	DS* high to DTACK* high Z	—	19	ns

FOOTNOTE:

(1) Clk is the cycle (ns) of the slowest clock (DS3—22 ns, E3—29 ns).

GENERAL NOTE:

1. CX28342/CX28343/CX28344/CX28346/CX28348 are in the system but any negative edge of RD* or positive edge of WR* starts a read/write cycle.

4.3.1 Additional Restrictions

The following restrictions apply:

- When the clock source has been changed due to a setup change (RxFIFEn, LineLp, SourceLp, PayldLp, RlineLp), the CX28342/3/4/6/8 should not be accessed for 20 of the slowest clock cycles
- After software reset, the CX28342/3/4/6/8 should not be accessed for 40 of the slowest clock cycles.
- The OneSec pulse minimal width should be 120 ns.
- When output pin INTR* resets (i.e., interrupt is activated), the microprocessor reads the Source Channel Status register. It must wait at least one-half cycle of the slowest clock to read the updated information in th Source Channel register.

4.4 JTAG Interface Timing

The JTAG Interface timer is specified and depicted in this section.

Figure 4-11. JTAG Interface Timing

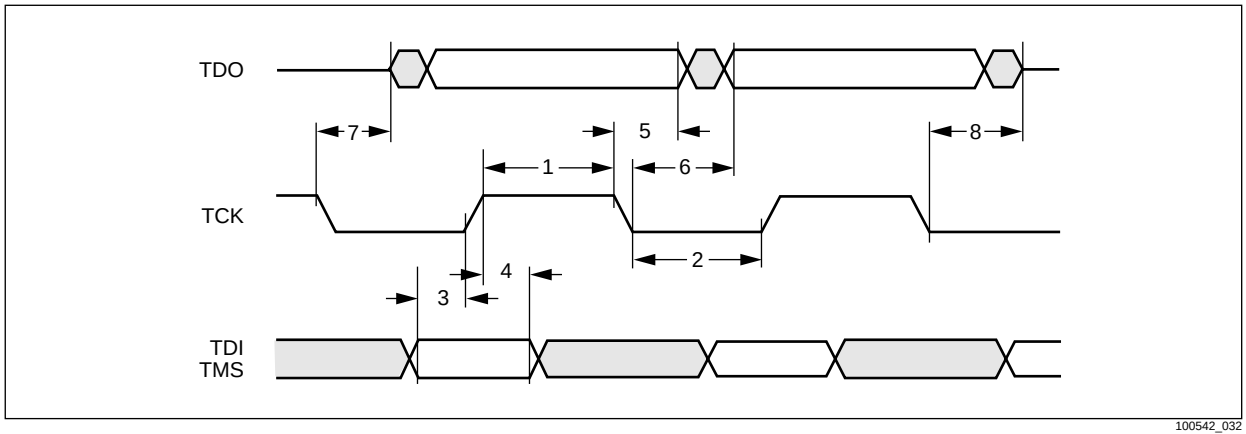


Table 4-11. Test and Diagonstic Interface Timing Requirements

Symbol	Parameter	Minimum	Maximum	Units
1	TCK Pulse Width High	80	—	ns
2	TCK Pulse Width Low	80	—	ns
3	TMS, TDI Setup to TCK Rising Edge	20	—	ns
4	TMS, TDI Hold after TCK High	20	—	ns

Table 4-12. Test and Diagnostic Interface Switching Characteristics

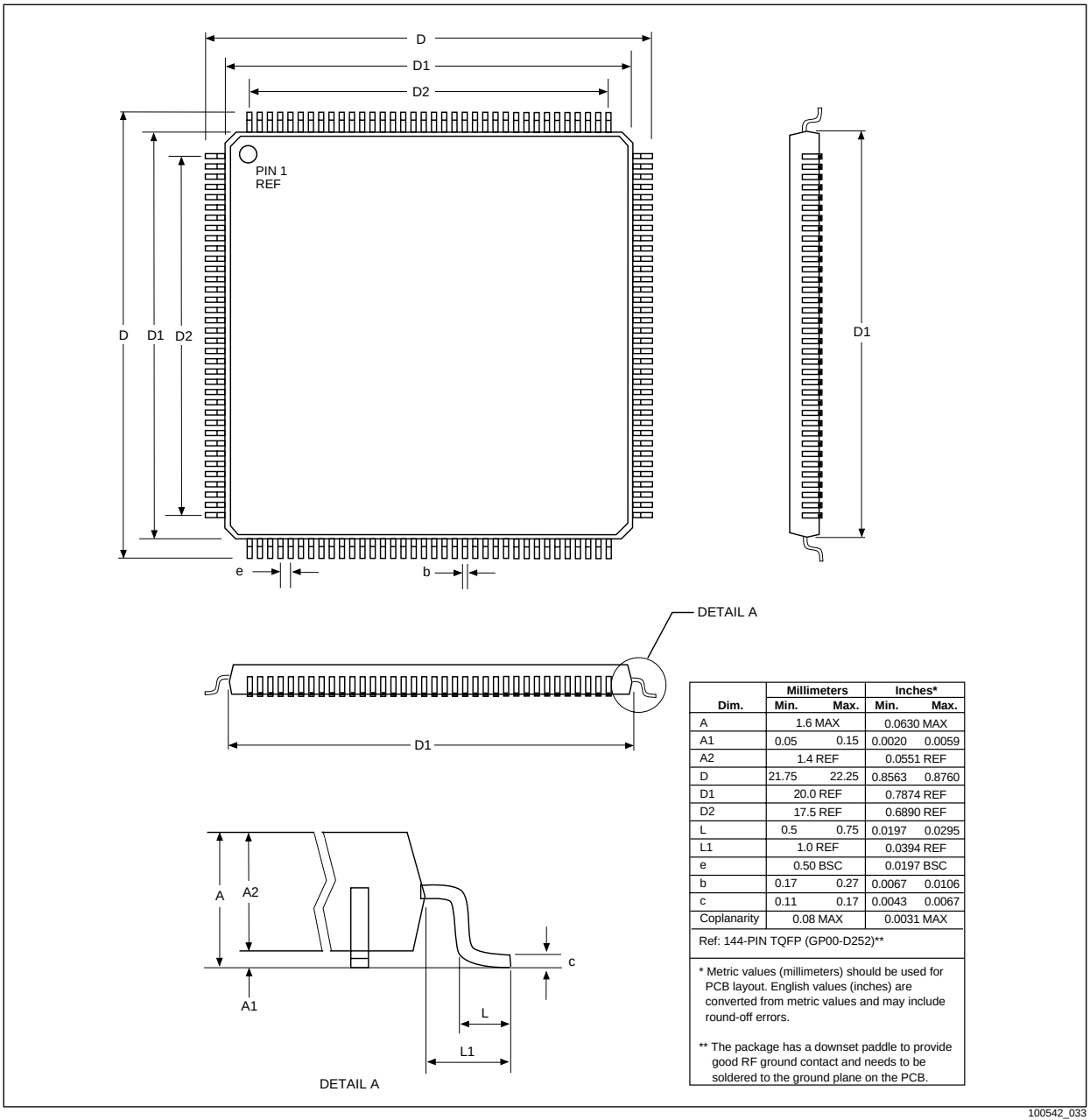
Symbol	Parameter	Minimum	Maximum	Units
5	TDO Hold after TCK Falling Edge	0	—	ns
6	TDO Delay after TCK Low	—	25	ns

4.5 Mechanical Specifications

4.5.1 Package Types

The package used is an ETQFP with 144 pins. The double, triple, and quad framer versions use the same package with the same number of pins.

Figure 4-12. Mechanical Specification for 144-pin ETQFP



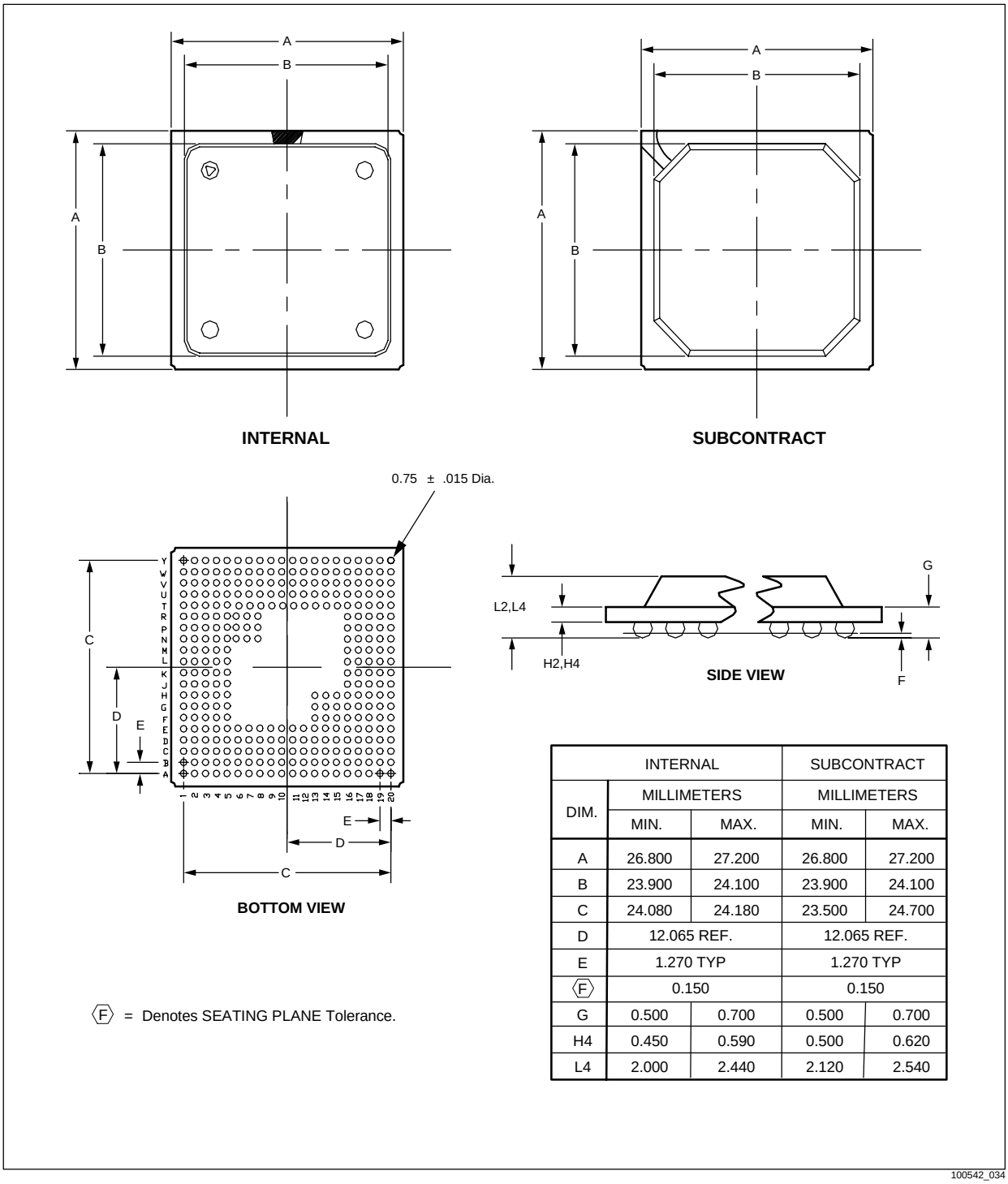
Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A		1.6 MAX		0.0630 MAX
A1	0.05	0.15	0.0020	0.0059
A2		1.4 REF		0.0551 REF
D	21.75	22.25	0.8563	0.8760
D1		20.0 REF		0.7874 REF
D2		17.5 REF		0.6890 REF
L	0.5	0.75	0.0197	0.0295
L1		1.0 REF		0.0394 REF
e		0.50 BSC		0.0197 BSC
b	0.17	0.27	0.0067	0.0106
c	0.11	0.17	0.0043	0.0067
Coplanarity		0.08 MAX		0.0031 MAX
Ref: 144-PIN TQFP (GP00-D252)**				

* Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may include round-off errors.

** The package has a downset paddle to provide good RF ground contact and needs to be soldered to the ground plane on the PCB.

100542_033

Figure 4-13. Mechanical Specification for 27x27 mm 318-Ball PBGA



DIM.	INTERNAL		SUBCONTRACT	
	MILLIMETERS		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	26.800	27.200	26.800	27.200
B	23.900	24.100	23.900	24.100
C	24.080	24.180	23.500	24.700
D	12.065 REF.		12.065 REF.	
E	1.270 TYP		1.270 TYP	
⟨F⟩	0.150		0.150	
G	0.500	0.700	0.500	0.700
H4	0.450	0.590	0.500	0.620
L4	2.000	2.440	2.120	2.540

⟨F⟩ = Denotes SEATING PLANE Tolerance.

4.6 Applicable Standards

The CX28344 quad framer design meets the requirements of the major standards for DS3 and E3. Reception and transmission formats are provided for the following standards:

- ANSI T1.107-1995
- ANSI T1.404-1994
- ITU-T G.751
- ITU-T G.832

The following are supported:

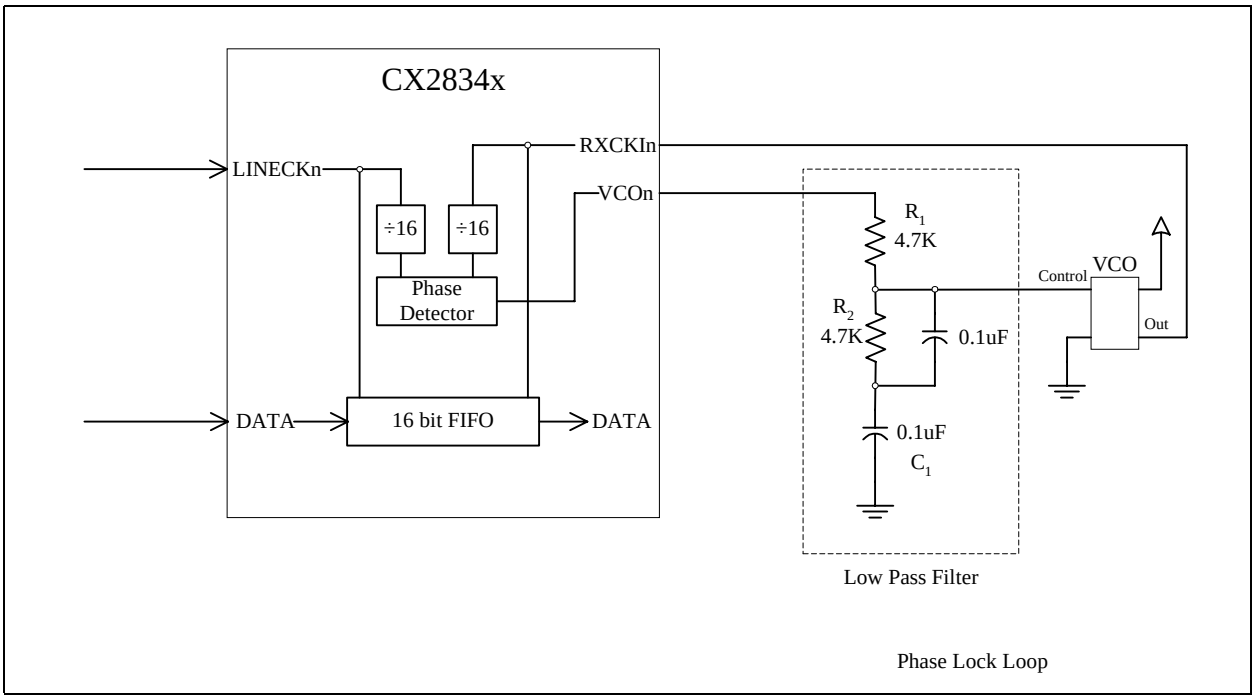
- DS3 M13/M23
- DS3 C-bit Parity
- E3 G.751
- E3 G.832

Both the HDLC/LAPD terminal data link and the FEAC channel, as defined in *T1.107-1995*, are supported. Maintenance features and criteria required by *Bellcore TR-TSY-000009*, *ANSI TI.231-1997*, and *ITU G.775* are furnished.

The framer provides an HDLC/LAPD receiver and transmitter for the data in the data link channels (C5 in the DS3 M13/M23, N bit in *G.751*, and GC or NR in *G.832*) according to *ITU-T* standard *Q.921* and *ISO/IEC 3309-1993*.

Appendix A: Dejitter Circuit Analysis

Figure A-1. CS2834x Dejitter Circuitry



The CX2834x framer dejitter circuitry consists of a 16-bit FIFO and a phase comparator. To complete the dejitter circuitry, a low-pass filter and VCO are added. This essentially builds a PLL that locks onto the input clock, LINECK, and clocks the data out of the FIFO with a smoothed clock edge.

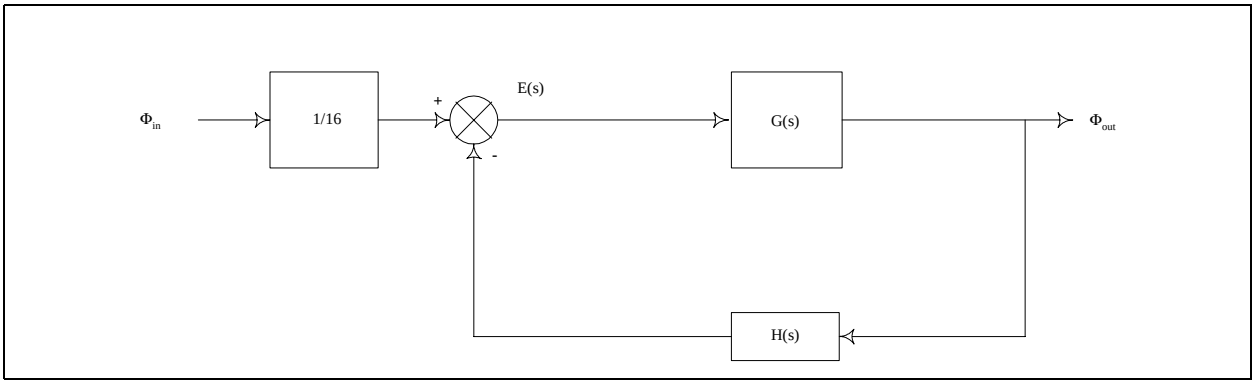
The data stream is clocked into the FIFO buffer with the incoming LINECK clock. The data stream is clocked out of the FIFO buffer and into the remaining receiver circuitry by RXCKI, which is a dejittered version of LINECK.

First the LINECK from the LIU is divided by 16. This is key; it ensures that the input clock is averaged over time. This in turn allows the PLL circuitry to lock onto a wider range of LINECK jitter and to provide the dejittered output. The RXCLI, which is the VCO output, is divided by 16. This along with the divided LINECK are fed into a phase detector. The output of the phase detector, VCOn, is then fed to a low-pass filter which provides the control voltage to the VCO.

What follows is an analysis of the dejitter circuit.

The dejitter control loop is represented as follows, where Φ_{in} is the incoming LINECK signal and Φ_{out} is the output from the VCO (RXCKI).

Figure A-2. Dejitter Control Loop



The error signal is the sum of the input signal divided by 16 and the VCO output divided by 16.

$$E(s) = \frac{\Phi_{in}}{16} - \Phi_{out} H(s) \quad \text{Eq. 1}$$

The output signal is the error signal times the gain of the system

$$\Phi_{out} = E(s)G(s) \quad \text{Eq. 2}$$

Rearranging equation 1 for Φ_{in}

$$\Phi_{in} = 16E(s) + 16\Phi_{out} H(s) \quad \text{Eq. 3}$$

The ratio of the output to input signal yields equation 4.

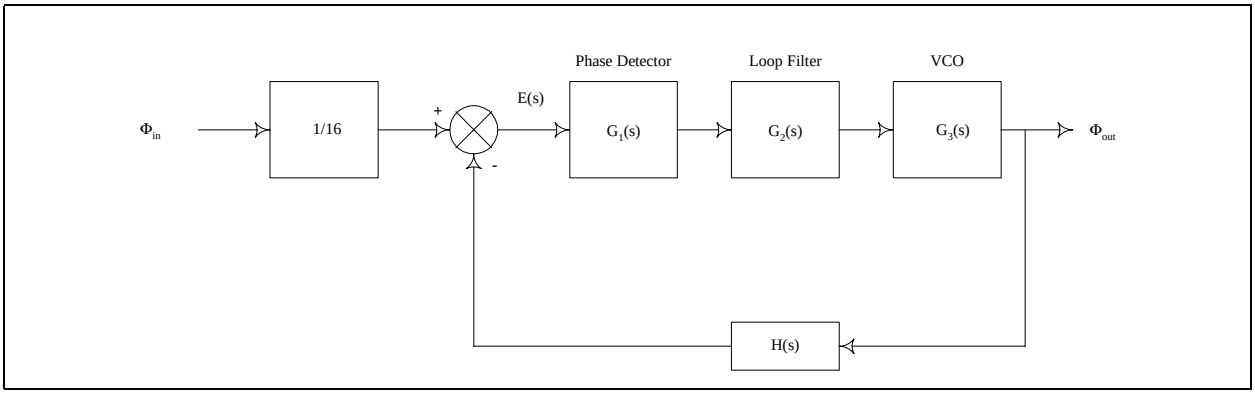
$$\frac{\Phi_{out}}{\Phi_{in}} = \frac{E(s)G(s)}{16\left(E(s) + E(s)G(s)\right)} \quad \text{Eq. 4}$$

Simplifying this to the closed loop equation for this system.

$$\frac{\Phi_{out}}{\Phi_{in}} = \frac{G(s)}{16\left(1 + G(s)H(s)\right)} \quad \text{Eq. 5}$$

The gain for the system involves the phase detector, the low-pass filter, and the VCO. Figure A-3 shows the system with these three components broken out.

Figure A-3. Components of System Gain



Transfer Function Closed Loop

$$\frac{G(s)}{16\left(1+H(s)G(s)\right)} \qquad \text{Eq. 6}$$

The phase detector gain is 3 volts per cycle of input.

$$G_1(s) = k_1 = \frac{3}{2\Pi} \quad \text{(v/rad)} \qquad \text{Eq. 7}$$

The low-pass filter contributes one pole and one zero.

$$G_2(s) = k_2\left(\frac{s+a}{s+b}\right) \qquad \text{Eq. 8}$$

where:

$$k_2 = \frac{R_2}{R_1 + R_2} \qquad \text{Eq. 9}$$

$$a = \frac{1}{R_2 C_1} = \frac{1}{\tau_1} \qquad \text{Eq. 10}$$

$$b = \frac{1}{(R_1 + R_2)C_1} = \frac{1}{\tau_1 + \tau_2} \qquad \text{Eq. 11}$$

$$G_3(s) = \frac{k_3}{s} \quad \text{(rad/v-s)} \qquad \text{Eq. 12}$$

The VCO is an integrator and contributes one pole.

$$G_3(s) = \frac{k_3}{s} \quad \text{(rad/v-s)} \qquad \text{Eq. 13}$$

The feedback loop consists of the divide by 16

$$H(s) = \frac{1}{16} \qquad \text{Eq. 14}$$

$$G(s) = k_1 \times k_2 \left(\frac{s+a}{s+b} \right) \times \frac{k_3}{s} \qquad \text{Eq. 15}$$

$$= \frac{k_1 k_2 k_3 (s+a)}{(s^2 + sb)} \qquad \text{Eq. 16}$$

Putting everything together, the loop equation becomes:

$$\frac{\frac{k_1 k_2 k_3 (s+a)}{(s^2 + sb)}}{16\left(1 + \frac{k_1 k_2 k_3 (s+a)}{(s^2 + sb)} \times \frac{1}{16}\right)} \qquad \text{Eq. 17}$$

Simplifying to the final form of the closed loop equation.

$$\frac{k_1 k_2 k_3 (s+a)}{16s^2 + (16b + k_1 k_2 k_3)s + k_1 k_2 k_3 a} \qquad \text{Eq. 18}$$

The characteristic equation for the system takes the form:

$$s^2 + 2\zeta\omega_n s + \omega_n^2 = 16(1 + G(s)H(s)) = 0 \qquad \text{Eq. 19}$$

Which is the denominator of the closed loop equation.

$$16s^2 + (16b + k_1 k_2 k_3)s + k_1 k_2 k_3 a = 0 \qquad \text{Eq. 20}$$

Therefore the natural frequency of the system is given by:

$$\omega_n^2 = \frac{k_1 k_2 k_3 a}{16} \qquad \text{Eq. 21}$$

And the damping factor by:

$$\zeta = \frac{(16b + k_1 k_2 k_3)}{32\omega_n} \quad \text{Eq. 22}$$

When designing the circuit, there are several criteria to keep in mind:

1. The loop gain

A high loop gain is desired so the loop will remain in lock with the incoming clocks. A higher loop gain allows a greater change in frequency before too much phase error is introduced. The gain is derived from the phase detector and the VCO.

The phase detector is set within the framer itself at approximately $3/2\pi$ v/rad. The VCO is selected by the designer. The gain from the VCO is in the form $2\pi\Delta f / \Delta v$ rad/v-s.

The hold-in range is approximately plus/minus the product of the phase detector and the VCO or

$\pm 3\Delta f / \Delta v$ (/s)

2. Natural Frequency (ω_n)

The natural frequency is determined by the passive components R1, R2, and C1. This is also the characteristic frequency of the loop where the -3 dB corner is located. The tradeoff is that with a high natural frequency more low frequency jitter is allowed to pass, but the system will react faster to step inputs.

3. Damping factor (ζ)

The damping factor should be chosen to allow the fastest excursion of the system output without the system becoming unstable. When the system frequency approaches the natural frequency, if underdamped, there is a tendancy for the system to become unstable, i.e. lock will be lost. Overshoot of the output signal will not settle to a steady state and ring. If overdamped, the system will have trouble obtaining lock, i.e. the system will not track. The problem with overdamped systems is getting to the steady state condition.

The goal is to allow some overshoot without allowing the system to be become completely unstable or to ring too long. In general, the ideal damping factor is 0.707.

The whole premise of the dejitter circuit as implemented in the CX2834x device is to provide a clock-to-data edge relationship that is stable and consistent.

It should be noted that when using the CX28344 with an LIU, there is a receive clock that is available even when there is no signal coming into the LIU. Therefore, the system will be locked to this clock and the PLL circuitry will not be hunting. The system should be optimized for step response inputs. The implication is the system will be limited by the ability of the PLL circuitry in the LIU.

Analyzing the circuit in Figure A-1 the values for the resistors, capacitor, and the VCO can be substituted into the derived equations.

Substituting the values for the system shown in Figure A-1 result in the coefficients shown to the right. k_1 is the phase detector built into the CX28344 and is a constant.

$$k_1 = \frac{3}{2\Pi} = 0.4775 \quad \text{(v/rad)}$$

$$k_2 = \frac{R_2}{R_1 + R_2} = \frac{4.75K\Omega}{4.75K\Omega + 4.75K\Omega} = \frac{1}{2}$$

k_3 is from the VCO and has a frequency range of 300 ppm over the control voltage range of 2.67 volts.

$$k_3 = \frac{2\Pi\Delta f}{\Delta v} = 31580 \quad \text{(rad/v-s)}$$

Substituting the values of 4.75 KΩ for the resistors and 0.1 µF for the capacitor:

$$a = \frac{1}{R_2 C_1} = 2105 \quad \text{(/s)}$$

$$b = \frac{1}{(R_1 + R_2)C_1} = 1053 \quad \text{(/s)}$$

The result for the natural frequency of the system is:

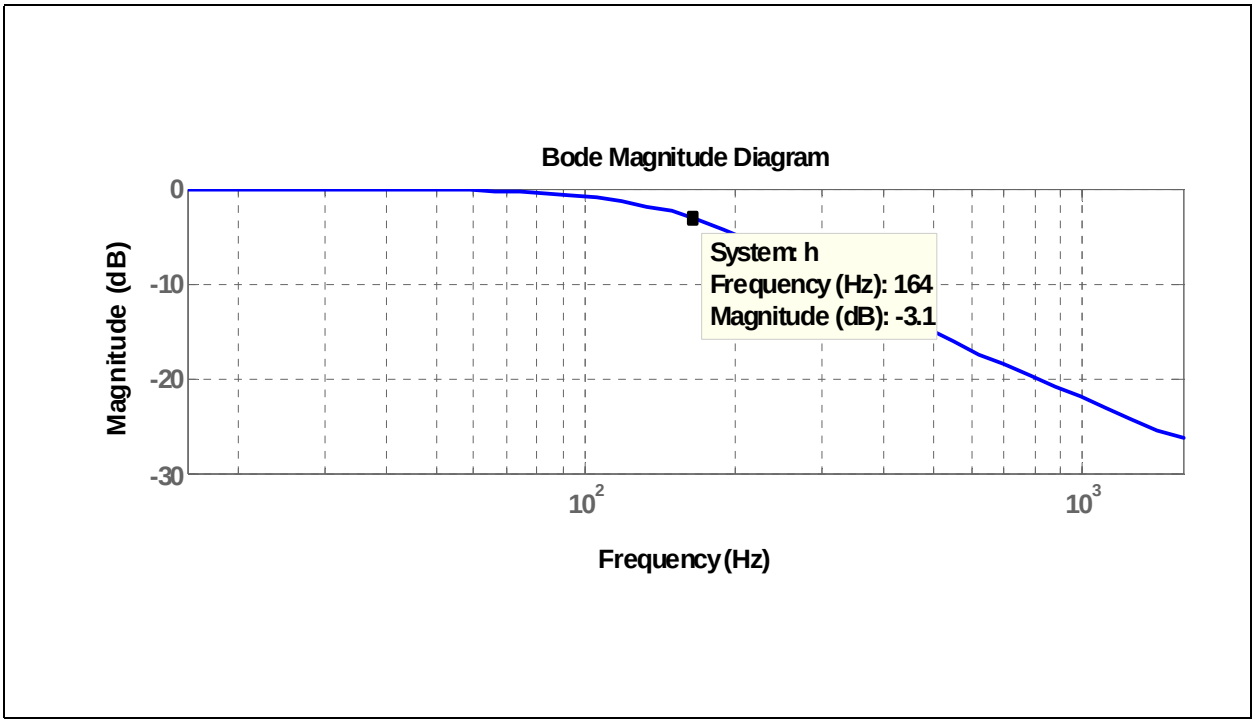
$$\omega_n = \sqrt{\frac{k_1 k_2 k_3 a}{16}} = 996 \qquad (\sim 159 \text{ Hz})$$

and the damping factor is:

$$\zeta = \frac{(16b + k_1 k_2 k_3)}{32\omega_n} = 0.765$$

The results from the analysis show a good damping factor of 0.765 and a natural frequency of 996 rad/s. Although it would be better to get the natural frequency lower so that more high frequency jitter would be filtered, the system response would suffer.

Figure A-4. Bode Diagram of the System



The test results shown in Figures A-5 and A-6 show very small jitter transfer and very good jitter tolerance. In Figure A-5, it can be seen where the approximate -3 dB point is located. As expected, the transfer is greater at the low frequencies and improves as jitter frequency increases.

Figure A-5. Jitter Transfer with FIFO Enabled

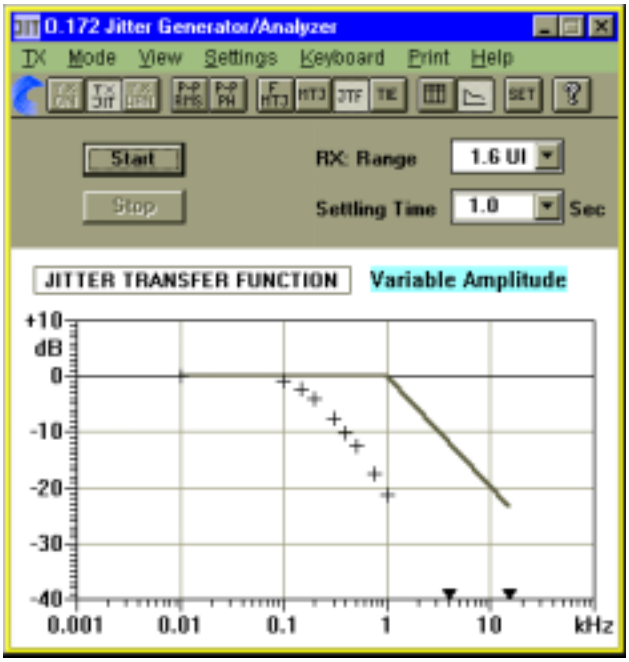
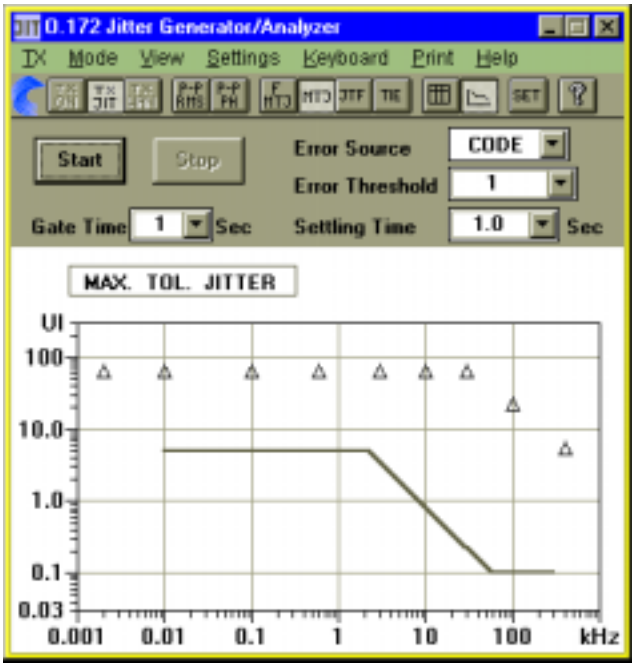


Figure A-6. Jitter Tolerance with FIFO Enabled



Figures A-7 and A-8 show the same system with the dejitter FIFO disabled. Without the FIFO enabled, the jitter transfer remains at 0 dB which means jitter out equals jitter in. In addition, the maximum tolerable jitter falls off at higher frequencies.

Figure A-7. Jitter Transfer with FIFO Disabled

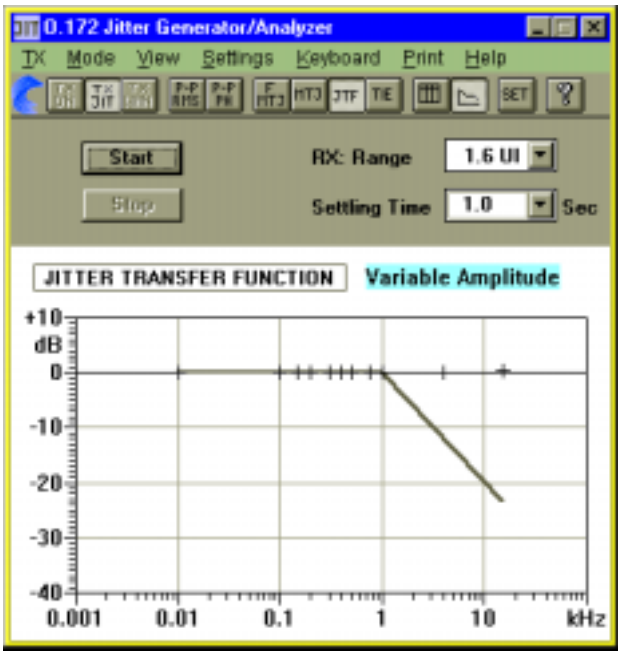
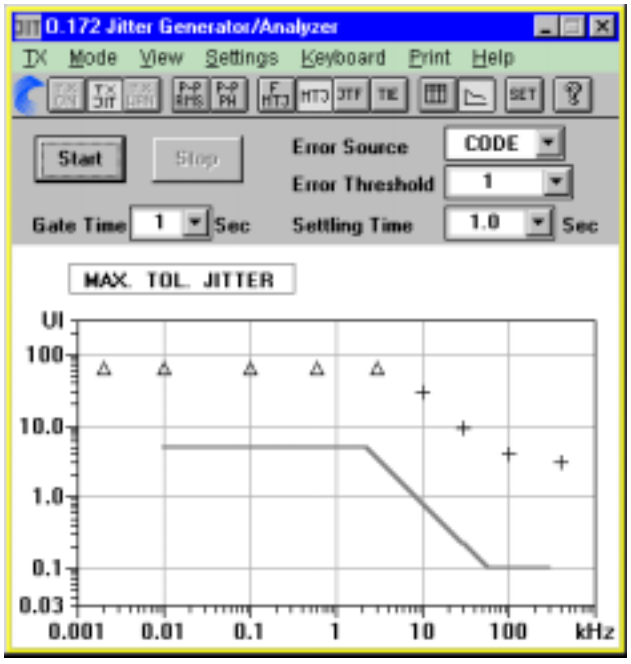


Figure A-8. Jitter Tolerance with FIFO Disabled



Test Equipment:

Wandel & Goltermann Advanced Network Tester - ANT-20

Additional Resources:

T. B. Mills; "The Phase Locked Loop IC as a Communication System Building Block"; AN-46, National Semiconductor ©1971.

M. Curtin and P O'Brien; "Phase-Locked Loops for High-Frequency Receivers and Transmitters - Part 1"; Analog Dialogue 33-3, Analog Devices.

R. L. Best; "Phase Locked Loops: Design, Simulation, and Applications"; 3rd Edition, McGraw Hill.

Appendix B: Frame Structure Summary

As per ANSI T1.107-1995 and ITU-T G.704-1995, in DS3 mode, a frame is composed of 4760 bits, of which, 4704 (4697 in M13/M23) form the payload, while 56 (63 in M13/M23) are overhead bits. The overhead bits are divided into several fields, which are described in Table B-1.

Table B-1. Overhead Bits in DS3 Mode

Field	Description
3 M-bits	Bits 2721, 3401 & 4081 for framing, bearing a “010” pattern
28 F-bits	Every 170 bits, from bit 86 to bit 4676 for subframing, bearing a “1001”x7 pattern
2 X-bits	Bits 1 and 681 for remote alarm indication (RAI), bearing a “11” pattern to signal error-free conditions, a “00” pattern to signal RAI
2 P-bits	Bits 1361 and 2041 for parity, bearing a “11” pattern if the digital sum of all the 4704 payload bits of the preceding frame equals 1, a “00” pattern if it equals 0
In DS3 M13/M23 Mode Only	
21 C-bits	Bits 171, 341, 511, 851, 1021, 1191, 1531, 1701, 1871, 2211, 2381, 2551, 2891, 3061, 3231, 3571, 3741, 3911, 4251, 4421, and 4591 for justification control bits of the payload data channels
7 stuff opportunity bits	Bits 597, 1278, 1959, 2640, 3321, 4002, and 4683
In DS3 C-bit Parity Mode Only	
1 Cb11 bit	Bit 171 for Application Identification Channel (AIC), set to 1
1 Cb12 bit	Bit 341 reserved, set to 1
1 Cb13 bit	Bit 511 for Far-End Alarm and Control (FEAC), bearing FEAC messages when active, set to 1 when inactive
3 Cb2 bits	Bits 851, 1021, and 1191 reserved, bearing a “111” pattern
3 Cb3 bits	Bits 1531, 1701, and 1871 for path parity, set to equal P-bits by terminating equipment (not to be modified by path equipment)
3 Cb4 bits	Bits 2211, 2381, and 2551 for Far-End Block Error (FEBE), bearing a “111” pattern to signal error-free conditions, any other to signal FEBE
3 Cb5 bits	Bits 2891, 3061, and 3231 for terminal data link (DL), bearing data link messages and flags when active, a “111” pattern when inactive
3 Cb6 bits	Bits 3571, 3741, and 3911 reserved, bearing a “111” pattern
3 Cb7 bits	Bits 4251, 4421, and 4591 reserved, bearing a “111” pattern

As per ITU-T G.751, in E3-G751 mode, a frame is composed of 1536 bits, of which, 1508 form the payload, while 28 are overhead bits. The overhead bits are divided into several fields, which are described in Table B-2.

Table B-2. Overhead Bits in E3G751 Mode

Field	Description
10 FAS bits	Bits 1 to 10 for framing, bearing a “1111010000” (left-to-right) pattern
1 A-bit	Bit 11 for remote alarm indication (RAI), set to 0 to signal error-free conditions, to 1 to signal RAI
1 N-bit	Bit 12 for terminal data link (DL), bearing data link messages and flags when active, set to 1 when inactive
12 C_j-bits	Bits 385 to 388, 769 to 772, and 1153 to 1156 for justification control bits of the payload data channels
4 stuff opportunity bits	Bits 1157 to 1160

As per ITU-T G.832-1995 and ETS 300 337-1997, in E3-G832 mode, a frame is composed of 537 bytes (octets), of which, 530 form the payload, while 7 are overhead bytes. The overhead bytes are divided into several fields, which are described in Table B-3.

Table B-3. Overhead Bytes in E3G832

Field	Description
2 FA bytes	Bytes 1 and 2 for framing, bearing a “1111011000101000” (left-to-right) pattern
1 EM byte	Byte 61 for BIP-8 even parity, each bit set to 1 if the digital sum of the 537 corresponding payload and overhead bits of the preceding frame equals 1, to 0 if it equals 0
1 TR byte	Byte 121 for trail trace, bearing 16-byte trail trace messages
1 RDI bit	Bit 1 of byte 181 (MA byte) for Remote Defect Indication (RDI), set to 0 to signal error-free conditions, to 1 to signal RDI
1 REI bit	Bit 2 of byte 181 (MA byte) for Remote Error Indication (REI), set to 0 to signal error-free conditions, to 1 to signal REI
3 PT bits	Bits 3 to 5 of byte 181 (MA byte) for Payload Type (PT) information
2 PD/MI bits	Bit 6 and 7 of byte 181 (MA byte) for Payload-Dependent (PD) information or Multiframe Indication (MI)
1 TM/SSM bit	Bit 8 of byte 181 (MA byte) for Timing Marker (TM) or Synchronization Status Message (SSM)
1 NR byte	Byte 241 for network operator use, optionally carrying a terminal data link (DL)
1 GC byte	Byte 301 for general-purpose communications channel, optionally carrying a terminal data link (DL)

Appendix C: B3ZS/HDB3 Encoding

The definitions of B3ZS and HDB3 encoding, according to the ITUT-G.703 standard, are:

- In DS3 mode of operation, when rail (bipolar) mode is enabled, B3ZS encoding is performed. Each block of three successive zeros is replaced by 00V or B0V. The choice of 00V or B0V is made so that the number of B pulses between consecutive V pulses is odd.
- Both in E3-G.751 and E3-832 modes of operation, when rail mode is enabled, HDB3 encoding is performed. Each block of four successive zeros is replaced by 000V or B00V. The choice of 000V or B00V is made so that the number of B pulses between consecutive V pulses is odd.

NOTE: In the definitions, B represents an inserted pulse conforming to the B3ZS/HDB3 rule, and V represents a violation.

Appendix D: Acronyms

Acronym	Definition
AIC	Application Identification Channel
AIS	Alarm Indication Signal
AMI	Alternate Mark Inversion
ATM	Asynchronous Transfer Mode
BER	Bit Error Ratio (Rate)
BGA	Ball Grid Array
BIP	Bit Interleaved Parity
BPV	Bipolar Violation
BSDL	Boundary Scan Description Language
CDM	Charged Device Model
DS	Digital Service (Signal)
EM	Error Monitoring
EOM	End of Message
ESD	Electrostatic Discharge
ETS	European Telecommunications Standards
FAS	Frame Alignment Signal
FBE	Framing Bit Error
FCS	Frame Check Sequence
FEAC	Far-End Alarm Control
FEBE	Far-End Block Error
FIFO	First-In First-Out
HBM	Human Body Model
HDLC	High-Level Data Link Control
IEEE	Institute of Electrical and Electronic Engineers
ISO	International Organization for Standardization
ITU	International Telecommunications Union
JTAG	Joint Test Action Group

Acronym	Definition
LAPD	Link Access Procedure Direct (Digital)
LCV	Line Code Violation
LIU	Line (LAN) Interface Unit
LOS	Loss of Signal
LSB	or LSBit - Least Significant Bit [use second form when confusion could result]
MA	Maintenance and Adaptation
MI	Multiframe Indication
MPU	Microprocessor Interface
MSB	or Msbit - Most Significant Bit [use second form when confusion could result]
NRZ	Non-Return to Zero
Nr	Network reserved bit
OOF	Out-of-Frame
PBD	P-Bit Disagreement
PBXs	Private Branch Exchanges
PCM	Pulse Code Modulation
PD	Protocol Discriminator/Payload Dependent
PER	Parity Error
PM	Performance Monitoring
PPER	Path Parity Error
RAI	Remote Alarm Indication
RDI	Remote Detection Indication or Remote Defect Indicator
RDL	Receive Data Link
REI	Remote Error Indication
RFEAC	Receive FEAC
Rx	or RX - Receiver
SEF	Severely Errored Framing Event
SSM	Synchronization Status Message
TBD	To Be Determined
TDL	Terminal Data Link
TM	Timing Marker
Tx	or TX - Transmitter
TTL	Transistor-Transistor Logic
VCO	Voltage Controlled Oscillator
XBD	X-Bit Disagreement

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