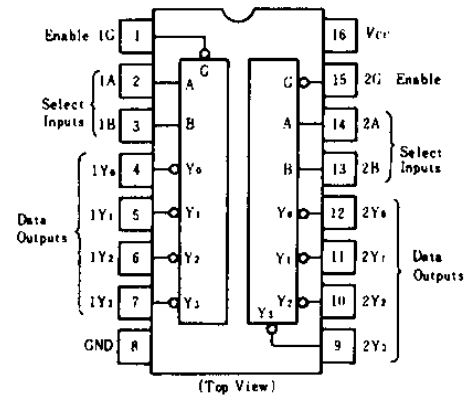
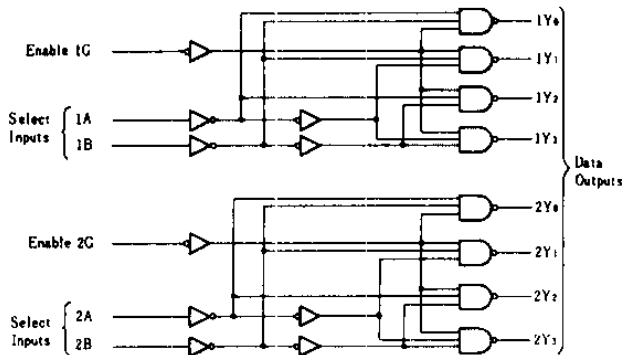


# HD74LS139 • Dual 2-line-to-4-line Decoders/Demultiplexers

The HD74LS139 comprises two individual two-line-to-four-line decoder in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

## PIN ARRANGEMENT

## BLOCK DIAGRAM



## FUNCTION TABLE

Inputs			Outputs			
Enable	Select		Y <sub>0</sub>	Y <sub>1</sub>	Y <sub>2</sub>	Y <sub>3</sub>
G	B	A	Y <sub>0</sub>	Y <sub>1</sub>	Y <sub>2</sub>	Y <sub>3</sub>
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H; high level, L; low level, X; irrelevant

## ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = -20 ~ +75°C)

Item	Symbol	Test Conditions	min	typ*	max	Unit	
Input voltage	V <sub>IH</sub>		2.0	—	—	V	
	V <sub>IL</sub>		—	—	0.8	V	
Output voltage	V <sub>OH</sub>	V <sub>CC</sub> =4.75V, V <sub>IH</sub> =2V, V <sub>IL</sub> =0.8V, I <sub>OH</sub> =-400μA	2.7	—	—	V	
	V <sub>OL</sub>	V <sub>CC</sub> =4.75V, V <sub>IH</sub> =2V, V <sub>IL</sub> =0.8V	I <sub>OL</sub> =4mA	—	—	0.4	V
			I <sub>OL</sub> =8mA	—	—	0.5	
Input current	I <sub>I</sub>	V <sub>CC</sub> =5.25V, V <sub>I</sub> =7V	—	—	0.1	mA	
	I <sub>IH</sub>	V <sub>CC</sub> =5.25V, V <sub>I</sub> =2.7V	—	—	20	μA	
	I <sub>IL</sub>	V <sub>CC</sub> =5.25V, V <sub>I</sub> =0.4V	—	—	-0.4	mA	
Short-circuit output current	I <sub>OS</sub>	V <sub>CC</sub> =5.25V	-5	—	-42	mA	
Supply current	I <sub>CC</sub>	V <sub>CC</sub> =5.25V, Outputs enabled and open	—	6.8	11	mA	
Input clamp voltage	V <sub>IK</sub>	V <sub>CC</sub> =4.75V, I <sub>IN</sub> =-18mA	—	—	-1.5	V	

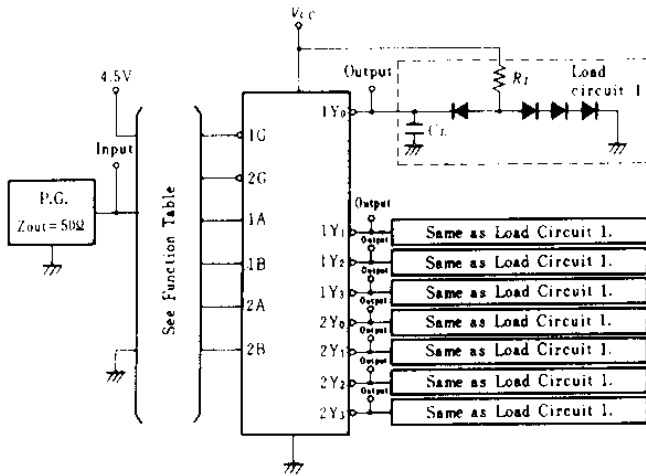
\* V<sub>CC</sub>=5V, T<sub>a</sub>=25°C

## SWITCHING CHARACTERISTICS (V<sub>CC</sub>=5V, T<sub>a</sub>=25°C)

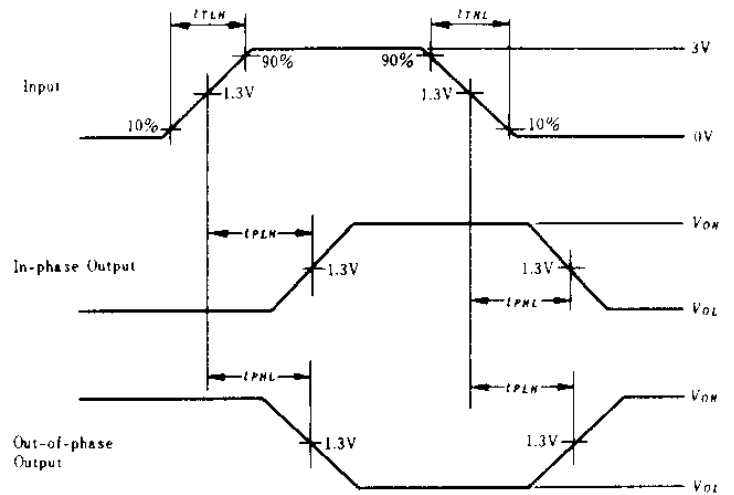
Item	Symbol	Inputs	Outputs	Levels of delay	Test Conditions	min	typ	max	Unit
Propagation delay time	t <sub>PLH</sub>	Binary	1Y <sub>0</sub> ~1Y <sub>3</sub>	2	C <sub>L</sub> =15pF R <sub>L</sub> =2kΩ	—	13	20	ns
	t <sub>PHL</sub>	Select				—	22	33	ns
	t <sub>PLH</sub>	1A, 1B	2Y <sub>0</sub> ~2Y <sub>3</sub>	3		—	18	29	ns
	t <sub>PHL</sub>	2A, 2B				—	25	38	ns
	t <sub>PLH</sub>	Enable	1Y <sub>0</sub> ~1Y <sub>3</sub>	2		—	16	24	ns
	t <sub>PHL</sub>	1G, 2G	2Y <sub>0</sub> ~2Y <sub>3</sub>			—	21	32	ns

## TESTING METHOD

### 1) Test Circuit

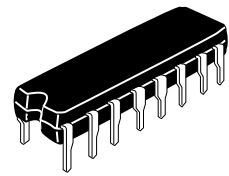
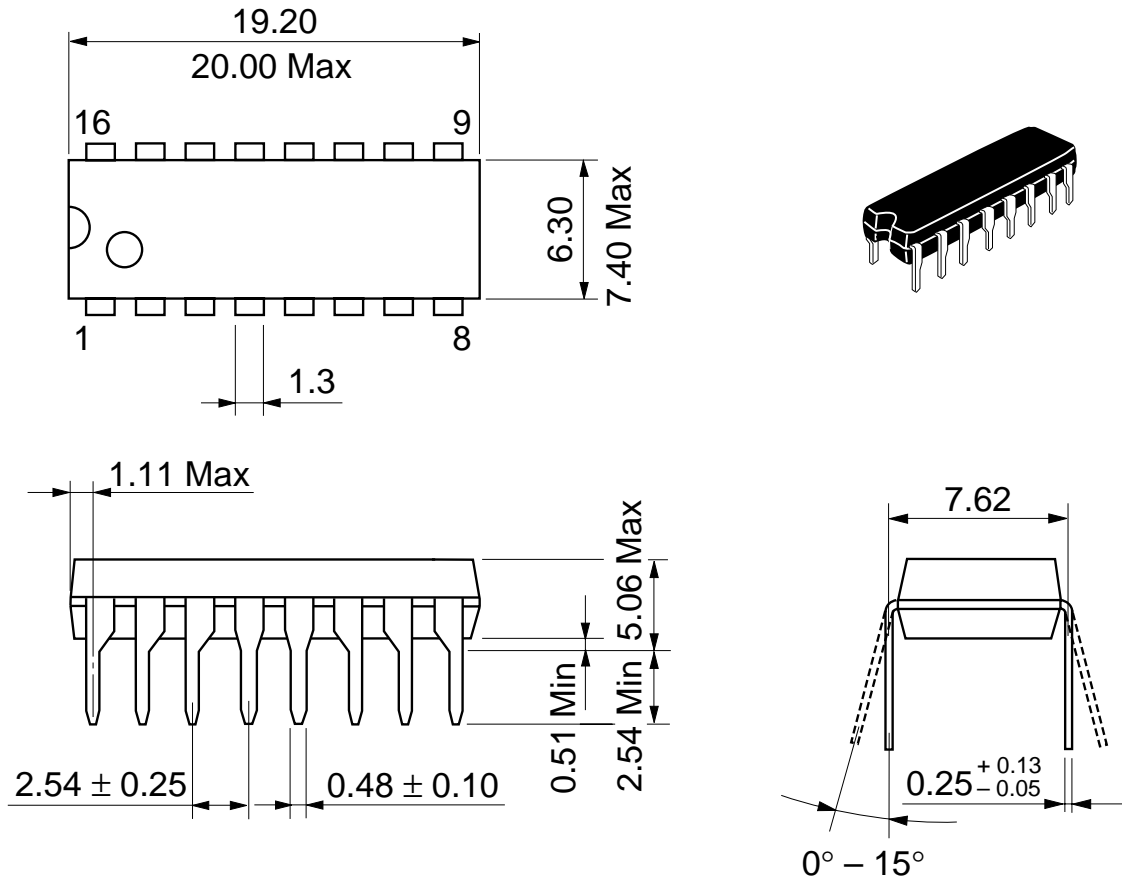


### Waveform



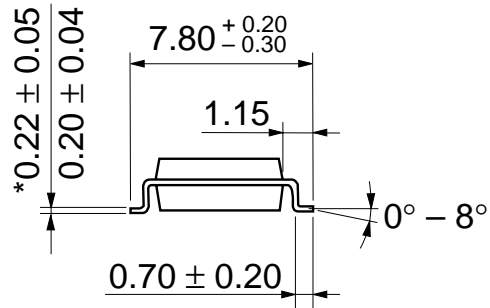
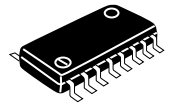
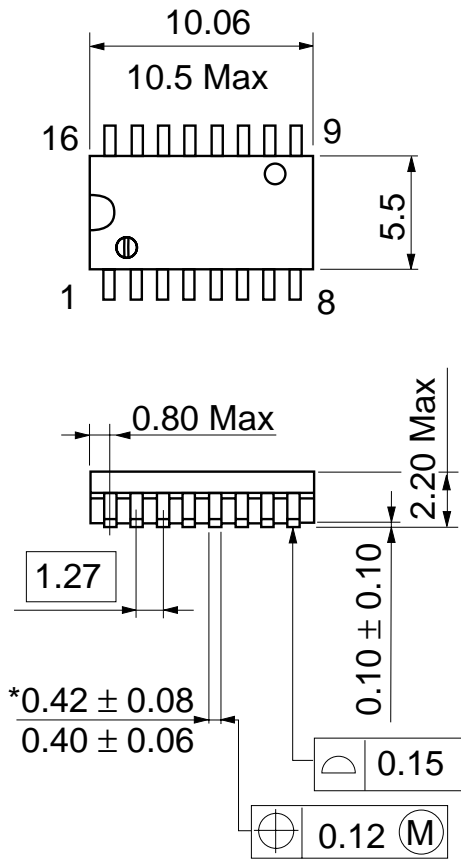
- Notes)
1. Input pulse;  $t_{TLH} \leq 15\text{ns}$ ,  $t_{THL} \leq 6\text{ns}$ ,  $PRR=1\text{MHz}$ , duty cycle=50%
  2.  $C_L$  includes probe and jig capacitance.
  3. All diodes are 1S2074 (H).

Unit: mm



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g

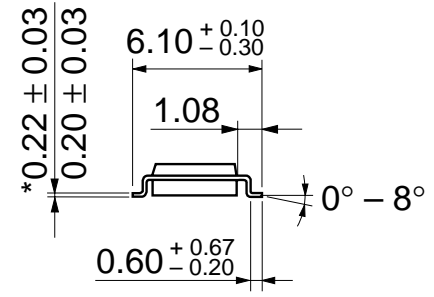
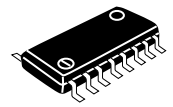
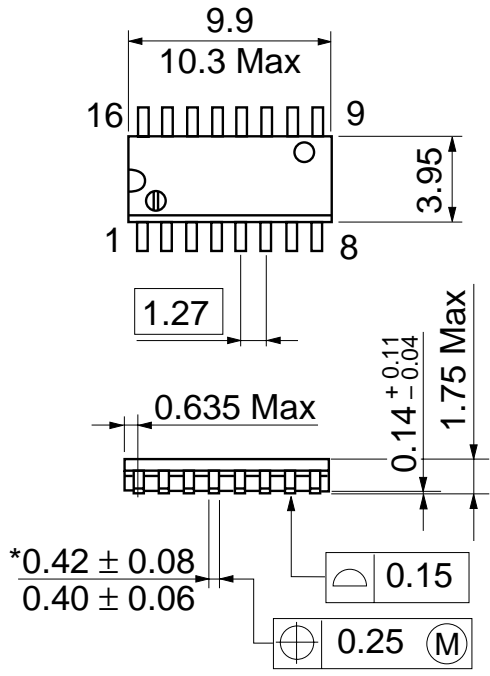
Unit: mm



Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g

\*Dimension including the plating thickness  
 Base material dimension

Unit: mm



\*Dimension including the plating thickness  
 \_\_\_\_\_  
 Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

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