M52957FP

DISTANCE DETECTION SIGNAL PROCESSING FOR 3V SUPPLY VOLTAGE

DESCRIPTION

M52957FP is a semiconductor integrated circuit containing distance detection signal processing circuit for 3V supply voltage.
This device transforms each optical inflow current I1 and I2 from PSD SENSOR into the voltage, and integrates that output after doing calculation corresponds to I1/(I1+I2), and outputs it as the time data(pulse term).

FEATURES

- Wide supply voltage range Vcc=2.2 to 5.5V
- Includes clamp level switching circuit
  (Switch is 16 kinds by outside control)
- Includes standby function
- Includes power on RESET function

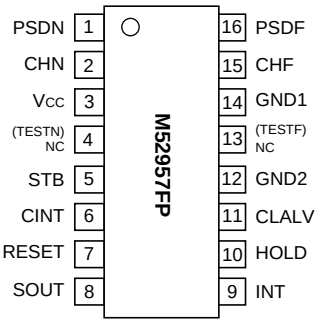
APPLICATION

Auto focus control for the CAMERA
Sensor for short distance etc

RECOMMENDED OPERATING CONDITION

Supply voltage range.....2.2 to 5.5V
Rated supply voltage.....3.0V

PIN CONFIGURATION (TOP VIEW)

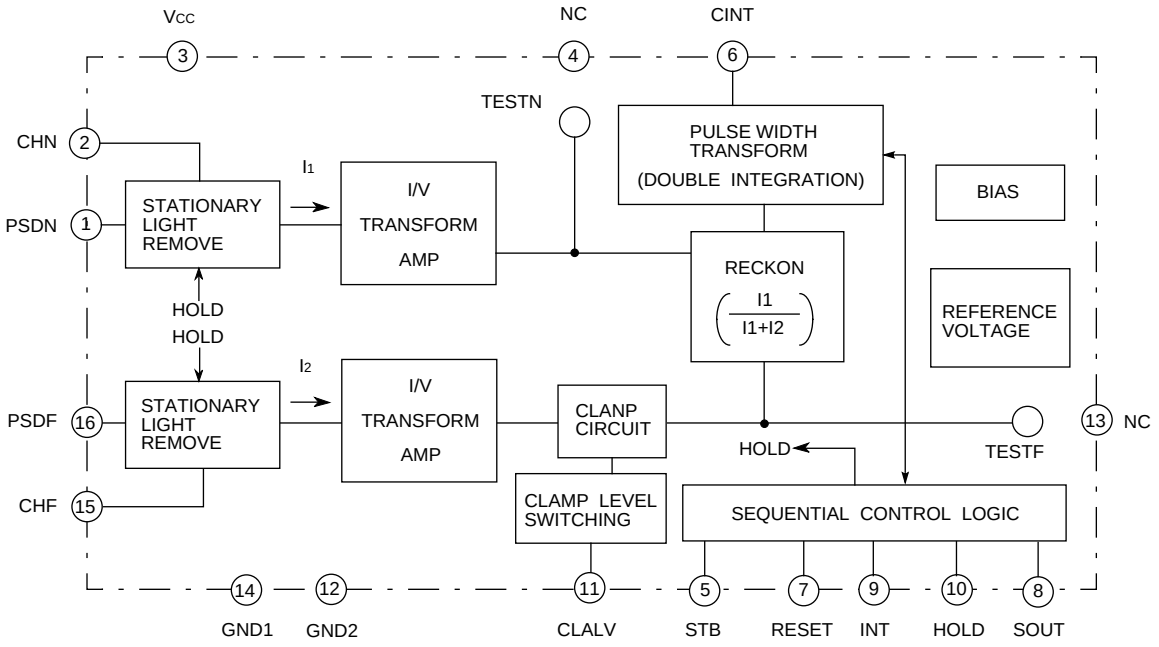


Outline 16P2E-A

NC:NO CONNECTION

BLOCK DIAGRAM

Note: pin4,13 is connected only engineering sample



ABSOLUTE MAXIMUM RATINGS (Ta=25˚C,unless otherwise noted)

Symbol	Parameter	Ratings	Unit	Remark
V_{CC}	Supply voltage	7.0	V	note 1
Pd	Power dissipation	320	mW	Ta=25˚C
Kθ	Thermal derating	-3.2	mW/˚C	Ta≧25˚C
V_{IF}	Pin supply voltage	7.0	V	Pin5,7,8,9,10,11
$V_{I/O}$	Another pin supply voltage	-0.3 to V_{CC}+0.3	V	note 2
I_{sout}	Output pin inflow current	0.5	mA	NPN open collector
T_{opr}	Operating temperature	-10 to 50	˚C	
T_{stg}	Storage temperature	-40 to 125	˚C	
V_{surge}	Surge voltage	±200V over		C=200PF R=0Ω

Note 1. As a principle,do not provide a supply voltage reversely.

2. As a principle,do not provide the terminals with the voltage over supply voltage or under ground voltage.

ELECTRICAL CHARACTERISTICS (Ta=25˚C,Vcc=3.0V, unless otherwise noted)

Symbol	Classification	Parameter	Test conditions	Limits			Unit
				Min.	Typ.	Max.	
V_{CC}		Operating supply voltage range		2.2	3.0	5.5	V
I_{CC1}	Consuming current	Usual consuming current		-	5.9	7.7	mA
I_{CC2}		While Rapid charge consuming current 1	While CH rapid charge consuming current	-	17.7	23.0	mA
I_{CC3}		While Rapid charge consuming current 2	While CH and CINT rapid charge consuming current	-	19.0	24.7	mA
I_{CC4}		While STAND BY consuming current		-	-	1.0	μA
V_{HOH}	HOLD pin	HOLD "H" input voltage		1.1	-	7.0	V
V_{HOL}		HOLD "L" input voltage		-0.3	-	0.3	V
I_{HOH}		HOLD "H" input current	V_{IH}=5.5V	-	-	1.0	μA
I_{HOL}		HOLD "L" input current	V_{IL}=0V	-100	-75	-50	μA
V_{INH}	INT pin	INT "H" input voltage		1.1	-	7.0	V
V_{INL}		INT "L" input voltage		-0.3	-	0.3	V
I_{INH}		INT "H" input current	V_{IH}=5.5V	-	-	1.0	μA
I_{INL}		INT "L" input current	V_{IL}=0V	-100	-75	-50	μA
V_{CLH}	CLALV pin	CLALV "H" input voltage		1.1	-	7.0	V
V_{CLL}		CLALV "L" input voltage		-0.3	-	0.3	V
I_{CLH}		CLALV "H" input current	V_{IH}=5.5V	-	-	1.0	μA
I_{CLL}		CLALV "L" input current	V_{IL}=0V	-100	-75	-50	μA
V_{REH}	RESET pin	RESET "H" input voltage		1.1	-	7.0	V
V_{REL}		RESET "L" input voltage		-0.3	-	0.3	V
I_{REH}		RESET "H" input current	V_{IH}=5.5V	-	-	1.0	μA
I_{REL}		RESET "L" input current	V_{IL}=0V	-100	-75	-50	μA
V_{STH}	STB pin	STB "H" input voltage		V_{CC} -0.3	-	7.0	V
V_{STL}		STB "L" input voltage		-0.3	-	0.3	V
I_{STH}		STB "H" input current	V_{IH}=5.5V	-	-	3.0	μA
I_{STL}		STB "L" input current	V_{IL}=0V	-150	-100	-50	μA
I_{CHQC}	HOLD C	CH rapid charge current	IPSD=5 μA, V_{CH}=0V	-2000	-1000	-500	μA
I_{CHC}		CH stationary charge current	V_{CH}=0V	-30	-20	-10	μA
I_{CHD}		CH stationary discharge current	V_{CH}=1.5V	10	20	30	μA

ELECTRICAL CHARACTERISTICS (cont.)

Symbol	Classification	Parameter	Test conditions	Limits			Unit
				Min.	Typ.	Max.	
I_{CINTC}	Double integration	CINT rapid charge current	V_{CI}=1V(CINT stable period)	84	120	156	µA
V_{CINT}		CINT reference voltage	GND criterion	1.6	1.8	2.0	V
I_{CI1}		The first integration current	V_{CINT}=1.5V V_{CHF}=2V, V_{CHN}=0V	4.2	6.0	7.8	µA
I_{CI2}		The second integration current		-3.31	-2.54	-1.77	µA
ΔI_{CI1}		The first integration current stability percentage		-	-	10	%
ΔI_{CI2}		The second integration current stability percentage		-	-	10	%
I_{CI12}		The first and second integration current ratio	$\lvert I_{CI1}\rvert / \lvert I_{CI2}\rvert$	2.12	2.36	2.60	
$D_{(9:1)-1}$	AF input condition 1	AF output time(9:1)-1	Near side 9 : Far side 1	11.78	13.40	15.02	msec
$D_{(6:4)-1}$		AF output time(6:4)-1	Near side 6 : Far side 4	7.77	8.95	10.13	msec
$D_{(3:7)-1}$		AF output time(3:7)-1	Near side 3 : Far side 7	3.77	4.51	5.25	msec
ΔAF-1		AF slope -1		6.57	8.89	11.21	msec
LAF-1		AF linearity-1		0.9	1.0	1.1	
$D_{(9:1)-2}$	AF input condition 2	AF output time(9:1)-2	Near side 9 : Far side1	11.78	13.40	15.02	msec
$D_{(6:4)-2}$		AF output time(6:4)-2	Near side 6 : Far side4	7.77	8.95	10.13	msec
$D_{(3:7)-2}$		AF output time(3:7)-2	Near side 3 : Far side7	3.77	4.51	5.25	msec
ΔAF-2		AF slope -2		6.57	8.89	11.21	msec
LAF-2		AF linearity-2		0.9	1.0	1.1	
$D_{(9:1)-3}$	AF input condition 3	AF output time(9:1)-3	Near side 9 : Far side1	11.78	13.40	15.02	msec
$D_{(6:4)-3}$		AF output time(6:4)-3	Near side 6 : Far side 4	7.77	8.95	10.13	msec
$D_{(3:7)-3}$		AF output time(3:7)-3	Near side 3 : Far side 7	3.77	4.51	5.25	msec
ΔAF-3		AF slope -3		6.57	8.89	11.21	msec
LAF-3		AF linearity-3		0.9	1.0	1.1	
$\Delta D_{(9:1)}$	AF input condition 1 minus 2	ΔAF output time(9:1)	Near side 9 : Far side1 (Consition 1-2)	-	-	280	µsec
$\Delta D_{(6:4)}$		ΔAF output time(6:4)	Near side 6 : Far side4 (Consition 1-2)	-	-	280	µsec
$\Delta D_{(3:7)}$		ΔAF output time(3:7)	Near side 3 : Far side7 (Consition 1-2)	-	-	280	µsec
I_{SOUTL}	Data	SOUT leak current	V_{IN}=5.5V	-	-	1.0	µA
V_{SOUTS}		SOUT saturation voltage	I_{OUT}=500µA	-	-	0.3	V
ΔINF	Sensor	Signal light saturation current		3.0	-	-	µA
I_{PSD}		Stationary light remove current		-	-	30	µA
I_{CLAM}		Clamp level	Change quantity for Typ. current	-30	-	30	%

I_{CC2}, I_{CC3}, I_{CC4}, I_{CHQC}, I_{CHC}, I_{CHD}, I_{CINTC}, V_{CINT}, I_{CI1}, I_{CI2}

Set up the logic control terminal, correspond to the parameter.

ΔI_{CI1}, ΔI_{CI2}

Change ratio between the first integration current and the second integration current at a voltage of C_{INT} that is {C_{INT} reference voltage(V_{CINT}) to 0.1V} and 1V.

$$\Delta I_{CI1}=(1-\frac{\text{The first integration current } (C_{INT}=1V)}{\text{The first integration current } (C_{INT}=V_{CINT} \text{ to } 0.1V)})\times 100\%$$

$$\Delta I_{CI2}=(1-\frac{\text{The second integration current } (C_{INT}=1V)}{\text{The second integration current } (C_{INT}=V_{CINT} \text{ to } 0.1V)})\times 100\%$$

$D_{(9:1)\text{-}1}$, $D_{(6:4)\text{-}1}$, $D_{(3:7)\text{-}1}$, ΔAF-1, LAF-1, $D_{(9:1)\text{-}2}$, $D_{(6:4)\text{-}2}$, $D_{(3:7)\text{-}2}$, ΔAF-2, LAF-2, $D_{(9:1)\text{-}3}$, $D_{(6:4)\text{-}3}$, $D_{(3:7)\text{-}3}$, ΔAF-3, LAF-3

Connect the resistance of 120kΩ instead of PSD and establish current output from photo coupler correspond to the parameter. And input the varied resistance ratio. And measure the pulse width of S_{OUT} output at that time,obtain AF slope and AF linearity from the equations below.

Input condition1 : I_{PSD}(Stationary light current)=0 I1+I2=100nA
Input condition2 : I_{PSD}(Stationary light current)=0 I1+I2=50nA
Input condition3 : I_{PSD}(Stationary light current)=10 μA I1+I2=100nA

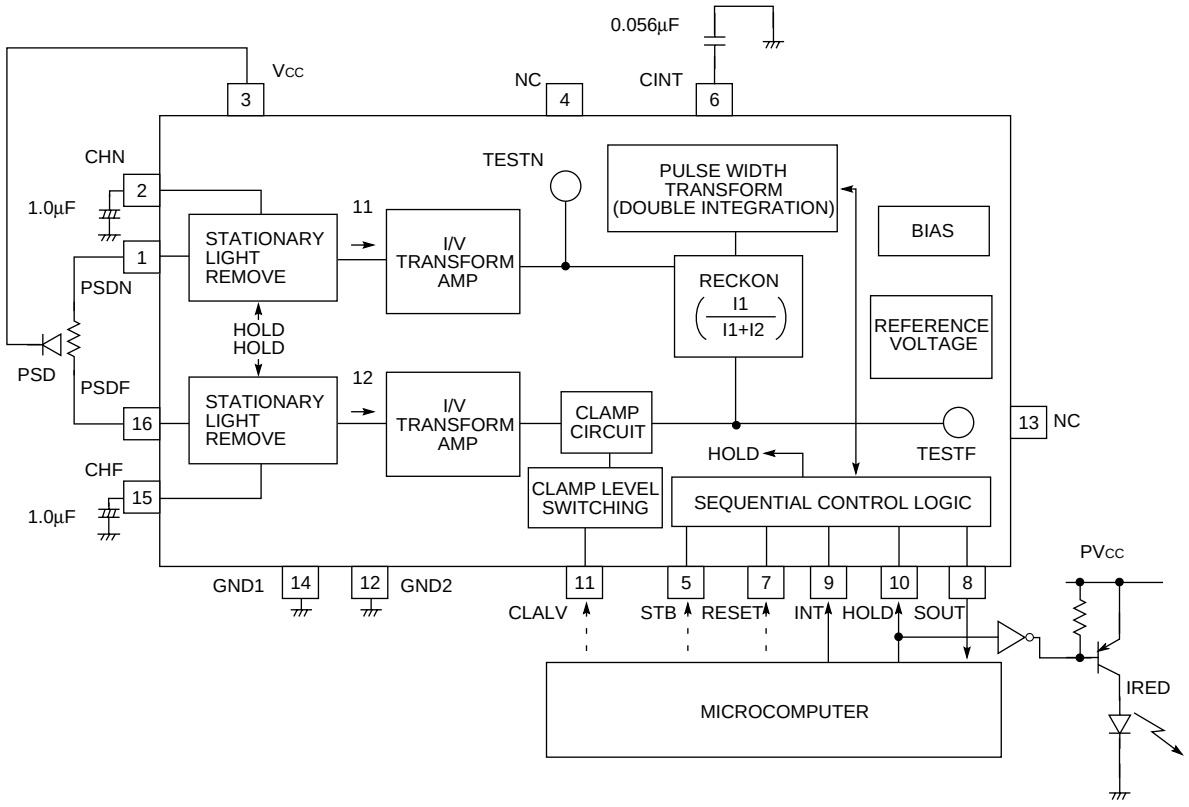
$D_{(9:1)}$....The pulse width of SOUT output at input with I1:I2=9:1
$D_{(6:4)}$....The pulse width of SOUT output at input with I1:I2=6:4
$D_{(3:7)}$....The pulse width of SOUT output at input with I1:I2=3:7

AF slope : $\Delta AF=D_{(9:1)}-D_{(3:7)}$
AF linearity : $L(AF)=(D_{(9:1)}-D_{(6:4)})/(D_{(6:4)}-D_{(3:7)})$
PSD quite resistance : 120kΩ

ΔI_{NF}, I_{PSD}

The input current of one side channel when stationary light remove circuit and I/V transform AMP is not saturated.

APPLICATION EXAMPLE



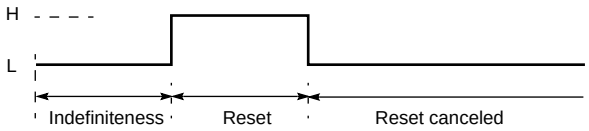
CONTROLS

(1) STB

This terminal enables IC to operate. IC is Standby at HIGH in this terminal. IC can operate at LOW in this terminal.

(2) RESET

This terminal resets the whole IC including a logic. This terminal resets IC at HIGH. This terminal cancel resetting IC at the edge from HIGH to LOW. IC includes power on reset function. The control from external is also possible. The reset term in IC takes OR between power on reset and control signal from external.



While this terminal is HIGH,dielectric divide pole countermeasures circuit of integration condenser is active.

(3) CLALV

This terminal sets up clamp level.

As including D/A of 4bit,16way clamp level setting is possible by inputting clock after reset is canceled(include none clamp).

Set up current value of each bit is on the right table.

The number of input clock and set up clamp level is as follows.

Bit	Set up current (Typ.)
1	0.125 nA
2	o.25 nA
3	0.5 nA
4	1.0 nA

Clock value	Clamp level(Typ.)
0	None clamp
1	0.125 nA
2	0.250 nA
3	0.375 nA
4	0.500 nA
5	0.625 nA
6	0.750 nA
7	0.875 nA
8	1.000 nA
9	1.125 nA
10	1.250 nA
11	1.375 nA

Clock value	Clamp level(Typ.)
12	1.500 nA
13	1.625 nA
14	1.750 nA
15	1.875 nA
16	None clamp
17	0.125 nA
18	0.250 nA
19	0.375 nA
20	0.500 nA

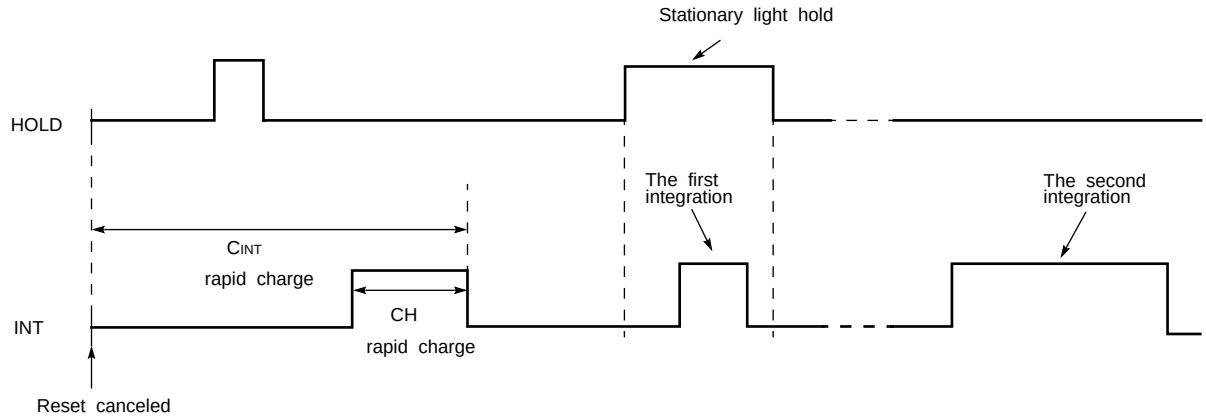
Clamp level is established with fall edge of input clock.

It repeats the same value after 16 clock.

(4) HOLD, INT

These terminals implement the following controls by inputting HIGH/LOW.

a. CINT rapid charge ON, OFF
b. CH rapid charge ON, OFF
c. Stationary light hold ON, OFF
d. The first integration ON, OFF
e. The second integration ON, OFF



a. CINT rapid charge

After reset is canceled, the capacity of CINT is charged rapidly until INT terminal first falls.

b. CH rapid charge

After reset is canceled, the capacity of CH is charged rapidly until INT terminal first rises and falls.

c. Stationary light hold

After reset is canceled, holds the stationary light while HOLD terminal is HIGH.

d. The first integration

After reset is canceled, as HOLD terminal is HIGH and INT terminal is HIGH, the first integration is implemented while INT terminal is HIGH. Therefore,the first integration must be finished(INT terminal from HIGH to LOW) until stationary light hold will be completed (HOLD terminal from HIGH to LOW)

e. The second integration

After reset is canceled, the second integration is implemented as HOLD terminal is LOW and INT terminal is HIGH. And,the second integration is completed by exceeding judgement level of CINT terminal although INT terminal is HIGH.

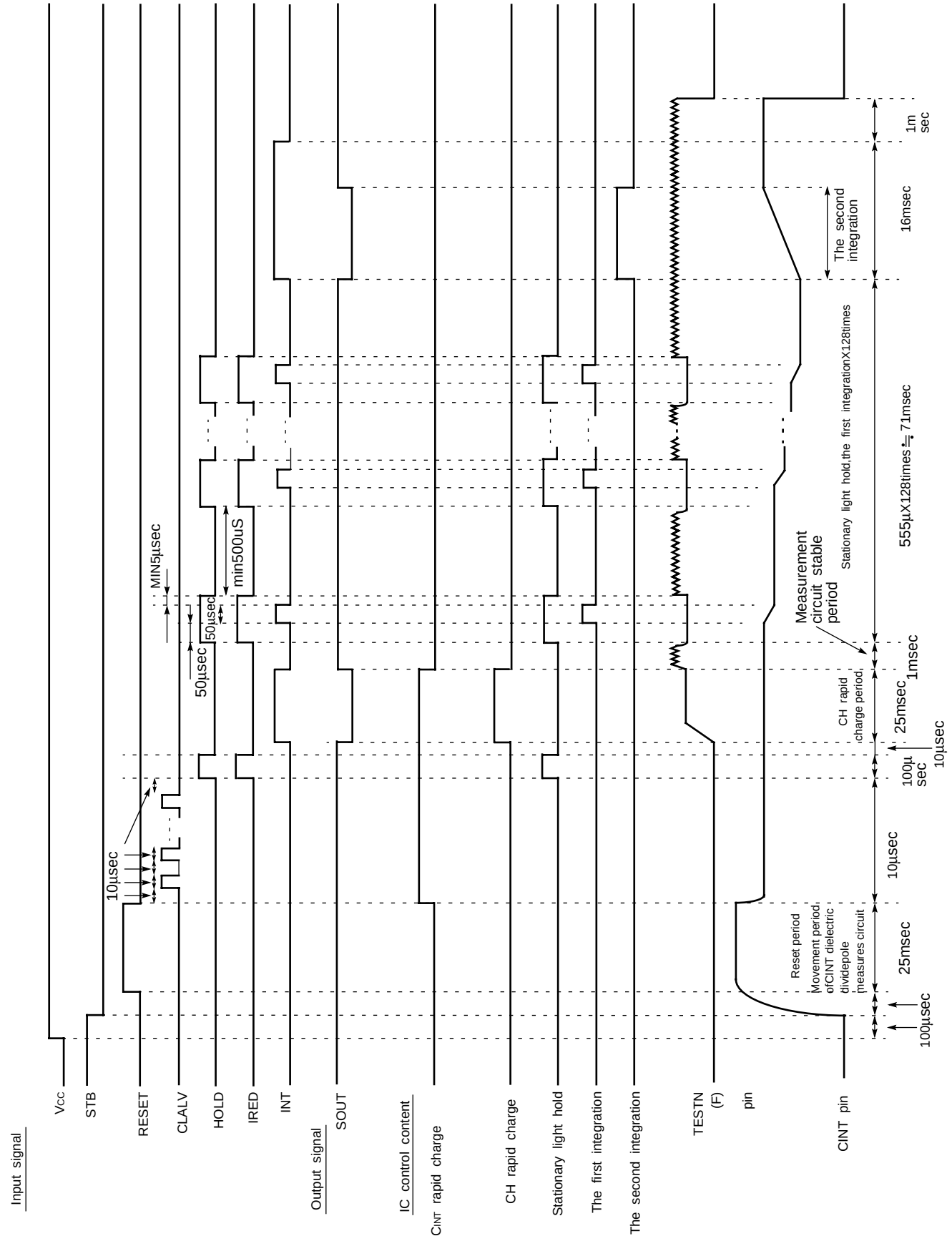
(5) SOUT

When the second integration starts,This terminal becomes from HIGH to LOW. If CINT terminal exceeds judge level or INT terminal becomes from HIGH to LOW, this terminal becomes from LOW to HIGH.

(notice) As the signal from microcomputer,the signal that controls IRED ON/OFF is required except for above mentioned control signals. But applying the timing of HOLD is available.

DISTANCE DETECTION SIGNAL PROCESSING FOR 3V SUPPLY VOLTAGE

SEQUENTIAL TIME CHART EXAMPLE



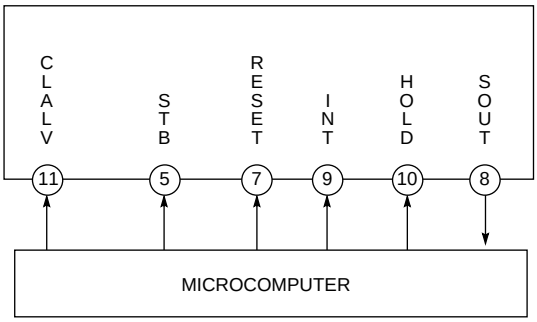
MASK OPTION

(1) The second integration current value can be doubled.

(2.5μ⟶5.0μA)

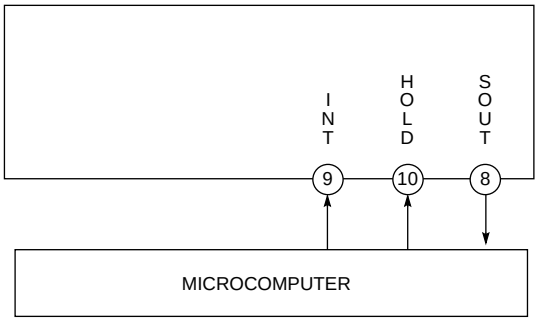
(2) Control terminal variation

① Full spec (typical)



This type uses CLALV, STB, RESET, INT, HOLD, SOUT terminal as I/F terminal to the microcomputer.
This is the typical type at M52957FP.

② Most simplified type



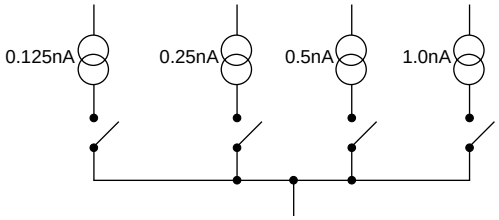
This type does not connect CLALV, STB, RESET terminals to the microcomputer.
When above mentioned terminals are not connected to the microcomputer without changing mask,connect each terminal to the ground. In this case,clamp level becomes 0 and standby function is lost. Power on reset in IC is used as reset.

③ Explanation of the terminal that can be simplified.

(a) CLALV

In the typical type,16way clamp levels can be set by the external control,but also the terminal can be simplified by mask option as follows.

1. Clamp level fixation
   Selects 1 point from 16 steps of clamp level and fixes it.
2. Clamp level 2 step changeover
   Selects 2 points from clamp level and switches it by changing CLALV terminal HIGH/LOW. However,as selecting 2 points, there is a following constraint.



Fixes 3 parts of 4 switches correspond to each bit in figure to ON or OFF,controls another part by CLALV terminal .

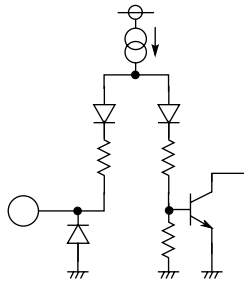
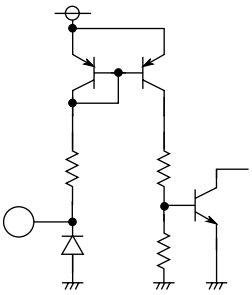
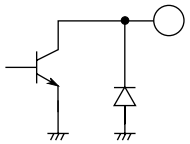
(b) STB

When no standby function required such as V_{CC} is switched ON/OFF,STB terminal can be eliminated.

(c) RESET

Since IC include power on reset circuit,RESET terminal can be eliminated. As merit of controlling RESET terminal from outside,distance detection time can be shortened because there is no need to switch V_{CC} or STB Terminal ON /OFF at consecutive distance detection.

DESCRIPTION OF PIN

Name	Peripheral circuit of pins	Parameter	Limits			Unit	Test conditions and note
			Min.	Typ.	Max.		
HOLD INT CLALV RESET		"H" input voltage	1.1	-	7.0	V	
		"L" input voltage	-	-	0.3		
		"H" input current	-	-	1.0	μA	V_{IH}=5.5V
		"L" input current	-100	-75	-50		V_{IL}=0V
STB		"H" input voltage	V_{CC} -0.3	-	7.0	V	
		"H" input voltage	-	-	0.3		
		"H" input current	-	-	3.0	μA	V_{IH}=5.5V
		"L" input current	-150	-100	-50		V_{IL}=0V
SOUT		"L" output voltage	-	-	0.3	V	I_{OL}=500μA
		"H" leak current	-	-	1.0	μA	V_{IN}=5.5V