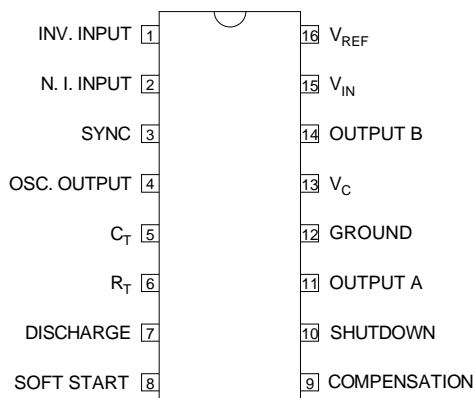


TOP VIEW



J Package – 16 Pin Ceramic DIP
N Package – 16 Pin Plastic DIP
D Package – 16 Pin Plastic (300) SOIC

**REGULATING
PULSE WIDTH
MODULATORS**

FEATURES

- 8 to 35V operation
- 5.1V reference trimmed to $\pm 1\%$
- 100Hz to 500kHz oscillator range
- Separate oscillator sync terminal
- Adjustable deadtime control
- Internal soft start
- Input undervoltage lockout
- Latching PWM to prevent multiple pulses
- Dual source/sink output drivers

Order Information

Part Number	J-Pack 16 Pin	N-Pack 16 Pin	D-16 16 Pin	Temp. Range	Note: To order, add the package identifier to the part number. eg. IP1525AJ IP3527AD-16
IP1525A	✓			-55 to +125°C	
IP1527A	✓			-55 to +125°C	
IP3525A	✓	✓	✓	0 to +70°C	
IP3527A	✓	✓	✓	0 to +70°C	

ABSOLUTE MAXIMUM RATINGS ($T_{case} = 25^{\circ}C$ unless otherwise stated)

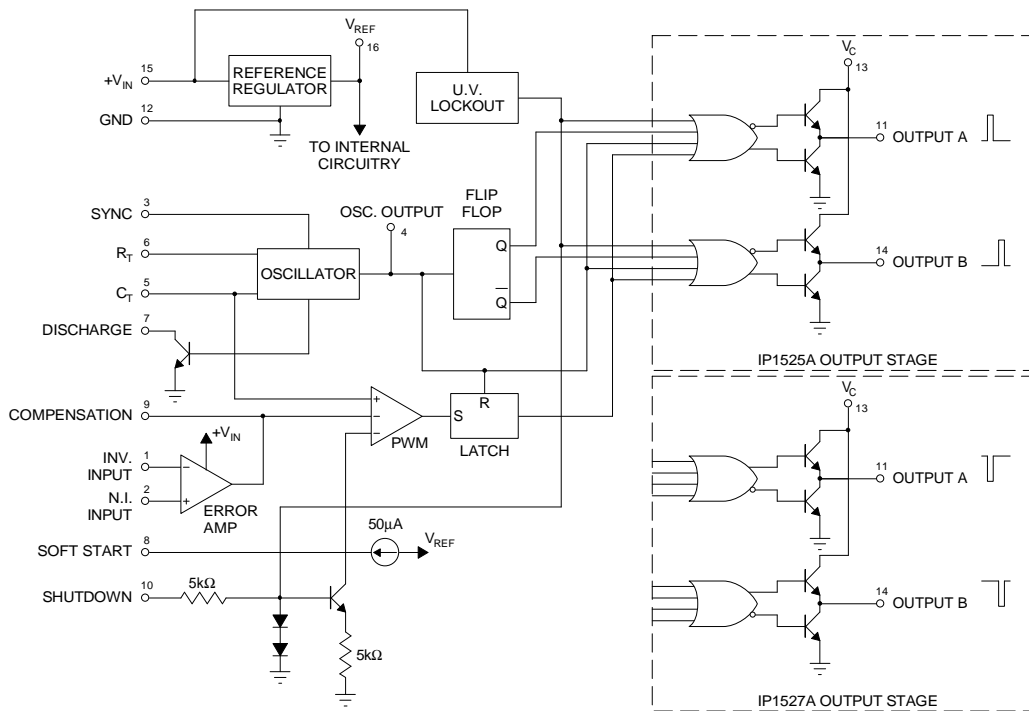
$+V_{IN}$	Input Voltage		+40V
	Collector Voltage		+40V
	Logic Inputs		-0.3 to +5.5V
	Analogue Inputs		-0.3 to $+V_{IN}$
	Output Current, Source or Sink		500mA
	Reference Output Load Current		Internally Limited
	Oscillator Charging Current		5mA
P_D	Power Dissipation	$T_A = 25^{\circ}C$ Derate @ $T_A > 50^{\circ}C$	1W 10mW/ $^{\circ}C$
P_D	Power Dissipation	$T_C = 25^{\circ}C$ Derate @ $T_C > 25^{\circ}C$	2W 16mW/ $^{\circ}C$
T_J	Operating Junction Temperature		See Ordering Information
T_{STG}	Storage Temperature Range		-65 to +150°C
T_L	Lead Temperature (soldering, 10 seconds)		+300°C

DESCRIPTION

The IP1525A and IP1527A families of PWM switching regulator control circuits offer improved performance and lower parts count when used in designing switching power supplies. Included are 5.1 volt reference, error amplifier, adjustable dead-time oscillator with synchronisation capability, latched PWM comparator, totem-pole output drivers, shutdown, soft start, and undervoltage lockout.

The IP1525A and IP1527A differ only in output phasing. The IP1525A output is low when “off”, while the IP1527A output is high when “off”.

BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

V_{IN}	Input Voltage	+8 to +35V
	Collector Voltage	+4.5 to +35V
	Sink/Source Load Current (Steady State)	0 to 100mA
	Sink/Source Load Current (Peak)	0 to 400mA
	Reference Load Current	0 to 20mA
	Oscillator Frequency Range	100Hz to 400kHz
R_T	Oscillator Timing Resistor	2k Ω to 200k Ω
C_T	Oscillator Timing Capacitor	470pF to 0.1 μ F
	Deadtime Resistor Range	0 to 500 Ω
	Operating Ambient Temperature Range	IP1525A / IP1527A IP3525A / IP3527A
		-55 to +125°C 0 to +70°C

ELECTRICAL CHARACTERISTICS (T_J = Over Operating Temperature Range unless otherwise stated)

Parameter	Test Conditions	IP1525A IP1527A			IP3525A IP3527A			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
REFERENCE SECTION								
Output Voltage	$T_J = 25^\circ\text{C}$	5.05	5.10	5.15	5.0	5.1	5.2	V
Line Regulation	$V_{IN} = 8$ to 35V		2	10		2	20	mV
Load Regulation	$I_L = 0$ to 20mA		5	50		5	50	
Temperature Stability			20	50		20	50	mV
Total Output Variation	Over Line, Load and Temp.	5.0		5.2	4.95		5.25	V
Short Circuit Current	$V_{REF} = 0$		80	100		80	100	mA
Output Noise Voltage	$f = 10$ Hz to 10kHz		40	200		40	200	μVrms
Long Term Stability			1	10		1	50	$\frac{\text{mV}}{\text{kHr}}$
OSCILLATOR SECTION ²								
Initial Accuracy			2	6		2	6	%
Voltage Stability	$V_{IN} = 8$ to 35V		0.3	1		1	2	
Temperature Stability			3	6		3	6	
Minimum Frequency	$R_T = 200\text{k}\Omega$ $C_T = 0.1\mu\text{F}$		90	120		90	120	Hz
Maximum Frequency	$R_T = 2\text{k}\Omega$ $C_T = 470\text{pF}$	400	600		400	600		kHz
Current Mirror	$I_{RT} = 2\text{mA}$	1.7	2.0	2.2	1.7	2.0	2.2	mA
Clock Amplitude		3.0	3.5		3.0	3.5		V
Clock Width	$T_J = 25^\circ\text{C}$	0.3	0.5	1.0	0.3	0.5	1.0	μs
Sync Threshold		1.2	2.0	2.8	1.2	2.0	2.8	V
Sync Input Current	Sync Voltage = 3.5V		1.0	2.5		1.0	2.5	mA
ERROR AMPLIFIER SECTION ³								
Input Offset Voltage			0.5	5		2	10	mV
Input Bias Current			1	10		1	10	μA
Input Offset Current				1			1	
DC Open Loop Gain	$R_L \geq 10\text{M}\Omega$	60	75		60	75		dB
Gain Bandwidth Product	$T_J = 25^\circ\text{C}$	1	2		1	2		MHz

NOTES

- Test Conditions unless otherwise stated:
 $V_{IN} = 20\text{V}$
 $T_J = -55$ to $+125^\circ\text{C}$ for IP1525A / IP1527A
 $T_J = 0$ to $+70^\circ\text{C}$ for IP3525A / IP3527A
- Oscillator Section Test Conditions:
 $f_{OSC} = 40\text{kHz}$ ($R_T = 3.6\text{k}\Omega$, $C_T = 0.01\mu\text{F}$, $R_D = 0$)
- Error Amplifier Section Test Condition:
 $V_{CM} = 5.1\text{V}$
- Output Driver Section Test Condition:
 $V_C = 20\text{V}$

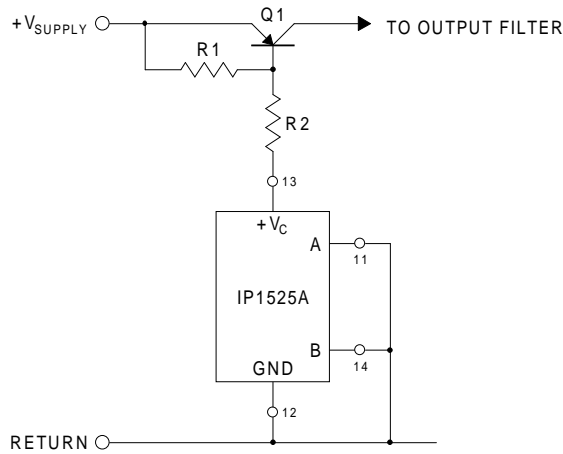
ELECTRICAL CHARACTERISTICS (T_J = Over Operating Temperature Range unless otherwise stated)

Parameter	Test Conditions	IP1525A IP1527A			IP3525A IP3527A			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
ERROR AMPLIFIER SECTION (cont.)³								
Output Low Level			0.2	0.5		0.2	0.5	V
Output High Level		3.8	5.6		3.8	5.6		
Common Mode Rejection	$V_{CM} = 1.5$ to $5.2V$	60	75		60	75		dB
Supply Voltage Rejection	$V_{IN} = 8$ to $35V$	50	60		50	60		
PWM COMPARATOR								
Minimum Duty Cycle	$V_{PIN1} - V_{PIN2} \geq 150mV$			0			0	%
Maximum Duty Cycle	$V_{PIN2} - V_{PIN1} \geq 150mV$	45	49		45	49		
Input Threshold	Zero Duty Cycle	0.6	0.9		0.6	0.9		V
Input Threshold	Max. Duty Cycle		3.3	3.6		3.3	3.6	
Input Bias Current			0.05	1.0		0.05	1.0	μA
SHUTDOWN SECTION								
Soft Start Current	$V_{SHUTDOWN} = 0V$	25	50	80	25	50	80	μA
Soft Start Low Level	$V_{SHUTDOWN} = 2V$		0.4	0.6		0.4	0.6	V
Shutdown Threshold	To Outputs	0.6	1.3	2.0	0.6	1.3	2.0	
Shutdown Input Current	$V_{SHUTDOWN} = 2.5V$		0.1	1.0		0.1	1.0	mA
Shutdown Delay	$V_{SHUTDOWN} = 2.5V$ $T_J = 25^\circ C$		0.2	0.5		0.2	0.5	μs
OUTPUT DRIVERS (each output)⁴								
Output Low Level	$I_{SINK} = 20mA$		0.2	0.4		0.2	0.4	V
	$I_{SINK} = 100mA$		1.0	2.0		1.0	2.0	
Output High Level	$I_{SOURCE} = 20mA$	18	19		18	19		V
	$I_{SOURCE} = 100mA$	17	18		17	18		
Undervoltage Lockout	$V_{COMP} = High$	5	7	8	5	7	8	V
Output Leakage	$V_C = 35V$			200			200	μA
Rise Time	$C_L = 1nF$ $T_J = 25^\circ C$		100	600		100	600	ns
Fall Time	$C_L = 1nF$ $T_J = 25^\circ C$		50	300		50	300	
TOTAL STANDBY CURRENT								
Supply Current	$V_{IN} = 35V$		10	20		10	20	mA

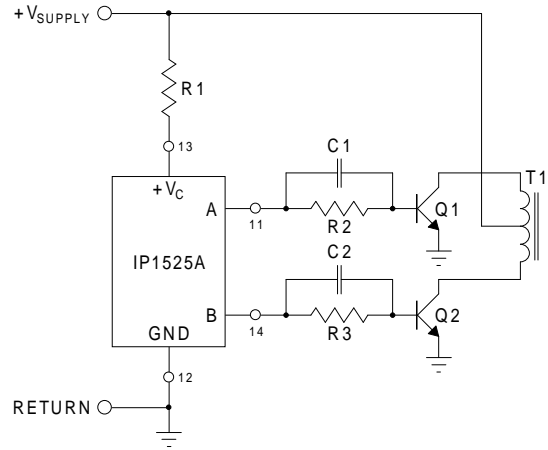
NOTES

- Test Conditions unless otherwise stated:
 $V_{IN} = 20V$
 $T_J = -55$ to $+125^\circ C$ for IP1525A / IP1527A
 $T_J = 0$ to $+70^\circ C$ for IP3525A / IP3527A
- Oscillator Section Test Conditions:
 $f_{OSC} = 40kHz$ ($R_T = 3.6k\Omega$, $C_T = 0.01\mu F$, $R_D = 0$)
- Error Amplifier Section Test Condition:
 $V_{CM} = 5.1V$
- Output Driver Section Test Condition:
 $V_C = 20V$

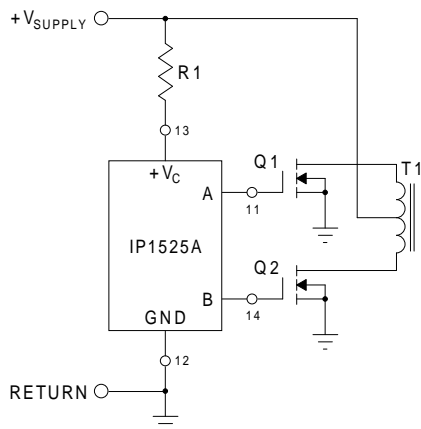
APPLICATIONS INFORMATION



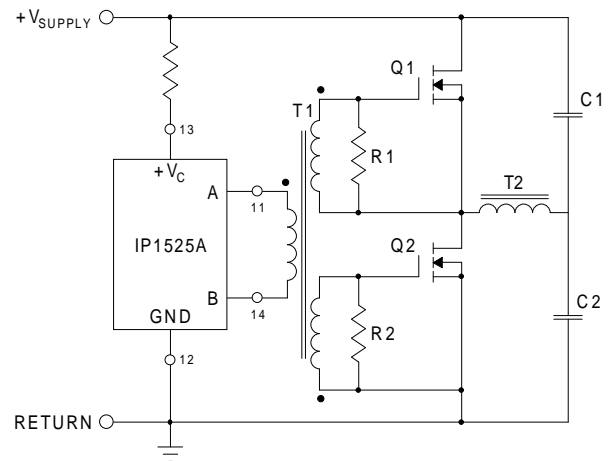
For single-ended supplies, the driver outputs are grounded. The V_C terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycle.



In conventional push-pull bipolar designs, forward base drive is controlled by R1-R3. Rapid turn-off times for the power devices are achieved with speed-up capacitors C1 and C2.



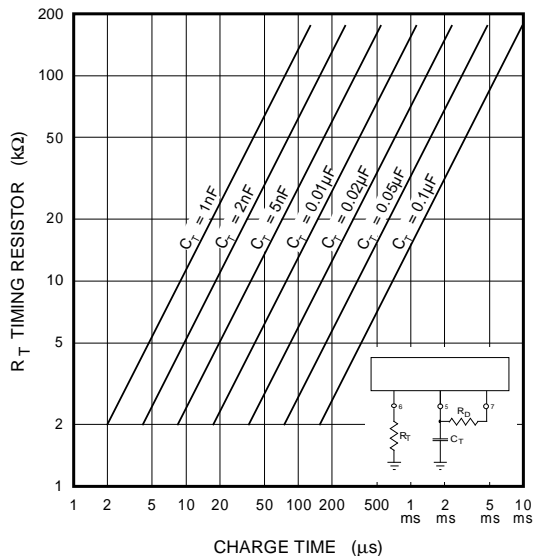
The low source impedance of the output drivers provides rapid charging of power FET input capacitance while minimizing external components.



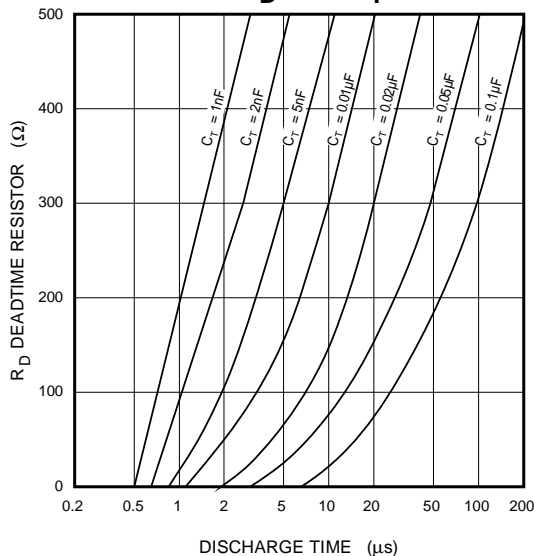
Low power transformers can be driven directly by the IP1525A. Automatic reset occurs during deadtime when both ends of the primary winding are switched to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

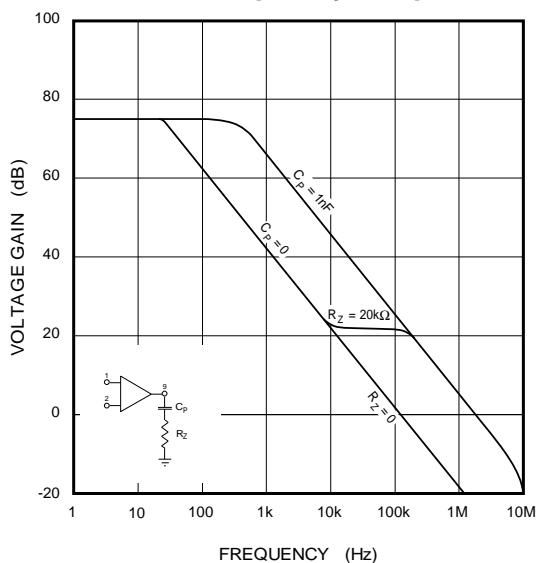
Oscillator Charge Time vs R_T and C_T



Oscillator Discharge Time vs. R_D and C_T



Error Amplifier Open-Loop Frequency Response



IP1525A Output Saturation Characteristics

