HOLT INTEGRATED CIRCUITS INC.

HI-6010

ARINC 429 TRANSMITTER/RECEIVER FOR 8 BIT BUS

GENERAL DESCRIPTION

The HI-6010 is a CMOS integrated circuit designed to interface the avionics data bus standard ARINC 429 to an 8 bit port. It contains one receiver and one transmitter. They operate independently except for the self test option and the parity option. The receiver demands that the incoming data meet the standard protocol and the transmitter outputs a standard protocol stream.

The HI-6010 provides flexible options for interfacing to the user system. The controlling processor can operate both the receiver and transmitter either by using hard wired flags and gates at the pins or by using software reads and writes of the Status Register and Control Register or a combination thereof.

The chip is programmable to operate with single 8 bit bytes requiring "on the fly transmitter loading and receiver downloading" or to operate in 32 bit "extended buffer" mode. In addition there is an option to use automatic label recognition after loading 8 possible labels for comparison. Parity and self test are also software programmable. Master Reset is activated only by taking the MR pin high.

Two clock inputs allow independent selection of the data rates of the transmitter and receiver. Each must be 4X the desired ARINC 429 frequency.

Error flags are generated for transmitter underwrites and for receiver data framing miscues, parity errors, and buffer overwrites.

The HI-6010 is a 5 volt chip that will require data translation from and to the ARINC bus. The HI-8482 and HI-8588 line receivers are available for the receiver side and the HI-318X, HI-838X and HI-858X line drivers are available for the transmitter side. The HI-8590 is also available with a line driver and a line receiver in a single 16-pin thermally enhanced ESOIC package.

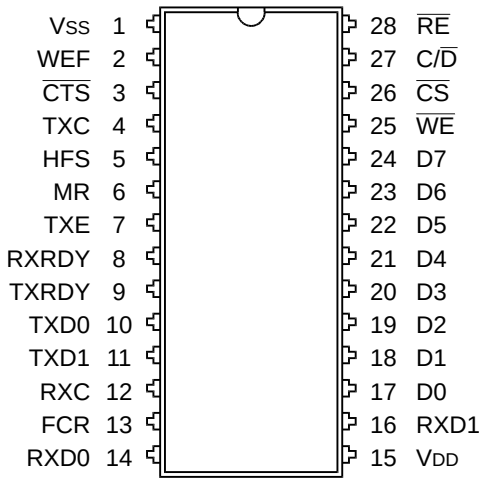
APPLICATIONS

- Avionics Data Communication
- Serial to Parallel Conversion
- Parallel to Serial Conversion

FEATURES

- ARINC 429 protocol controller with interface to an 8 bit bus
- Automatic label recognition option
- 8 bit or 32 bit buffering option
- Self test and parity options
- CMOS / TTL logic pins
- Plastic and ceramic package options - surface mount or DIP
- Military processing available

PIN CONFIGURATION (Top View)



Pin numbers apply for plastic and ceramic DIP and for plastic PLCC. Consult factory for pin out of 48 lead ceramic leadless chip carrier.

OPERATING SUPPLY VOLTAGE

- VDD = 5.0 VOLTS ±5%
- VSS = 0.0 VOLTS

PIN DESCRIPTIONS

PIN	SYMBOL	FUNCTION	DESCRIPTION
1	V_{SS}	POWER	0.0 Volts
2	WEF	OUTPUT	Error indication if high. Status register must be read to determine specific error.
3	$\overline{CTS}$	INPUT	Enables data transmission when low.
4	TXC	INPUT	Source clock for data transmission. 4 times bit rate.
5	HFS	INPUT	Hardware feature select.
6	MR	INPUT	Master reset, active high.
7	TXE	OUTPUT	Low when transmission in progress.
8	RXRDY	OUTPUT	High when data of received word is available.
9	TXRDY	OUTPUT	High when data of a transmitted word may be input.
10	TXD0	OUTPUT	"Zeroes" data output of transmitter.
11	TXD1	OUTPUT	"Ones" data output of transmitter.
12	RXC	INPUT	Source clock for data reception. 4 times bit rate.
13	FCR	OUTPUT	First character received flag.
14	RXD0	INPUT	"Zeroes" data input to receiver.
15	V_{DD}	POWER	5 Volts ±5%
16	RXD1	INPUT	"Ones" data input to receiver.
17	D0	I / O	Data bus
18	D1	I / O	Data bus
19	D2	I / O	Data bus
20	D3	I / O	Data bus
21	D4	I / O	Data bus
22	D5	I / O	Data bus
23	D6	I / O	Data bus
24	D7	I / O	Data bus
25	$\overline{WE}$	INPUT	8 bit data bus input control active low.
26	$\overline{CS}$	INPUT	Chip select, active low.
27	C/$\overline{D}$	INPUT	High for control or status register operations, low for data
28	$\overline{RE}$	INPUT	8 bit data bus output control, active low.

USING THE RECEIVER

The receiver logic is independent of the transmitter except in the following ways:

1. Self Test
2. Parity Option

In self test, the transmitter outputs route to the receiver inputs internally ignoring the external inputs. Also in self test, the external receiver clock is replaced with the transmitter clock.

The parity option affects both the receiver and transmitter. Either both are operational or neither.

HARDWARE CONTROL OF THE RECEIVER

PIN 2 - WEF

WEF is an error indicator. It goes high for a transmitter "underwrite" (failure to keep up with byte loading) and pin 2 goes high for any one of three receiver errors. The status register will show which of the three errors occurred:

Status Register Bit	Error
SR3	Received a parity error
SR4	Data Overwritten
SR5	Receiving sequence error

The possible Receiver sequence errors are:

1. RXD0 and RXD1 simultaneously a one.
2. Less than 32 bits before 3 nulls.
3. More than 32 bits.

There are no errors flagged for labels received that don't match stored labels when in the label recognition mode. Errors are cleared by MR or by reading the Status Register.

PIN 5 - HFS and the CONTROL REGISTER

This pin, along with the control register, sets up the functioning (e.g. modes) of the chip. If HFS is low, the

USING THE RECEIVER (con't)

receiver is not programmable to the 32 bit "extended buffer" mode nor to the label recognition mode. Affecting the receiver:

CONTROL BIT NAME	PROGRAM VALUE	PIN 5 VALUE	OPERATION
CR1	X 0 1	0 1 1	No action No action Next 8 data read cycles will read stored labels. One time only sequence on each transiton of CR1 to a 1.
CR2	0 1	X X	Receiver is disabled Receiver is enabled
CR3*	0 1	X X	RXRDY goes high normally Blocks RXRDY for one ARINC word
CR4	0 1	X X	Self test disabled Self test enabled
CR5	0 1 0 1	0 0 1 1	No parity errors enabled and 32nd bit is data Parity error flag enabled 32 bit "extended mode" enabled and parity enabled. 8 bit "one byte at a time" mode and parity enabled.
CR7	X 0 1	0 1 1	Label recognition not programmable Label recognition disabled Label recognition enabled

* CR3 will be automatically reset to 0 after being programmed to a 1 at the completion of an ARINC word reception. This allows a software label recognition different from the automatic option available.

PIN 6 - MR

When MR is a 1, the control word is set to 0X10 0101 (CR7 - CR0). For the receiver this sets up 8 bit mode with the receiver and parity enabled. MR also initializes the registers and logic. The first ARINC reception will only occur **after** a word gap.

PIN 8 - RXRDY

In 8 bit mode, this pin goes high whenever 8 bits are received without error. In 32 bit mode this pin goes high after all 32 bits are received with no error. This flag may be inhibited for one ARINC word if CR3 is programmed to 1. This flag is also inhibited in label recognition if the incoming ARINC label does notmatch one of the stored 8 labels.

PIN 12 - RXC

This pin must have a clock applied that is 4X the desired receive frequency.

PIN 13 - FCR

In 8 bit mode, this pin flags the first character (byte) received. In 32 bit mode, this pin goes high for a valid 32 bit word. The pin is not affected by CR3 programming.

PIN 14 - RXD0 and PIN 16 - RXD1

These pins must be 5 volt logic levels. There must be a translator between the ARINC bus and these inputs. Typically a receiver chip, such as the HI-8482 or HI-8588 is inserted between the ARINC bus and the logic chips. RXD0 is looking for a high level for zero inputs and RXD1 is looking for a high level for one inputs. When both inputs are low this is referred to as the Null state.

SOFTWARE CONTROL OF THE RECEIVER

By writing to the Control Register and reading the Status Register the controlling processor can operate the receiver without hardware interrupts. The Control Register in combination with the wiring of pin 5 was explained above. The Status Register bits pertaining to the receiver are explained below:

STATUS BIT	VALUE	MEANING
SR1	0 1	No receiver data Receiver data ready
SR3	0 1	No parity error Parity error - Parity was even
SR4	0 1	Receiver data not overwritten Receiver data was overwritten
SR5	0 1	Receiver data received without framing error Framing error - Did not receive exactly 32 good bits
SR6	0 1	Did not receive first byte Received first byte - Same flag as pin 13

COMMUNICATING WITH THE CONTROL AND STATUS REGISTERS

Pin 27, C/$\overline{D}$, must be high to read the status register or write the control register. Reading the status register resets errors. There is no provision to read the control register.

LABEL RECOGNITION OPTION

Pin 5 must be high if label recognition is selected in either the 8 or 32 bit modes and all eight label buffers must be written using redundant labels, if necessary.

The chip compares the incoming label to the stored labels. If a match is found, the data is processed. If a match is not found, no indicators of receiving ARINC data are presented.

LOADING LABELS

After the write that changes CR7 from 0 to 1, the next 8 writes of data (C/$\overline{D}$ is a zero for data) will load the label registers. Labels must be loaded whenever pin 5 goes from low to high.

READING LABELS

After the write that changes CR1 from 0 to 1, the next 8 data reads are labels.

USING THE TRANSMITTER

The transmitter logic is independent of the receiver except in the following ways:

1. Self Test
2. Parity Option

In self test the transmitter outputs route to the receiver inputs internally and the TXD0 and TXD1 outputs are inhibited.

When parity is enabled, both the receiver and transmitter are affected. Odd parity is automatically generated in the 32nd bit if this option is selected.

HARDWARE CONTROL OF THE TRANSMITTER

PIN 2 - WEF

This output goes high for 1 transmitter error and 3 receiver errors. To determine which error is being flagged, read the Status Register. Reading the Status Register also clears the error flag. The transmitter will not function until the error is cleared. It can also be cleared by MR going high.

The only possible transmitter error is generated when running in 8 bit mode. For the transmitter this means loading the last 3 bytes while the transmission is in progress. Failure to load a byte before the previous byte's 8th bit is transmitted will generate the error, indicated by status bit SR7 set to a 1.

PIN 3 - $\overline{\text{CTS}}$

This pin is a hardware gate for transmissions. If the transmitter buffer is loaded and Control Register bit CR0 is a one, the only inhibit of the transmitter would be for $\overline{\text{CTS}}$ to be a one. When taken low, transmission of an ARINC word is enabled. It may be pulsed to release each transmitted word.

PIN 4 - TXC

The data rate of transmission is controlled by this pin. This clock must be 4X the desired date rate.

PIN 5 - HFS and the CONTROL REGISTER

This pin along with the Control Register sets the functioning of the chip. For the transmitter:

CONTROL BIT NAME	PROGRAM VALUE	PIN 5 VALUE	OPERATION
CR0	0	X	Transmitter is disabled
	1	X	Transmitter is enabled
CR4	0	X	Not in self test
	1	X	Self test enabled
CR5	0	0	8 bit mode + data in 32nd bit
	1	0	8 bit mode + parity enabled
	0	1	32 bit mode with parity enabled
	1	1	8 bit mode with parity enabled

PIN 6 - MR

The chip is initialized whenever this pin goes high. The Control Register is set to 0X10 0101 (CR7 - CR0). For the transmitter this sets up 8 bit mode with the transmitter enabled.

PIN 7 - TXE

Whenever a transmission begins, this pin goes low and returns high after the transmission is complete.

PIN 9 - TXRDY

Whenever TXRDY is a one, data may be written into the transmitter buffer. In 8 bit "one byte at a time" mode, this pin may bemonitored to indicate when to write the next 8 bits.

PIN 10 - TXD0 and PIN 11 - TXD1

TXD0 will go high during a transmission if the data is zero. TXD1 goes high if data is a one. When both pins are low this is referred to as the Null state. Typically an ARINC transmitter chip, such as the HI-8382, HI-8383, HI-8585 or HI-8586 is connected to these pins to translate the 5 volt levels to the proper ARINC bus levels.

SOFTWARE CONTROL OF THE TRANSMITTER

By writing into the Control Register and reading the Status Register, the controlling processor can operate the transmitter independent of the flags at the pins. Transmission can be initiated by changing CR0 from a 0 to a 1 after the transmitter buffer has been loaded. Then the Status Register may bemonitored as follows:

STATUS BIT	VALUE	MEANING
SR0	0	Do not load the transmitter buffer
	1	Ready to load the transmitter buffer
SR2	0	Transmission in progress
	1	Transmitter is idle
SR7	0	No transmission error
	1	8 bit mode only error for underwriting data

APPLICATIONS TIPS

Cabling Noise -The HI-6010 has TTL compatible inputs and therefore they are susceptible to noise near ground. If the data bus is passed by ribbon cable or the equivalent to the device under test, it is possible to get significant glitches on the Master Reset line. The problem will appear to be a pattern sensitive failure. One cure is simply to adequately bypass Master Reset. Another is to buffer the HI-6010 inputs near the chip.

Receiver Seems Dead - After Master Reset the HI-6010 receivermustseeawordgapbeforethefirstARINCdatabit.

Error flags must be cleared by either a Status Register Read or by a Master Reset. The operation of either the transmitter or the receiver is inhibited upon error.

8 BIT "ONE BYTE AT A TIME" TRANSMIT USING TXRDY, PIN 9, TO TRIGGER NEXT BYTE LOAD

PINS																			
$\overline{RE}$	C/$\overline{D}$	$\overline{CS}$	$\overline{WE}$	D7	D6	D5	D4	D3	D2	D1	D0	MR	HFS	$\overline{CTS}$	TXE	RXRDY	TXRDY	FCR	
28	27	26	25	24	23	22	21	20	19	18	17	6	5	3	7	8	9	13	COMMENTS
1	1	0	P	0	0	0*	0	0	0	0	1	0	0	X	1	X	1	X	Load Control Word
1	0	0	P	TD8	TD7	TD6	TD5	TD4	TD3	TD2	TD1	0	0	0	0	X	0	X	TXRDY & TXE Go Low After Load Data
1	0	0	1	X	X	X	X	X	X	X	X	0	0	0	0	X	1	X	Monitor Pin 9 to Go High
1	0	0	P	TD16	TD15	TD14	TD13	TD12	TD11	TD10	TD9	0	0	0	0	X	0	X	After Pin 9 High Then Load Next Byte
1	0	0	1	X	X	X	X	X	X	X	X	0	0	0	0	X	1	X	Monitor Pin 9 to Go High
1	0	0	P	TD24	TD23	TD22	TD21	TD20	TD19	TD18	TD17	0	0	0	0	X	0	X	Load
1	0	0	1	X	X	X	X	X	X	X	X	0	0	0	0	X	1	X	Monitor Pin 9 to Go High
1	0	0	P	TD32	TD31	TD30	TD29	TD28	TD27	TD26	TD25	0	0	0	0	X	0	X	Load
1	0	1	1	X	X	X	X	X	X	X	X	0	0	0	1	X	1	X	Transmission Complete

* With Pin 5 low, Control Register Bit 5 selects if the 32nd bit is either odd parity or data.
P = Pulse
X = Don't Care

8 BIT "ONE BYTE AT A TIME" TRANSMIT MONITORING STATUS REGISTER BIT 0

PINS																			
$\overline{RE}$	C/$\overline{D}$	$\overline{CS}$	$\overline{WE}$	D7	D6	D5	D4	D3	D2	D1	D0	MR	HFS	$\overline{CTS}$	TXE	RXRDY	TXRDY	FCR	
28	27	26	25	24	23	22	21	20	19	18	17	6	5	3	7	8	9	13	COMMENTS
1	1	0	P	0	0	0*	0	0	0	0	1	0	0	0	1	X	1	X	Load Control Word D0 = 1
1	0	0	P	TD8	TD7	TD6	TD5	TD4	TD3	TD2	TD1	0	0	0	0	X	0	X	Load Data to Transmit - Byte 1
P	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	X	0	X	Status Bits 0, 2 & 7 (TXRDY, TXE & ERROR)
P	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	X	1	X	Status Bit 0 Goes High
1	0	0	P	TD16	TD15	TD14	TD13	TD12	TD11	TD10	TD9	0	0	0	0	X	0	X	Load the Next Byte to Transmit
P	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	X	0	X	Monitor Status Bit 0
P	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	X	1	X	Detect a Transition
1	0	0	P	TD24	TD23	TD22	TD21	TD20	TD19	TD18	TD17	0	0	0	0	X	0	X	Load 3rd Byte
P	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	X	0	X	Monitor Status Bit 0
P	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	X	1	X	Detect a Transition
1	0	0	P	TD32	TD31	TD30	TD29	TD28	TD27	TD26	TD25	0	0	0	0	X	0	X	Load 4th Byte

* With Pin 5 low, Control Register Bit 5 selects if the 32nd bit is either odd parity or data.
P = Pulse
X = Don't Care

RECEIVING 32 BIT WORDS HARDWARE INTERRUPT

PINS																		COMMENTS
$\overline{RE}$	C/$\overline{D}$	$\overline{CS}$	$\overline{WE}$	D7	D6	D5	D4	D3	D2	D1	D0	MR	HFS	$\overline{CTS}$	TXE	RXRDY	TXRDY	FCR	
28	27	26	25	24	23	22	21	20	19	18	17	6	5	3	7	8	9	13	
1	1	0	P	0	0	0	0	0	1	0	0	0	1	X	X	0	X	0	Write CR: 32 Bit Recieve & No Label Recogn.
1	1	0	1	X	X	X	X	X	X	X	X	0	1	X	X	1	X	1	Await Pin 8 or Pin 13 to Go High
P	0	0	1	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	0	1	X	X	1	X	1	Read 1st Byte
P	0	0	1	RD16	RD15	RD14	RD13	RD12	RD11	RD10	RD9	0	1	X	X	1	X	1	Read 2nd Byte
P	0	0	1	RD24	RD23	RD22	RD21	RD20	RD19	RD18	RD17	0	1	X	X	1	X	1	Read 3rd Byte
P	0	0	1	PAR	RD31	RD30	RD29	RD28	RD27	RD26	RD25	0	1	X	X	1	X	1	Read 4th Byte
1	0	0	1	X	X	X	X	X	X	X	X	0	1	X	X	0	X	0	

P = Pulse
X = Don't Care

RECEIVING 8 BIT MODE SOFTWARE INTERRUPT

PINS																		COMMENTS
$\overline{RE}$	C/$\overline{D}$	$\overline{CS}$	$\overline{WE}$	D7	D6	D5	D4	D3	D2	D1	D0	MR	HFS	$\overline{CTS}$	TXE	RXRDY	TXRDY	FCR	
28	27	26	25	24	23	22	21	20	19	18	17	6	5	3	7	8	9	13	
1	1	0	P	0	0	1	0	0	1	0	0	0	1	X	X	0	X	0	Write CR: 8 Bit Receive & Not Label Recong.
P	1	0	1	0	0	0	0	0	X	0	0	0	1	X	X	0	X	0	Monitor the Status Register
P	1	0	1	0	1	0	0	0	X	1	0	0	1	X	X	1	X	1	SR 1 & SR 6 Go High - First Character
P	0	0	1	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	0	1	X	X	0	X	0	Read 1st Byte
P	1	0	1	0	0	0	0	0	X	0	0	0	1	X	X	0	X	0	Look for SR 1 to Go High Again
P	1	0	1	0	0	0	0	0	X	1	0	0	1	X	X	1	X	0	
P	0	0	1	RD16	RD15	RD14	RD13	RD12	RD11	RD10	RD9	0	1	X	X	0	X	0	Read 2nd Byte
P	1	0	1	0	0	0	0	0	X	0	0	0	1	X	X	0	X	0	Look for SR 1 to Go High Again
P	1	0	1	0	0	0	0	0	X	1	0	0	1	X	X	1	X	0	
P	0	0	1	RD24	RD23	RD22	RD21	RD20	RD19	RD18	RD17	0	1	X	X	0	X	0	Read 3rd Byte
P	1	0	1	0	0	0	0	0	X	0	0	0	1	X	X	0	X	0	Look for SR 1 to Go High Again
P	1	0	1	0	0	0	0	0	X	1	0	0	1	X	X	1	X	0	
P	0	0	1	PAR	RD31	RD30	RD29	RD28	RD27	RD26	RD25	0	1	X	X	0	X	0	Read 4th Byte

P = Pulse
X = Don't Care

TRANSMIT IN 32 BIT MODE (EXTENDED BUFFER) USING $\overline{CTS}$ TO INITIATE

PINS																			
$\overline{RE}$	C/$\overline{D}$	$\overline{CS}$	$\overline{WE}$	D7	D6	D5	D4	D3	D2	D1	D0	MR	HFS	$\overline{CTS}$	TXE	RXRDY	TXRDY	FCR	
28	27	26	25	24	23	22	21	20	19	18	17	6	5	3	7	8	9	13	COMMENTS
1	1	0	P	0	0	0	0	0	0	0	1	0	1	1	1	X	1	X	Load Control Word D5 = 0 & D0 = 1
1	0	0	P	TD8	TD7	TD6	TD5	TD4	TD3	TD2	TD1	0	1	1	1	X	0	X	Load Data to Transmit - Byte 1
1	0	0	P	TD16	TD15	TD14	TD13	TD12	TD11	TD10	TD9	0	1	1	1	X	0	X	Load Data to Transmit - Byte 2
1	0	0	P	TD24	TD23	TD22	TD21	TD20	TD19	TD18	TD17	0	1	1	1	X	0	X	Load Data to Transmit - Byte 3
1	0	0	P	X	TD31	TD30	TD29	TD28	TD27	TD26	TD25	0	1	1	1	X	1	X	Load Data to Transmit - Byte 4
1	1	1	1	X	X	X	X	X	X	X	X	0	1	0	1	X	1	X	Take $\overline{CTS}$ Low to Start Transmitting 32nd Bit Will Be Parity

P = Pulse
X = Don't Care

TRANSMIT IN 32 BIT MODE (EXTENDED BUFFER) USING SOFTWARE WRITE TO CONTROL REGISTER

PINS																			
$\overline{RE}$	C/$\overline{D}$	$\overline{CS}$	$\overline{WE}$	D7	D6	D5	D4	D3	D2	D1	D0	MR	HFS	$\overline{CTS}$	TXE	RXRDY	TXRDY	FCR	
28	27	26	25	24	23	22	21	20	19	18	17	6	5	3	7	8	9	13	COMMENTS
1	1	0	P	0	0	0	0	0	0	0	0	0	1	0	1	X	1	X	Load Control Word D5 = 0 & D0 = 0
1	0	0	P	TD8	TD7	TD6	TD5	TD4	TD3	TD2	TD1	0	1	0	1	X	0	X	Load Data to Transmit - Byte 1
1	0	0	P	TD16	TD15	TD14	TD13	TD12	TD11	TD10	TD9	0	1	0	1	X	0	X	Load Data to Transmit - Byte 2
1	0	0	P	TD24	TD23	TD22	TD21	TD20	TD19	TD18	TD17	0	1	0	1	X	0	X	Load Data to Transmit - Byte 3
1	0	0	P	X	TD31	TD30	TD29	TD28	TD27	TD26	TD25	0	1	0	1	X	1	X	Load Data to Transmit - Byte 4
1	1	0	P	0	0	0	0	0	0	0	1	0	1	0	0	X	1	X	Write Control Word D0 = 1 32nd Bit Will Be Parity

P = Pulse
X = Don't Care

LOADING LABELS

PINS																		COMMENTS
$\overline{RE}$	C/$\overline{D}$	$\overline{CS}$	$\overline{WE}$	D7	D6	D5	D4	D3	D2	D1	D0	MR	HFS	$\overline{CTS}$	TXE	RXRDY	TXRDY	FCR	
28	27	26	25	24	23	22	21	20	19	18	17	6	5	3	7	8	9	13	
1	1	0	P	0	0	0	0	0	1	0	0	0	1	X	X	X	X	X	Control Bit 7 Must Be 0 First
1	1	0	P	1	0	0	0	0	1	0	0	0	1	X	X	X	X	X	Write 1 into Control Bit 7
1	0	0	P	1L7	1L6	1L5	1L4	1L3	1L2	1L1	1L0	0	1	X	X	X	X	X	Load the 1st Label
1	0	0	P	2L7	2L6	2L5	2L4	2L3	2L2	2L1	2L0	0	1	X	X	X	X	X	Load the 2nd Label
1	0	0	P	3L7	3L6	3L5	3L4	3L3	3L2	3L1	3L0	0	1	X	X	X	X	X	Load the 3rd Label
1	0	0	P	4L7	4L6	4L5	4L4	4L3	4L2	4L1	4L0	0	1	X	X	X	X	X	Load the 4th Label
1	0	0	P	5L7	5L6	5L5	5L4	5L3	5L2	5L1	5L0	0	1	X	X	X	X	X	Load the 5th Label
1	0	0	P	6L7	6L6	6L5	6L4	6L3	6L2	6L1	6L0	0	1	X	X	X	X	X	Load the 6th Label
1	0	0	P	7L7	7L6	7L5	7L4	7L3	7L2	7L1	7L0	0	1	X	X	X	X	X	Load the 7th Label
1	0	0	P	8L7	8L6	8L5	8L4	8L3	8L2	8L1	8L0	0	1	X	X	X	X	X	Load the 8th Label

P = Pulse
X = Don't Care

READING LABELS

PINS																		COMMENTS
$\overline{RE}$	C/$\overline{D}$	$\overline{CS}$	$\overline{WE}$	D7	D6	D5	D4	D3	D2	D1	D0	MR	HFS	$\overline{CTS}$	TXE	RXRDY	TXRDY	FCR	
28	27	26	25	24	23	22	21	20	19	18	17	6	5	3	7	8	9	13	
1	1	0	P	1	0	0	0	0	1	0	0	0	1	X	X	X	X	X	Make Sure Bit 1 of Control Word is 0
1	1	0	P	1	0	0	0	0	1	1	0	0	1	X	X	X	X	X	Write 1 into Control Bit 1
P	0	0	1	1L7	1L6	1L5	1L4	1L3	1L2	1L1	1L0	0	1	X	X	X	X	X	Read the 1st Label
P	0	0	1	2L7	2L6	2L5	2L4	2L3	2L2	2L1	2L0	0	1	X	X	X	X	X	Read the 2nd Label
P	0	0	1	3L7	3L6	3L5	3L4	3L3	3L2	3L1	3L0	0	1	X	X	X	X	X	Read the 3rd Label
P	0	0	1	4L7	4L6	4L5	4L4	4L3	4L2	4L1	4L0	0	1	X	X	X	X	X	Read the 4th Label
P	0	0	1	5L7	5L6	5L5	5L4	5L3	5L2	5L1	5L0	0	1	X	X	X	X	X	Read the 5th Label
P	0	0	1	6L7	6L6	6L5	6L4	6L3	6L2	6L1	6L0	0	1	X	X	X	X	X	Read the 6th Label
P	0	0	1	7L7	7L6	7L5	7L4	7L3	7L2	7L1	7L0	0	1	X	X	X	X	X	Read the 7th Label
P	0	0	1	8L7	8L6	8L5	8L4	8L3	8L2	8L1	8L0	0	1	X	X	X	X	X	Read the 8th Label

P = Pulse
X = Don't Care

TIMING DIAGRAMS

DATA BUS TIMING - READ

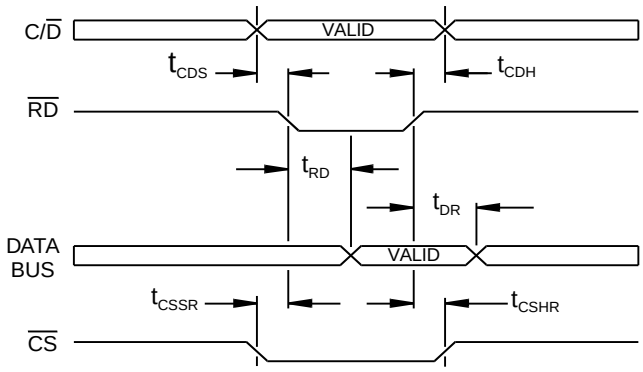


Figure 1.

DATA BUS TIMING - WRITE

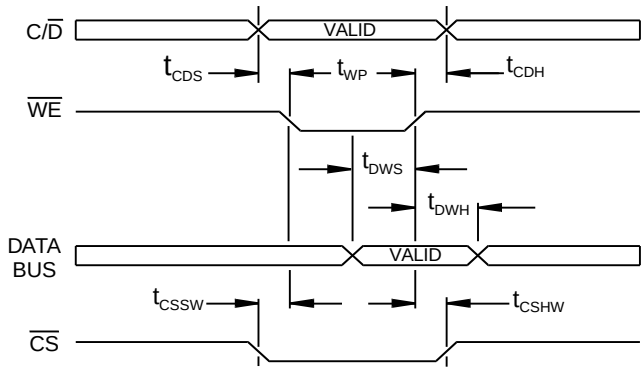


Figure 2.

TRANSMTTER OPERATION

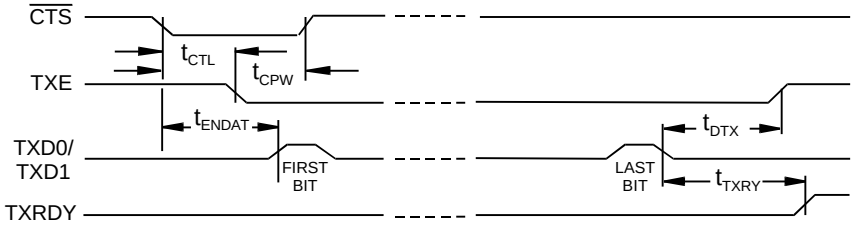


Figure 3.

RECEIVER OPERATION

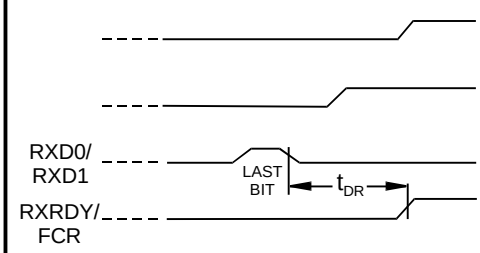


Figure 4.

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to V_{SS} = 0V)

Supply Voltage:	V_{DD}	-0.5V to +7.0V	
Input Voltage Range	V_{IN}	-0.5V to V_{DD} +0.5V	
Input Current	I_{IN}	+10mA	
Output Current	I_{OUT}	+25mA	
Power Dissipation	P_D	500mW	
Operating Temperature Range:	T_A (Industrial)	-40°C to +85°C	
	T_A (Hi temp & Military)	-55°C to +125°C	
Storage Temperature Range:	T_{STG}	-65°C to +150°C	
Lead Temperature	T_{LEAD}	300°C for 60 Seconds	

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

V_{DD} = 5.0V, V_{SS} = 0V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Operating Voltage	V_{DD}		4.5	5	5.5	V
Min. Input Voltage (HI)	V_{IH}		2.1	1.4		V
Max. Input Voltage (LO)	V_{IL}			1.4	0.7	V
Min. Input Current (HI)	I_{IH}	V_{IH} = 4.9V	-1.5			µA
Max. Input Current (LO)	I_{IL}	V_{IL} = 0.1V			1.5	µA
Min. Output Voltage (HI)	V_{OH}	I_{OUT} = -1.5mA	2.7			V
Max. Output Voltage (LO)	V_{IH}	I_{OUT} = 1.8mA			0.7	V
Operating Current Drain	I_{DD}	f = 400KHz		0.8	2.8	mA
Input Capacitance	C_{IN}	Not tested			20	pF

AC ELECTRICAL CHARACTERISTICS

V_{DD} = 5.0V, V_{SS} = 0V, T_A =Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
DATA BUS TIMING - READ (See Figure 1.)					
Setup C/$\overline{D}$ to $\overline{RD}$	t_{CDS}	50			ns
Hold C/$\overline{D}$ to $\overline{RD}$	t_{CDH}	0			ns
Delay $\overline{RD}$ to Data	t_{RC}			200	ns
Delay Data Bus Hi-Z from $\overline{RD}$	t_{RD}			150	ns
Setup $\overline{CS}$ to $\overline{RD}$	t_{CSSR}	0			ns
Hold $\overline{RD}$ to $\overline{CS}$	t_{CSHR}	0			ns
DATA BUS TIMING - WRITE (See Figure 2.)					
Set C/$\overline{D}$ to $\overline{WE}$	t_{CDS}	0			ns
Hold C/$\overline{D}$ to $\overline{WE}$	t_{CDH}	0			ns
Setup Data Bus to $\overline{WE}$	t_{WDS}	200			ns
Hold Data Bus to $\overline{WE}$	t_{DWH}	100			ns
Setup $\overline{CS}$ to $\overline{WE}$	t_{CSSW}	0			ns
Hold $\overline{CS}$ to $\overline{WE}$	t_{CSHW}	0			ns
Pulse Width $\overline{WE}$	t_{WP}	200			ns
TRANSMITTER TIMING (See Figure 3.)					
Delay TXE from $\overline{CTS}$	t_{CTL}	1.5		2.0	CLKS
Delay TXRDn from $\overline{CTS}$	t_{ENDAT}	1			CLK
Delay TXRDY from last TXDn	t_{TXRDY}	16			CLKS
Delay TXE from last TXDn	t_{TDTX}		4		DATA BITS
$\overline{CTS}$ pulse width	t_{CPW}	1			CLK
RECEIVER TIMING (See Figure 4.)					
Delay Last RXDn to RXRDY	t_{DR}			3	CLKS

ORDERING INFORMATION

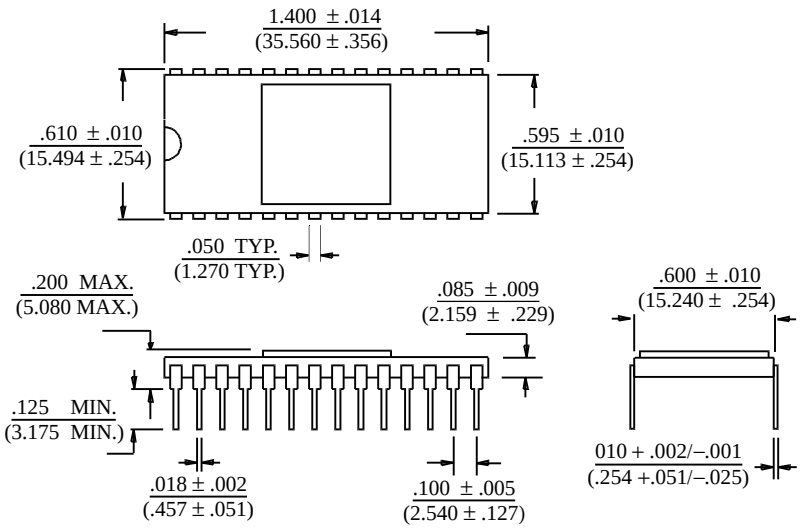
PART NUMBER	PACKAGE DESCRIPTION	TEMPERATURE RANGE	FLOW	BURN IN	LEAD FINISH
HI-6010C	28 PIN CERAMIC SIDE BRAZED DIP	-40°C TO +85°C	I	NO	GOLD
HI-6010CT	28 PIN CERAMIC SIDE BRAZED DIP	-55°C TO +125°C	T	NO	GOLD
HI-6010CM-01	28 PIN CERAMIC SIDE BRAZED DIP	-55°C TO +125°C	M	YES	SOLDER
HI-6010J	28 PIN PLASTIC J -LEAD PLCC	-40°C TO +85°C	I	NO	SOLDER
HI-6010JT	28 PIN PLASTIC J -LEAD PLCC	-55°C TO +125°C	T	NO	SOLDER

HI-6010 PACKAGE DIMENSIONS

inches (millimeters)

28-PIN CERAMIC SIDE-BRAZED DIP

Package Type: 28C



28-PIN PLASTIC PLCC

Package Type: 28J