

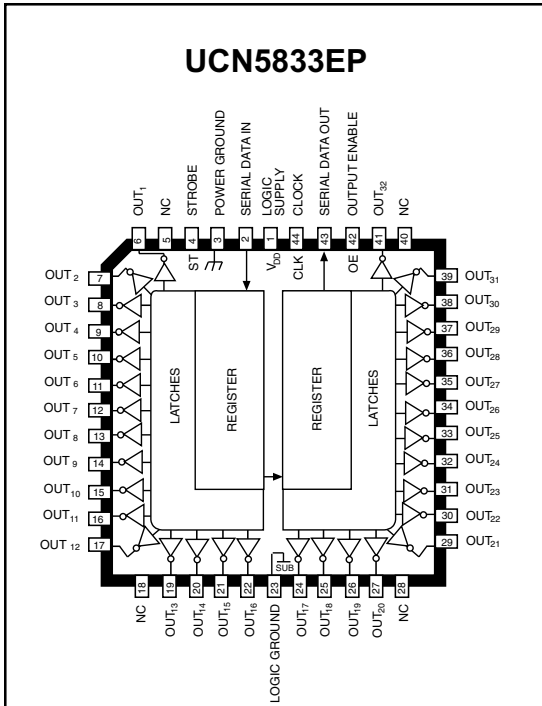
# 5833

## BiMOS II 32-BIT SERIAL-INPUT, LATCHED DRIVER

Designed to reduce logic supply current, chip size, and system cost, the UCN5833A/EP integrated circuits offer high-speed operation for thermal printers. These devices can also be used to drive multiplexed LED displays or incandescent lamps within their 125 mA peak output current rating. The combination of bipolar and MOS technologies gives BiMOS II smart power ICs an interface flexibility beyond the reach of standard buffers and power driver circuits.

These 32-bit drivers have bipolar open-collector npn Darlington outputs, a CMOS data latch for each of the drivers, a 32-bit CMOS shift register, and CMOS control circuitry. The high-speed CMOS shift registers and latches allow operation with most microprocessor-based systems at data input rates above 3.3 MHz. Use of these drivers with TTL may require input pull-up resistors to ensure an input logic high.

The UCN5833A is supplied in a 40-pin dual in-line plastic package with 0.600" (15.24 mm) row spacing. At an ambient temperature of +75°C, all outputs of the DIP-packaged device will sustain 50 mA continuously. For high-density applications, the UCN5833EP is available. This 44-lead plastic chip carrier (quad pack) is intended for surface-mounting on solder lands with 0.050" (1.27 mm) centers. CMOS serial data outputs permit cascading for applications requiring additional drive lines.



Dwg. No. A-13,049

### ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature

Output Voltage, $V_{OUT}$ . . . . .	30 V
Logic Supply Voltage, $V_{DD}$ . . . . .	7.0 V
Input Voltage Range, $V_{IN}$ . . . . .	-0.3 V to $V_{DD} + 0.3$ V
Continuous Output Current, $I_{OUT}$ (each output) . . . . .	125 mA
Package Power Dissipation, $P_D$	
(UCN5833A) . . . . .	3.5 W*
(UCN5833EP) . . . . .	2.5 W*
Operating Temperature Range, $T_A$ . . . . .	-20°C to +85°C
Storage Temperature Range, $T_S$ . . . . .	-55°C to +150°C

\* Derate linearly to 0 W at +150°C.

Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

### FEATURES

- To 3.3 MHz Data Input Rate
- 30 V Minimum Output Breakdown
- Darlington Current-Sink Outputs
- Low-Power CMOS Logic and Latches

Always order by complete part number:

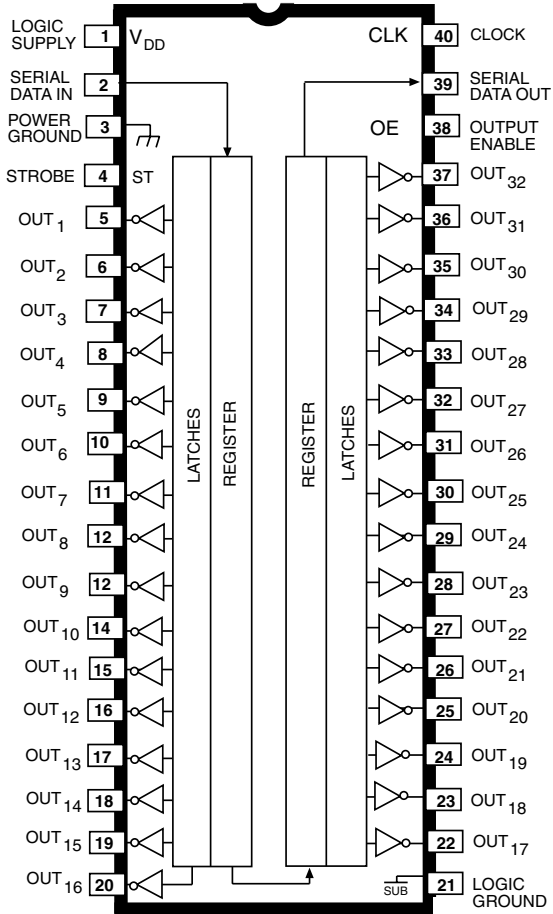
Part Number	Package
UCN5833A	40-Pin DIP
UCN5833EP	44-Lead PLCC



# 5833

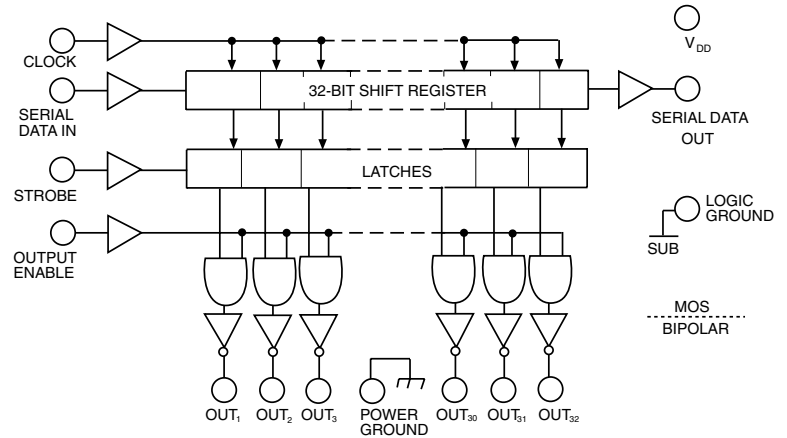
## BiMOS II 32-BIT SERIAL-INPUT, LATCHED DRIVER

### UCN5833A



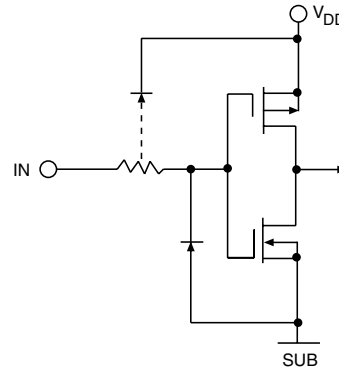
Dwg. No. A-13,048

### FUNCTIONAL BLOCK DIAGRAM



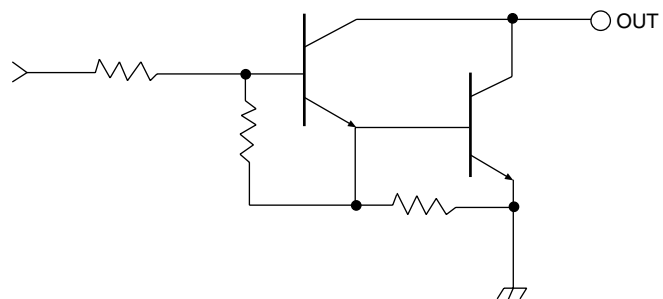
Dwg. No. A-13,057

### TYPICAL INPUT CIRCUIT



Dwg. No. A-13,050

### TYPICAL OUTPUT DRIVER



Dwg. No. A-13,051



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**SERIAL-INPUT,**  
**LATCHED DRIVER**

**ELECTRICAL CHARACTERISTICS at  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = 5\text{ V}$  (unless otherwise noted).**

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	$I_{CEX}$	$V_{OUT} = 30\text{ V}$ , $T_A = 70^\circ\text{C}$	—	10	$\mu\text{A}$
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_{OUT} = 50\text{ mA}$	—	1.2	V
		$I_{OUT} = 100\text{ mA}$	—	1.7	V
Input Voltage	$V_{IN(1)}$		3.5	5.3	V
	$V_{IN(0)}$		-0.3	+0.8	V
Input Current	$I_{IN(1)}$	$V_{IN} = 5.0\text{ V}$	—	1.0	$\mu\text{A}$
	$I_{IN(0)}$	$V_{IN} = 0\text{ V}$	—	-1.0	$\mu\text{A}$
Serial Output Voltage	$V_{OUT(1)}$	$I_{OUT} = -200\ \mu\text{A}$	4.5	—	V
	$V_{OUT(0)}$	$I_{OUT} = 200\ \mu\text{A}$	—	0.3	V
Supply Current	$I_{DD}$	One output ON, $I_{OUT} = 100\text{ mA}$	—	1.0	mA
		All outputs OFF	—	50	$\mu\text{A}$
Output Rise Time	$t_r$	$I_{OUT} = 100\text{ mA}$ , 10% to 90%	—	500	ns
Output Fall Time	$t_f$	$I_{OUT} = 100\text{ mA}$ , 90% to 10%	—	500	ns

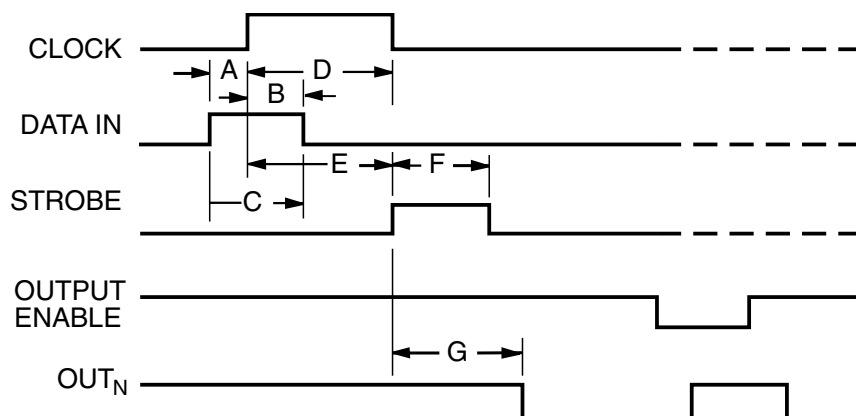
NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.

### TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents						Serial Data Output	Strobe Input	Latch Contents						Output Enable Input	Output Contents					
		$I_1$	$I_2$	$I_3$	...	$I_{N-1}$	$I_N$			$I_1$	$I_2$	$I_3$	...	$I_{N-1}$	$I_N$		$I_1$	$I_2$	$I_3$	...	$I_{N-1}$	$I_N$
H		H	$R_1$	$R_2$	...	$R_{N-2}$	$R_{N-1}$	$R_{N-1}$														
L		L	$R_1$	$R_2$	...	$R_{N-2}$	$R_{N-1}$	$R_{N-1}$														
X		$R_1$	$R_2$	$R_3$	...	$R_{N-1}$	$R_N$	$R_N$														
		X	X	X	...	X	X	X	L	$R_1$	$R_2$	$R_3$	...	$R_{N-1}$	$R_N$							
		$P_1$	$P_2$	$P_3$	...	$P_{N-1}$	$P_N$	$P_N$	H	$P_1$	$P_2$	$P_3$	...	$P_{N-1}$	$P_N$	H						
										X	X	X	...	X	X	L	H	H	H	...	H	H

L = Low Logic Level   H = High Logic Level   X = Irrelevant   P = Present State   R = Previous State

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**SERIAL-INPUT,**  
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Dwg. No. A-12,276A

**TIMING CONDITIONS**

(V<sub>DD</sub> = 5.0 V, Logic Levels are V<sub>DD</sub> and Ground)

<b>A.</b> Minimum Data Active Time Before Clock Pulse (Data Set-Up Time).....	<b>75 ns</b>
<b>B.</b> Minimum Data Active Time After Clock Pulse (Data Hold Time) .....	<b>75 ns</b>
<b>C.</b> Minimum Data Pulse Width .....	<b>150 ns</b>
<b>D.</b> Minimum Clock Pulse Width .....	<b>150 ns</b>
<b>E.</b> Minimum Time Between Clock Activation and Strobe .....	<b>300 ns</b>
<b>F.</b> Minimum Strobe Pulse Width .....	<b>100 ns</b>
<b>G.</b> Typical Time Between Strobe Activation and Output Transition .....	<b>500 ns</b>

Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be low during serial data entry.

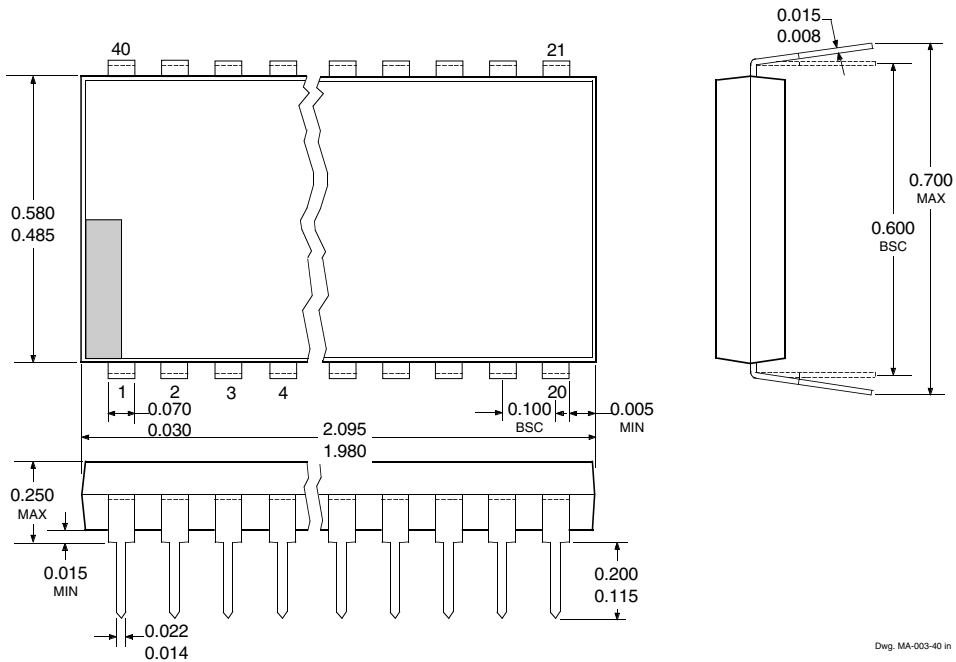
When the OUTPUT ENABLE input is low, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the OUTPUT ENABLE input high, the outputs are controlled by the state of the latches.



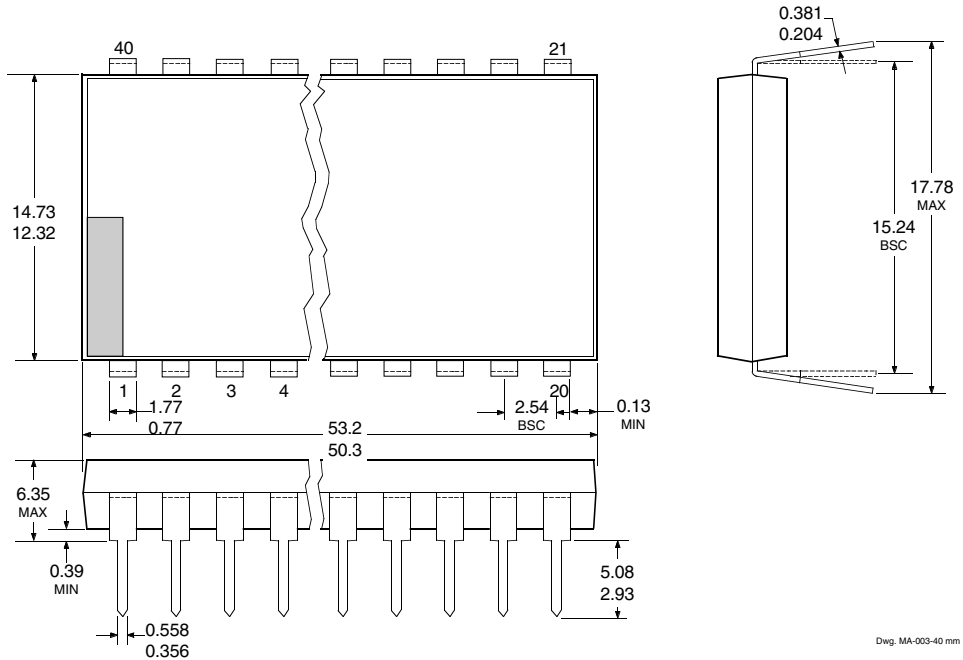
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## UCN5833A Dimensions in Inches (controlling dimensions)



## Dimensions in Millimeters (for reference only)



- NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.  
2. Lead spacing tolerance is non-cumulative.  
3. Lead thickness is measured at seating plane or below.



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**5833**  
***BiMOS II 32-BIT***  
***SERIAL-INPUT,***  
***LATCHED DRIVER***

***POWER***  
***INTERFACE DRIVERS***

Function	Output Ratings*		Part Number†
<b>SERIAL-INPUT LATCHED DRIVERS</b>			
8-Bit (saturated drivers)	-120 mA	50 V‡	5895
8-Bit	350 mA	50 V	5821
8-Bit	350 mA	80 V	5822
8-Bit	350 mA	50 V‡	5841
8-Bit	350 mA	80 V‡	5842
8-Bit (constant-current LED driver)	75 mA	17 V	6275
8-Bit (DMOS drivers)	250 mA	50 V	6595
8-Bit (DMOS drivers)	350 mA	50 V‡	6A595
8-Bit (DMOS drivers)	100 mA	50 V	6B595
10-Bit (active pull-downs)	-25 mA	60 V	5810-F and 6809/10
12-Bit (active pull-downs)	-25 mA	60 V	5811 and 6811
16-Bit (constant-current LED driver)	75 mA	17 V	6276
20-Bit (active pull-downs)	-25 mA	60 V	5812-F and 6812
32-Bit (active pull-downs)	-25 mA	60 V	5818-F and 6818
32-Bit	100 mA	30 V	5833
32-Bit (saturated drivers)	100 mA	40 V	5832
<b>PARALLEL-INPUT LATCHED DRIVERS</b>			
4-Bit	350 mA	50 V‡	5800
8-Bit	-25 mA	60 V	5815
8-Bit	350 mA	50 V‡	5801
8-Bit (DMOS drivers)	100 mA	50 V	6B273
8-Bit (DMOS drivers)	250 mA	50 V	6273
<b>SPECIAL-PURPOSE DEVICES</b>			
Unipolar Stepper Motor Translator/Driver	1.25 A	50 V‡	5804
Addressable 8-Bit Decoder/DMOS Driver	250 mA	50 V	6259
Addressable 8-Bit Decoder/DMOS Driver	350 mA	50 V‡	6A259
Addressable 8-Bit Decoder/DMOS Driver	100 mA	50 V	6B259
Addressable 28-Line Decoder/Driver	450 mA	30 V	6817

\* Current is maximum specified test condition, voltage is maximum rating. See specification for sustaining voltage limits. Negative current is defined as coming out of (sourcing) the output.

† Complete part number includes additional characters to indicate operating temperature range and package style.

‡ Internal transient-suppression diodes included for inductive-load protection.



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