

54ABT16646

16-Bit Transceivers and Registers with TRI-STATE® Outputs

General Description

The 'ABT16646 consists of bus transceiver circuits with TRI-STATE, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a high logic level. Control \overline{OE} and direction pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or the B register or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control \overline{OE} is Active LOW. In the isolation mode (control \overline{OE} HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

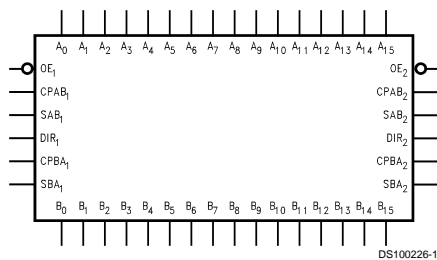
Features

- Independent registers for A and B buses
- Multiplexed real-time and stored data
- A and B output sink capability of 48 mA, source capability of 24 mA
- Guaranteed latching protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability
- Standard Microcircuit Drawing (SMD) 5962-9450202

Ordering Code

Military	Package Number	Package Description
54ABT16646W-QML	WA56A	56-Lead Cerpack

Logic Symbol



Pin Names	Description
A ₀ -A ₁₅	Data Register A Inputs/ TRI-STATE Outputs
B ₀ -B ₁₅	Data Register B Inputs/ TRI-STATE Outputs
CPAB _n , CPBA _n	Clock Pulse Inputs
SAB _n , SBA _n	Select Inputs
\overline{OE}_n	Output Enable Input
DIR	Direction Control Input

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Connection Diagram

Pin Assignment for Cerpack

DIR ₁	1	56	\overline{OE}_1
CFAB ₁	2	55	CPBA ₁
SAB ₁	3	54	SBA ₁
GND	4	53	GND
A ₀	5	52	B ₀
A ₁	6	51	B ₁
V _{CC}	7	50	V _{CC}
A ₂	8	49	B ₂
A ₃	9	48	B ₃
A ₄	10	47	B ₄
GND	11	46	GND
A ₅	12	45	B ₅
A ₆	13	44	B ₆
A ₇	14	43	B ₇
A ₈	15	42	B ₈
A ₉	16	41	B ₉
A ₁₀	17	40	B ₁₀
GND	18	39	GND
A ₁₁	19	38	B ₁₁
A ₁₂	20	37	B ₁₂
A ₁₃	21	36	B ₁₃
V _{CC}	22	35	V _{CC}
A ₁₄	23	34	B ₁₄
A ₁₅	24	33	B ₁₅
GND	25	32	GND
SAB ₂	26	31	SBA ₂
CFAB ₂	27	30	CPBA ₂
DIR ₂	28	29	\overline{OE}_2

DS100226-2

Real Time Transfer A-Bus to B-Bus

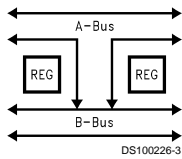


FIGURE 1.

Storage from Bus to Register

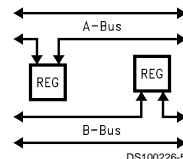


FIGURE 3.

Real Time Transfer B-Bus to A-Bus

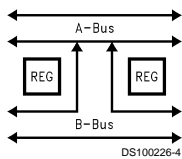


FIGURE 2.

Transfer from Register to Bus

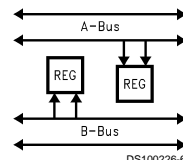


FIGURE 4.

Function Table

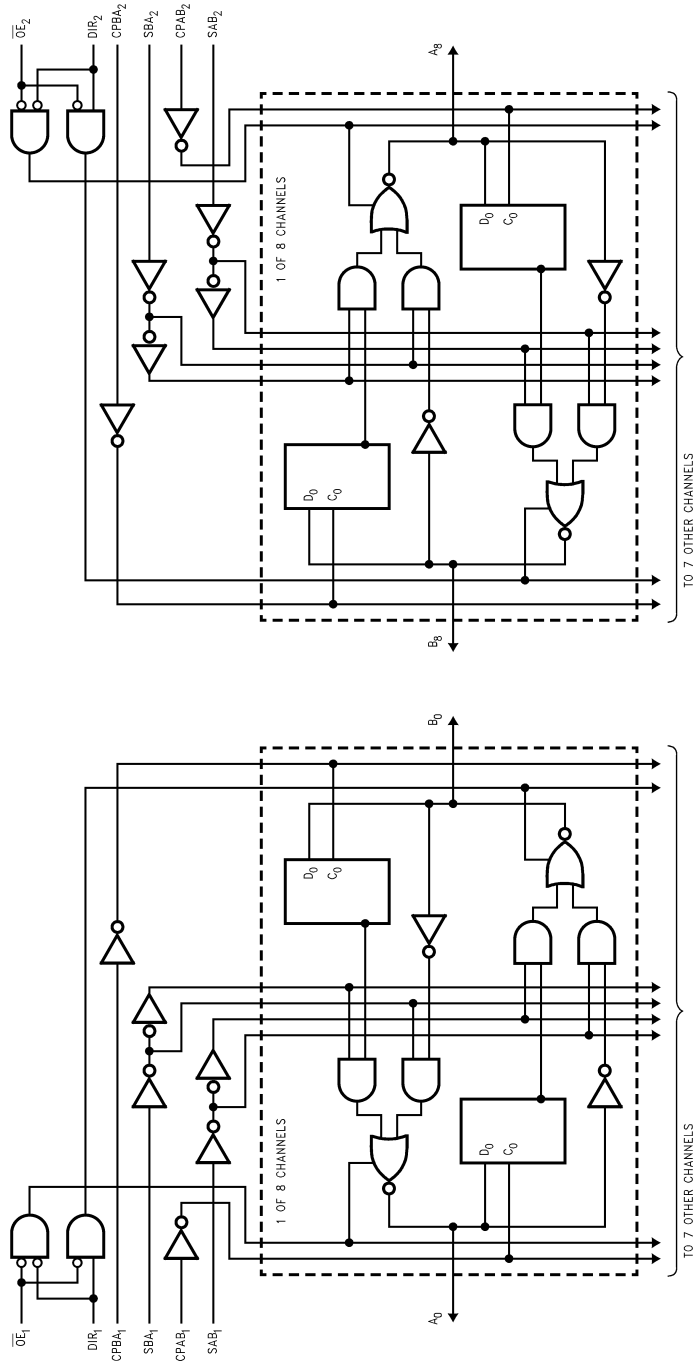
Inputs						Data I/O (Note 1)		Output Operation Mode
\overline{OE}_1	DIR ₁	CPAB ₁	CPBA ₁	SAB ₁	SBA ₁	A ₀₋₇	B ₀₋₇	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	N	X	X	X			Clock An Data into A Register
H	X	X	N	X	X			Clock Bn Data Into B Register
L	H	X	X	L	X	Input	Output	An to Bn—Real Time (Transparent Mode)
L	H	N	X	L	X			Clock An Data to A Register
L	H	H or L	X	H	X			A Register to Bn (Stored Mode)
L	H	N	X	H	X			Clock An Data into A Register and Output to Bn
L	L	X	X	X	L	Output	Input	Bn to An—Real Time (Transparent Mode)
L	L	X	N	X	L			Clock Bn Data into B Register
L	L	X	H or L	X	H			B Register to An (Stored Mode)
L	L	X	N	X	H			Clock Bn into B Register and Output to An

H = HIGH Voltage Level X = Immaterial

L = LOW Voltage Level N = LOW-to-HIGH Transition.

Note 1: The data output functions may be enabled or disabled by various signals at the \overline{OE} and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs. Also applies to data I/O (A and B: 8-15) and #2 control pins.

Logic Diagram



DS1002267

Absolute Maximum Ratings (Note 2)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	
Ceramic	-55°C to +175°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 3)	-0.5V to +7.0V
Input Current (Note 3)	-30 mA to +5.0 mA
Voltage Applied to Any Output in the Disable or Power-Off State in the HIGH State	-0.5V to +5.5V -0.5V to V _{CC}
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)
DC Latchup Source Current	-500 mA

Over Voltage Latchup (I/O)

10V

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Supply Voltage	
Military	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100 mV/ns

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	ABT16646			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V _{IL}	Input LOW Voltage	0.8			V		Recognized LOW Signal
V _{CD}	Input Clamp Diode Voltage	-1.2			V	Min	I _{IN} = -18 mA (Non I/O Pins)
V _{OH}	Output HIGH Voltage	54ABT	2.5				I _{OH} = -3 mA, (A _n , B _n) I _{OH} = -24 mA, (A _n , B _n)
		54ABT	2.0				
V _{OL}	Output LOW Voltage	54ABT	0.55		V	Min	I _{OL} = 48 mA, (A _n , B _n)
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA, (Non-I/O Pins) All Other Pins Grounded
I _{IH}	Input HIGH Current	5			μA	Max	V _{IN} = 2.7V (Non-I/O Pins) (Note 5) V _{IN} = V _{CC} (Non-I/O Pins)
I _{BVI}	Input HIGH Current Breakdown Test	7			μA	Max	V _{IN} = 7.0V (Non-I/O Pins)
I _{BVIT}	Input HIGH Current Breakdown Test (I/O)	100			μA	Max	V _{IN} = 5.5V (A _n , B _n)
I _{IL}	Input LOW Current	-5			μA	Max	V _{IN} = 0.5V (Non-I/O Pins) (Note 5) V _{IN} = 0.0V (Non-I/O Pins)
I _{IH} + I _{OZH}	Output Leakage Current	50			μA	0V-5.5V	V _{OUT} = 2.7V (A _n , B _n); \overline{OE} = 2.0V
I _{IL} + I _{OZL}	Output Leakage Current	-50			μA	0V-5.5V	V _{OUT} = 0.5V (A _n , B _n); \overline{OE} = 2.0V
I _{OS}	Output Short-Circuit Current	-100	-275		mA	Max	V _{OUT} = 0V (A _n , B _n)
I _{CEX}	Output HIGH Leakage Current	50			μA	Max	V _{OUT} = V _{CC} (A _n , B _n)
I _{ZZ}	Bus Drainage Test	100			μA	0.0V	V _{OUT} = 5.5V (A _n , B _n); All Others GND
I _{CCH}	Power Supply Current	2.0			mA	Max	All Outputs HIGH
I _{CCL}	Power Supply Current	60			mA	Max	All Outputs LOW
I _{CCZ}	Power Supply Current	2.0			mA	Max	Outputs TRI-STATE; All Others GND
I _{CCT}	Additional I _{CC} /Input	2.5			mA	Max	V _I = V _{CC} - 2.1V All Other Outputs at V _{CC} or GND
I _{CCD}	Dynamic I _{CC} (Note 5)	No Load	0.23		mA/MHz	Max	Outputs Open \overline{OE} , DIR, and SEL = GND, Non-I/O = GND or V _{CC} (Note 4) One Bit toggling, 50% duty cycle

DC Electrical Characteristics (Continued)

Note 4: For 8-bit toggling, $I_{CCD} < 1.4$ mA/MHz.

Note 5: Guaranteed but not tested.

DC Electrical Characteristics

Symbol	Parameter	Min	Max	Units	V _{CC}	Conditions C _L = 50 pF, R _L = 500Ω
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}		1.0	V	5.0	T _A = 25°C (Note 6)
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}		-1.5	V	5.0	T _A = 25°C (Note 6)

Note 6: Max number of outputs defined as (n). n - 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

AC Electrical Characteristics

Symbol	Parameter	54ABT		Units	Fig. No.
		T _A = -55°C to +125°C V _{CC} = 4.5V-5.5V C _L = 50 pF			
		Min	Max		
f _{max}	Max Clock Frequency	125		MHz	
t _{PLH}	Propagation Delay	1.0	6.9	ns	Figure 8
t _{PHL}	Clock to Bus	1.0	7.7		
t _{PLH}	Propagation Delay	1.0	5.8	ns	Figure 8
t _{PHL}	Bus to Bus	1.0	7.0		
t _{PLH}	Propagation Delay	1.0	7.1	ns	Figure 8
t _{PHL}	SBA _n or SAB _n to A _n to B _n	1.0	7.2		
t _{PZH}	Enable Time	1.0	6.4	ns	Figure 10
t _{PZL}	\overline{OE}_n to A _n or B _n	1.0	6.5		
t _{PHZ}	Disable Time	1.0	7.6	ns	Figure 10
t _{PLZ}	\overline{OE}_n to A _n or B _n	1.0	6.5		
t _{PZH}	Enable Time	1.0	6.4	ns	Figure 10
t _{PZL}	DIR _n to A _n or B _n	1.0	6.7		
t _{PHZ}	Disable Time	1.0	8.1	ns	Figure 10
t _{PLZ}	DIR _n to A _n or B _n	1.0	7.1		

AC Operating Requirements

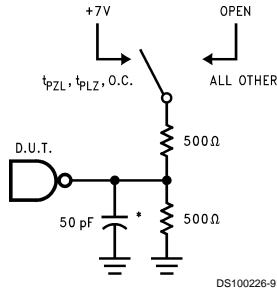
Symbol	Parameter	54ABT		Units	Fig. No.
		T _A = -55°C to +125°C V _{CC} = 4.5V-5.5V C _L = 50 pF			
		Min	Max		
t _{S(H)}	Setup Time, HIGH	4.0		ns	Figure 11
t _{S(L)}	or LOW Bus to Clock				
t _{H(H)}	Hold Time, HIGH	0.5		ns	Figure 11
t _{H(L)}	or LOW Bus to Clock				
t _{W(H)}	Pulse Width,	4.3		ns	Figure 9
t _{W(L)}	HIGH or LOW				

Capacitance

Symbol	Parameter	Typ	Units	Conditions $T_A = 25^\circ\text{C}$
C_{IN}	Input Capacitance	5	pF	$V_{CC} = 0\text{V}$ (non I/O pins)
$C_{I/O}$ (Note 7)	Output Capacitance	11	pF	$V_{CC} = 5.0\text{V}$ (A_n, B_n)

Note 7: $C_{I/O}$ is measured at frequency, $f = 1\text{ MHz}$, per MIL-STD-883B, Method 3012.

AC Loading



*Includes jig and probe capacitance

FIGURE 5. Standard AC Test Load

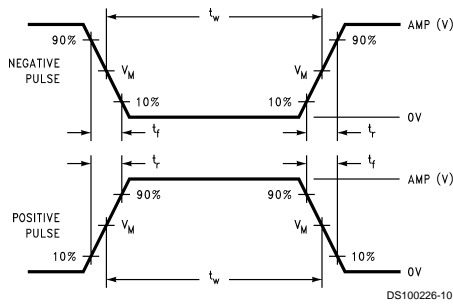


FIGURE 6. $V_M = 1.5\text{V}$ Input Pulse Requirements

Amplitude	Rep. Rate	t_w	t_r	t_f
3V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 7. Test Input Signal Requirements

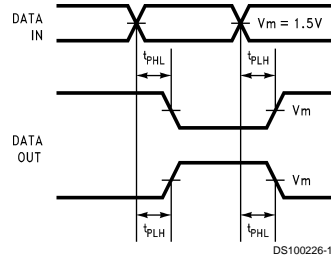


FIGURE 8. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

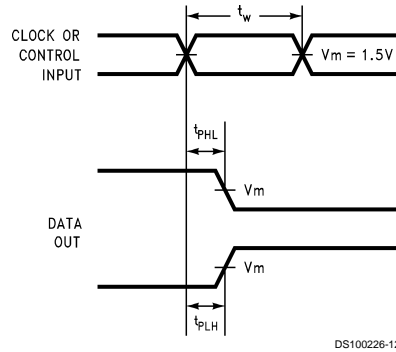


FIGURE 9. Propagation Delay, Pulse Width Waveforms

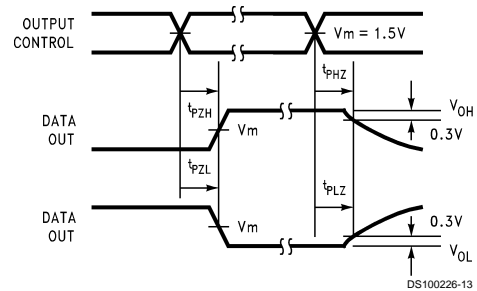


FIGURE 10. TRI-STATE Output HIGH and LOW Enable and Disable Times

AC Loading (Continued)

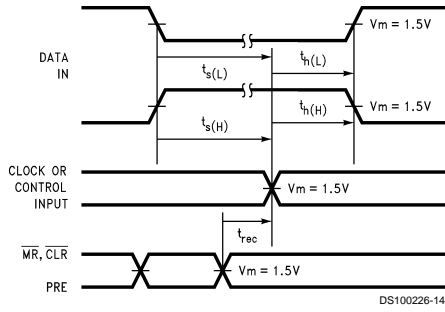
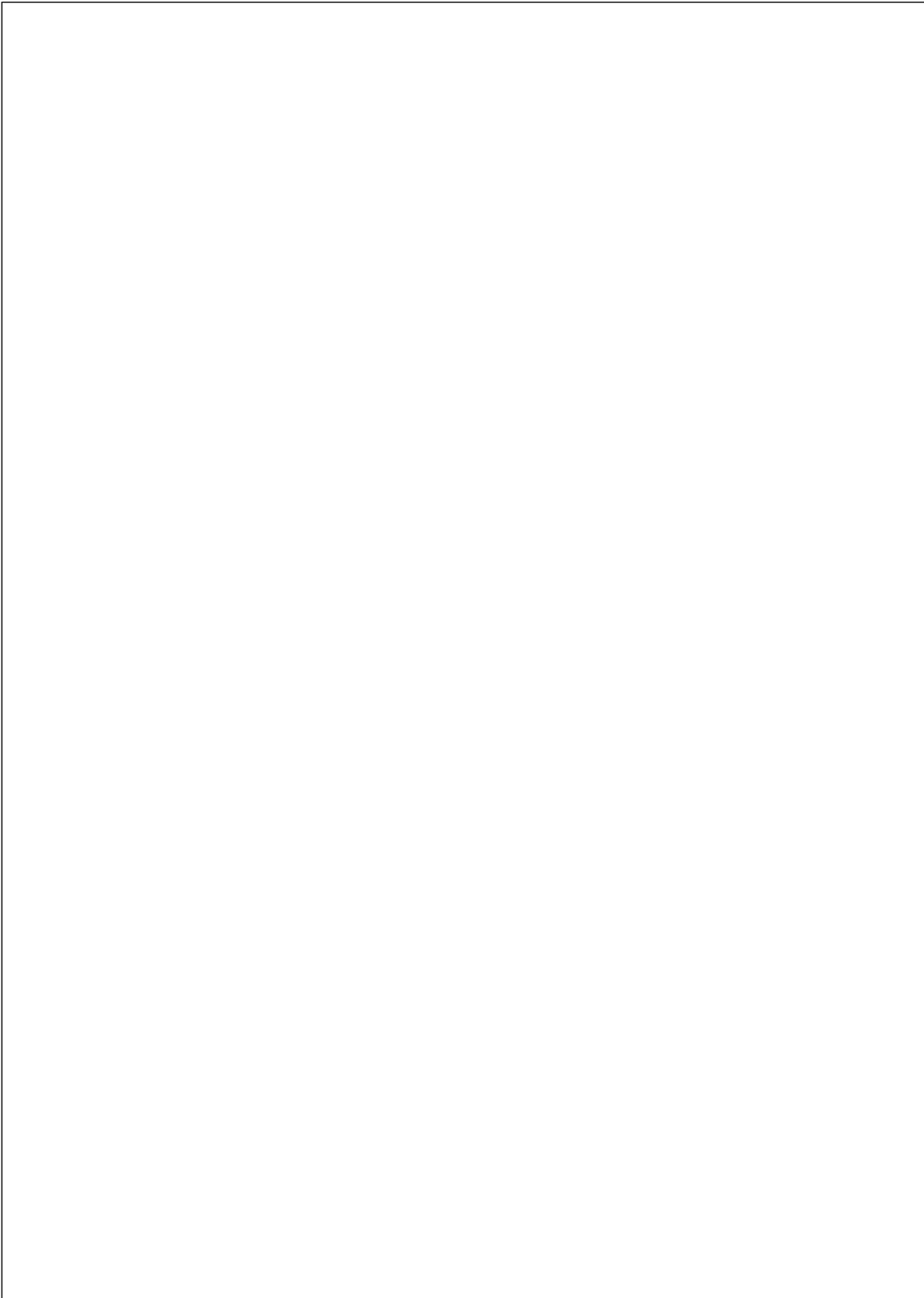
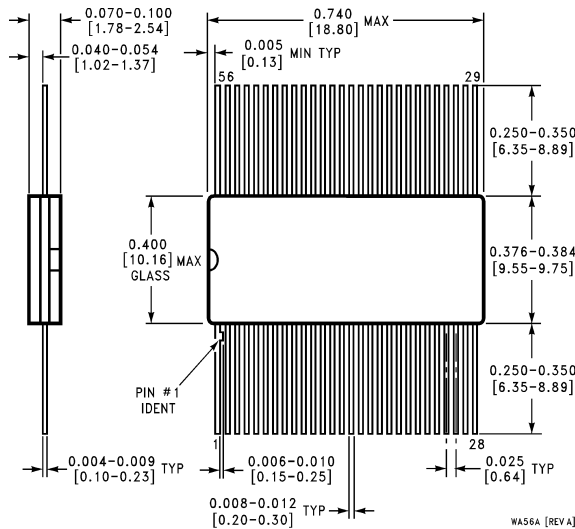


FIGURE 11. Setup Time, Hold Time and Recovery Time Waveforms

Book
Extract
End



Physical Dimensions inches (millimeters) unless otherwise noted



**56-Lead Cerpack
NS Package Number WA56A**

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