DATA SHEET

SAA5261; SAA5262; SAA5263
10-page intelligent teletext decoders

Product specification
File under Integrated Circuits, IC02

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Philips
Semiconductors

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FEATURES

SAA5261, SAA5262 and SAA5263

- Complete 625-line teletext decoder in a single integrated circuit thereby reducing printed-circuit board area and cost
- Automatic detection of transmitted pages so that only existing pages will be selected by page-up and page-down once inventory validated
- Automatic detection of transmitted Fastext links or service information (packet 8/30)
- On-screen display for user interface (menus, etc.) using teletext and dedicated menu icons
- Video Programming System (VPS) decoding
- Wide Screen Signalling (WSS) decoding
- 8-page Fastext decoder
- 6-page TOP decoder in addition to capture of Basic TOP Table (BTT) and 3 Additional Information Table (AIT) pages
- 4-page user defined list mode
- Yugoslavian, Cyrillic, Greek/Turkish, Thai, Arabic/Hebrew, Pan-European and Arabic/English/French language coverage
- High level command interface via I^{2}C-bus giving easy control from a low software overhead
- High level command interface is backward compatible to SAFARI interface
- 625 and 525 line display
- RGB interface to standard colour decoder ICs, push-pull output drive
- Versatile 8-bit open-drain I/O expander
- Single 12 MHz crystal oscillator for reduced cost
- +5 V power supply.

SAA5262 and SAA5263

- Automatic Channel Installation (ACI)
- Enhanced SAFARI interface providing additional commands.

SAA5263

- Electronic Programme Guide (EPG) feature.

GENERAL DESCRIPTION

The SAA526xPS ICs are single-chip 10-page 625-line World System Teletext (WST) decoders with a high level command interface, SAFARI compatible.

It has been designed so that the overall system cost is kept to a minimum. This has been achieved through the capability of the device to be driven from a single +5 V power supply, low cost 12 MHz crystal oscillator and the high level command interface, which offers the benefit of low software overhead in the TV microcontroller.

The SAA526xPS offers automatic detection of Fastext or TOP transmissions. The device also incorporates a facility to detect the pages in the transmission, which allows only transmitted pages to be selected by page-up and page-down.

SAA5262 and SAA5263 provide Automatic Channel Installation (ACI) information.

SAA5263 provides access to Electronic Programme Guide (EPG) information.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA5261PS	SDIP52	plastic shrink dual in-line package; 52 leads (600 mil)	SOT247-1
SAA5262PS	SDIP52	plastic shrink dual in-line package; 52 leads (600 mil)	SOT247-1
SAA5263PS	SDIP52	plastic shrink dual in-line package; 52 leads (600 mil)	SOT247-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage	4.5	5.0	5.5	V
$I_{DDD(M)}$	microcontroller supply current	–	20	35	mA
I_{DDA}	analog supply current	–	35	50	mA
$I_{DDD(T)}$	teletext supply current	–	50	80	mA
f_{xtal}	crystal frequency	–	12	–	MHz
T_{amb}	operating ambient temperature	–20	–	+70	°C

BLOCK DIAGRAM

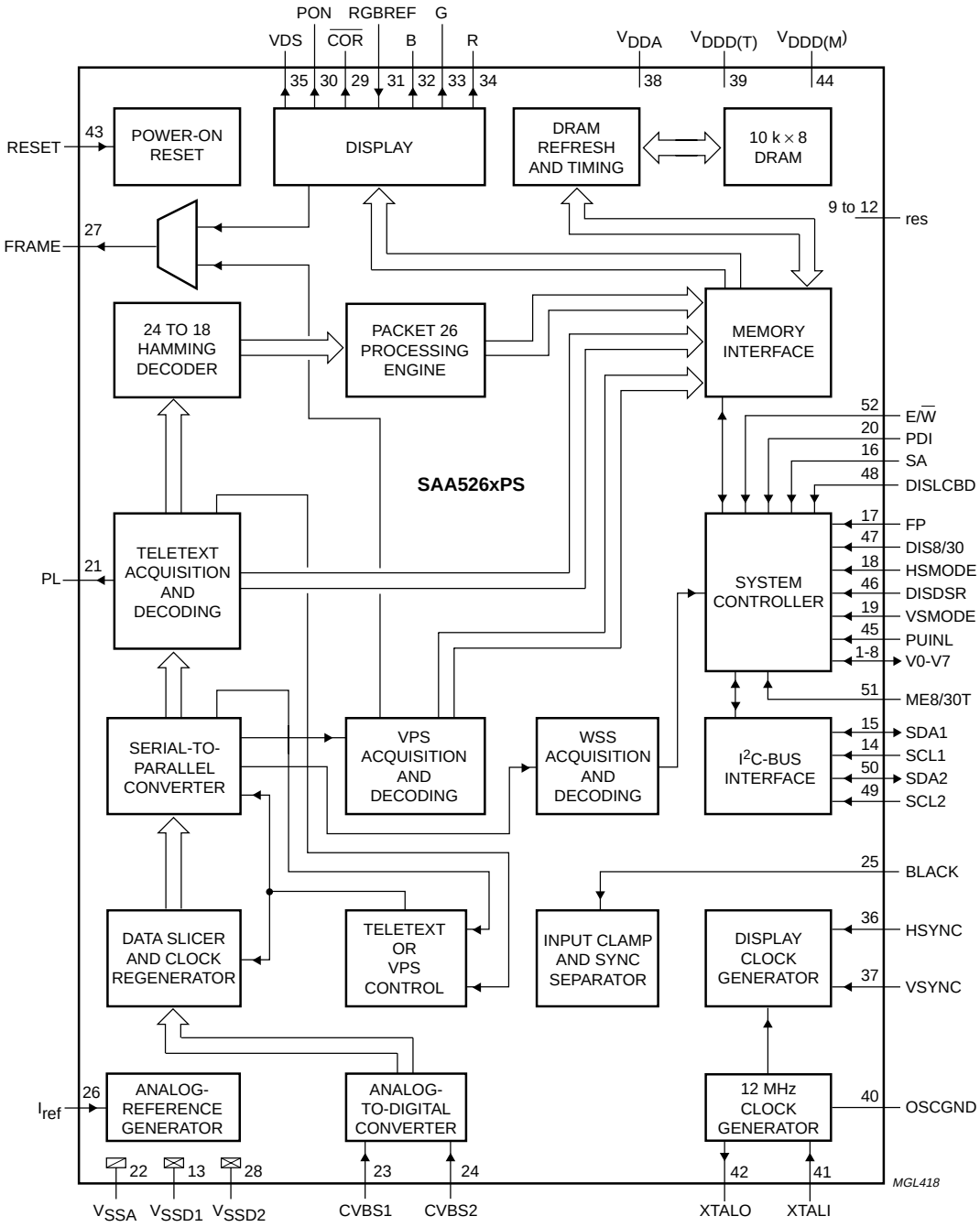


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V0	1	versatile open-drain input/output bit 0 (should be tied HIGH)
V1	2	versatile open-drain input/output bit 1 (should be tied HIGH)
V2	3	versatile open-drain input/output bit 2 (should be tied HIGH)
V3	4	versatile open-drain input/output bit 3 (should be tied HIGH)
V4	5	versatile open-drain input/output bit 4 (should be tied HIGH)
V5	6	versatile open-drain input/output bit 5 (should be tied HIGH)
V6	7	versatile open-drain input/output bit 6 (should be tied HIGH)
V7	8	versatile open-drain input/output bit 7 (should be tied HIGH)
res	9	reserved
res	10	reserved
res	11	reserved
res	12	reserved
V_{SSD1}	13	digital ground 1
SCLK1	14	serial clock input 1 (NVRAM)
SDAT1	15	serial data input/output 1 (NVRAM)
SA	16	slave address input: LOW selects 58H; HIGH selects 60H
FP	17	field polarity input: LOW selects first half line; HIGH selects second half line at the start of an even field
HSMODE	18	horizontal sync mode control input: LOW selects HSYNC on rising edge
VSMODE	19	vertical sync mode control input. LOW selects VSYNC on rising edge
PDI	20	power-down imminent input: this input should be pulled LOW to indicate that the system is about to lose power
PL	21	phase-lock output: HIGH indicates that the system is phase-locked to the CVBS input
V_{SSA}	22	analog ground
CVBS1	23	CVBS input: this signal is applied via a 100 nF capacitor (nominal input 1 V (p-p)
CVBS2	24	this pin should be connected to ground if unused
BLACK	25	black level input: a 100 nF capacitor should be connected to V_{SSA}
I_{ref}	26	reference current input for analog circuits: for correct operation a 27 kΩ resistor should be connected to V_{SSA}
FRAME	27	Frame output for use in non-interlaced displays: during teletext off, teletext mixed with TV picture and subtitles this pin is inactive. In full teletext mode this pin provides a 25 Hz square wave. FRAME = 1 = odd, FRAME = 0 = even.
V_{SSD2}	28	digital ground 2
$\overline{COR}$	29	contrast reduction: active LOW output which allows selective contrast reduction of the television picture to enhance a mixed mode display
PON	30	picture on output: HIGH indicates that a TV picture is present and that the SAA526xPS is in TV mode, mix mode, subtitle mode or news flash mode
RGBREF	31	RGB reference input: drive level reference for RGB outputs
B	32	blue dot rate character output of the blue colour information: the high voltage level is defined by the RGBREF pin (can source 4 mA)

SYMBOL	PIN	DESCRIPTION
G	33	green dot rate character output of the green colour information: the high voltage level is defined by the RGBREF pin (can source 4 mA)
R	34	red dot rate character output of the red colour information: the high voltage level is defined by the RGBREF pin (can source 4 mA)
VDS	35	push-pull output for blanking the TV picture
HSYNC	36	horizontal sync input: the polarity of this pulse is set by input HSMODE
VSYNC	37	vertical sync input: the polarity of this pulse is set by input VSMODE
V_{DDA}	38	analog supply voltage (+5 V)
$V_{DDD(T)}$	39	digital supply voltage for teletext circuits (+5 V)
OSCGND	40	ground for crystal oscillator
XTALI	41	12 MHz crystal oscillator input
XTALO	42	12 MHz crystal oscillator output
RESET	43	reset input
$V_{DDD(M)}$	44	digital supply voltage for microcontroller (+5 V)
PUINL	45	power-up in list mode control input: LOW selects auto TOP/Fastext on power-up; HIGH selects LIST mode on power-up
DISDSR	46	disable default status row input: LOW enables display of status row
DIS8/30	47	disable packet 8/30 display input: LOW enables display of packet 8/30
DISLCBD	48	disable Link Control Byte (LCB) decode input: LOW enables decoding of the LCB in Fastext
SCLK2	49	serial clock input (I^2C-bus)
SDAT2	50	serial data input/output (I^2C-bus)
ME8/30T	51	mesh 8/30 and time displays input: HIGH will select a meshed display for the packet 8/30 and time
E/$\overline{W}$	52	East/West language select input: LOW selects West language

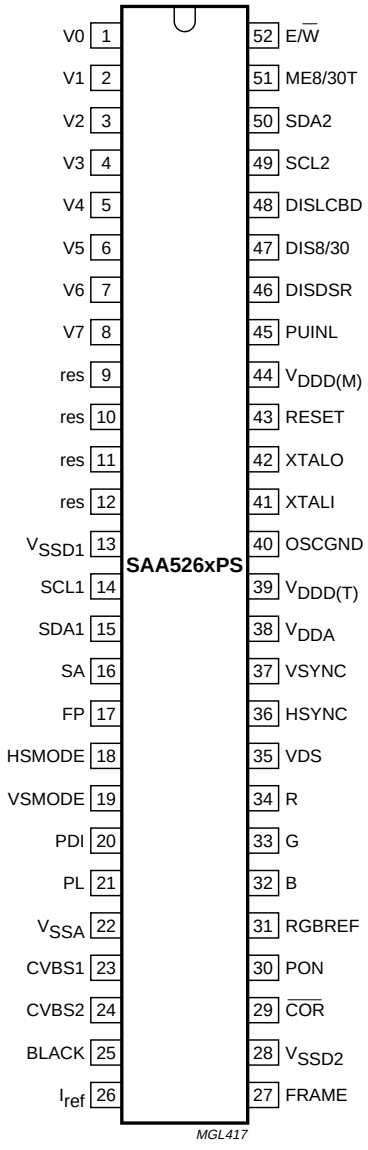


Fig.2 Pin configuration.

HIGH LEVEL COMMAND INTERFACE

The I²C-bus interface is used to pass control commands and data between the SAA526xPS and the television microcontroller. The interface uses high level commands, which are backward compatible with the SAFARI interface.

The formats for the I²C-bus transmission are as follows:

Table 1 User command

START	I²C-bus ADDRESS	WRITE	ACK	COMMAND	ACK	STOP

Table 2 System command

START	I²C-bus ADDRESS	WRITE	ACK	COMMAND	ACK	PARAMETER	ACK	STOP

Table 3 System read

START	I²C-bus ADDRESS	READ	ACK	DATA	NACK	STOP

Table 4 I²C-bus address

PIN 16 = LOW		PIN 16 = HIGH	
ADDRESS	**DESCRIPTION**	**ADDRESS**	**DESCRIPTION**
01 01 100	read = 1; write = 0	0110 000	read = 1; write = 0

Table 5 Control commands

COMMAND BYTE (HEX)	DATA BYTE	COMMAND DESCRIPTION
03	–	picture
04	–	TV status
07	–	time
10	–	program 0
11	–	program 1
12	–	program 2
13	–	program 3
14	–	program 4
15	–	program 5
16	–	program 6
17	–	program 7
18	–	program 8
19	–	program 9
1A	–	program 10
1B	–	program 11
1C	–	program 12
1D	–	program 13
1E	–	program 14
1F	–	program 15
20	–	red
21	–	green
22	–	yellow
23	–	subtitle
24	–	text status
25	–	hold
26	–	reveal
27	–	cancel
28	–	index
29	–	list toggle
2B	–	reveal toggle
2C	–	store
2D	–	previous
2F	–	subcode
30	–	digit 1
31	–	digit 2
32	–	digit 3

COMMAND BYTE (HEX)	DATA BYTE		COMMAND DESCRIPTION
33	–		digit 4
34	–		digit 5
35	–		digit 6
36	–		digit 7
37	–		digit 8
38	–		digit 9
39	–		digit 0
3A	–		size
3B	–		up
3C	–		down
3D	–		cyan
3E	–		mix
3F	–		text
4A	0		read PAL + line
89	00 to 41		select list
91	00 to 03 or 00 to 80		force mode
92	00		read broadcast status
93	00 or 01		read network identification
94	0		read PCS byte
98	OSD data		OSD mode on
99	0		OSD mode off
9A	0		OSD display on
9B	0		OSD display off
9C	0		OSD cursor on
9D	0		OSD cursor off
9E	0, row, column		OSD position
9F	0 followed by 20 bytes		OSD data write
A0	00 to FF		bitwise parameter or V7 to V0
A1	00 to FF		bitwise parameter and V7 to V0
A2	00 to FF		returns V7 to V0 on I^2C-bus read
A3	PWM No.	PWM data	PWM control
B0	reg	data	or text register
B1	reg	data	and text register
B2	reg	data	read text register
B8	0		quick list

COMMAND BYTE (HEX)	DATA BYTE	COMMAND DESCRIPTION
SAA5262 and SAA5263 only		
B9	0	get time
C0	0 = disable	set ACI mode
	1 = enable	
C1	0	get ACI status
C2	0	select next ACI channel
C3	information type	get ACI information
D0	0	get device version
D1	page type and page number	set page number
D2	page type	get page number
D3	page type and language	set language
D4	page type	get language
D5	row 24 control	enable/disable row 24
D6	start column and length string	set row 24 contents
D7	string type, index length and string	set string contents
D8	option type and values	set option
D9	movement type	move cursor
SAA5263 only		
C8	EPG mode	set EPG mode
C9	0	get EPG status
CA	number and list of features	set EPG feature list
CB	0	get number of EPG CNIs found
CC	CNI index	get found EPG CNIs
CD	number and list of CNIs	set EPG CNI list
CE	table type, item type and string index	get EPG item information

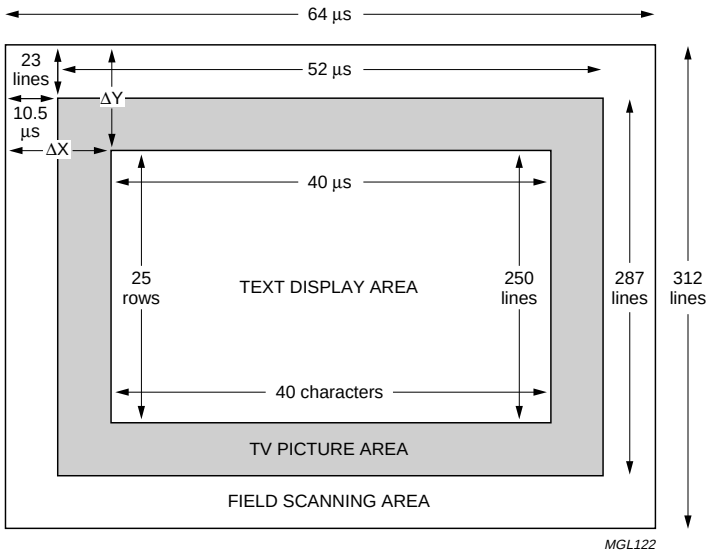


Fig.3 625 display format.

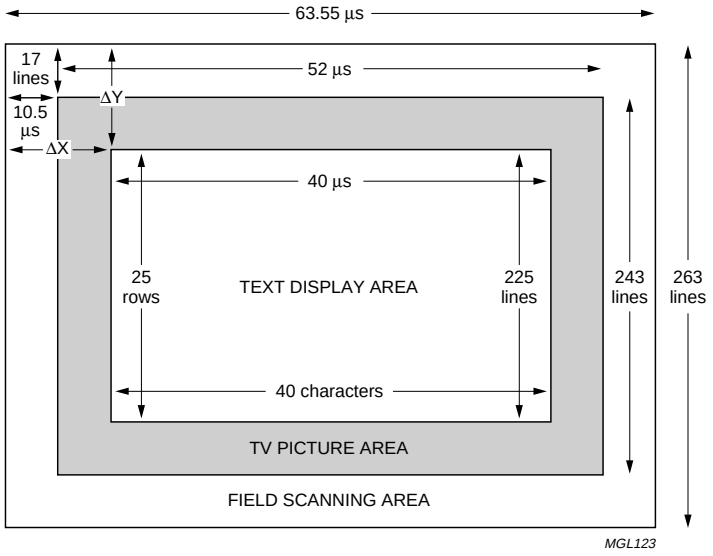


Fig.4 525 display format.

CHARACTER SETS

Geographical coverage

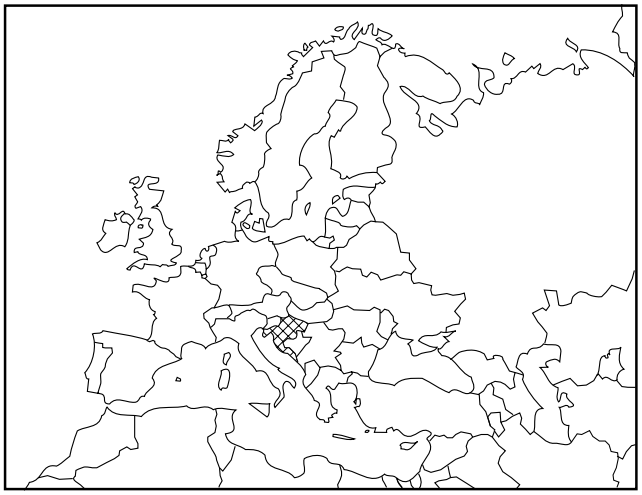


Fig.5 SAA5261PS/101 Yugoslavia.

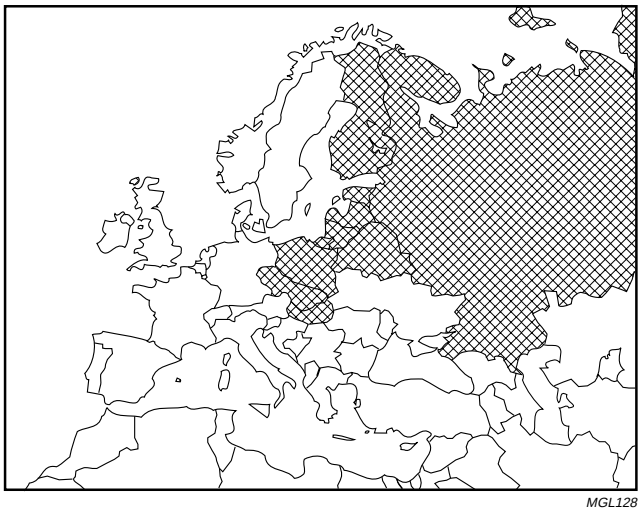


Fig.6 SAA5261PS/109 Cyrillic, SAA5262PS/122 Cyrillic.

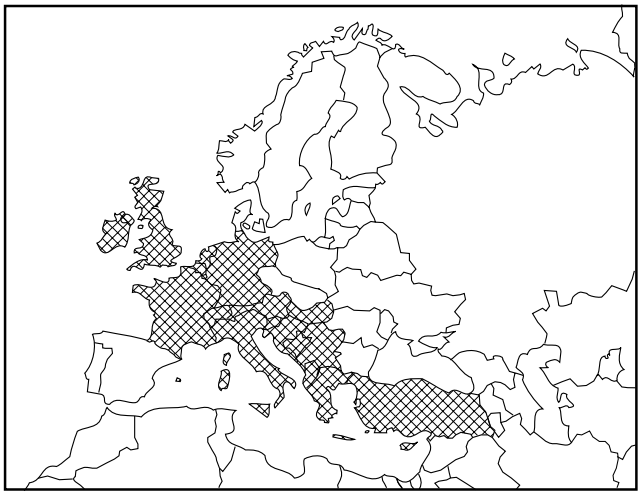


Fig.7 SAA5261/113 Greek/Turkish, SAA5262PS/123 Greek/Turkish.

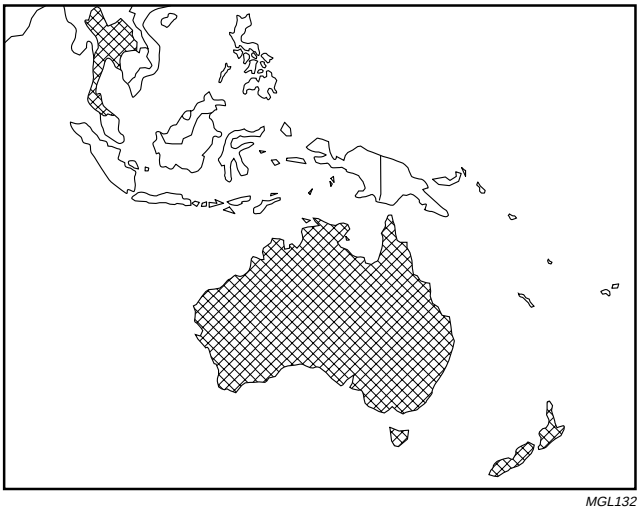


Fig.8 SAA5261PS/104 Thai, SAA5262PS/124 Thai.

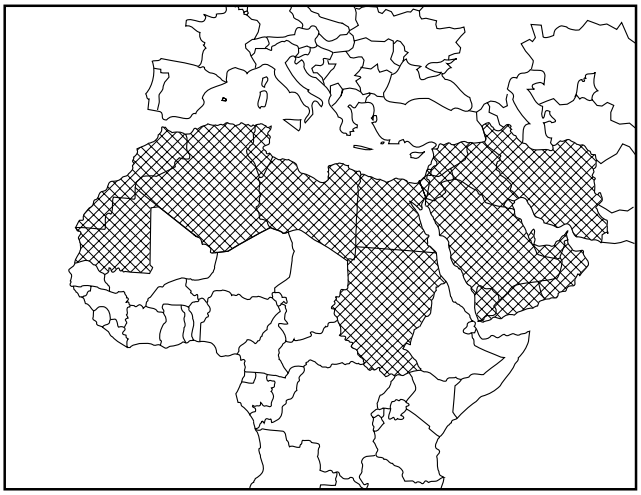


Fig.9 SAA5261P/105 Arabic/Hebrew, SAA5262PS/125 Arabic/Hebrew.

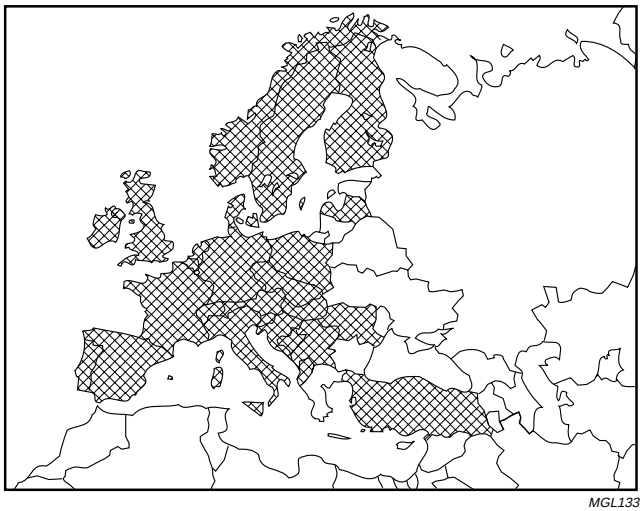


Fig.10 SAA5261PS/117 Pan-European, SAA5262PS/128 Pan-European/Eastern, SAA5263PS/137 Pan-European.

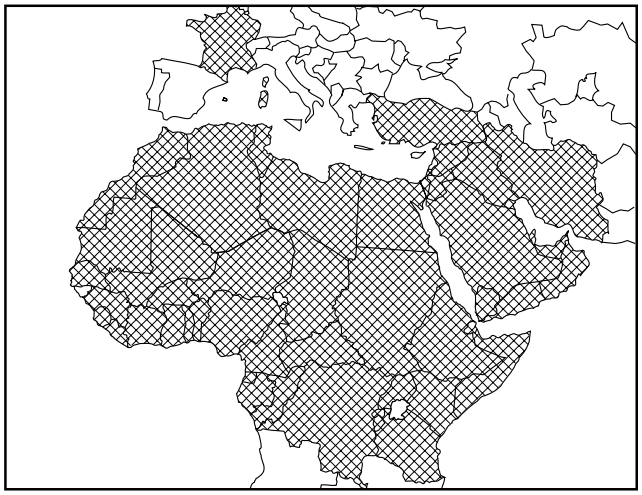


Fig.11 SAA5261PS/108 Arabic/English/French, SAA5262PS/126 Arabic/English/French.

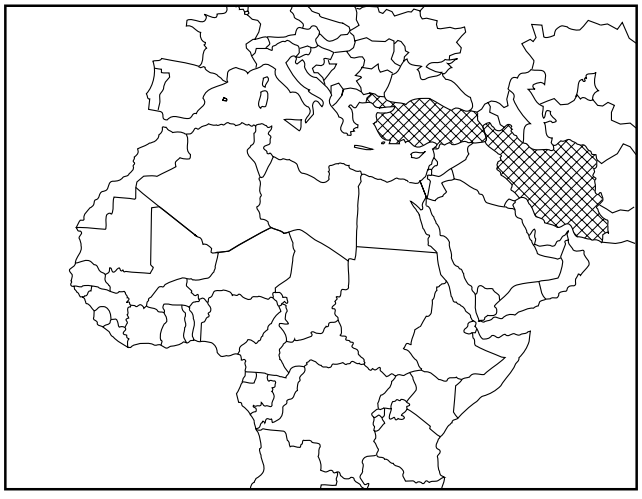


Fig.12 SAA5261PS/110 Iranian, SAA5262PS/120 Iranian.

The character sets for the languages Yugoslavian, Cyrillic, Greek/Turkish, Thai, Arabic/Hebrew, Pan-European, Arabic/English/French and Iranian are available on request.

LIMITING VALUES

In accordance with Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltages		–0.3	+6.5	V
V_{DDA}	analog supply voltage		–0.3	+6.5	V
V_I	input voltage (any input)	note 1	–0.3	$V_{DDD(M)}$ + 0.5	V
V_O	output voltage (any output)	note 1	–0.3	$V_{DDD(M)}$ + 0.5	V
I_O	output current (each output)		–	±10	mA
$I_{I/OK}$	DC input or output diode current		–	±20	mA
T_{amb}	operating ambient temperature		–20	+70	°C
T_{stg}	storage temperature		–55	+125	°C

Note

1. This maximum value has an absolute maximum of 6.5 V independent of V_{DDD}.

QUALITY AND RELIABILITY

This device will meet Philips Semiconductors general quality specification for business group *“Consumer Integrated Circuits SNW-FQ-611-Part E”*. The principal requirements are shown in Tables 6 to 9.

Group A

Table 6 Acceptance tests per lot; note 1

TEST	REQUIREMENTS
Mechanical	cumulative target: <80 ppm
Electrical	cumulative target: <80 ppm

Note

1. ppm = fraction of defective devices, in parts per million.

Group B

Table 7 Processability tests (by package family); note 1

TEST	REQUIREMENTS
Solderability	<7% LTPD
Mechanical	<15% LTPD
Solder heat resistance	<15% LTPD

Note

1. LTPD = Lot Tolerance Percent Defective.

Group C

Table 8 Reliability tests (by package family); note 1

TEST	CONDITIONS	REQUIREMENTS
Operational life	168 hours at T_j = 150 °C	<1000 FPM at T_j = 70 °C
Humidity life	temperature, humidity, bias 1000 hours, T_{amb} = 85 °C, 85% RH (or equivalent test)	<2000 FPM
Temperature cycling performance	$T_{stg(min)}$ to $T_{stg(max)}$	<2000 FPM

Note

1. FPM = fraction of devices failing at test conditions, in Failures Per Million.

Table 9 Reliability tests (by device type)

TEST	CONDITIONS	REQUIREMENTS
ESD and latch-up	ESD human body model 100 pF, 1.5 kΩ	<2000 V
	ESD machine model 200 pF, 0 Ω	<200 V
	latch-up	100 mA, 1.5V_{DDD} (absolute maximum)

CHARACTERISTICS

$V_{DDD(M)}$ = 5 V ±10%; V_{SS} = 0 V; T_{amb} = –20 to +70°C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
$V_{DDD(M)}$	microcontroller supply voltage	referenced to V_{SSD}	4.5	5.0	5.5	V
V_{DDA}	analog supply voltage	referenced to V_{SSD}	4.5	5.0	5.5	V
$V_{DDD(T)}$	teletext supply voltage	referenced to V_{SSD}	4.5	5.0	5.5	V
$I_{DDD(M)}$	microcontroller supply current		–	20	35	mA
I_{DDA}	analog supply current		–	35	50	mA
$I_{DDD(T)}$	teletext supply current		–	50	80	mA
Digital inputs						
PIN RESET						
V_{IL}	LOW-level input voltage		–0.3	–	0.2$V_{DDD(M)}$ – 0.1	V
V_{IH}	HIGH-level input voltage		0.7$V_{DDD(M)}$	–	$V_{DDD(M)}$ + 0.3	V
I_{LI}	input leakage current	V_i = 0 to $V_{DDD(M)}$	–10	–	+10	µA
C_i	input capacitance		–	–	4	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PINS HSYNC AND VSYNC						
$V_{th(f)}$	switching threshold falling		$0.2V_{DDD(M)}$	–	–	V
$V_{th(r)}$	switching threshold rising		–	–	$0.8V_{DDD(M)}$	V
V_{hys}	hysteresis voltage		–	$0.33V_{DDD(M)}$	–	V
C_i	input capacitance		–	–	4	pF
Digital outputs						
PINS R, G AND B: note 1						
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	0	–	0.2	V
V_{OH}	HIGH-level output voltage	I_{OH} = –2 mA	V_{RGBREF} – 0.3	V_{RGBREF}	V_{RGBREF} + 0.4	V
$\lvert Z_O \rvert$	output impedance		–	–	150	Ω
C_L	load capacitance		–	–	50	pF
I_O	DC output current		–	–	–4	mA
$t_{o(r)}$	output rise time	between 10 and 90%; C_L = 50 pF	–	–	20	ns
$t_{o(f)}$	output fall time	between 90 and 10%; C_L = 50 pF	–	–	20	ns
PIN VDS						
V_{OL}	LOW-level output voltage	I_{OL} = 1.6 mA	0	–	0.2	V
V_{OH}	HIGH-level output voltage	I_{OH} = –1.6 mA	$V_{DDD(M)}$ – 0.3	–	$V_{DDD(M)}$ + 0.4	V
C_L	load capacitance		–	–	50	pF
$t_{o(r)}$	output rise time	between 10 and 90%; C_L = 50 pF	–	–	20	ns
$t_{o(f)}$	output fall time	between 90 and 10%; C_L = 50 pF	–	–	20	ns
PINS R, G, B AND VDS						
$t_{d(skew)}$	skew delay between any two pins		–	–	20	ns
PIN $\overline{COR}$ (OPEN-DRAIN OUTPUT)						
V_{OH}	HIGH-level pull-up output voltage		–	–	$V_{DDD(M)}$	V
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	0	–	0.5	V
I_{OL}	LOW-level output current		–	–	2	mA
C_L	load capacitance		–	–	25	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PIN FRAME						
V_{OH}	HIGH-level output voltage	I_{OL} = 8 mA	0	–	0.5	V
V_{OL}	LOW-level output voltage	I_{OL} = –8 mA	$V_{DDD(M)}$ – 0.5	–	$V_{DDD(M)}$	V
I_{OL}	LOW-level output current		–8	–	+8	mA
C_L	load capacitance		–	–	100	pF
Digital inputs/outputs						
PINS V0 TO V7						
V_{IL}	LOW-level input voltage		–0.3	–	$0.2V_{DDD(M)}$ – 0.1	V
V_{IH}	HIGH-level input voltage		3.0	–	$V_{DDD(M)}$ + 0.3	V
C_i	input capacitance		–	–	4	pF
V_{OL}	LOW-level output voltage	I_{OL} = 10 mA	0	–	0.45	V
C_L	load capacitance		–	–	50	pF
PINS SCL AND SDA (PINS 14, 15, 49 AND 50)						
V_{IL}	LOW-level input voltage		–0.3	–	+1.5	V
V_{IH}	HIGH-level input voltage		3.0	–	$V_{DDD(M)}$ + 0.3	V
C_i	input capacitance		–	–	5	pF
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	0	–	0.5	V
C_L	load capacitance		–	–	400	pF
$t_{o(f)}$	output fall time	between 3 and 1 V	–	–	200	ns
Digital inputs						
PINS VSMODE, HSMODE, PDI, SA, FP, PUINL, DISDSR, DIS8/30, DISLCBD, ME8/30T AND E/$\overline{W}$						
V_{IL}	LOW-level input voltage		–0.3	–	$0.2V_{DDD(M)}$ – 0.1	V
V_{IH}	HIGH-level input voltage		$0.2V_{DDD(M)}$ + 0.9	–	$V_{DDD(M)}$ + 0.3	V
C_i	input capacitance		–	–	4	pF
C_L	load capacitance		–	–	50	pF
Digital outputs						
PINS PL AND PON						
V_{OL}	LOW-level output voltage	I_{OL} = 10 mA	0	–	0.45	V
C_L	load capacitance		–	–	50	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog inputs						
PINS CVBS0 AND CVBS1						
V_{sync}	sync voltage amplitude		0.1	0.3	0.6	V
$V_{vid(p-p)}$	video input voltage amplitude (peak-to-peak value)		0.7	1.0	1.4	V
Z_{source}	source impedance		–	–	250	Ω
V_{IH}	HIGH-level input voltage		3.0	–	$V_{DDD(M)}$ + 0.3	V
$\|Z_i\|$	input impedance		2.5	5.0	–	kΩ
C_i	input capacitance		–	–	10	pF
PIN I_{ref}						
R_{VSS}	resistor to ground		–	27	–	kΩ
RGBREF: note 1						
V_i	input voltage		–0.3	–	$V_{DDD(M)}$	V
I_I	DC input current		–	–	12	mA
Analog input/output						
PIN BLACK						
C_{BLACK}	storage capacitor to ground		–	100	–	nF
V_{BLACK}	black level voltage for nominal sync amplitude		1.8	2.15	2.5	V
I_{LI}	input leakage current		–10	–	+10	μA
Crystal oscillator						
PIN XTALI						
V_{IL}	LOW-level input voltage		–0.3	–	$0.2V_{DDD(M)} - 0.1$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDD(M)}$	–	$V_{DDD(M)}$ + 0.3	V
C_i	input capacitance		–	–	10	pF
PIN XTALO						
C_o	output capacitance		–	–	10	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CRYSTAL SPECIFICATION: note 2						
f_{xtal}	nominal frequency		–	12	–	MHz
C_L	load capacitance		–	32	–	pF
C1	series capacitance	T_{amb} = 25 °C	–	18.5	–	fF
C0	parallel capacitance	T_{amb} = 25 °C	–	4.9	–	pF
R_{res}	resonance resistance	T_{amb} = 25 °C	–	35	–	Ω
T_{xtal}	temperature range		–20	+25	+70	°C
X_j	adjustment tolerance	T_{amb} = 25 °C	–	–	$\pm 50 \times 10^{-6}$	
X_d	drift		–	–	$\pm 30 \times 10^{-6}$	

Notes

1. All RGB current is sourced from the RGBREF pin. The maximum effective series resistance between RGBREF and the R, G and B pins is 150 Ω.
2. Crystal order number 4322 143 05561.

TIMING CHARACTERISTICS

SYMBOL	PARAMETER	INPUT	OUTPUT	I²C-BUS SPECIFICATION
SCL timing				
$t_{HD;STA}$	START condition hold time	≥4.0 µs	note 1	≥4.0 µs
t_{LOW}	SCL LOW time	≥4.7 µs	note 1	≥4.7 µs
t_{HIGH}	SCL HIGH time	≥4.0 µs	≥4.0 µs; note 2	≥4.0 µs
$t_{r(SCL)}$	SCL rise time	≤1.0 µs	note 3	≤1.0 µs
$t_{f(SCL)}$	SCL fall time	≤0.3 µs	≤0.3 µs; note 4	≤0.3 µs
SDA timing				
$t_{SU;DAT1}$	data set-up time	≥250 ns	note 1	≥250 ns
$t_{HD;DAT}$	data hold time	≥0 ns	note 1	≥0 ns
$t_{SU;STA}$	repeated START set-up time	≥4.7 µs	note 1	≥4.7 µs
$t_{SU;STO}$	STOP condition set-up time	≥4.0 µs	note 1	≥4.0 µs
t_{BUF}	bus free time	≥4.7 µs	note 1	≥4.7 µs
$t_{r(SDA)}$	SDA rise time	≤1.0 µs	note 3	≤1.0 µs
$t_{f(SDA)}$	SDA fall time	≤0.3 µs	≤0.3 µs; note 4	≤0.3 µs

Notes

1. This parameter is determined by the user software. It must comply with the I²C-bus specification.
2. This value gives the auto-clock pulse length which meets the I²C-bus specification for the special crystal frequency. Alternative, the SCL pulse must be timed by software.
3. The rise time is determined by the external bus line capacitance and pull-up resistor. It must be less than 1 µs.
4. The maximum capacitance on bus lines SDA and SCL is 400 pF.

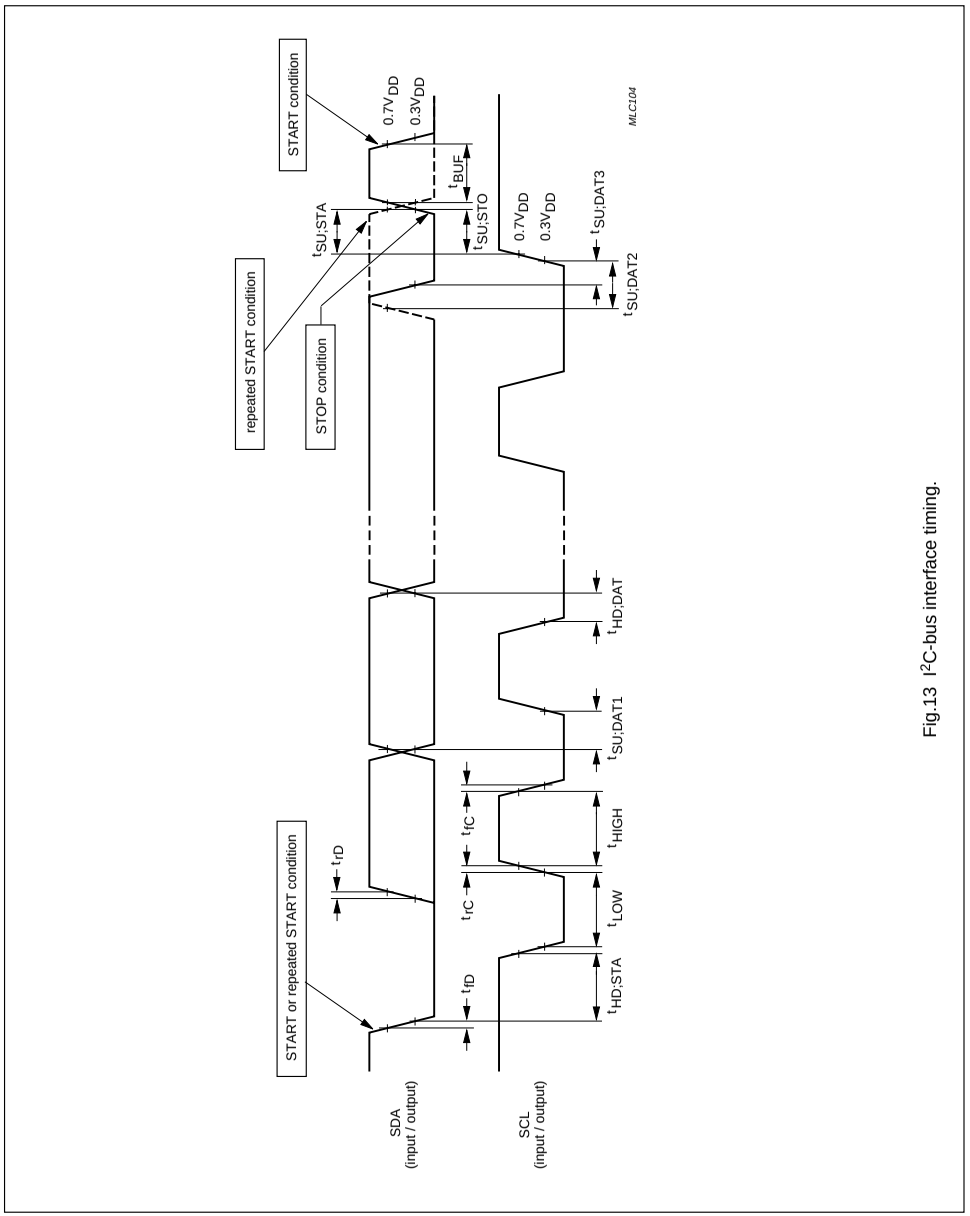
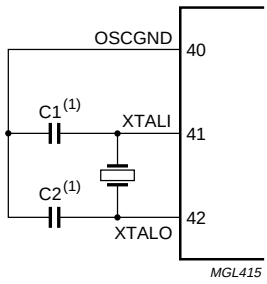


Fig.13 I²C-bus interface timing.

CLOCK GENERATOR

The oscillator circuit is a single-stage inverting amplifier in a Pierce oscillator configuration. The circuitry between pins XTALI and XTALO is basically an inverter biased to the transfer point. A crystal must be used as the feedback element to complete the oscillator circuitry. It is operated in parallel resonance. XTALI is the high gain amplifier input and XTALO is the output.

To drive the device externally XTALI is driven from an external source and XTALO is left open-circuit.



(1) The values of C1 and C2 depend on the crystal specification: $C1 = C2 = 2C_L$.

Fig.14 Oscillator circuit.

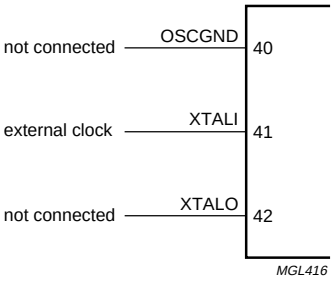


Fig.15 Oscillator circuit driven from external source.

EMC GUIDELINES

Optimization of circuit return paths and minimisation of common mode noise will be assisted by using a double-sided PCB with a low inductance ground plane.

On a single-sided PCB a local ground plane under the whole IC should be present, as shown in Fig.16. This should be connected by the widest possible connection back to the PCB ground connection and bulk electrolytic decoupling capacitor. It should preferably not connect to other grounds on the way and no wire links should be present in this connection. The use of wire links increases ground bounce by introducing inductance into the ground.

The supply pins can be decoupled at the pin to the ground plane under the IC. This is easily accomplished using surface mount capacitors, which are more effective than leaded components at high frequency. Using a device socket will unfortunately add to the area and inductance of the external bypass loop.

A ferrite bead or inductor with resistive characteristics at high frequency may be utilized in the supply line close to the decoupling capacitor to provide a high impedance. To prevent pollution by conduction onto signal lines (which may then radiate) signals connected to the +5 V supply via a pull up resistor should not be connected to the IC side of the ferrite component.

OSCGND should be connected only to the crystal load capacitors and not the local or circuit ground.

Keep physical connection distances to associated active devices short.

Route output traces with close proximity mutually coupled ground return paths.

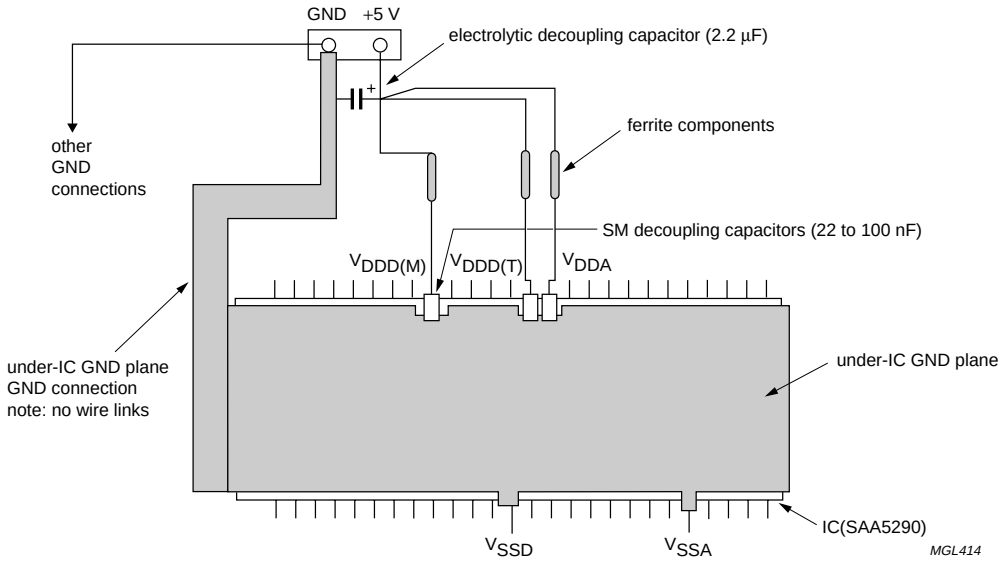


Fig.16 Power supply and ground connections for SOT247-1.

APPLICATION INFORMATION

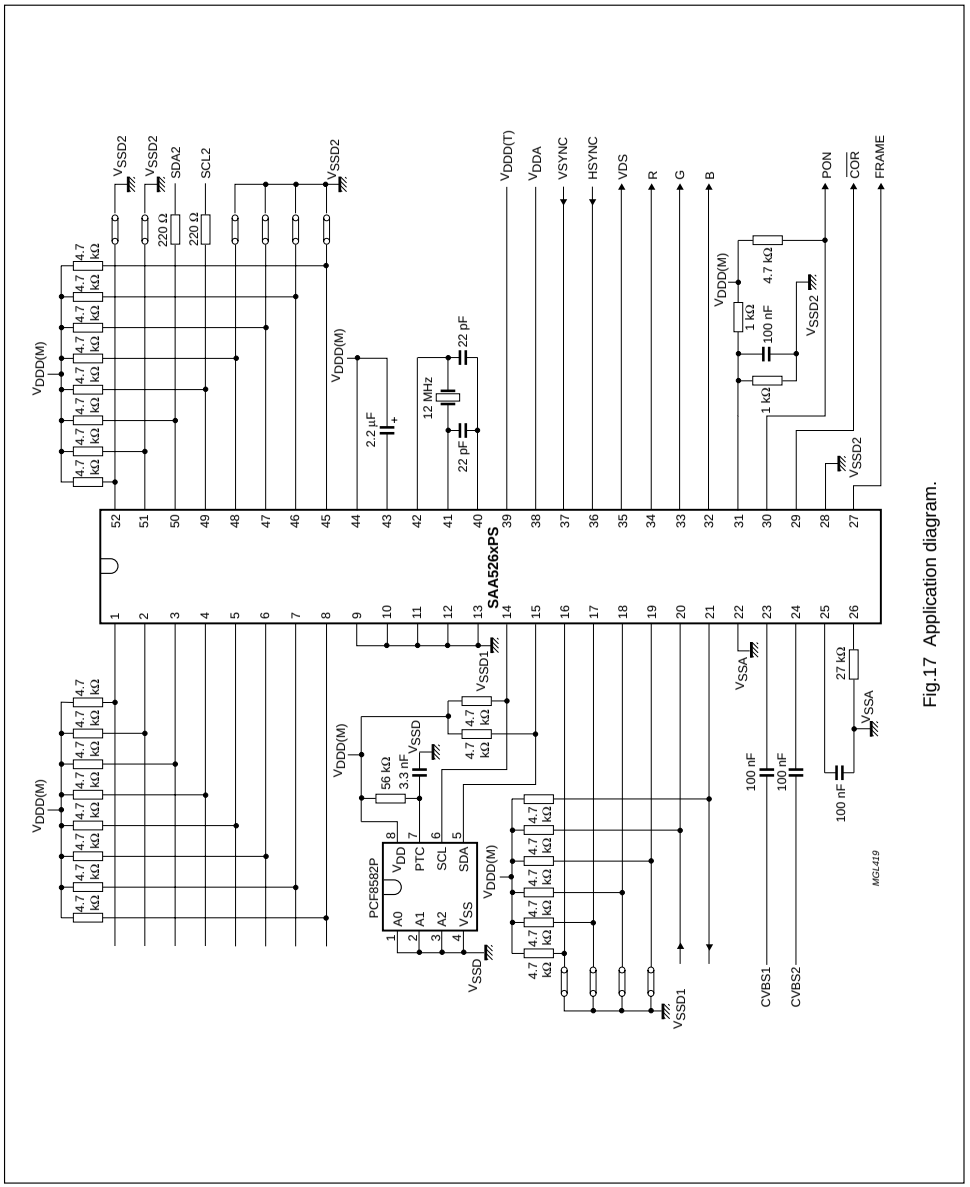
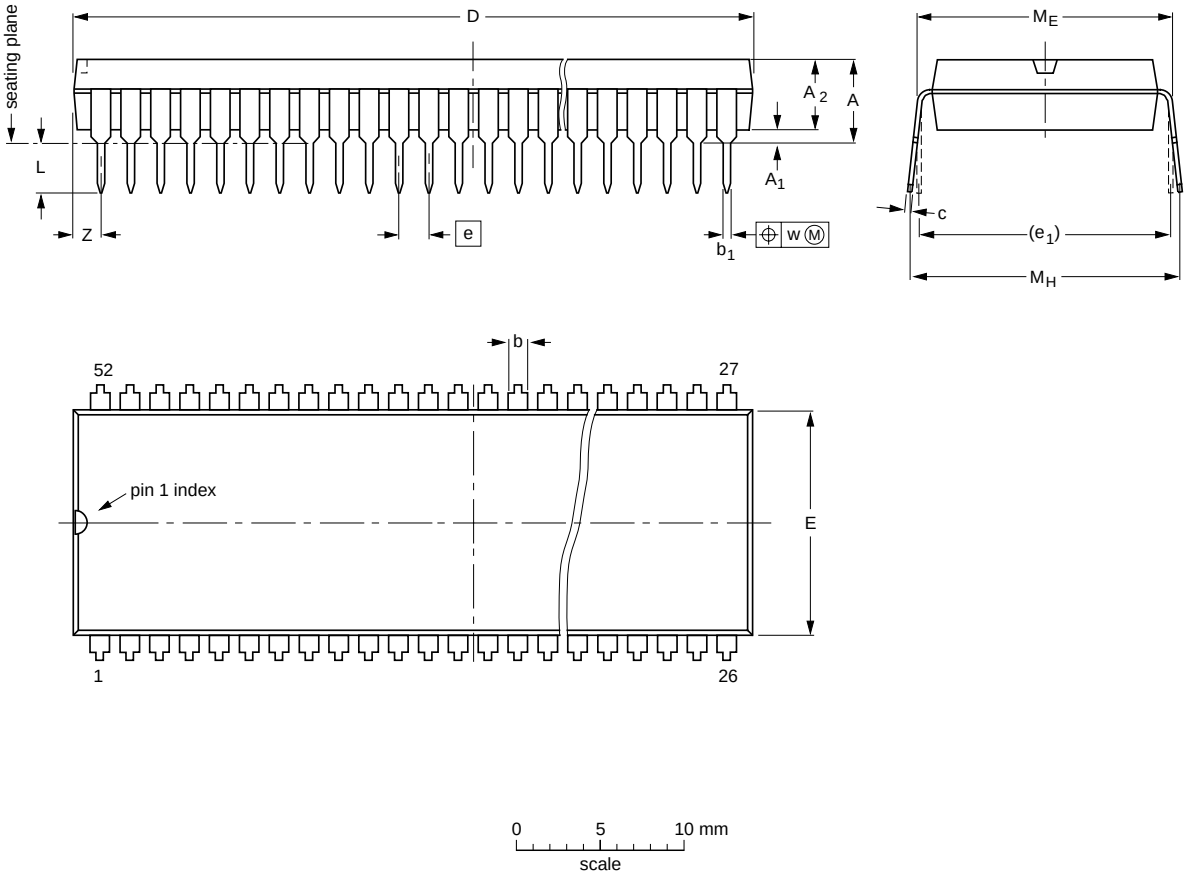


Fig.17 Application diagram.

PACKAGE OUTLINE

SDIP52: plastic shrink dual in-line package; 52 leads (600 mil) **SOT247-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.08	0.51	4.0	1.3 0.8	0.53 0.40	0.32 0.23	47.9 47.1	14.0 13.7	1.778	15.24	3.2 2.8	15.80 15.24	17.15 15.90	0.18	1.73

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT247-1						~~90-01-22~~ 95-03-11

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
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Where application information is given, it is advisory and does not form part of the specification.	

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