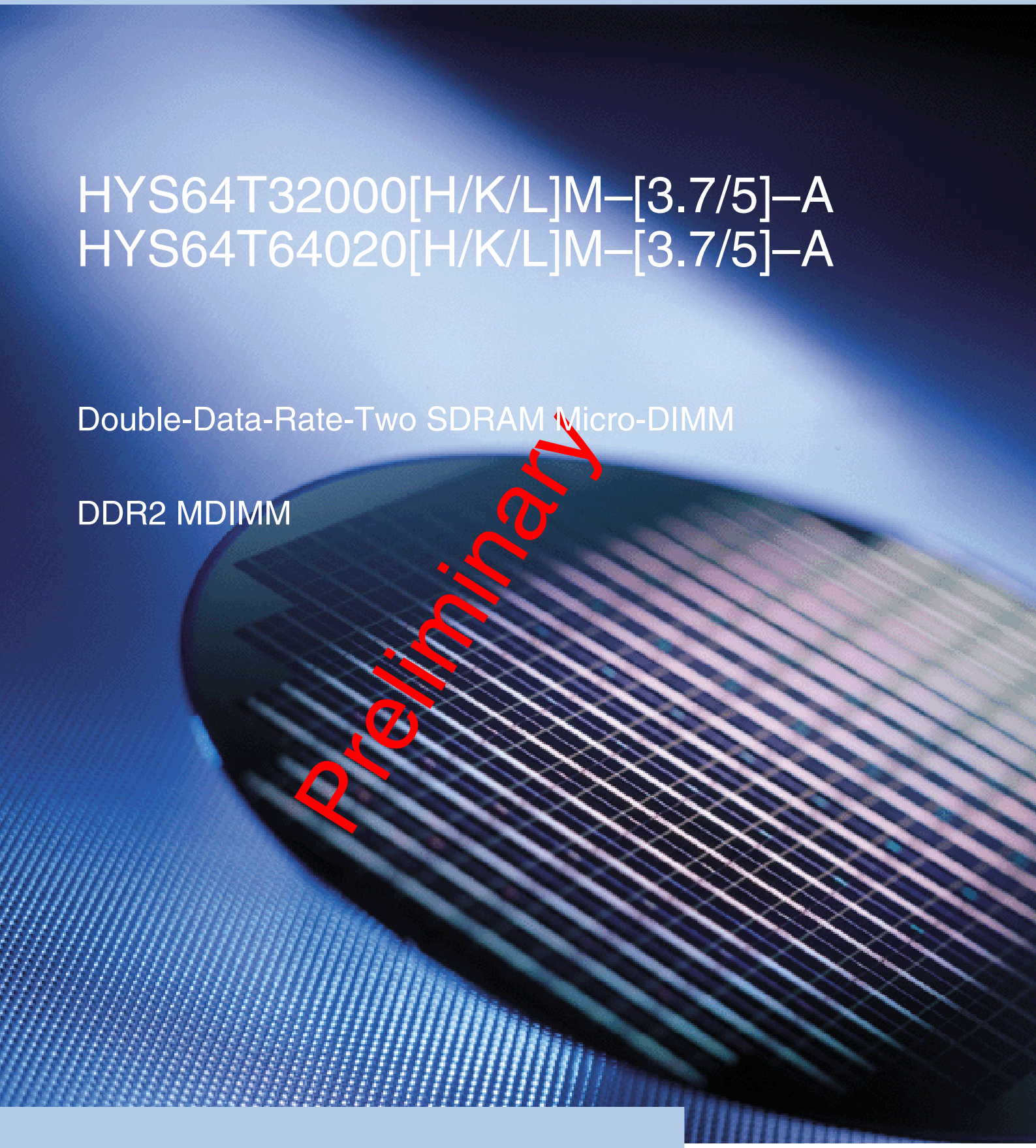
HYS64T32000[H/K/L]M–[3.7/5]–A
HYS64T64020[H/K/L]M–[3.7/5]–A

Double-Data-Rate-Two SDRAM Micro-DIMM

DDR2 MDIMM



Memory Products

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HYS64T32000[H/K/L]M–[3.7/5]–A
HYS64T64020[H/K/L]M–[3.7/5]–A

Double-Data-Rate-Two SDRAM Micro-DIMM

DDR2 MDIMM

Preliminary

Memory Products

Never stop thinking.

HYS64T[3200/6402]0[H/K/L]M–[3.7/5]–A
Preliminary

Revision History:	**Rev. 0.6**	**2004-06**
Previous Revision:	Rev. 0.5	2004-04

Page	Subjects (major changes since last revision)
All	Added production variants with “H” instead of “L” in product type

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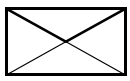

Preliminary

Table of Contents

1 Overview

This chapter gives an overview of the Double-Data-Rate-Two SDRAM Micro-DIMM product family and describes its main characteristics.

1.1 Features

- 214-pin PC2-4200 and PC2-3200 DDR2 SDRAM memory modules for use as main memory when installed in systems such as mobile personal computers.
- 32M × 64 and 64M × 64 module organisation and 32M × 16 chip organisation
- JEDEC standard Double-Data-Rate-Two Synchronous DRAMs (DDR2 SDRAM) with a single + 1.8 V (± 0.1 V) power supply
- Built with 512Mb DDR2 SDRAMs in P-TFBGA-84-2 chipsize packages
- Programmable CAS Latencies (3, 4 and 5), Burst Length (8 & 4) and Burst Type
- Burst Refresh, Distributed Refresh and Self Refresh
- All inputs and outputs SSTL_1.8 compatible
- OCD (Off-Chip Driver Impedance Adjustment) and ODT (On-Die Termination)
- Serial Presence Detect with E^2PROM
- Micro-DIMM Dimensions (nominal) : 30 mm high, 54.0 mm wide
- Based on JEDEC standard reference layouts Raw Card “A” & “B”
- 2-piece type Mezzanine Socket with 0,4 mm contact centers

Table 1 Performance

Product Type Speed Code			**–3.7**	**–5**	**Units**
Speed Grade			PC2–4200 4–4–4	PC2–3200 3–3–3	—
max. Clock Frequency	@CL5	f_{CK5}	266	200	MHz
	@CL4	f_{CK4}	266	200	MHz
	@CL3	f_{CK3}	200	200	MHz
min. RAS-CAS-Delay		t_{RCD}	15	15	ns
min. Row Precharge Time		t_{RP}	15	15	ns
min. Row Active Time		t_{RAS}	45	45	ns
min. Row Cycle Time		t_{RC}	60	60	ns

1.2 Description

The INFINEON HYS64T[3200/6402]0[H/K/L]M–[3.7/5]–A module family are low profile Unbuffered Micro-DIMM modules “MDIMMs” with 30,0 mm height based on DDR2 technology. DIMMs are available as 32M × 64 and 64M × 64 organisation and density, intended for mounting into 214-pin mezzanine connector sockets.

The memory array is designed with 512Mb Double-Data-Rate-Two (DDR2) Synchronous DRAMs. Decoupling capacitors are mounted on the PCB board. The DIMMs feature serial presence detect based on a serial E^2PROM device using the 2-pin I^2C protocol. The first 128 bytes are programmed with configuration data and are write protected; the second 128 bytes are available to the customer.

Table 2 Ordering Information

Product Type	Compliance Code	Description	SDRAM Technology
HYS64T64020KM-3.7-A	512MB 2Rx16 PC2-4200M-444-11-A0	two ranks 512 MByte DIMM	512 Mbit (×16)
HYS64T32000KM-3.7-A	256MB 1Rx16 PC2-4200M-444-11-B0	one rank 256 MByte DIMM	
HYS64T64020KM-5-A	512MB 2Rx16 PC2-3200M-333-11-A0	two ranks 512 MByte DIMM	
HYS64T32000KM-5-A	256MB 1Rx16 PC2-3200M-333-11-B0	one rank 256 MByte DIMM	
HYS64T64020HM-3.7-A	512MB 2Rx16 PC2-4200M-444-11-A0	two ranks 512 MByte DIMM	512 Mbit (×16)
HYS64T64020LM-3.7-A	512MB 2Rx16 PC2-4200M-444-11-A0	two ranks 512 MByte DIMM	green Product
HYS64T32000HM-3.7-A	256MB 1Rx16 PC2-4200M-444-11-B0	one rank 256 MByte DIMM	
HYS64T32000LM-3.7-A	256MB 1Rx16 PC2-4200M-444-11-B0	one rank 256 MByte DIMM	
HYS64T64020HM-5-A	512MB 2Rx16 PC2-3200M-333-11-A0	two ranks 512 MByte DIMM	
HYS64T64020LM-5-A	512MB 2Rx16 PC2-3200M-333-11-A0	two ranks 512 MByte DIMM	
HYS64T32000HM-5-A	256MB 1Rx16 PC2-3200M-333-11-B0	one rank 256 MByte DIMM	
HYS64T32000LM-5-A	256MB 1Rx16 PC2-3200M-333-11-B0	one rank 256 MByte DIMM	

The Compliance Code is printed on the module label and provides technical details to the user, e. g. "512MB 2R×16 PC2-4200M-444-11-A0" where "512MB" tells the density in megabytes, "2R ×16" means 2 ranks on module built of ×16 components, "PC2-4200M" means DDR2 Micro-DIMM with 4.26 GB/s module bandwidth, "444-11" means CAS latency of 4, RCD[1] latency of 4, and RP[2] latency of 4 using JEDEC SPD revision 1.1, and “A0” means JEDEC raw card A revision 0.

All product types end with a place code, designating the silicon die revision. Example: HYS72T64000KM–5–A, indicating Rev. A dies are used for DDR2 SDRAM components. For all INFINEON DDR2 module and component nomenclature see **Chapter 8** of this data sheet.

Table 3 Address Format

DIMM Density	Module Organization	Memory Ranks	# of SDRAMs	# of row/bank/column bits	Raw Card
256 MByte	32M × 64	1	4	13/2/10	B
512 MByte	64M × 64	2	8	13/2/10	A

Table 4 Components on Modules[1)]

Product Type	DRAM Components	DRAM Density	DRAM Organisation
HYS64T32000HM[2)] HYS64T32000LM[2)]	HYB18T512160AF[2)]	512 Mbit	32M × 16
HYS64T32000KM	HYB18T512160AC	512 Mbit	32M × 16
HYS64T64020HM[2)] HYS64T64020LM[2)]	HYB18T512160AF[2)]	512 Mbit	32M × 16
HYS64T64020KM	HYB18T512160AC	512 Mbit	32M × 16

1) For a detailed description of all functionalities of the DRAM components on these modules see the component data sheet.

2) Green Product

1) RCD: Row Column Delay

2) RP: Row Precharge

1.3 Pin Configuration

The pin configuration of the DDR2 SDRAM Micro-DIMM is listed by function in **Table 5** (214 pins). The abbreviations used in columns Pin and Buffer Type are explained in **Table 6** and **Table 7** respectively. The pin numbering is depicted in **Figure 1**.

Table 5 Pin Configuration of MDIMM

Pin#	Name	Pin Type	Buffer Type	Function
Clock Signals				
122	CK0	I	SSTL	**Clock Signals 1:0**
194	CK1	I	SSTL	
123	$\overline{CK0}$	I	SSTL	**Complement Clock Signals 1:0**
195	$\overline{CK1}$	I	SSTL	
43	CKE0	I	SSTL	**Clock Enables**
147	CKE1	I	SSTL	*Note: 2-rank module*
	NC	NC		*Note: 1-rank module*
Control Signals				
165	$\overline{S0}$	I	SSTL	**Chip Select Rank 0**
62	$\overline{S1}$	I	SSTL	**Chip Select Rank 1** *Note: 2-rank module*
	NC	NC		*Note: 1-rank module*
163	$\overline{RAS}$	I	SSTL	**Row Address Strobe**
60	$\overline{CAS}$	I	SSTL	**Column Address Strobe**
56	$\overline{WE}$	I	SSTL	**Write Enable**
Address Signals				
55	BA0	I	SSTL	**Bank Address 1:0**
162	BA1	I	SSTL	
161	A0	I	SSTL	**Address Inputs 9:0**
159	A1	I	SSTL	
52	A2	I	SSTL	
158	A3	I	SSTL	
51	A4	I	SSTL	
50	A5	I	SSTL	
157	A6	I	SSTL	
48	A7	I	SSTL	
155	A8	I	SSTL	
154	A9	I	SSTL	
54	A10	I	SSTL	**Address Input 10/Autoprecharge**
	AP	I	SSTL	
47	A11	I	SSTL	**Address Input 11**
153	A12	I	SSTL	**Address Input 12**

Table 5 Pin Configuration of MDIMM

Pin#	Name	Pin Type	Buffer Type	Function
Data Signals				
3	DQ0	I/O	SSTL	**Data Bus 63:0**
4	DQ1	I/O	SSTL	
9	DQ2	I/O	SSTL	
10	DQ3	I/O	SSTL	
109	DQ4	I/O	SSTL	
110	DQ5	I/O	SSTL	
114	DQ6	I/O	SSTL	
115	DQ7	I/O	SSTL	
12	DQ8	I/O	SSTL	
13	DQ9	I/O	SSTL	
21	DQ10	I/O	SSTL	
22	DQ11	I/O	SSTL	
117	DQ12	I/O	SSTL	
118	DQ13	I/O	SSTL	
125	DQ14	I/O	SSTL	
126	DQ15	I/O	SSTL	
24	DQ16	I/O	SSTL	
25	DQ17	I/O	SSTL	
30	DQ18	I/O	SSTL	
31	DQ19	I/O	SSTL	
128	DQ20	I/O	SSTL	
129	DQ21	I/O	SSTL	
133	DQ22	I/O	SSTL	
134	DQ23	I/O	SSTL	
33	DQ24	I/O	SSTL	
34	DQ25	I/O	SSTL	
38	DQ26	I/O	SSTL	
39	DQ27	I/O	SSTL	
136	DQ28	I/O	SSTL	
137	DQ29	I/O	SSTL	
142	DQ30	I/O	SSTL	
143	DQ31	I/O	SSTL	
67	DQ32	I/O	SSTL	
68	DQ33	I/O	SSTL	
73	DQ34	I/O	SSTL	
74	DQ35	I/O	SSTL	
174	DQ36	I/O	SSTL	
175	DQ37	I/O	SSTL	
179	DQ38	I/O	SSTL	

Table 5 Pin Configuration of MDIMM

Pin#	Name	Pin Type	Buffer Type	Function
180	DQ39	I/O	SSTL	**Data Bus 63:0**
76	DQ40	I/O	SSTL	
77	DQ41	I/O	SSTL	
81	DQ42	I/O	SSTL	
82	DQ43	I/O	SSTL	
182	DQ44	I/O	SSTL	
183	DQ45	I/O	SSTL	
188	DQ46	I/O	SSTL	
189	DQ47	I/O	SSTL	
84	DQ48	I/O	SSTL	
85	DQ49	I/O	SSTL	
92	DQ50	I/O	SSTL	
93	DQ51	I/O	SSTL	
191	DQ52	I/O	SSTL	
192	DQ53	I/O	SSTL	
200	DQ54	I/O	SSTL	
201	DQ55	I/O	SSTL	
95	DQ56	I/O	SSTL	
96	DQ57	I/O	SSTL	
101	DQ58	I/O	SSTL	
102	DQ59	I/O	SSTL	
203	DQ60	I/O	SSTL	
204	DQ61	I/O	SSTL	
208	DQ62	I/O	SSTL	
209	DQ63	I/O	SSTL	
112	DM0	I	SSTL	**Data Masks 7:0**
120	DM1	I	SSTL	*Note: See block diagram for corresponding DQ M signals*
131	DM2	I	SSTL	
36	DM3	I	SSTL	
177	DM4	I	SSTL	
79	DM5	I	SSTL	
90	DM6	I	SSTL	
206	DM7	I	SSTL	

Table 5 Pin Configuration of MDIMM

Pin#	Name	Pin Type	Buffer Type	Function
7	DQS0	I/O	SSTL	**Data Strobes 7:0**
6	$\overline{\text{DQS0}}$	I/O	SSTL	*Note: See block diagram for corresponding DQS signals*
19	DQS1	I/O	SSTL	
18	$\overline{\text{DQS1}}$	I/O	SSTL	
28	DQS2	I/O	SSTL	
27	$\overline{\text{DQS2}}$	I/O	SSTL	
140	DQS3	I/O	SSTL	
139	$\overline{\text{DQS3}}$	I/O	SSTL	
71	DQS4	I/O	SSTL	
70	$\overline{\text{DQS4}}$	I/O	SSTL	
186	DQS5	I/O	SSTL	
185	$\overline{\text{DQS5}}$	I/O	SSTL	
198	DQS6	I/O	SSTL	
197	$\overline{\text{DQS6}}$	I/O	SSTL	
99	DQS7	I/O	SSTL	
98	$\overline{\text{DQS7}}$	I/O	SSTL	
EEPROM				
105	SCL	I	CMOS	**Serial Presence Detect (SPD) Clock Input**
104	SDA	I/O	OD	**SPD Data Input/Output**
211	SA0	I	CMOS	**SPD Address 1:0**
213	SA1	I	CMOS	
Power Supplies				
1	V_{REF}	AI	–	**I/O Reference Voltage**
42, 45, 49, 53, 57, 61, 64, 146, 149, 152, 156, 160, 164, 168, 171	V_{DD}	PWR	–	**Power Supply**
107	V_{DDSPD}	PWR	–	**EEPROM Power Supply**
2, 5, 8, 11, 14, 17, 20, 23, 26, 29, 32, 35, 37, 40, 66, 69, 72, 75, 78, 80, 83, 86, 89, 91, 94, 97, 100, 103, 108, 111, 113, 116, 119, 121, 124, 127, 130, 132, 135, 138, 141, 144, 173, 176, 178, 181, 184, 187, 190, 193, 196, 205, 199, 202, 207, 210	V_{SS}	GND	–	**Ground Plane**
Other Pins				
166	ODT0			**On-Die Termination Control 1:0**
63	ODT1			*Note: 2-rank module*
	NC			*Note: 1-rank module*
15, 16, 41, 44, 46, 58, 59, 65, 87, 88, 106, 145, 148, 150, 151, 167, 169, 170, 172, 212, 214	NC	NC	–	**Not connected** *Note: Pins not connected on Infineon MDIMMs*

Table 6 Abbreviations for Pin Type

Abbreviation	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
PWR	Power
GND	Ground
NC	Not Connected

Table 7 Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic (SSTL_1.8)
CMOS	CMOS Levels
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR.

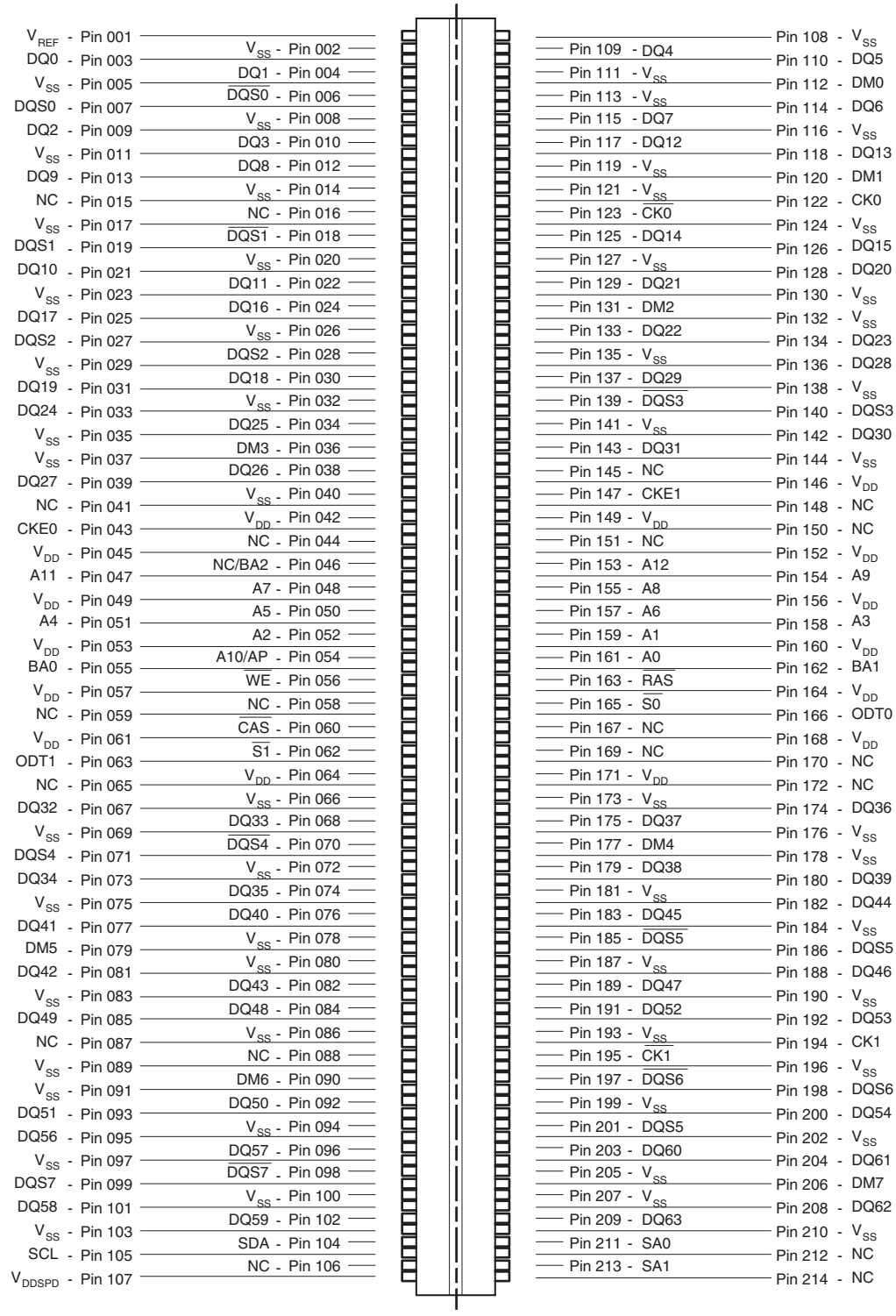

Figure 1 Pin Configuration for Two-Piece Mezzanine Socket on MDIMM (214 pins)

Table 8 Input/Output Functional Description

Symbol	Type	Polarity	Function
CK[1:0], $\overline{CK}$[1:0]	I	Cross point	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and the falling edge of $\overline{CK}$. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
CKE[1:0]	I	Active High	Activates the DDR2 SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down Mode or the Self Refresh Mode.
$\overline{S}$[1:0]	I	Active Low	Enables the associated DDR2 SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by S0; Rank 1 is selected by S1.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	I	Active Low	When sampled at the cross point of the rising edge of CK,and falling edge of $\overline{CK}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation to be executed by the SDRAM.
BA[1:0]	I	—	Selects internal SDRAM memory bank
ODT[1:0]	I	Active High	Asserts on-die termination for DQ, DM, DQS, and $\overline{DQS}$ signals if enabled via the DDR2 SDRAM mode register.
A[9:0], A10/AP, A[12:11]	I	—	During a Bank Activate command cycle, defines the row address when sampled at the crosspoint of the rising edge of CK and falling edge of $\overline{CK}$. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0-BAn defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA[1:0] to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA[1:0] inputs. If AP is low, then BA[1:0] are used to define which bank to precharge.
DQ[63:0]	I/O	—	Data Input/Output pins
DM[7:0]	I	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect.
DQS[7:0], $\overline{DQS}$[7:0]	I/O	Cross point	The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode the data strobe is sourced by the DDR2 SDRAM and is sent at the leading edge of the data window. $\overline{DQS}$ signals are complements, and timing is relative to the crosspoint of respective DQS and $\overline{DQS}$. If the module is to be operated in single ended strobe mode, all $\overline{DQS}$ signals must be tied on the system board to V_{SS} through a 20 Ω to 10 kΩ resistor and DDR2 SDRAM mode registers programmed appropriately.
V_{DD}, V_{DDSPD}, V_{SS}	Supply	—	Power supplies for core, I/O, Serial Presence Detect, and ground for the module.
SDA	I/O	—	This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resistor must be connected from SDA to to V_{DDSPD} on the motherboard to act as a pull-up.
SCL	I	—	This signal is used to clock data into and out of the SPD EEPROM.
SA[1:0]	I	—	Address pins used to select the Serial Presence Detect base address.

2 Block Diagrams

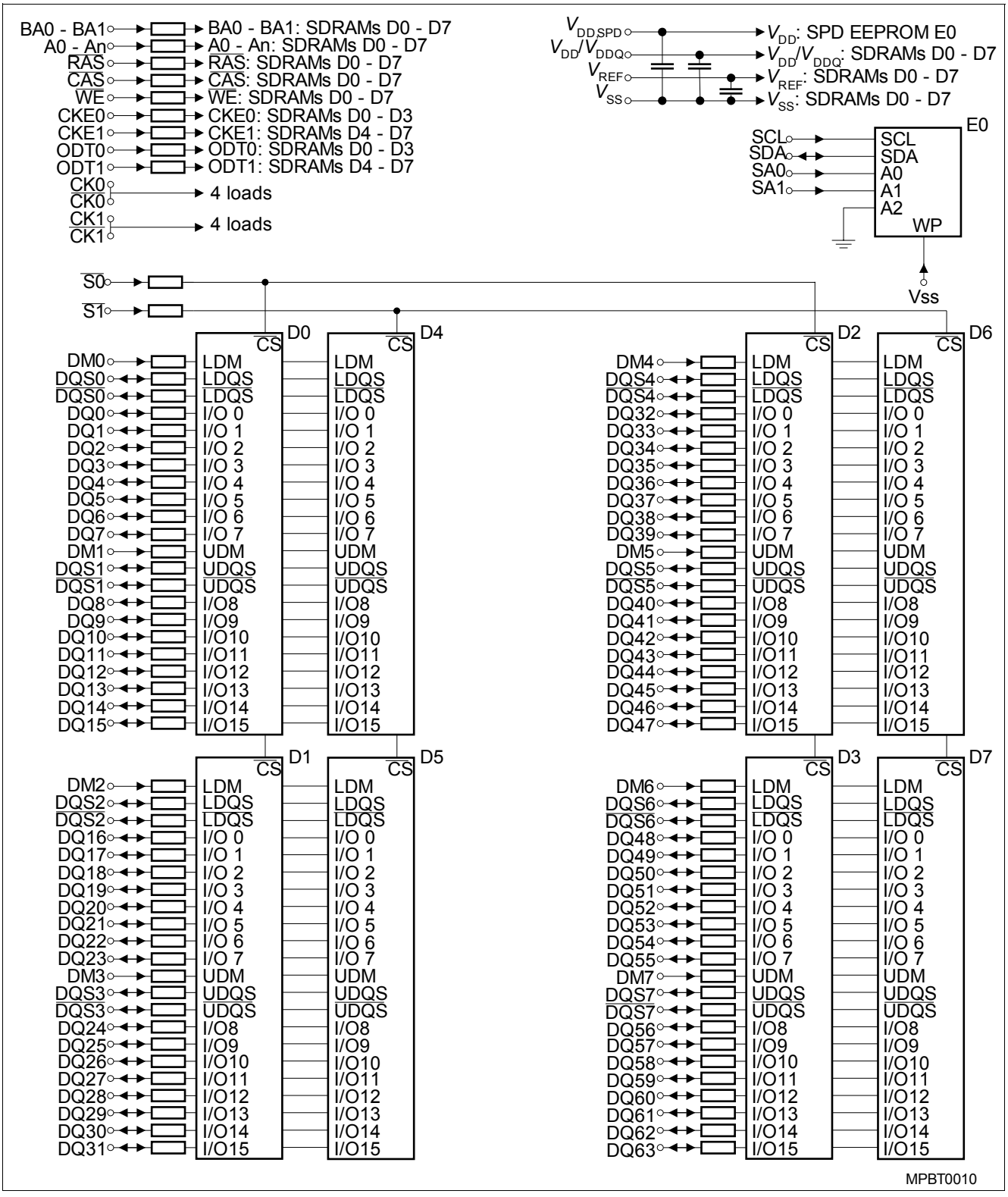

Figure 2 Block Diagram Raw Card A (x64, 2 Ranks, x16)

Notes

1. *DQ, DQS, DM resistors are 22 Ω ±5 %*
2. *$\overline{S0}$, $\overline{S1}$, BAn, An, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, ODTO, ODT1, CKEO, CKE1 resistors are 3 Ω ±5 %*

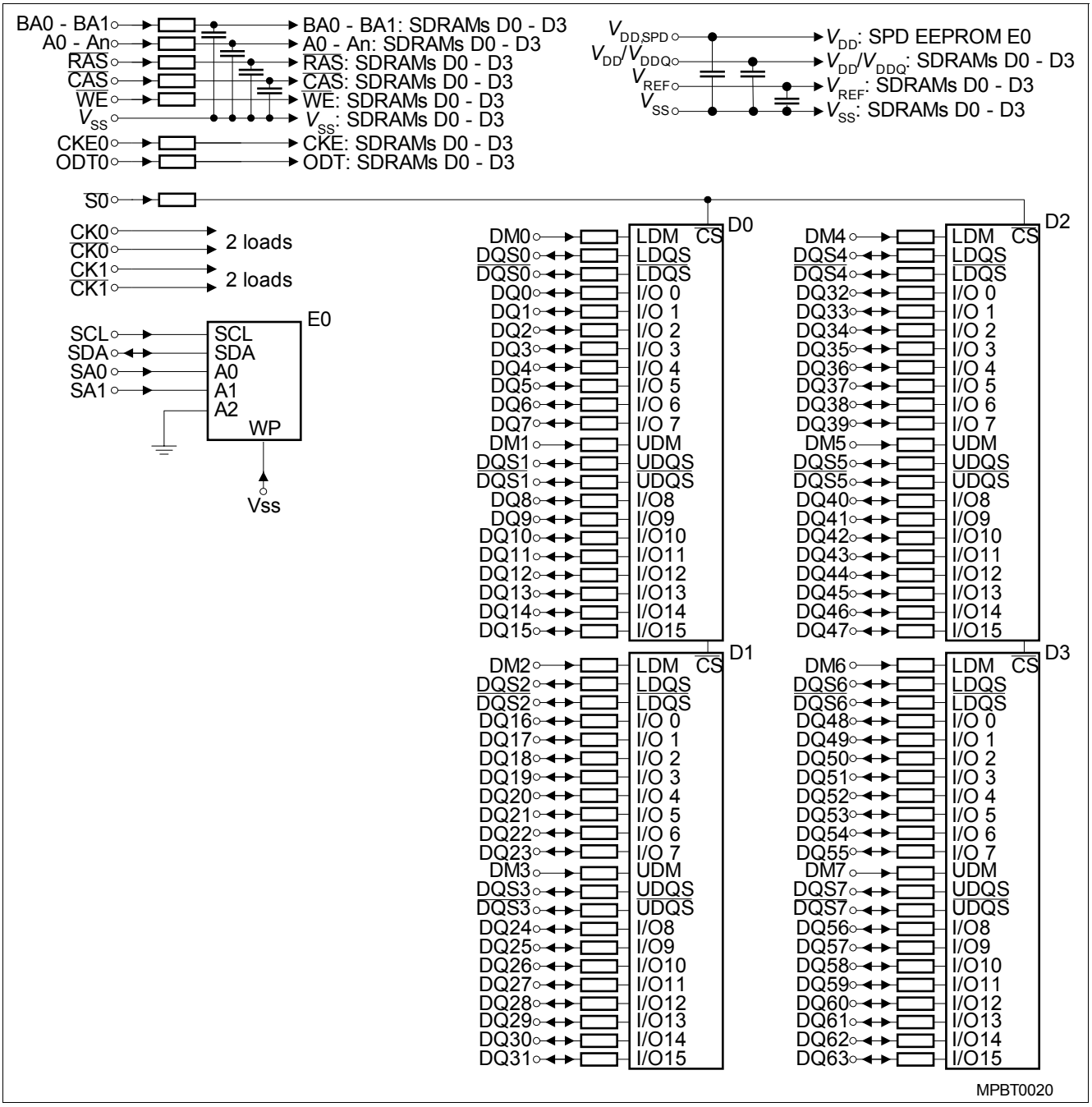

Figure 3 Block Diagram Raw Card B (x64, 1 Rank, x16)

Notes

1. *DQ, DQS, DM resistors are 22 Ω ±5 %*
2. *S0, BAn, An, RAS, CAS, WE, ODTO, CKEO resistors are 3 Ω ±5 %*
3. *Load matching Capacitors on BA0 - BA1, A0 - An, RAS, CAS, WE, with 8 pF ± 0.5pF*

3 Electrical Characteristics

3.1 Operating Conditions

Table 9 Absolute Maximum Ratings

Parameter	Symbol	Values		Unit	Note/Test Condition
		Min.	Max.		
Voltage on any pins relative to V_{SS}	V_{IN}, V_{OUT}	– 0.5	2.3	V	1)
Voltage on V_{DD} relative to V_{SS}	V_{DD}	– 1.0	2.3	V	1)
Voltage on V_{DDQ} relative to V_{SS}	V_{DDQ}	– 0.5	2.3	V	1)
Storage Humidity (without condensation)	H_{STG}	5	95	%	1)

1) Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

Table 10 Operating Conditions

Parameter	Symbol	Values		Unit	Notes
		min.	max.		
Operating temperature (ambient)	T_{OPR}	0	+65	°C	
DRAM Case Temperature	T_{CASE}	0	+95	°C	1)2)3)4)
Storage Temperature	T_{STG}	– 50	+100	°C	
Barometric Pressure (operating & storage)		105	69	kPa	5)
Operating Humidity (relative)	H_{OPR}	10	90	%	

1) DRAM Component Case Temperature is the surface temperature in the center on the top side of any of the DRAMs. For measurement conditions, please refer to the JEDEC document JESD51-2

2) Within the DRAM Component Case Temperature Range all DRAM specifications will be supported

3) Above 85 °C DRAM Case Temperature the Auto-Refresh command interval has to be reduced to t_{REFI} = 3.9 µs

4) Self-Refresh period is hard-coded in the DRAMs and therefore it is imperative that the system ensures the DRAM is below 85 °C Case Temperature before initiating Self-Refresh operation.

5) Up to 3000 m.

Table 11 Supply Voltage Levels and DC Operating Conditions

Parameter	Symbol	Limit Values			Unit	Notes
		min.	nom.	max.		
Device Supply Voltage	V_{DD}	1.7	1.8	1.9	V	—
Output Supply Voltage	V_{DDQ}	1.7	1.8	1.9	V	1)
Input Reference Voltage	V_{REF}	0.49 × V_{DDQ}	0.5 × V_{DDQ}	0.51 × V_{DDQ}	V	2)
SPD Supply Voltage	V_{DDSPD}	1.7	—	3.6	V	
DC Input Logic High	$V_{IH\ (DC)}$	V_{REF} + 0.125	—	V_{DDQ} + 0.3	V	
DC Input Logic Low	$V_{IL\ (DC)}$	– 0.30	—	V_{REF} – 0.125	V	

1) Under all conditions, V_{DDQ} must be less than or equal to V_{DD}

2) Peak to peak AC noise on V_{REF} may not exceed ± 2% $V_{REF\ (DC)}$. V_{REF} is also expected to track noise in V_{DDQ}.

4 I_{DD} Specifications and Conditions

Table 12 I_{DD} Measurement Conditions[1)2)]

Parameter	Symbol
Operating Current 0 One bank Active - Precharge; $t_{CK} = t_{CKmin.}$, $t_{RC} = t_{RCmin.}$, $t_{RAS} = t_{RASmin.}$, CKE is HIGH, CS is high between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD0}
Operating Current 1 One bank Active - Read - Precharge; I_{OUT} = 0 mA, BL = 4, $t_{CK} = t_{CKmin.}$, $t_{RC} = t_{RCmin.}$, $t_{RAS} = t_{RASmin.}$, $t_{RCD} = t_{RCDmin.}$,AL = 0, CL = $CL_{min.}$; CKE is HIGH, $\overline{CS}$ is high between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD1}
Precharge Power-Down Current Other control and address inputs are STABLE, Data bus inputs are FLOATING.	I_{DD2P}
Precharge Standby Current All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CKmin.}$; Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD2N}
Precharge Quiet Standby Current All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CKmin.}$; Other control and address inputs are STABLE, Data bus inputs are FLOATING.	I_{DD2Q}
Active Power-Down Current All banks open; $t_{CK} = t_{CKmin.}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to “0” (Fast Power-down Exit);	$I_{DD3P(0)}$
Active Power-Down Current All banks open; $_{tCK} = t_{CKmin.}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to “1” (Slow Power-down Exit);	$I_{DD3P(1)}$
Active Standby Current Burst Read: All banks open; Continuous burst reads; BL = 4; AL = 0, CL = $CL_{min.}$; $t_{CK} = t_{CKmin.}$; $t_{RAS} = t_{RASmax.}$, $t_{RP} = t_{RPmin.}$; CKE is HIGH, $\overline{CS}$ is high between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; I_{OUT} = 0 mA.	I_{DD3N}
Operating Current Burst Read: All banks open; Continuous burst reads; BL = 4; AL = 0, CL = $CL_{min.}$; $t_{CK} = t_{CKmin.}$; $t_{RAS} = t_{RASmax.}$, $t_{RP} = t_{RPmin.}$; CKE is HIGH, $\overline{CS}$ is high between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; I_{OUT} = 0 mA.	I_{DD4R}
Operating Current Burst Write: All banks open; Continuous burst writes; BL = 4; AL = 0, CL = $CL_{min.}$; $t_{CK} = t_{CKmin.}$; $t_{RAS} = t_{RASmax.}$, $t_{RP} = t_{RPmin.}$; CKE is HIGH, $\overline{CS}$ is high between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING;	I_{DD4W}
Burst Refresh Current $t_{CK} = t_{CKmin.}$, Refresh command every $t_{RFC} = t_{RFCmin.}$ interval, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD5B}
Distributed Refresh Current $t_{CK} = t_{CKmin.}$, Refresh command every $t_{RFC} = t_{REFI}$ interval, CKE is LOW and $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD5D}

Table 12 I_{DD} Measurement Conditions[1)2)] (cont'd)

Parameter	Symbol
Self-Refresh Current CKE ≤ 0.2 V; external clock off, CK and $\overline{CK}$ at 0 V; Other control and address inputs are FLOATING, Data bus inputs are FLOATING. RESET = Low. I_{DD6} current values are guaranteed up to T_{CASE} of 85 °C max.	I_{DD6}
All Bank Interleave Read Current All banks are being interleaved at minimum t_{RC} without violating t_{RRD} using a burst length of 4. Control and address bus inputs are STABLE during DESELECTS. I_{out} = 0 mA.	I_{DD7}

1) V_{DDQ} = 1.8 V ± 0.1 V; V_{DD} = 1.8 V ± 0.1 V

2) For details and notes see the relevant INFINEON component data sheet

Table 13 I_{DD} Specification

Product Type	HYS64T32000HM-5-A HYS64T32000LM-5-A HYS64T32000KM-5-A	HYS64T32000HM-3.7-A HYS64T32000LM-3.7-A HYS64T32000KM-3.7-A	HYS64T64020HM-5-A HYS64T64020LM-5-A HYS64T64020KM-5-A	HYS64T64020HM-3.7-A HYS64T64020LM-3.7-A HYS64T64020KM-3.7-A	Unit	Notes
Organization	**256 MB**	**256 MB**	**512 MB**	**512 MB**		
	1 Rank	**1 Rank**	**2 Ranks**	**2 Ranks**		
	×64	**×64**	**×64**	**×64**		
Symbol	**Max.**	**Max.**	**Max.**	**Max.**		
I_{DD0}	280	320	296	336	mA	1)2)
I_{DD1}	300	360	316	376	mA	1)2)
I_{DD2P}	16	16	32	32	mA	1)3)
I_{DD2N}	128	160	256	320	mA	1)3)
I_{DD2Q}	100	120	200	240	mA	1)3)
$I_{DD3P(0)}$	52	64	104	128	mA	1)3)
$I_{DD3P(1)}$	20	20	40	40	mA	1)3)
I_{DD3N}	140	160	280	320	mA	1)3)
I_{DD4R}	340	400	356	416	mA	1)2)
I_{DD4W}	360	440	376	456	mA	1)2)
I_{DD5B}	480	520	496	536	mA	1)2)
I_{DD5D}	24	24	40	40	mA	1)3)
I_{DD6}	16	16	32	32	mA	1)3)
I_{DD7}	840	880	856	896	mA	1)2)

1) Calculated values from component data. ODT disabled. I_{DD1}, I_{DD4R}, and I_{DD7} are defined with the outputs disabled.

2) For 2-rank modules only: The other rank is in I_{DD2P} Precharge Power-Down Standby Current mode

3) For 2-rank modules only: Both ranks are in the same I_{DD} mode

4.1 I_{DD} Test Conditions

For testing the I_{DD} parameters, the timing parameters as in Table 14 are used.

Table 14 IDD Measurement Test Condition

Parameter	Symbol	-3.7	-5	Unit
		PC2-4200-4-4-4	PC2-3200-3-3-3	
CAS Latency	CL_{min}	4	3	t_{CK}
Clock Cycle Time	t_{CKmin}	3.75	5	ns
Active to Read or Write delay	t_{RCDmin}	15	15	ns
Active to Active / Auto-Refresh command period	t_{RCmin}	60	60	ns
Active bank A to Active bank B command delay	t_{RRDmin}	10	10	ns
Active to Precharge Command	t_{RASmin}	45	45	ns
Precharge Command Period	t_{RPmin}	15	15	ns
Auto-Refresh to Active / Auto-Refresh command period	t_{RFCmin}	105	105	ns
Average periodic Refresh interval	t_{REFI}	7.8	7.8	µs

4.2 ODT (On Die Termination) Current

The ODT function adds additional current consumption to the DDR2 SDRAM when enabled by the EMRS(1). Depending on address bits A[6,2] in the EMRS(1) a “weak” or “strong” termination can be selected. The current consumption for any terminated input pin, depends on the input pin is in tri-state or driving “0” or “1”, as long a ODT is enabled during a given period of time.

Table 15 ODT current per terminated pin

Parameter	Symbol	min.	typ.	max.	Unit	EMRS(1) State
Enabled ODT current per DQ ODT is HIGH; Data Bus inputs are FLOATING	I_{ODTO}	5	6	7.5	mA/DQ	A6 = 0, A2 = 1
		2.5	3	3.75	mA/DQ	A6 = 1, A2 = 0
Active ODT current per DQ ODT is HIGH; worst case of Data Bus inputs are STABLE or SWITCHING.	I_{ODTT}	10	12	15	mA/DQ	A6 = 0, A2 = 1
		5	6	7.5	mA/DQ	A6 = 1, A2 = 0

Note: For power consumption calculations the ODT duty cycle has to be taken into account

5 Electrical Characteristics & AC Timings

Table 16 AC Timing - Absolute Specifications –5/–3.7[1)]

Parameter	Symbol	–3.7		–5		Unit	Notes
		PC2-4200M		PC2-3200M			
		Min.	Max.	Min.	Max.		
DQ output access time from CK/$\overline{CK}$	t_{AC}	-500	+500	–600	+600	ps	
$\overline{CAS}$ A to $\overline{CAS}$ B Command Period	t_{CCD}	2	—	2	—	t_{CK}	
CK, $\overline{CK}$ high-level width	t_{CH}	0.45	0.55	0.45	0.55	t_{CK}	
Clock cycle time	t_{CK3}	5000	8000	5000	8000	ps	2)
	t_{CK4}	3750	8000	5000	8000	ps	3)
CKE minimum high and low pulse width	t_{CKE}	3	—	3	—	t_{CK}	
CK, $\overline{CK}$ low-level width	t_{CL}	0.45	0.55	0.45	0.55	t_{CK}	
Auto precharge write recovery + precharge time	t_{DAL}	WR + t_{RP}	—	WR + t_{RP}	—	t_{CK}	
Minimum time clocks remain ON after CKE asynchronously drops low	t_{DELAY}	t_{IS} + t_{CK} + t_{IH}	—	t_{IS} + t_{CK}+ t_{IH}	—	ns	
DQ and DM input hold time	t_{DH}	225	—	275	—	ps	
DQ and DM input pulse width (each input)	t_{DIPW}	0.35	—	0.35	—	t_{CK}	
DQS output access time from CK/$\overline{CK}$	t_{DQSCK}	–450	+450	–500	+500	ps	
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	0.35	—	t_{CK}	
DQS-DQ skew (for DQS & associated DQ signals)	t_{DQSQ}	—	300	—	350	ps	
Write command to 1st DQS latching transition	t_{DQSS}	WL - 0.25	WL + 0.25	WL – 0.25	WL + 0.25	t_{CK}	
DQ and DM input setup time	t_{DS}	100	—	150	—	ps	
DQS falling edge hold time from CLK (write cycle)	t_{DSH}	0.2	—	0.2	—	t_{CK}	
DQS falling edge to CLK setup time (write cycle)	t_{DSS}	0.2	—	0.2	—	t_{CK}	
Clock Half Period	t_{HP}	min. (t_{CL}, t_{CH})		min. (t_{CL}, t_{CH})		t_{CK}	
Data-out high-impedance time from CK/$\overline{CK}$	t_{HZ}	—	t_{ACmax}	—	t_{ACmax}	ps	
Address and control input hold time	t_{IH}	375	—	475	—	ps	
Control and Addr. input pulse width (each input)	t_{IPW}	0.6	—	0.6	—	t_{CK}	
Address and control input setup time	t_{IS}	250	—	350	—	ps	
DQ low-impedance from CK / $\overline{CK}$	$t_{LZ(DQ)}$	2×t_{ACmin}	t_{ACmax}	2×t_{ACmin}	t_{ACmax}	ps	
DQS low-impedance from CK / $\overline{CK}$	$t_{LZ(DQS)}$	t_{ACmin}	t_{ACmax}	t_{ACmin}	t_{ACmax}	ps	
Mode register set command cycle time	t_{MRD}	2	—	2	—	t_{CK}	
OCD drive mode output delay	t_{OIT}	0	12	0	12	ns	

Table 16 AC Timing - Absolute Specifications –5/–3.7[1)]

Parameter	Symbol	–3.7		–5		Unit	Notes
		PC2-4200M		PC2-3200M			
		Min.	Max.	Min.	Max.		
Data Output hold time from DQS	t_{QH}	$t_{HP}-t_{QHS}$	—	$t_{HP}-t_{QHS}$	—	t_{CK}	
Data hold skew factor	t_{QHS}	—	400	—	450	ps	
Active to Precharge command	t_{RAS}	45	70000	45	70000	ns	
Active to Active/Auto-refresh command period	t_{RC}	60	—	60	—	ns	
Active to Read or Write delay (with and without Auto-Precharge) delay	t_{RCD}	15	—	15	—	ns	
Average Periodic Refresh Interval	t_{REFI}	—	7.8	—	7.8	µs	4)
		—	3.9	—	3.9	µs	5)
Auto-refresh to Active/Auto-refresh command period	t_{RFC}	105	—	105	—	ns	
Precharge command period	t_{RP}	15	—	15	—	ns	
Read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK}	
Read postamble	t_{RPST}	0.40	0.60	0.40	0.60	t_{CK}	
Active bank A to Active bank B command	t_{RRD}	10	—	10	—	ns	
Internal read to precharge command delay	t_{RTP}	7.5	—	7.5	—	ns	
Write preamble	t_{WPRE}	0.25	—	0.25	—	t_{CK}	
Write postamble	t_{WPST}	0.40	0.60	0.40	0.60	t_{CK}	
Write recovery time	t_{WR}	15	—	15	—	ns	
Internal write to read command delay	t_{WTR}	7.5	—	10	—	ns	
Exit power down to any valid command (other than NOP or Deselect)	t_{XARD}	2	—	2	—	t_{CK}	
Exit active power-down mode to read command (slew exit, lower power)	t_{XARDS}	6 – AL	—	6 – AL	—	t_{CK}	
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	2	—	t_{CK}	
Exit Self-Refresh to non-read command	t_{XSNR}	t_{RFC} + 10	—	t_{RFC} + 10	—	ns	
Exit Self-Refresh to read command	t_{XSRD}	200	—	200	—	t_{CK}	

1) For details and notes see the relevant INFINEON component datasheet

2) CL = 3

3) CL = 4 & 5

4) 0 °C ≤ T_{CASE} ≤ 85 °C

5) 85 °C < T_{CASE} ≤ 95 °C

Table 17 ODT AC Electrical Characteristics and Operating Conditions (all speed bins)

Symbol	Parameter / Condition	Min.	Max.	Unit
t_{AOND}	ODT turn-on delay	2	2	t_{CK}
t_{AON}	ODT turn-on	$t_{AC(min)}$	$t_{AC(max)}$ + 1 ns	ns
t_{AONPD}	ODT turn-on (Power-Down Modes)	$t_{AC(min)}$ + 2 ns	2 t_{CK} + $t_{AC(max)}$ + 1 ns	ns
t_{AOFD}	ODT turn-off delay	2.5	2.5	t_{CK}
t_{AOF}	ODT turn-off	$t_{AC(min)}$	$t_{AC(max)}$ + 0.6 ns	ns
t_{AOFPD}	ODT turn-off delay (Power-Down Modes)	$t_{AC(min)}$ + 2 ns	2.5 t_{CK} + $t_{AC(max)}$ + 1 ns	ns
t_{ANPD}	ODT to Power Down Mode Entry Latency	3	—	t_{CK}
t_{AXPD}	ODT Power Down Exit Latency	8	—	t_{CK}

6 SPD Codes

Table 18 SPD Codes for PC2-4200M and PC2-3200M

Product Type		HYS64T64020LM–3.7–A	HYS64T64020KM–3.7–A	HYS64T64020HM–3.7–A	HYS64T32000LM–3.7–A	HYS64T32000KM–3.7–A	HYS64T32000HM–3.7–A	HYS64T64020LM–5–A	HYS64T64020KM–5–A	HYS64T64020HM–5–A	HYS64T32000LM–5–A	HYS64T32000KM–5–A	HYS64T32000HM–5–A
Organization		**512 MByte**			**256 MByte**			**512 MB**			**256 MB**		
		×64			**×64**			**×64**			**×64**		
		2 Ranks (×16)			**1 Rank (×16)**			**2 Ranks (×16)**			**1 Rank (×16)**		
Label Code		**PC2-4200M-444**			**PC2-4200M-444**			**PC2-3200M-333**			**PC2-3200M-333**		
Jedec SPD Revision		**Rev 1.1**			**Rev 1.1**			**Rev 1.1**			**Rev 1.1**		
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in E^2PROM	80	80	80	80	80	80	80	80	80	80	80	80
1	Total number of Bytes in E^2PROM	08	08	08	08	08	08	08	08	08	08	08	08
2	Memory Type (DDR = 07h)	08	08	08	08	08	08	08	08	08	08	08	08
3	Number of Row Addresses	0D	0D	0D	0D	0D	0D	0D	0D	0D	0D	0D	0D
4	Number of Column Addresses	0A	0A	0A	0A	0A	0A	0A	0A	0A	0A	0A	0A
5	Number of DIMM Ranks	61	61	61	60	60	60	61	61	61	60	60	60
6	Data Width	40	40	40	40	40	40	40	40	40	40	40	40
7	not used	00	00	00	00	00	00	00	00	00	00	00	00
8	Interface Voltage Levels	05	05	05	05	05	05	05	05	05	05	05	05
9	t_{CK} @ CL_{max} (Byte 18) [ns]	3D	3D	3D	3D	3D	3D	50	50	50	50	50	50
10	t_{AC} SDRAM @ CLmax (Byte 18) [ns]	50	50	50	50	50	50	60	60	60	60	60	60
11	Error Correction Support (non- / ECC)	00	00	00	00	00	00	00	00	00	00	00	00
12	Refresh Rate/Type	82	82	82	82	82	82	82	82	82	82	82	82
13	Primary SDRAM Width	10	10	10	10	10	10	10	10	10	10	10	10
14	Error Checking SDRAM Width	00	00	00	00	00	00	00	00	00	00	00	00
15	not used	00	00	00	00	00	00	00	00	00	00	00	00
16	Burst Length Supported	0C	0C	0C	0C	0C	0C	0C	0C	0C	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04	04	04	04	04	04	04	04	04	04
18	CAS Latency	38	38	38	38	38	38	38	38	38	38	38	38
19	not used	00	00	00	00	00	00	00	00	00	00	00	00
20	DIMM Type Information	08	08	08	08	08	08	08	08	08	08	08	08
21	DIMM Attributes	00	00	00	00	00	00	00	00	00	00	00	00

Table 18 SPD Codes for PC2-4200M and PC2-3200M

Product Type		HYS64T64020LM–3.7–A	HYS64T64020KM–3.7–A	HYS64T64020HM–3.7–A	HYS64T32000LM–3.7–A	HYS64T32000KM–3.7–A	HYS64T32000HM–3.7–A	HYS64T64020LM–5–A	HYS64T64020KM–5–A	HYS64T64020HM–5–A	HYS64T32000LM–5–A	HYS64T32000KM–5–A	HYS64T32000HM–5–A
Organization		**512 MByte**			**256 MByte**			**512 MB**			**256 MB**		
		×64			**×64**			**×64**			**×64**		
		2 Ranks (×16)			**1 Rank (×16)**			**2 Ranks (×16)**			**1 Rank (×16)**		
Label Code		**PC2-4200M-444**			**PC2-4200M-444**			**PC2-3200M-333**			**PC2-3200M-333**		
Jedec SPD Revision		**Rev 1.1**			**Rev 1.1**			**Rev 1.1**			**Rev 1.1**		
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
22	Component Attributes	01	01	01	01	01	01	01	01	01	01	01	01
23	t_{CK} @ CL_{max} -1 (Byte 18) [ns]	3D	3D	3D	3D	3D	3D	50	50	50	50	50	50
24	t_{AC} SDRAM @ CL_{max} -1 [ns]	50	50	50	50	50	50	60	60	60	60	60	60
25	t_{CK} @ CL_{max} -2 (Byte 18) [ns]	50	50	50	50	50	50	50	50	50	50	50	50
26	t_{AC} SDRAM @ CL_{max} -2 [ns]	60	60	60	60	60	60	60	60	60	60	60	60
27	t_{RPmin} [ns]	3C	3C	3C	3C	3C	3C	3C	3C	3C	3C	3C	3C
28	t_{RRDmin} [ns]	28	28	28	28	28	28	28	28	28	28	28	28
29	t_{RCDmin} [ns]	3C	3C	3C	3C	3C	3C	3C	3C	3C	3C	3C	3C
30	t_{RASmin} [ns]	2D	2D	2D	2D	2D	2D	2D	2D	2D	2D	2D	2D
31	Module Density per Rank	40	40	40	40	40	40	40	40	40	40	40	40
32	t_{AS}, t_{CS} [ns]	25	25	25	25	25	25	35	35	35	35	35	35
33	t_{AH}, t_{CH} [ns]	37	37	37	37	37	37	47	47	47	47	47	47
34	t_{DS} [ns]	10	10	10	10	10	10	15	15	15	15	15	15
35	t_{DH} [ns]	22	22	22	22	22	22	27	27	27	27	27	27
36	t_{WR} [ns]	3C	3C	3C	3C	3C	3C	3C	3C	3C	3C	3C	3C
37	t_{WTR} [ns]	1E	1E	1E	1E	1E	1E	28	28	28	28	28	28
38	t_{RTP} [ns]	1E	1E	1E	1E	1E	1E	1E	1E	1E	1E	1E	1E
39	Analysis Characteristics	00	00	00	00	00	00	00	00	00	00	00	00
40	t_{RC} and t_{RFC} extension	00	00	00	00	00	00	00	00	00	00	00	00
41	t_{RCmin} [ns]	3C	3C	3C	3C	3C	3C	3C	3C	3C	3C	3C	3C
42	t_{RFCmin} [ns]	69	69	69	69	69	69	69	69	69	69	69	69
43	t_{CKmax} [ns]	80	80	80	80	80	80	80	80	80	80	80	80
44	$t_{DQSQmax}$ [ns]	1E	1E	1E	1E	1E	1E	23	23	23	23	23	23
45	t_{QHSmax} [ns]	28	28	28	28	28	28	2D	2D	2D	2D	2D	2D
46	PLL Relock Time	00	00	00	00	00	00	00	00	00	00	00	00
47	Tc(max) Delta / DT4R4W Delta	53	53	53	53	53	53	51	51	51	51	51	51
48	Psi(T-A) DRAM	72	72	72	72	72	72	72	72	72	72	72	72
49	DT0	52	52	52	52	52	52	42	42	42	42	42	42

Table 18 SPD Codes for PC2-4200M and PC2-3200M

Product Type		HYS64T64020LM–3.7–A	HYS64T64020KM–3.7–A	HYS64T64020HM–3.7–A	HYS64T32000LM–3.7–A	HYS64T32000KM–3.7–A	HYS64T32000HM–3.7–A	HYS64T64020LM–5–A	HYS64T64020KM–5–A	HYS64T64020HM–5–A	HYS64T32000LM–5–A	HYS64T32000KM–5–A	HYS64T32000HM–5–A
Organization		**512 MByte**			**256 MByte**			**512 MB**			**256 MB**		
		×64			**×64**			**×64**			**×64**		
		2 Ranks (×16)			**1 Rank (×16)**			**2 Ranks (×16)**			**1 Rank (×16)**		
Label Code		**PC2-4200M-444**			**PC2-4200M-444**			**PC2-3200M-333**			**PC2-3200M-333**		
Jedec SPD Revision		**Rev 1.1**			**Rev 1.1**			**Rev 1.1**			**Rev 1.1**		
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
50	DT2N (UDIMM) or DT2Q (RDIMM)	2B	2B	2B	2B	2B	2B	23	23	23	23	23	23
51	DT2P	1D	1D	1D	1D	1D	1D	1D	1D	1D	1D	1D	1D
52	DT3N	1D	1D	1D	1D	1D	1D	19	19	19	19	19	19
53	DT3Pfast	23	23	23	23	23	23	1C	1C	1C	1C	1C	1C
54	DT3Pslow	16	16	16	16	16	16	16	16	16	16	16	16
55	DT4R / DT4R4W Sign	36	36	36	36	36	36	2E	2E	2E	2E	2E	2E
56	DT5B	1C	1C	1C	1C	1C	1C	1A	1A	1A	1A	1A	1A
57	DT7	30	30	30	30	30	30	2D	2D	2D	2D	2D	2D
58	Psi(ca) PLL	00	00	00	00	00	00	00	00	00	00	00	00
59	Psi(ca) REG	00	00	00	00	00	00	00	00	00	00	00	00
60	DTPLL	00	00	00	00	00	00	00	00	00	00	00	00
61	DTREG / Toggle Rate	00	00	00	00	00	00	00	00	00	00	00	00
62	SPD Revision	11	11	11	11	11	11	11	11	11	11	11	11
63	Checksum of Byte 0-62	C0	C0	C0	BF	BF	BF	12	12	12	11	11	11
64	JEDEC ID Code of Infineon (1)	C1	C1	C1	C1	C1	C1	C1	C1	C1	C1	C1	C1
65	JEDEC ID Code of Infineon (2)	00	00	00	00	00	00	00	00	00	00	00	00
66	JEDEC ID Code of Infineon (3)	00	00	00	00	00	00	00	00	00	00	00	00
67	JEDEC ID Code of Infineon (4)	00	00	00	00	00	00	00	00	00	00	00	00
68	JEDEC ID Code of Infineon (5)	00	00	00	00	00	00	00	00	00	00	00	00
69	JEDEC ID Code of Infineon (6)	00	00	00	00	00	00	00	00	00	00	00	00
70	JEDEC ID Code of Infineon (7)	00	00	00	00	00	00	00	00	00	00	00	00
71	JEDEC ID Code of Infineon (8)	00	00	00	00	00	00	00	00	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx
73	Product Type, Char 1	36	36	36	36	36	36	36	36	36	36	36	36
74	Product Type, Char 2	34	34	34	34	34	34	34	34	34	34	34	34
75	Product Type, Char 3	54	54	54	54	54	54	54	54	54	54	54	54
76	Product Type, Char 4	36	36	36	33	33	33	36	36	36	33	33	33

Table 18 SPD Codes for PC2-4200M and PC2-3200M

Product Type		HYS64T64020LM–3.7–A	HYS64T64020KM–3.7–A	HYS64T64020HM–3.7–A	HYS64T32000LM–3.7–A	HYS64T32000KM–3.7–A	HYS64T32000HM–3.7–A	HYS64T64020LM–5–A	HYS64T64020KM–5–A	HYS64T64020HM–5–A	HYS64T32000LM–5–A	HYS64T32000KM–5–A	HYS64T32000HM–5–A
Organization		**512 MByte**			**256 MByte**			**512 MB**			**256 MB**		
		×64			**×64**			**×64**			**×64**		
		2 Ranks (×16)			**1 Rank (×16)**			**2 Ranks (×16)**			**1 Rank (×16)**		
Label Code		**PC2-4200M-444**			**PC2-4200M-444**			**PC2-3200M-333**			**PC2-3200M-333**		
Jedec SPD Revision		**Rev 1.1**			**Rev 1.1**			**Rev 1.1**			**Rev 1.1**		
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
77	Product Type, Char 5	34	34	34	32	32	32	34	34	34	32	32	32
78	Product Type, Char 6	30	30	30	30	30	30	30	30	30	30	30	30
79	Product Type, Char 7	32	32	32	30	30	30	32	32	32	30	30	30
80	Product Type, Char 8	30	30	30	30	30	30	30	30	30	30	30	30
81	Product Type, Char 9	4C	4B	48	4C	4B	48	4C	4B	48	4C	4B	48
82	Product Type, Char 10	4D	4D	4D	4D	4D	4D	4D	4D	4D	4D	4D	4D
83	Product Type, Char 11	33	33	33	33	33	33	35	35	35	35	35	35
84	Product Type, Char 12	2E	2E	2E	2E	2E	2E	41	41	41	41	41	41
85	Product Type, Char 13	37	37	37	37	37	37	20	20	20	20	20	20
86	Product Type, Char 14	41	41	41	41	41	41	20	20	20	20	20	20
87	Product Type, Char 15	20	20	20	20	20	20	20	20	20	20	20	20
88	Product Type, Char 16	20	20	20	20	20	20	20	20	20	20	20	20
89	Product Type, Char 17	20	20	20	20	20	20	20	20	20	20	20	20
90	Product Type, Char 18	20	20	20	20	20	20	20	20	20	20	20	20
91	Module Revision Code	0x	0x	0x	0x	0x	0x	0x	0x	0x	0x	0x	0x
92	Test Program Revision Code	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx
95	Module Serial Number (1)	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx
96	Module Serial Number (2)	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx
97	Module Serial Number (3)	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx
98	Module Serial Number (4)	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx
99 - 127	Not used	00	00	00	00	00	00	00	00	00	00	00	00
128-255	BLANK	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF

7 Package Outlines

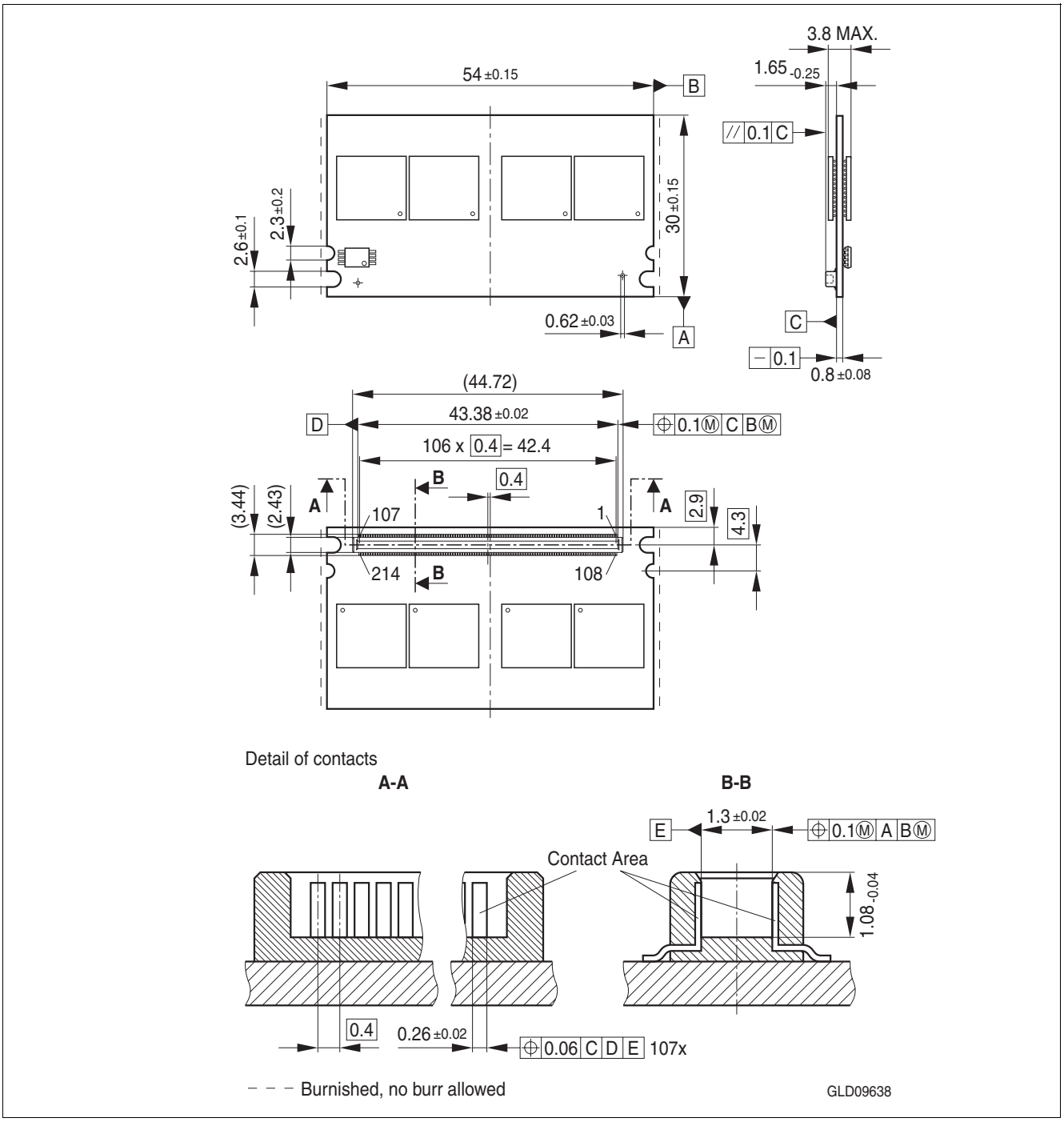

Figure 4 PCB Raw Card A Component Placement L-DIM-214-1

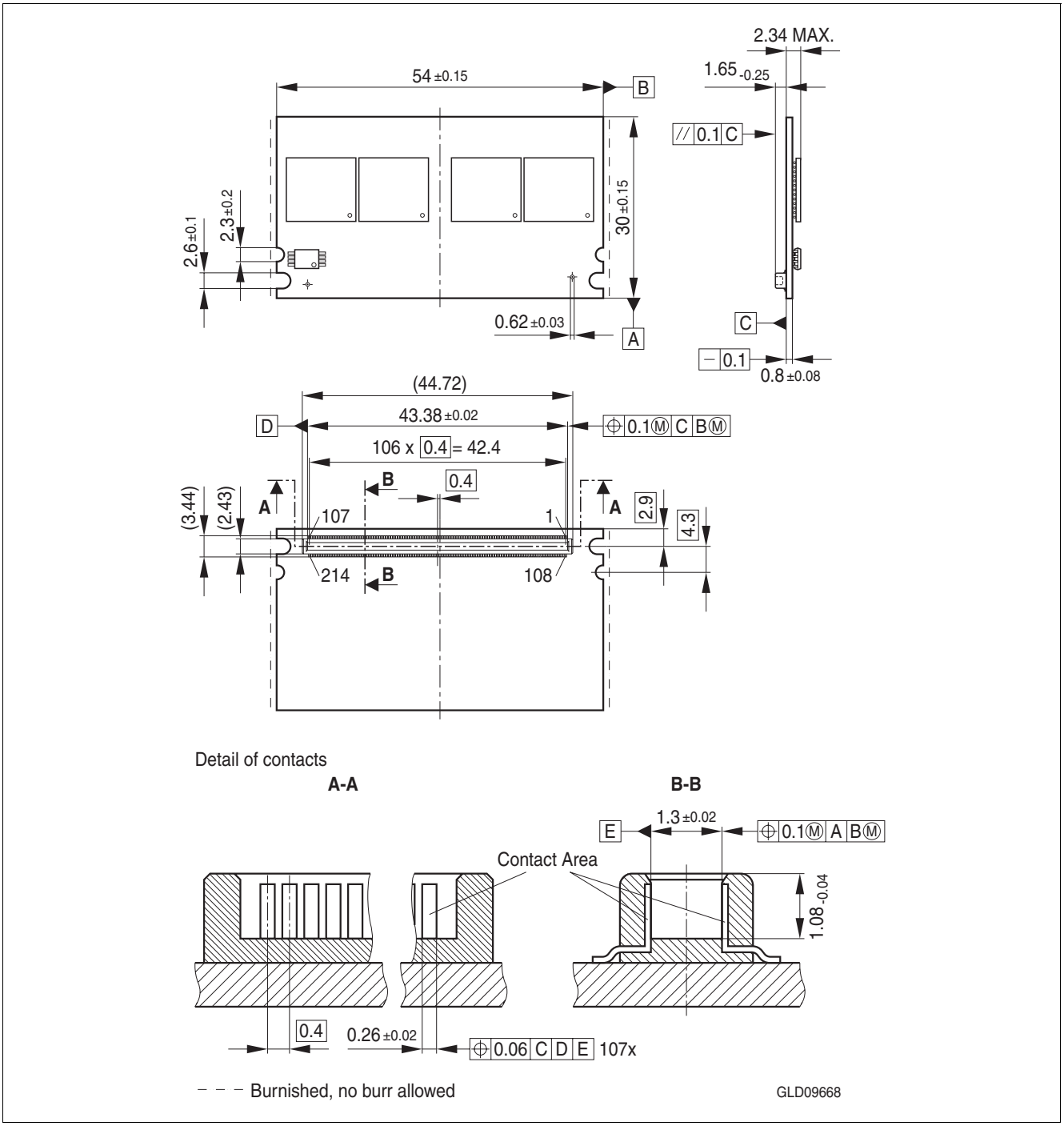

Figure 5 PCB Raw Card B Component Placement L-DIM-214-2

8 Product Type Nomenclature (DDR2 DRAMs and DIMMs)

Infineon's nomenclature uses simple coding combined with some propriatory coding. Table 20 provides examples for module and component product type number as well as the field number. The detailed field description together with possible values and coding explanation is listed for modules in Table 21 and for components in Table 22.

Table 20 Nomenclature Fields and Examples

Example for	Field Number										
	1	2	3	4	5	6	7	8	9	10	11
Micro-DIMM	HYS	64	T	64	0	2	0	K	M	–5	–A
DDR2 DRAM	HYB	18	T	512	16		0	A	C	–5	

Table 21 DDR2 DIMM Nomenclature

Field	Description	Values	Coding
1	INFINEON Modul Prefix	HYS	Constant
2	Module Data Width [bit]	64	Non-ECC
		72	ECC
3	DRAM Technology	T	DDR2
4	Memory Density per I/O [Mbit]; Module Density[1)]	32	256 MByte
		64	512 MByte
		128	1 GByte
		256	2 GByte
5	Raw Card Generation	0 .. 9	look up table
6	Number of Module Ranks	0, 2, 4	1, 2, 4
7	Product Variations	0 .. 9	look up table
8	Package, Lead-Free Status	A .. Z	look up table
9	Module Type	S	**S**O-DIMM
		M	**M**icro-DIMM
		R	**R**egistered
		U	**U**nbuffered
10	Speed Grade	–3.7	PC2–4200 4–4–4
		–5	PC2–3200 3–3–3
11	Die Revision	–A	First
		–B	Second

1) Multiplying "Memory Density per I/O" with "Module Data Width" and dividing by 8 for Non-ECC and 9 for ECC modules gives the overall module memory density in MBytes as listed in column "Coding".

Table 22 DDR2 DRAM Nomenclature

Field	Description	Values	Coding
1	INFINEON Component Prefix	HYB	Constant
2	Interface Voltage [V]	18	SSTL1.8
3	DRAM Technology	T	DDR2
4	Component Density [Mbit]	256	256 Mbit
		512	512 Mbit
		1G	1 Gbit
		2G	2 Gbit
5+6	Number of I/Os	40	×4
		80	×8
		16	×16
7	Product Variations	0 .. 9	look up table
8	Die Revision	A	First
		B	Second
9	Package, Lead-Free Status	C	FBGA, lead-containing
		F	FBGA, lead-free
10	Speed Grade	–3.7	DDR2-533
		–5	DDR2-400
11	N/A for Components		

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