128Kx32 CMOS High Speed Static RAM

FEATURES

- 128Kx32 bit CMOS Static
- Random Access Memory Array
  - Fast Access Times: 12, 15, 17, 20, and 25ns
  - Individual Byte Enables
  - User Configurable Organization with Minimal Additional Logic
  - Master Output Enable and Write Control
  - TTL Compatible Inputs and Outputs
  - Fully Static, No Clocks
- Surface Mount Package
  - 68 Lead PLCC, No. 99 (JEDEC MO-47AE)
  - Small Footprint, 0.990 Sq. In.
  - Multiple Ground Pins for Maximum Noise Immunity
- Single +5V (±5%) Supply Operation

DESCRIPTION

The EDI8L32128C is a high speed, high performance, four megabit density Static RAM organized as a 128Kx32 bit array.

Four Chip Enables, Write Control, and Output Enable provide the user with a flexible memory solution. The user may independently enable each of the four bytes, and, with minimal additional peripheral logic, the unit may be configured as a 256Kx16 or 512Kx8 array.

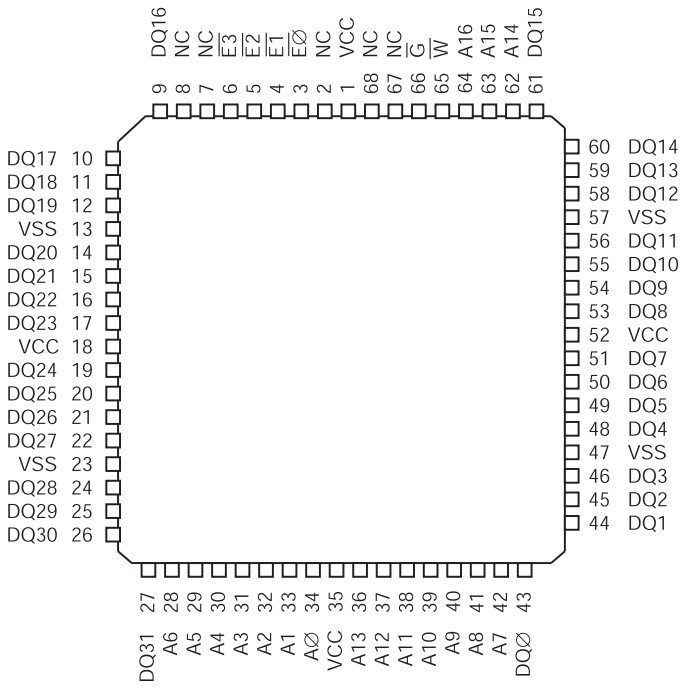
Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation and providing equal access and cycle times for ease of use.

The EDI8L32128C, allows 4 megabits of memory to be placed in less than 0.990 square inches of board space; a savings of 0.885 square inches over four standard 128Kx8 components.

NOTE: Solder Reflow temperature should not exceed 230°C

FIG. 1 PIN CONFIGURATION

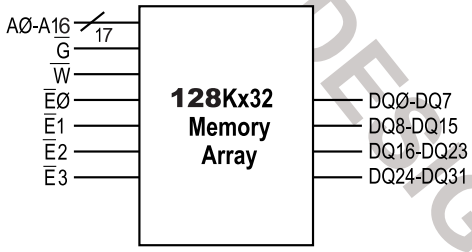
TOP VIEW



PIN DESCRIPTION

AØ-16	Address Inputs
$\overline{E}$Ø-3	Chip Enables (One per Byte)
$\overline{W}$	Master Write Enable
$\overline{G}$	Master Output Enable
DQØ-31	Common Data Input/Output
VCC	Power (+5V±5%)
VSS	Ground
NC	No Connection

BLOCK DIAGRAM



NOTE: *Pin 2 & 67 on the 64Kx32 (EDI8L3265C) and the 256Kx32 (EDI8L32256C) are word select pins.*

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS}	-0.5V to 7.0V
Operating Temperature T_A (Ambient)	
Commercial	0°C to +70°C
Industrial	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Power Dissipation	4 Watts
Output Current.	20 mA
Junction Temperature, T_J	175°C

**Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.*

TRUTH TABLE

$\overline{E}$	$\overline{W}$	$\overline{G}$	Mode	Output	Power
H	X	X	Standby	High Z	I_{CC2},I_{CC3},
L	H	H	Output Disable	High Z	I_{CC1}
L	X	X	Output Disable	High Z	I_{CC1}
L	H	L	Read	D_{OUT}	I_{CC1}
L	L	X	Write	D_{IN}	I_{CC1}

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	--	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	-0.3	--	0.8	V

CAPACITANCE

(f = 1.0MHz, V_{IN} = V_{CC} or V_{SS})

Parameter	Sym	Max	Unit
Address Lines	C_A	40	pF
Data Lines	$C_{D/Q}$	10	pF
Write & Output Enable Lines	$\overline{W}$, $\overline{G}$	40	pF
Chip Enable Lines/Byte Select	$\overline{E}_{0-3}$	8	pF

DC ELECTRICAL CHARACTERISTICS

Parameter	Sym	Conditions	Typ	Max				Units
				12*	15	17	20/25	
Operating Power Supply Current	I_{CC1}	W= V_{IL}, $I_{I/O}$ = 0mA, Min Cycle	620	720	680	640	600	mA
Standby (TTL) Supply Current	I_{CC2}	E ž V_{IH}, V_{IN} - V_{IL} or V_{IN} ž V_{IH}, f = ØMHz		160	160	160	160	mA
Full Standby CMOS Supply Current	I_{CC3}	E ž V_{CC} -0.2V V_{IN} ž V_{CC} -0.2V or V_{IN} - 0.2V		20	20	20	20	mA
Input Leakage Current	I_{LI}	V_{IN} = 0V to V_{CC}				±10		µA
Output Leakage Current	I_{LO}	$V_{I/O}$ = 0V to V_{CC}				±10		µA
Output High Volltage	V_{OH}	I_{OH} = -4.0mA	2.4					V
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA				0.4		V

Typical: TA = 25°C, VCC = 5.0V

AC TEST CONDITIONS

Figure 2

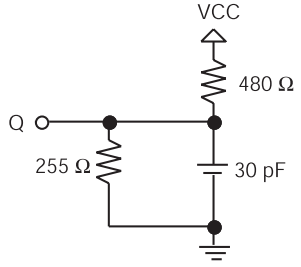
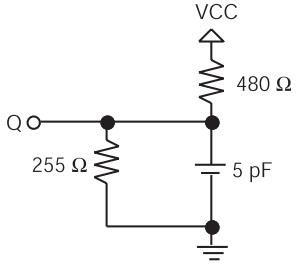


Figure 3



Input Pulse Levels	Vss to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 2

NOTE: *For tEHQZ, tGHQZ and tWLQZ, CL = 5pF Figure 3)*

AC CHARACTERISTICS - READ CYCLE

Parameter	Symbol JEDEC	Alt.	12ns Min	12ns Max	15ns Min	15ns Max	17ns Min	17ns Max	20ns Min	20ns Max	25n Min	25n Max	Units
Read Cycle Time	t_{AVAV}	t_{RC}	12		15		17		20		25		ns
Address Access Time	t_{AVQV}	t_{AA}		12		15		17		20		25	ns
Chip Enable Access Time	t_{ELQV}	t_{ACS}		12		15		17		20		25	ns
Chip Enable to Output in Low Z (1)	t_{ELQX}	t_{CLZ}	2		3		3		3		3		ns
Chip Disable to Output in High Z (1)	t_{EHQZ}	t_{CHZ}		7		8		8		10		10	ns
Output Hold from Address Change	t_{AVQX}	t_{OH}	3		3		3		3		3		ns
Output Enable to Output Valid	t_{GLQV}	t_{OE}		5		6		8		8		10	ns
Output Enable to Output in Low Z (1)	t_{GLQX}	t_{OLZ}	2		2		2		2		0		ns
Output Disable to Output in High Z(1)	t_{GHQZ}	t_{OHZ}		4		5		6		8		10	ns

NOTE 1: *Parameter guaranteed, but not tested.*

FIG. 4 READ CYCLE 1 - $\overline{W}$ HIGH, $\overline{G}$, $\overline{E}$ LOW

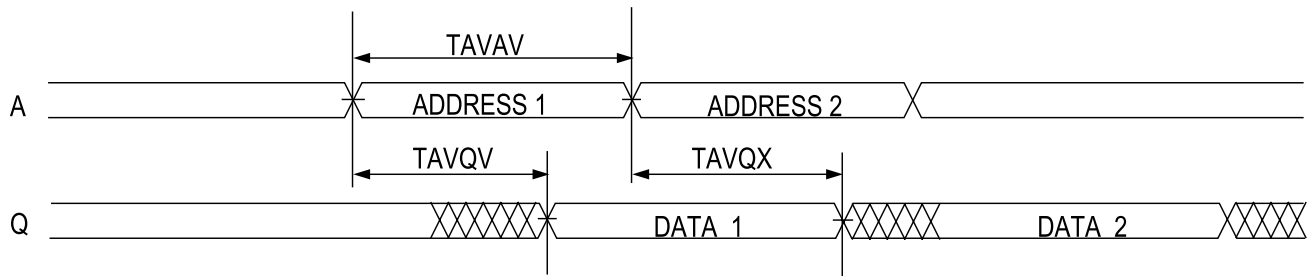
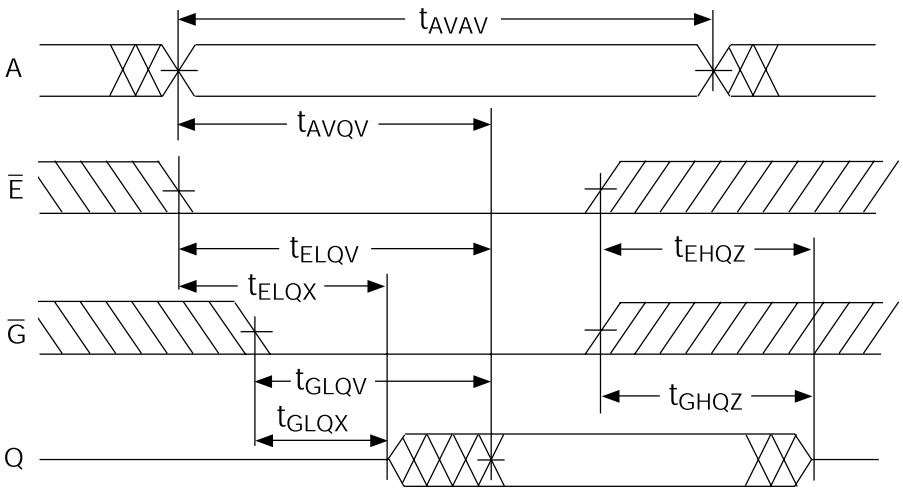


FIG. 5 READ CYCLE 2 - $\overline{W}$ HIGH



AC CHARACTERISTICS - WRITE CYCLE

Parameter	Symbol JEDEC	Alt.	12ns Min	12ns Max	15ns Min	15ns Max	17ns Min	17ns Max	20ns Min	20ns Max	25ns Min	25ns Max	Units
Write Cycle Time	t_{AVAV}	t_{WC}	12		15		17		20		25		ns
Chip Enable to End of Write	t_{ELWH}	t_{CW}	8		9		10		15		20		ns
	t_{ELEH}	t_{CW}	8		9		10		15		20		ns
Address Setup Time	t_{AVWL}	t_{AS}	0		0		0		0		0		ns
	t_{AVEL}	t_{AS}	0		0		0		0		0		ns
Address Valid to End of Write	t_{AVWH}	t_{AW}	9		10		12		15		15		ns
	t_{AVEH}	t_{AW}	9		10		12		15		15		ns
Write Pulse Width	t_{WLWH}	t_{WP}	9		10		12		15		15		ns
	t_{WLEH}	t_{WP}	9		10		12		15		15		ns
Write Recovery Time	t_{WHAX}	t_{WR}	0		0		0		0		0		ns
	t_{EHAX}	t_{WR}	0		0		0		0		0		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		0		0		0		0		ns
	t_{EHDX}	t_{DH}	0		0		0		0		0		ns
Write to Output in High Z (1)	t_{WLQZ}	t_{WHZ}	0	5	0	6	0	7	0	7	0	10	ns
Data to Write Time	t_{DVWH}	t_{DW}	5		6		8		8		12		ns
	t_{DVEH}	t_{DW}	5		6		8		8		12		ns
Output Active from End of Write (1)	t_{WHQX}	t_{WLZ}	2		2		2		2		2		ns

NOTE: *Parameter guaranteed, but not tested.*

FIG. 6 WRITE CYCLE 1 - $\overline{W}$ CONTROLLED

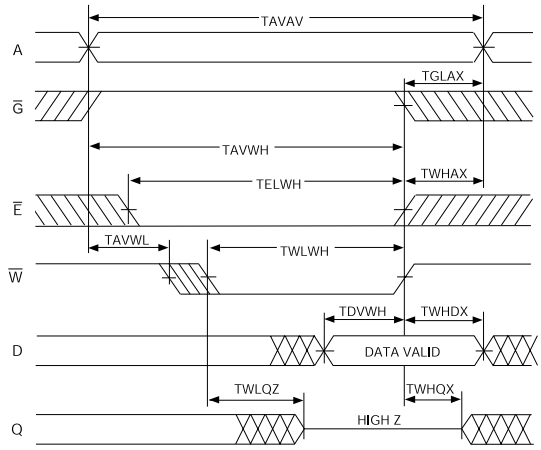
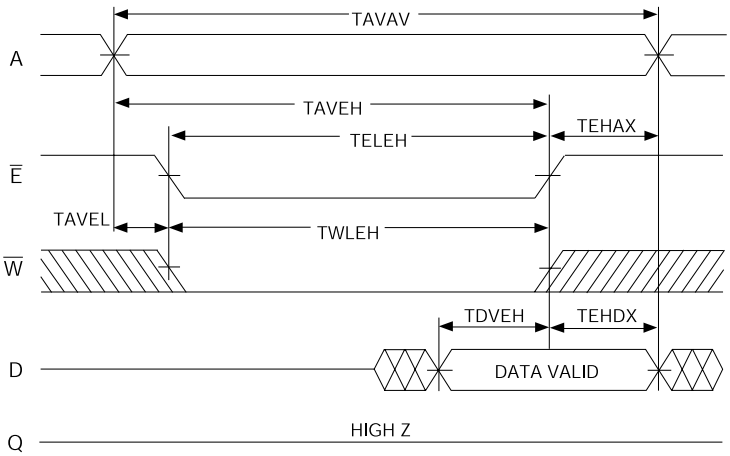


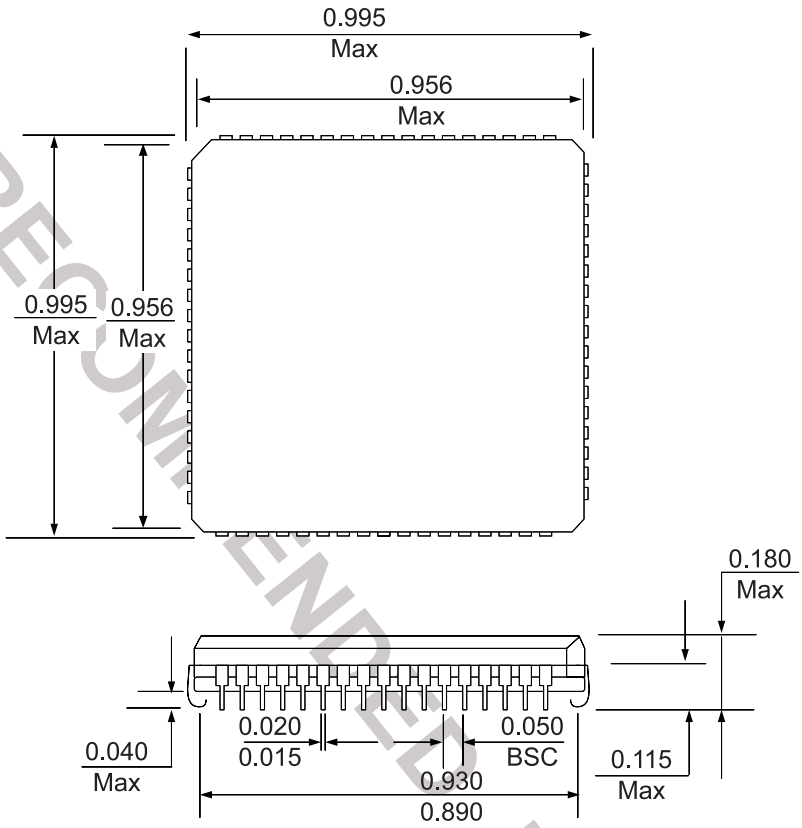
FIG. 7 WRITE CYCLE 2 - $\overline{E}$ CONTROLLED



PACKAGE DESCRIPTION

PACKAGE NO. 99: 68 LEAD PLCC

JEDEC MO-47AE



ALL DIMENSIONS ARE IN INCHES

ORDERING INFORMATION

Commercial (0°C to +70°C) Part Number	Speed (ns)	Package No.
EDI8L32128C12AC	12	99
EDI8L32128C15AC	15	99
EDI8L32128C17AC	17	99
EDI8L32128C20AC	20	99
EDI8L32128C25AC	25	99

Industrial (-40°C to +85°C) Part Number	Speed (ns)	Package No.
EDI8L32128C15AI	15	99
EDI8L32128C17AI	17	99
EDI8L32128C20AI	20	99