DRAM MODULE

2 MEG x 32 DRAM

FAST PAGE MODE

FEATURES

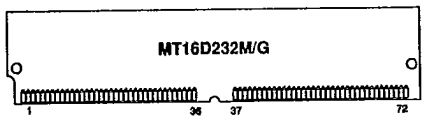
- Industry standard pinout in a 72-pin single-in-line package
- High-performance, CMOS silicon gate process.
- Single 5V ±10% power supply
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- Low power, 48mW standby; 3600mW active, typical
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ and HIDDEN
- 1,024-cycle refresh distributed across 16ms
- Optional FAST PAGE MODE access cycle

OPTIONS MARKING

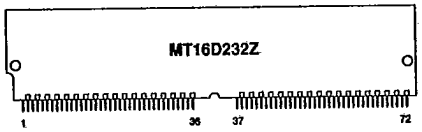
- Timing
  - 70ns access - 7
  - 80ns access - 8
  - 100ns access -10
- Packages
  - Leadless 72-pin SIMM M
  - Leadless 72-pin SIMM (Gold) G
  - Leaded 72-pin ZIP Z

PIN ASSIGNMENT (Top View)

72-Pin SIMM (I-6)



72-Pin ZIP (J-5)



PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	19	NC	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ29
5	DQ18	23	DQ22	41	$\overline{CAS2}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{CAS3}$	60	DQ30
7	DQ19	25	DQ23	43	$\overline{CAS1}$	61	DQ14
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ31
9	DQ20	27	DQ24	45	$\overline{RAS1}$	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ32
11	NC	29	NC	47	$\overline{WE}$	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	A9	50	DQ25	68	PRD2
15	A3	33	$\overline{RAS3}$	51	DQ10	69	PRD3
16	A4	34	$\overline{RAS2}$	52	DQ26	70	PRD4
17	A5	35	NC	53	DQ11	71	NC
18	A6	36	NC	54	DQ27	72	Vss

GENERAL DESCRIPTION

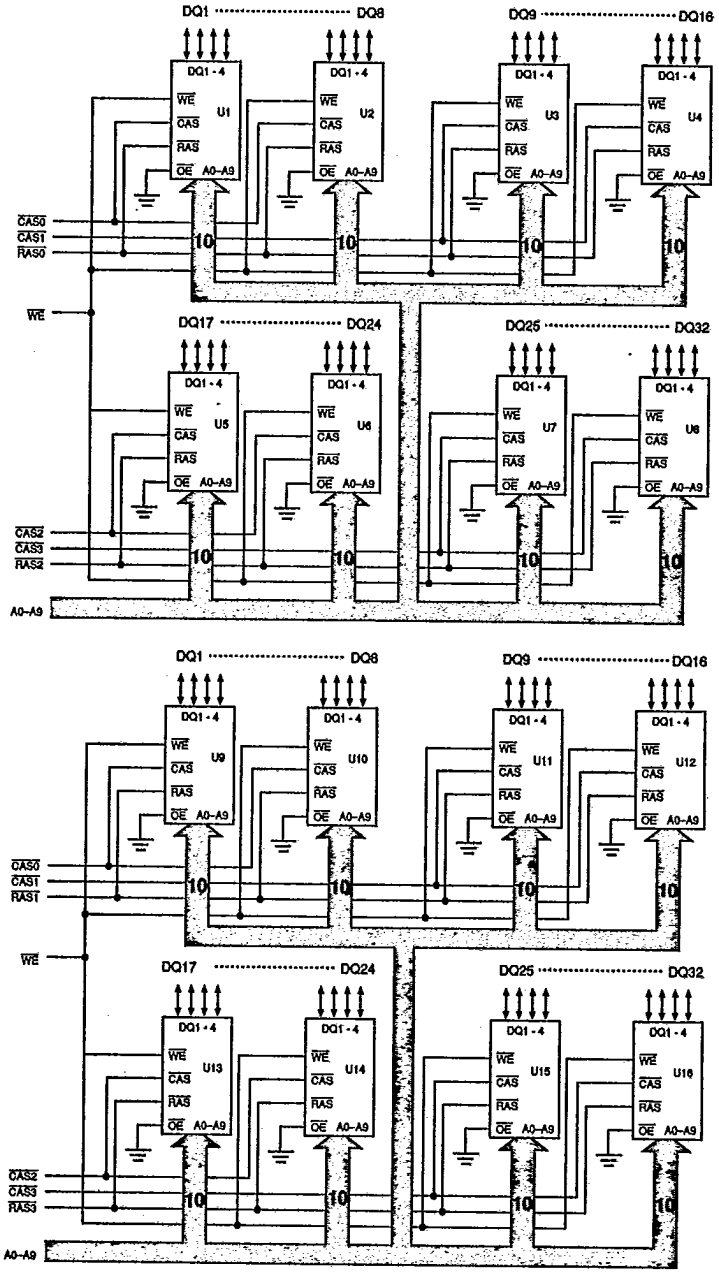
The MT16D232 is a randomly accessed solid-state memory containing 2,097,152 words organized in a x32 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. EARLY-WRITE occurs when $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN REFRESH) so that all 1,024 combination of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence.

T-46-23-17

FUNCTIONAL BLOCK DIAGRAM



U1-U16 = MT4C4001DJ

TRUTH TABLE

Function		RAS	CAS	WE	Addresses tR	Addresses tC	DQ1-32
Standby		H	X	X	X	X	High Impedance
READ		L	L	H	ROW	COL	Valid Data Out
EARLY-WRITE		L	L	L	ROW	COL	Valid Data In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Valid Data Out
	2nd Cycle	L	H→L	H	n/a	COL	Valid Data Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	L	ROW	COL	Valid Data In
	2nd Cycle	L	H→L	L	n/a	COL	Valid Data In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High Impedance
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Valid Data Out
	WRITE	L→H→L	L	L	ROW	COL	Valid Data In
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	High Impedance

PRESENCE DETECT

SYMBOL	-7	-8	-10
PRD1	NC	VSS	NC
PRD2	NC	VSS	NC
PRD3	VSS	VSS	NC
PRD4	NC	NC	NC

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss .....-1.0V to +7.0V
Operating Temperature, TA(Ambient) .....0°C to +70°C
Storage Temperature (Plastic) .....-55°C to +150°C
Power Dissipation 16W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ± 10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs		VIH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs		VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ VIN ≤ Vcc (All other pins not under test = 0V) For each package input	A0-A9, $\overline{WE}$	II	-32	32	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ VOUT ≤ Vcc) For each package input	DQ1-DQ32	IOZ	-24	24	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -5mA)		VOH	2.4		V	1
Output Low Voltage (IOUT = 5mA)		VOL		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: tRC = tRC (MIN))	ICC1	816	736	656	mA	2
OPERATING CURRENT: FAST PAGE MODE ($\overline{RAS}$ = VIL, $\overline{CAS}$ = Cycling: tPC = tPC (MIN))	ICC2	576	496	416	mA	2
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = VIH after 8 $\overline{RAS}$ cycles (MIN))	ICC3	32	32	32	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V after 8 $\overline{RAS}$ cycles (MIN)). (All other inputs at Vcc -0.2V or Vss +0.2V)	ICC4	16	16	16	mA	
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = VIH)	ICC5	816	736	656	mA	2
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	ICC6	816	736	656	mA	2

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	CI1		80	pF	17
Input Capacitance: $\overline{WE}$	CI2		112	pF	17
Input Capacitance: $\overline{CAS0}$-$\overline{CAS3}$, $\overline{RAS0}$-$\overline{RAS3}$	CI4		28	pF	17
Input/Output Capacitance: DQ1-DQ32	CIO		14	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

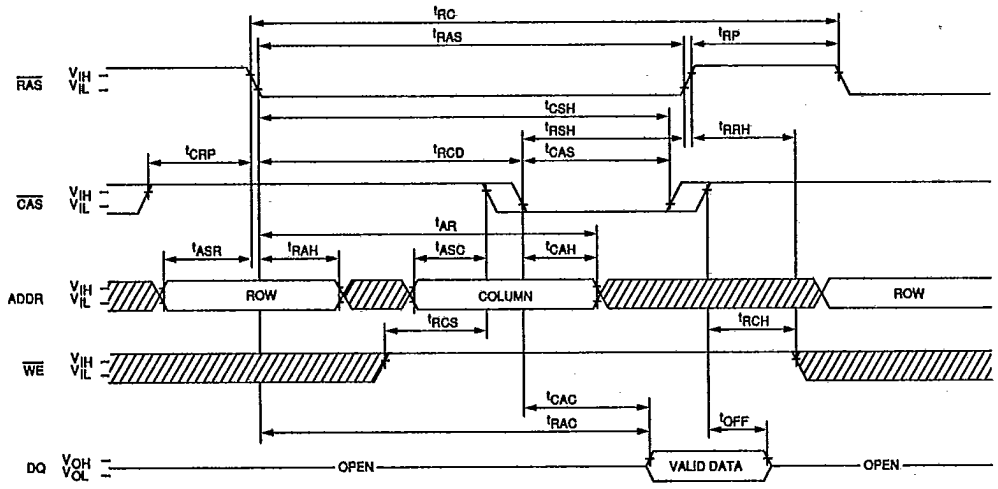
(Notes: 3, 4, 5, 10, 11, 16, 17) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ± 10%)

A.C. CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	130		150		180		ns	6, 7
FAST-PAGE-MODE cycle time	tPC	40		45		55		ns	6, 7
Access time from $\overline{RAS}$	tRAC		70		80		100	ns	7, 8
Access time from $\overline{CAS}$	tCAC		20		20		25	ns	7, 9
$\overline{RAS}$ pulse width	tRAS	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	tRSH	20		20		25		ns	
$\overline{RAS}$ precharge time	tRP	50		60		70		ns	
$\overline{CAS}$ pulse width	tCAS	20	100,000	20	100,000	25	100,000	ns	
$\overline{CAS}$ hold time	tCSH	70		80		100		ns	
$\overline{CAS}$ precharge time	tCPN	10		10		15		ns	18
$\overline{CAS}$ precharge time (FAST PAGE MODE)	tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	50	20	60	25	75	ns	13
$\overline{CAS}$ to $\overline{RAS}$ setup time	tCRP	5		5		20		ns	
Row address setup time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		15		ns	
Column address setup time	tASC	0		0		0		ns	
Column address hold time	tCAH	15		15		20		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	55		60		70		ns	
Read command setup time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	14
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	
Output buffer turn-off delay	tOFF	0	20	0	20	0	20	ns	12
$\overline{WE}$ command setup time	tWCS	0		0		0		ns	
Write command hold time	tWCH	15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	55		60		75		ns	
Write command pulse width	tWP	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		20		25		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		20		25		ns	
Data-in setup time	tDS	0		0		0		ns	15
Data-in hold time	tDH	15		15		20		ns	15
Data-in hold time referenced to $\overline{RAS}$	tDHR	55		60		75		ns	
Transition time (rise or fall)	tT	3	50	3	50	3	50	ns	16
Refresh period (256 cycles)	tREF		16		16		16	ms	20
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	tCHR	15		15		15		ns	19
$\overline{CAS}$ set-up time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH)	tCSR	10		10		10		ns	19
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	0		0		0		ns	19

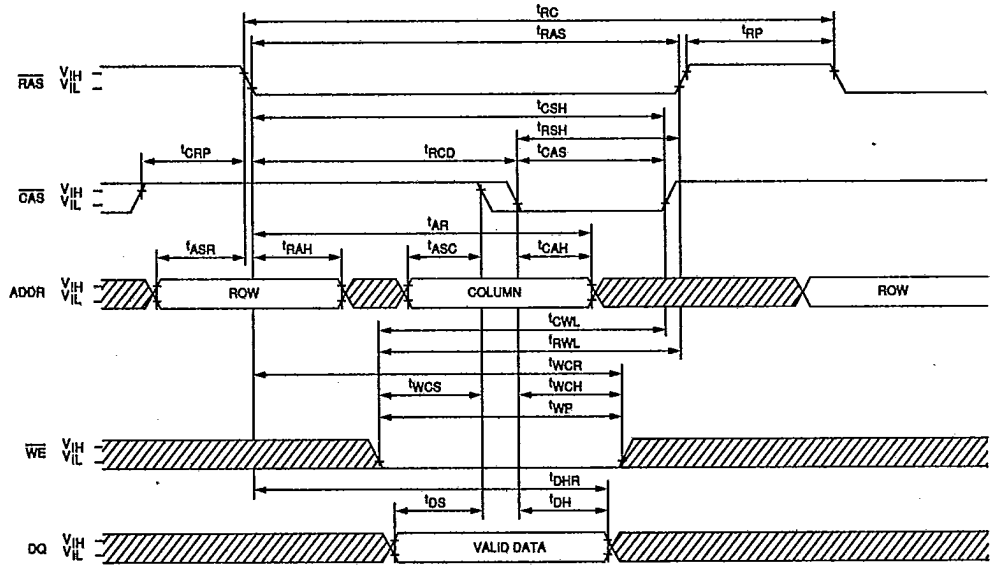
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ REFRESH cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 16ms refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \geq ^tRCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is calculated from the equation $C = I^{dt}/_{dv}$ with dv = 3V and V_{CC} = 5V.
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP. Note 8 applies to determine valid data out.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1-U16.

READ CYCLE



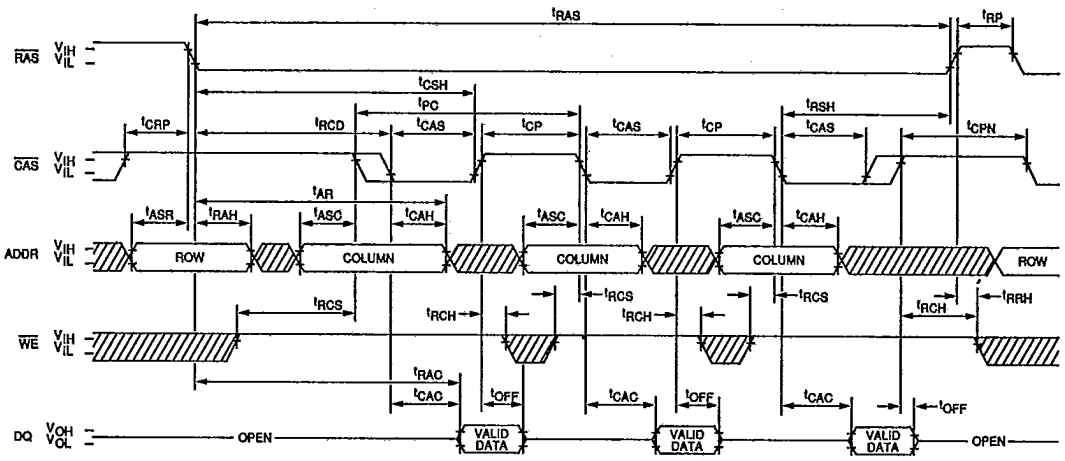
EARLY-WRITE CYCLE



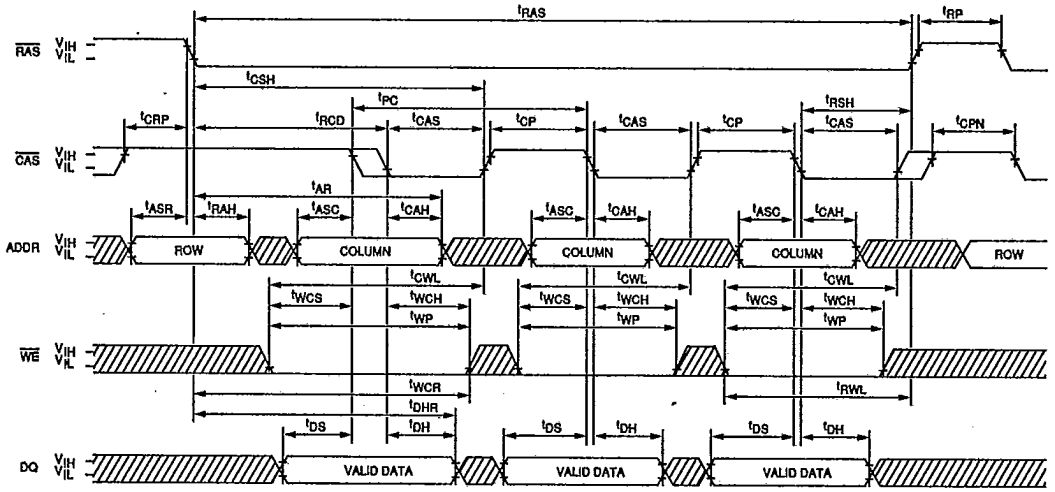
DON'T CARE

UNDEFINED

FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



DON'T CARE

UNDEFINED

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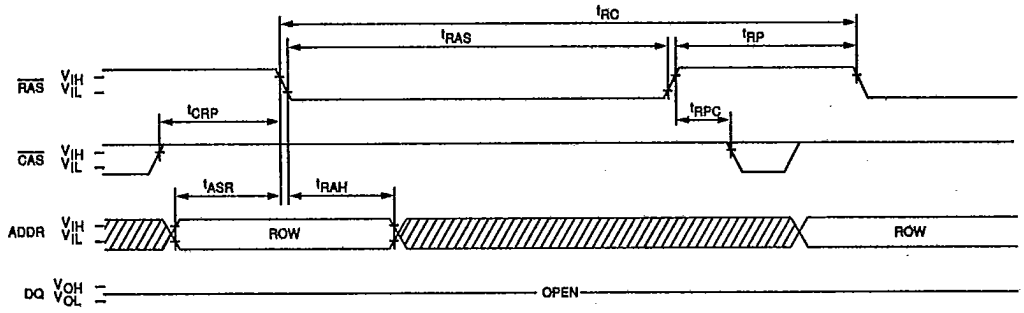
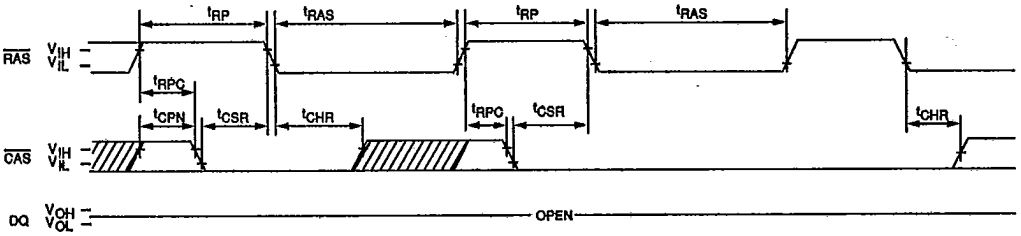
RAS-ONLY REFRESH CYCLE
(ADDR = A_0 - A_9; WE = DON'T CARE)



CAS-BEFORE-RAS REFRESH CYCLE
(A_0 - A_9, WE = DON'T CARE)



HIDDEN REFRESH CYCLE
(WE = HIGH) [20]