INTEGRATED CIRCUITS

DATA SHEET

SAA4997H
VErtical Reconstruction IC (VERIC) for PALplus

Preliminary specification
File under Integrated Circuits, IC02

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Philips Semiconductors

PHILIPS

FEATURES

- PALplus decoding
- Vertical reconstruction
- Quadrature mirror filter
- Luminance and chrominance processing
- Controlling.

GENERAL DESCRIPTION

The VErtical Reconstruction IC (VERIC) for PALplus (VERIC) is especially designed for use in conjunction with the Motion Adaptive Colour Plus And Control IC (MACPACIC) to decode the transmitted PALplus video signal in PALplus colour TV receivers. It provides the full vertical resolution of a PALplus picture from the letter box part and the decoded helper information.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–	5.25	V
T_{amb}	operating ambient temperature	0	70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA4997H	QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT319-2

BLOCK DIAGRAMS

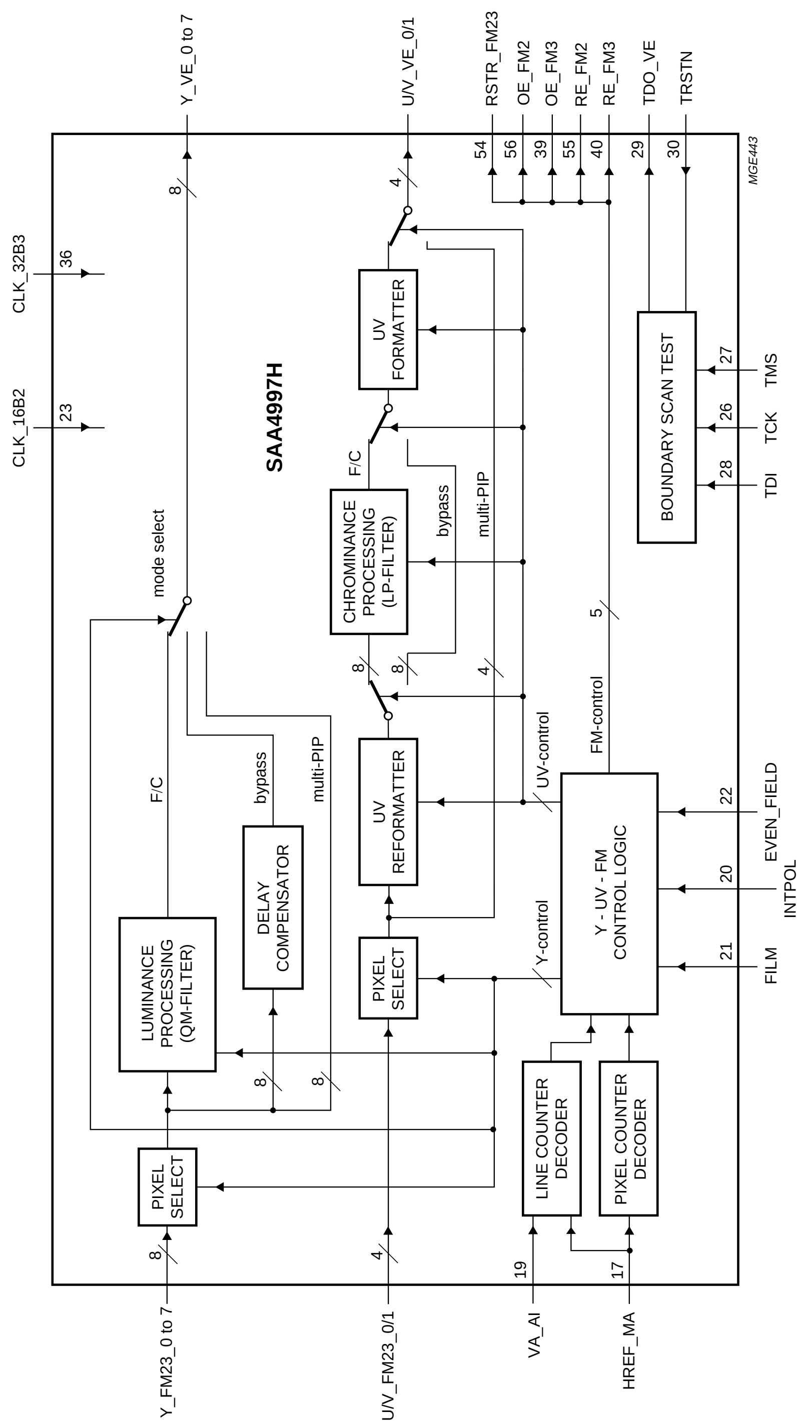
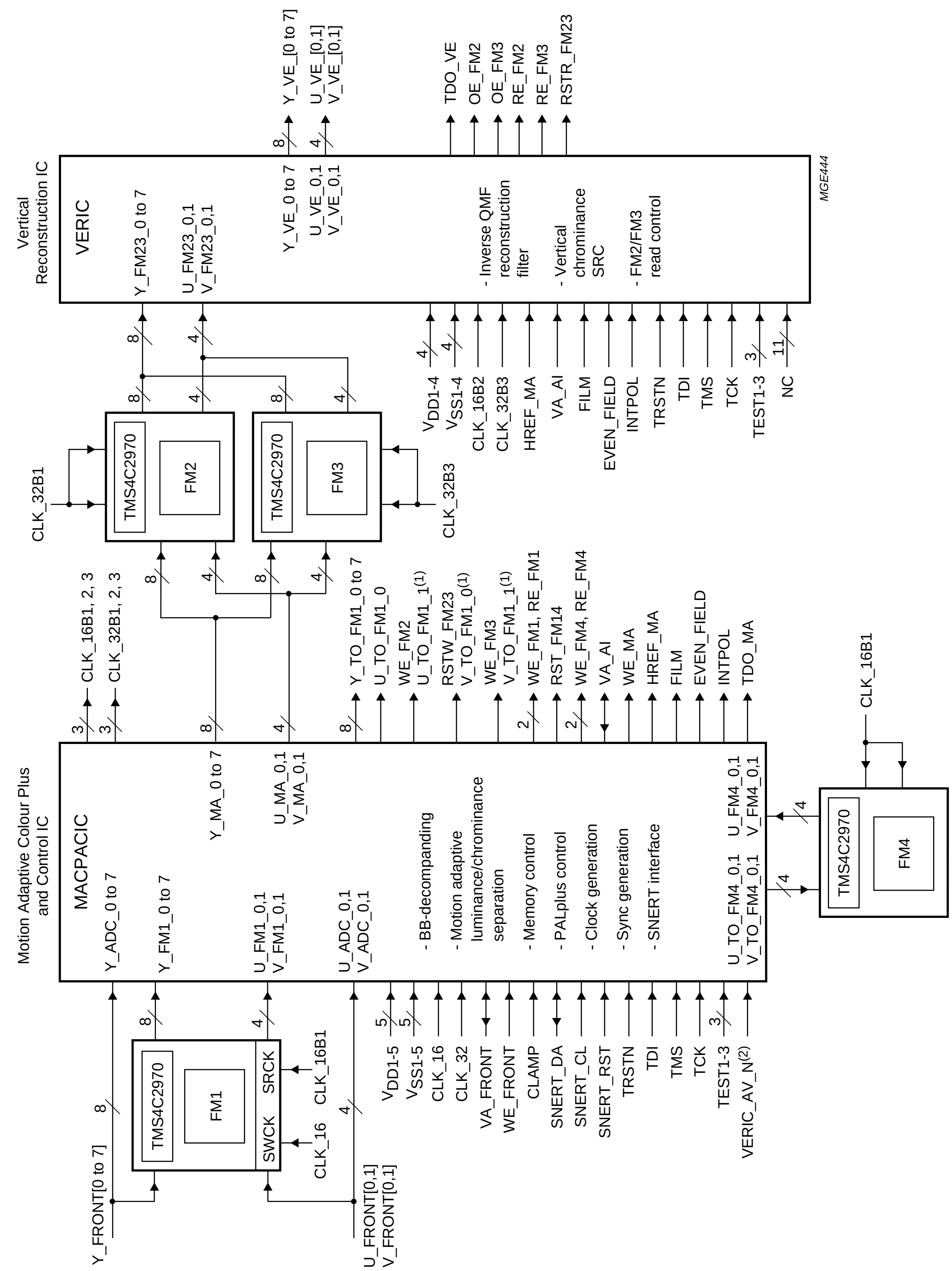


Fig.1 Block diagram.



(1) In case of stand alone MACPACIC the output signals are U_TO_FM1_1, V_TO_FM1_0 or V_TO_FM1_1; otherwise the output signals are WE_FM2, RSTW_FM23 or WE_FM3.

(2) VERIC available: VERIC_AV_N is connected to V_{SS}.

Fig.2 Block diagram of the PALplus decoder module.

PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
Y_VE_1	1	output	luminance output data bit 1
Y_VE_0	2	output	luminance output data bit 0
U_VE_1	3	output	chrominance output data bit 1 U-component
U_VE_0	4	output	chrominance output data bit 0 U-component
V_VE_1	5	output	chrominance output data bit 1 V-component
V_VE_0	6	output	chrominance output data bit 0 V-component
V_{SS1}	7	input	ground 1
V_{DD1}	8	input	positive supply voltage 1 (+5 V)
n.c.	9	–	not connected
n.c.	10	–	not connected
n.c.	11	–	not connected
n.c.	12	–	not connected
n.c.	13	–	not connected
n.c.	14	–	not connected
n.c.	15	–	not connected
n.c.	16	–	not connected
HREF_MA	17	input	horizontal reference
n.c.	18	–	not connected
VA_AI	19	input	vertical reference pulse related to output data
INTPOL	20	input	INTPOL = 1: PALplus interpolation active
			INTPOL = 0: VERIC switched to bypass mode (standard signal)
FILM	21	input	FILM = 0: CAMERA mode
			FILM = 1: FILM mode
EVEN_FIELD	22	input	EVEN_FIELD = 0: odd field related to MACPACIC input data
			EVEN_FIELD = 1: even field related to MACPACIC input data
CLK_16B2	23	input	buffered clock input (16 MHz)
V_{SS2}	24	input	ground 2
V_{DD2}	25	input	positive supply voltage 2 (+5 V)
TCK	26	input	boundary scan test clock input
TMS	27	input	boundary scan test mode select input
TDI	28	input	boundary scan test data input
TDO_VE	29	output	boundary scan test data output
TRSTN	30	input	boundary scan test reset input
n.c.	31	–	not connected
n.c.	32	–	not connected
TEST1	33	tbf	test pins
TEST2	34	tbf	
TEST3	35	tbf	
CLK_32B3	36	input	buffered clock input (32 MHz)
V_{SS3}	37	input	ground 3

SYMBOL	PIN	TYPE	DESCRIPTION
V_{DD3}	38	input	positive supply voltage 3 (+5 V)
OE_FM3	39	output	output enable field memory 3
RE_FM3	40	output	read enable field memory 3
V_FM23_1	41	input	chrominance input data bit 1 V-component
V_FM23_0	42	input	chrominance input data bit 0 V-component
U_FM23_1	43	input	chrominance input data bit 1 U-component
U_FM23_0	44	input	chrominance input data bit 0 U-component
Y_FM23_7	45	input	Y input data bit 7
Y_FM23_6	46	input	Y input data bit 6
Y_FM23_5	47	input	Y input data bit 5
Y_FM23_4	48	input	Y input data bit 4
Y_FM23_3	49	input	Y input data bit 3
n.c.	50	–	not connected
Y_FM23_2	51	input	Y input data bit 2
Y_FM23_1	52	input	Y input data bit 1
Y_FM23_0	53	input	Y input data bit 0
RSTR_FM23	54	output	reset read field memory 2 and 3
RE_FM2	55	output	read enable field memory 2
OE_FM2	56	output	output enable field memory 2
V_{DD4}	57	input	positive supply voltage 4 (+5 V)
V_{SS4}	58	input	ground 4
Y_VE_7	59	output	luminance output data bit 7
Y_VE_6	60	output	luminance output data bit 6
Y_VE_5	61	output	luminance output data bit 5
Y_VE_4	62	output	luminance output data bit 4
Y_VE_3	63	output	luminance output data bit 3
Y_VE_2	64	output	luminance output data bit 2

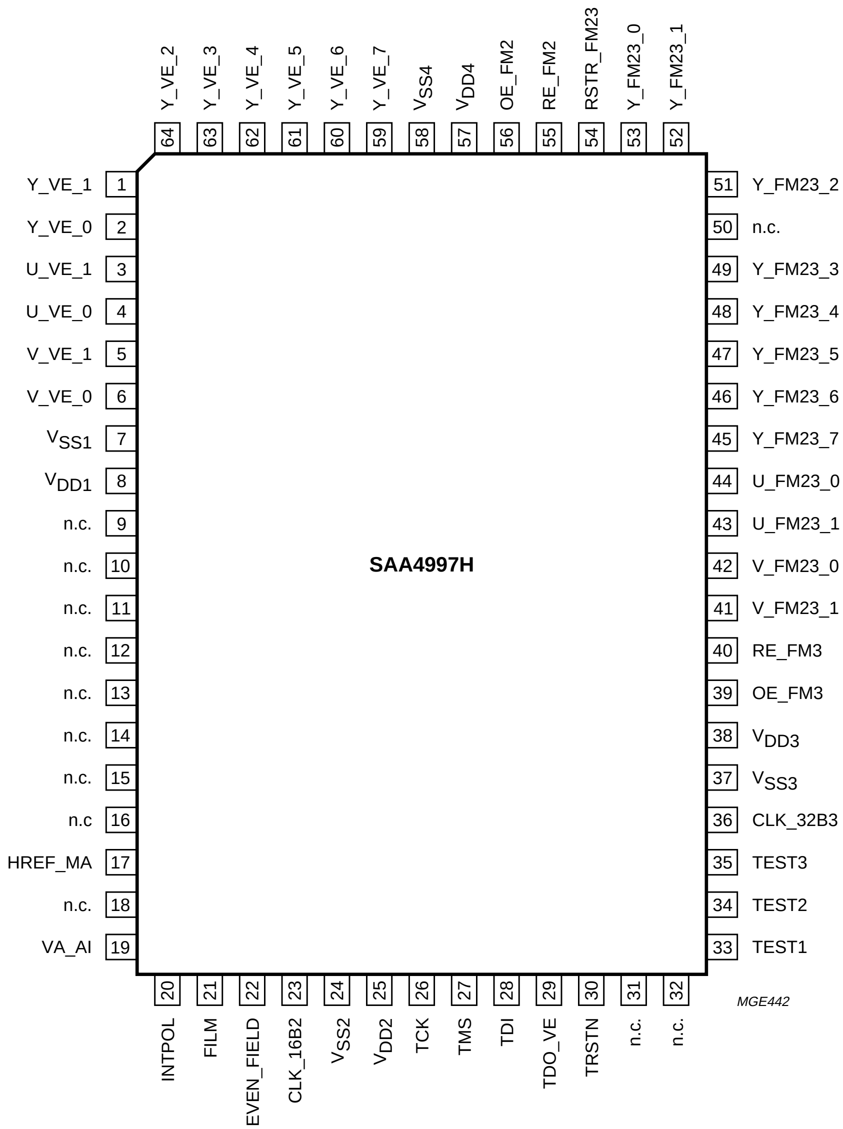


Fig.3 Pin configuration.

FUNCTIONAL DESCRIPTION

Introduction

As shown in Fig.2 the PALplus module consists of two special integrated circuits:

- Motion Adaptive Colour Plus And Control IC (MACPACIC)
- VErtical Reconstruction IC (VERIC)

and four field memories TMS4C2970.

The MACPACIC and the VERIC are intended to generate digitally decoded 50 Hz YUV signals. The MACPACIC performs the decompanding function for the helper lines and the motion adaptive luminance/chrominance separation. Furthermore, PALplus system controlling, memory controlling and clock generation are carried out in this circuit.

The function of the VERIC is to reconstruct the separated 2×72 helper lines and the 430 main lines into a standard 576 lines frame according the PALplus system description *"REV 2.0"*. Chrominance is converted from 430 lines to 576 lines using a vertical sample rate converter.

The data of the VERIC are clocked out with 16 MHz. The Y : U : V bandwidth ratio is 4 : 1 : 1.

The functional block diagram of the VERIC is shown in Fig.1. The device consists of 3 main parts:

- Luminance processing
- Chrominance processing
- Controlling.

The input data are delivered by the field memories FM2 and FM3, which include multiplexed first and second field data processed by the MACPACIC. The luminance and chrominance input data of the VERIC are clocked with 32 MHz (CLK_32B3). Internally the device operates at 32 or 16 MHz clock frequency.

Luminance processing

In the PALplus encoder the luminance signal is separated vertically into two sub-bands by a special Quadrature Mirror Filter (QMF).

A vertical low-pass sub-band consists of the 430 main letter box lines per frame, and a vertical high-pass sub-band includes the 144 helper lines per frame.

The used QMF technique has two advantages:

- Essentially loss-free data processing
- Cancellation of alias components in the main and helper signal in the decoder.

The luminance vertical conversion process in the decoder is complementary to that of the encoder.

In the decoder the inverse QMF function is implemented to recombine the two separated sub-bands and to generate the original video signal with 576 active lines per frame.

Each output line is calculated from up to seven input lines stored in line memories containing main or helper information. The various lines are multiplied by switched coefficients, changing every line within a sequence of four lines, depending on the specific mode (CAMERA or FILM).

In case of standard PAL reception, the VERIC is switched to bypass mode controlled by the signal INTPOL.

For multi-PIP processing the VERIC is also switched to bypass mode, but controlling of FM2/3 is different (see Fig.6). The total signal delay between the MACPACIC input and the VERIC output is one line for this mode. FM2/3 are driven with 32 MHz clock frequency.
The non-multiplexed input data are clocked out with 16 MHz.

Chrominance processing

The chrominance processing is carried out by the vertical interpolation filter (poly phase filter).

In CAMERA and FILM mode, intra-field vertical sample rate conversion is carried out.

One output line is calculated out of three or four lines in CAMERA or FILM mode using different coefficients or passed through in bypass mode.

Control functions

The VERIC controller generates the necessary internal control signals for the line memories, formatters, reformatters, the selector signals for the multiplexers and the read signals for the field memories FM2/3.

The system control input signals EVEN_FIELD, INTPOL and FILM are derived from the control part of the MACPACIC. The field selection information EVEN_FIELD is related to the input data of the MACPACIC and is adapted in the VERIC to its input data.

The control functions are described in Tables 1 and 2.

Table 1 EVEN_FIELD

VALUE	STATUS
EVEN_FIELD = 1	even field selected
EVEN_FIELD = 0	odd field selected

Table 2 INTPOL and FILM

VALUE		STATUS
INTPOL = 0	FILM = 0	bypass mode; standard signals
INTPOL = 1	FILM = 0	interpolation active; PALplus CAMERA mode
INTPOL = 0	FILM = 1	bypass mode; multi-PIP
INTPOL = 1	FILM = 1	interpolation active; PALplus FILM mode

Modes and delays

The PALplus module can operate in two different hardware configurations:

- Full PALplus configuration (MACPACIC and VERIC)
- Stand alone MACPACIC.

The vertical interpolation of the VERIC can be activated by the signal INTPOL depending on the PALplus signalling bits, transmitted in line 23 indicating the type of signal being received.

However, the delay between input data of the MACPACIC and output data of the VERIC always has to be 1.5 fields. This is achieved with a suitable read timing of the field memories FM2 and FM3 controlled by VA_AI which is derived from the field length measurement in the MACPACIC.

In case of INTPOL = LOW and additionally FILM = HIGH (FILM mode), the VERIC is switched to multi-PIP mode. In case the delay between input of the MACPACIC and output of the VERIC is one line (1024 CLK_16 periods).

The line and pixel timings of the VERIC are shown in Figures 5 to 14.

Table 3 Delays

MODE	FIELD	VERIC I/O DELAY
FILM mode	first	2 lines
	second	3 lines
CAMERA mode	first	3 lines
	second	4 lines

Input/Output formats

INPUT FORMATS

The luminance input range of the main and helper signal has the following values:

Main signal: black = 16, white = 191 (straight binary)

Helper signal: ±70, mid = 128 (straight binary)

Chrominance format: ±90, mid = 0 (two’s complement).

OUTPUT FORMATS

Luminance format: black = 16, white = 191 (straight binary)

Blanking: code 16

Chrominance format: ±90, mid = 0 (two’s complement)

Blanking: code 0.

Test activities

The pins TEST1, TEST2 and TEST3 are provided to perform the IC test activities, such as scan test.

The pins TRSTN, TDI, TMS, TCK and TDO_VE are intended for a boundary scan test.

DC CHARACTERISTICS

T_j = 0 to 125 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		4.75	5.0	5.25	V
I_{DD}	supply current	V_{DD} = 5 V	–	–	80	mA
$I_{DD(q)}$	quiescent supply current	all inputs to V_{DD} or V_{SS}	–	–	100	µA
Inputs						
V_{IL}	LOW level input voltage		–0.5	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DD}	V
I_{LI}	input leakage current		–	–	1.0	µA
Outputs						
V_{OL}	LOW level output voltage	I_O = 20 µA	–	–	0.1	V
V_{OH}	HIGH level output voltage	I_O = 20 µA	V_{DD} – 0.1	–	–	V
I_{OL}	LOW level output current	V_O = 0.5 V	4.0	–	–	mA
I_{OH}	HIGH level output current	$V_O = V_{DD}$ – 0.5 V	4.0	–	–	mA

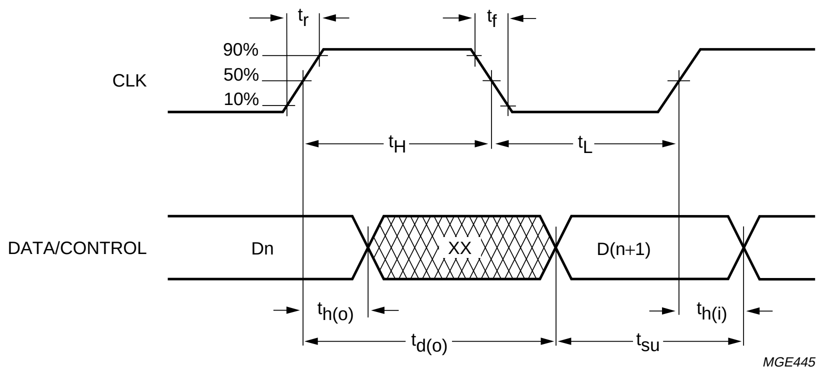
AC CHARACTERISTICS

T_j = 0 to 125 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clock timing CLK_32B3 (see Fig.4)						
$T_{CY(32)}$	cycle time		28.1	31.25	–	ns
t_H	HIGH time		9.2	–	–	ns
t_L	LOW time		9.2	–	–	ns
t_r	rise time		2.0	–	4.0	ns
t_f	fall time		2.0	–	4.0	ns
Δf_{clk}	deviation of clock frequency		–10	–	+10	%
Clock timing CLK_16B2 (see Fig.4)						
$T_{CY(16)}$	cycle time		56.2	–	–	ns
t_H	HIGH time		20.5	–	–	ns
t_L	LOW time		20.5	–	–	ns
t_r	rise time		2.0	–	4.0	ns
t_f	fall time		4.0	–	4.0	ns
δ	duty cycle	$\delta = \frac{t_H}{t_L}$	40	–	50	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input data timing (CLK_32)						
t_{su}	input data set-up time					
	CLK_16B2		−4.7	–	–	ns
	Y and UV_FM23		−0.8	–	–	ns
$t_{h(i)}$	input data hold time					
	CLK_16B2		5.1	–	–	ns
	Y and UV_FM23		5.2	–	–	ns
Input control timing (CLK_16B2)						
HREF_MA, VA_AI, FILM, EVEN_FIELD AND INTPOL						
t_{su}	input data set-up time		4.5	–	–	ns
$t_{h(i)}$	input data hold time		0.1	–	–	ns
Output data timing (CLK_16B2)						
Y AND UV_FM23						
$t_{h(o)}$	output data hold time	C_L = 15 pF	8	–	–	ns
$t_{d(o)}$	output data delay time	C_L = 15 pF	–	–	27	ns
Output control timing (CLK_32B3)						
OE_FM2, OE_FM3, RE_FM2, RE_FM3 AND RSTR_FM23						
$t_{h(o)}$	output data hold time	C_L = 15 pF	5	–	–	ns
$t_{d(o)}$	output data delay time	C_L = 15 pF	–	–	20	ns
Delays						
$t_{w(HREF)}$	HREF_MA pulse width		–	$60 \times T_{CY(16)}$	–	ns
$t_{d(RE)}$	delay RE_FM2/3 to HREF_MA		–	$127 \times T_{CY(32)}$	–	ns
$t_{w(RE)}$	RE_FM2/3 pulse width		–	$1680 \times T_{CY(32)}$	–	ns
$t_{d(VE)(MA)}$	delay HREF_MA to YUV_VE		–	$80 \times T_{CY(16)}$	–	ns
$t_{d(VE)}$	delay data input to output		–	$16 \times T_{CY(16)}$	–	ns
$t_{d(VE)}$	delay data input to output	multi-PIP	–	$2 \times T_{CY(16)}$	–	ns
$t_{d(RSTR)}$	delay RSTR	multi-PIP	–	$2016 \times T_{CY(32)}$	–	ns
$t_{d(FM2)}$	delay FM2 input to output	multi-PIP	–	$2040 \times T_{CY(32)}$	–	ns

TIMING



Data input: CLK = CLK_32B3
Data output: CLK = CLK_16B2
Control input: CLK = CLK_16B2
Control output: CLK = CLK_32B3

Fig.4 Data/control input/output set-up and hold timing.

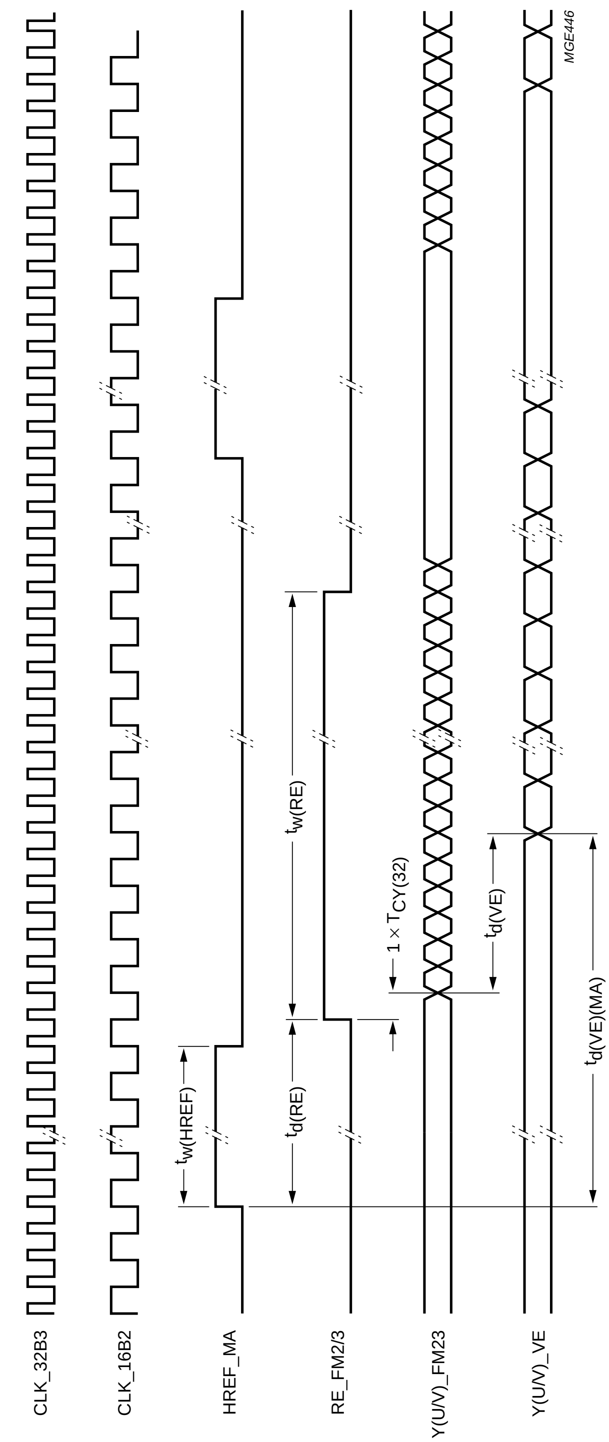
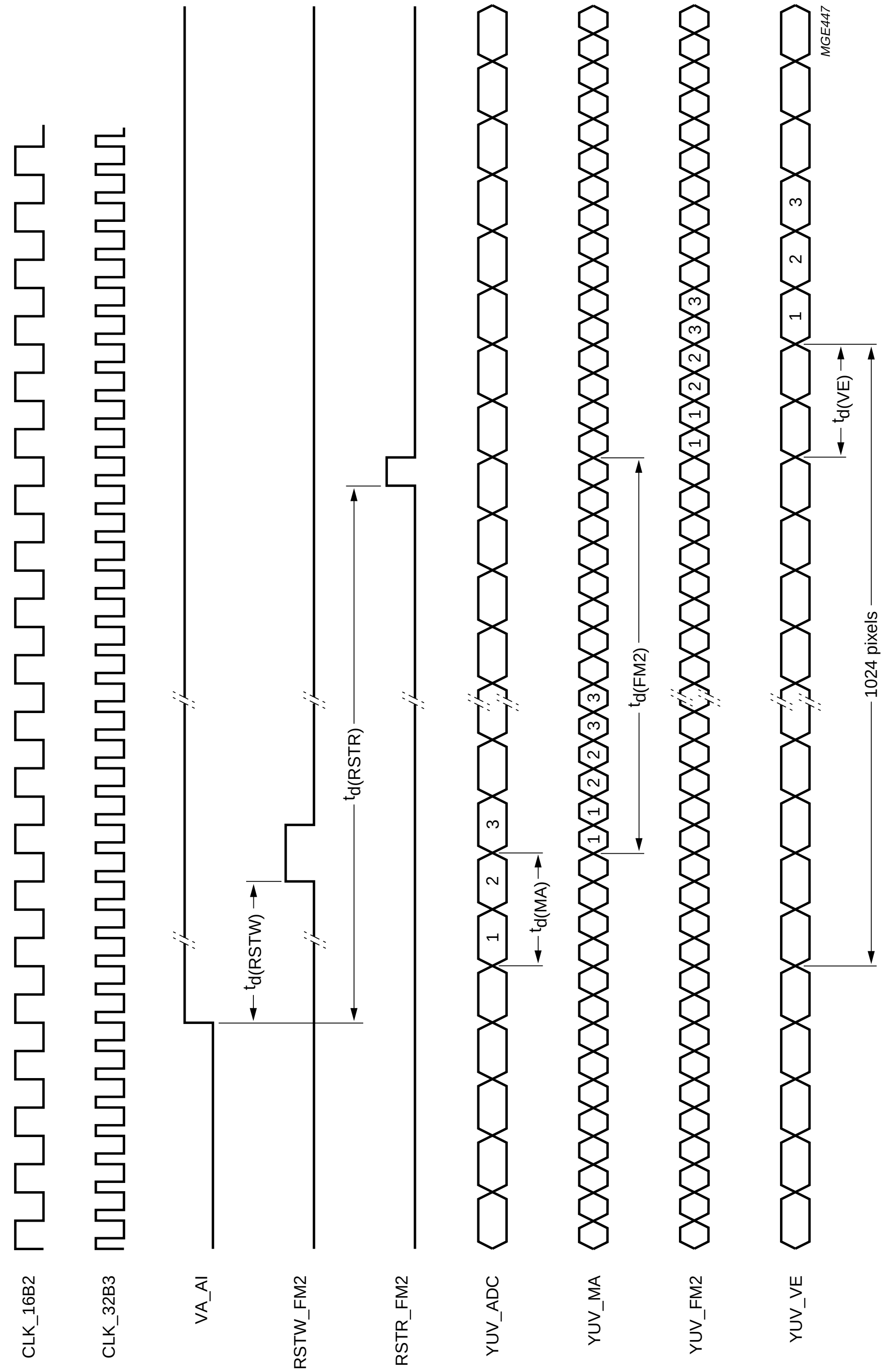


Fig.5 Pixel timing (except multi-PIP mode).



WE_FM2 and RE_FM2 are constant HIGH; YUV_MA = MACPACIC input.

Fig.6 Pixel timing multi-PIP mode (MACPACIC input to VERIC output).

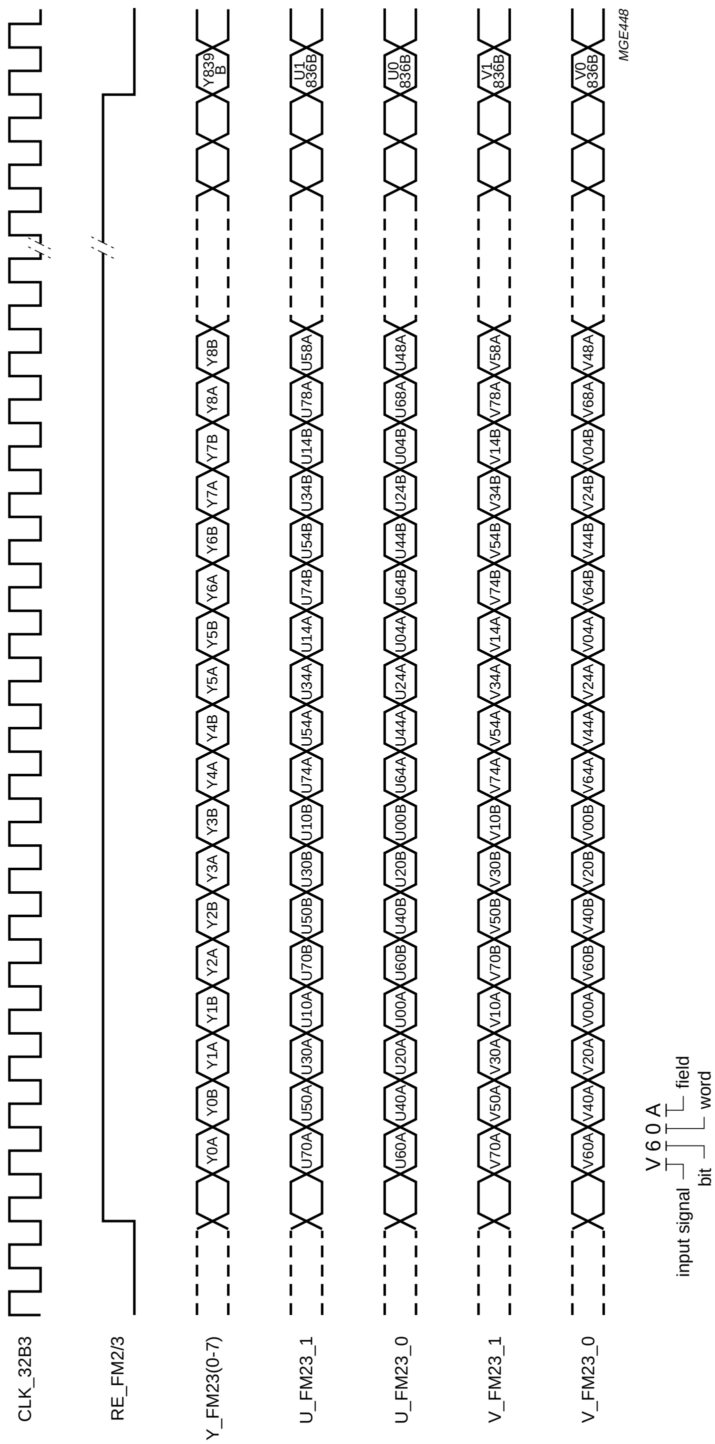


Fig.7 Input data timing (except multi-PIP mode).

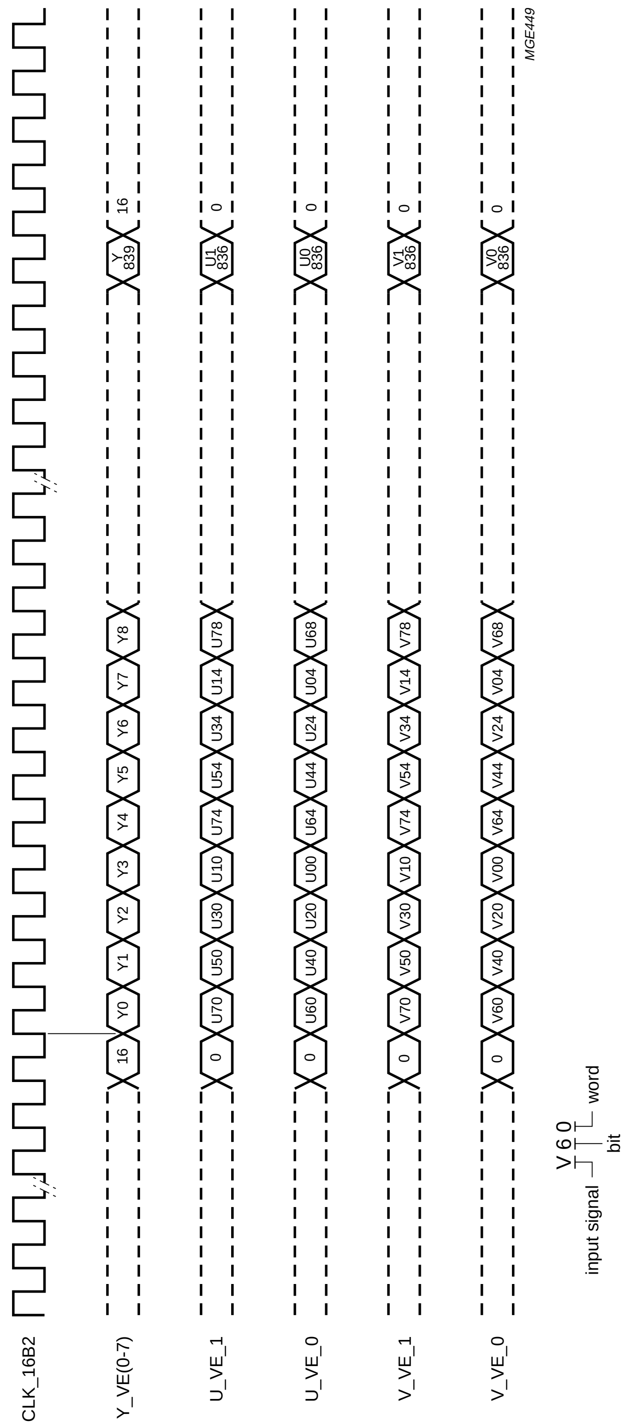


Fig.8 Output data timing.

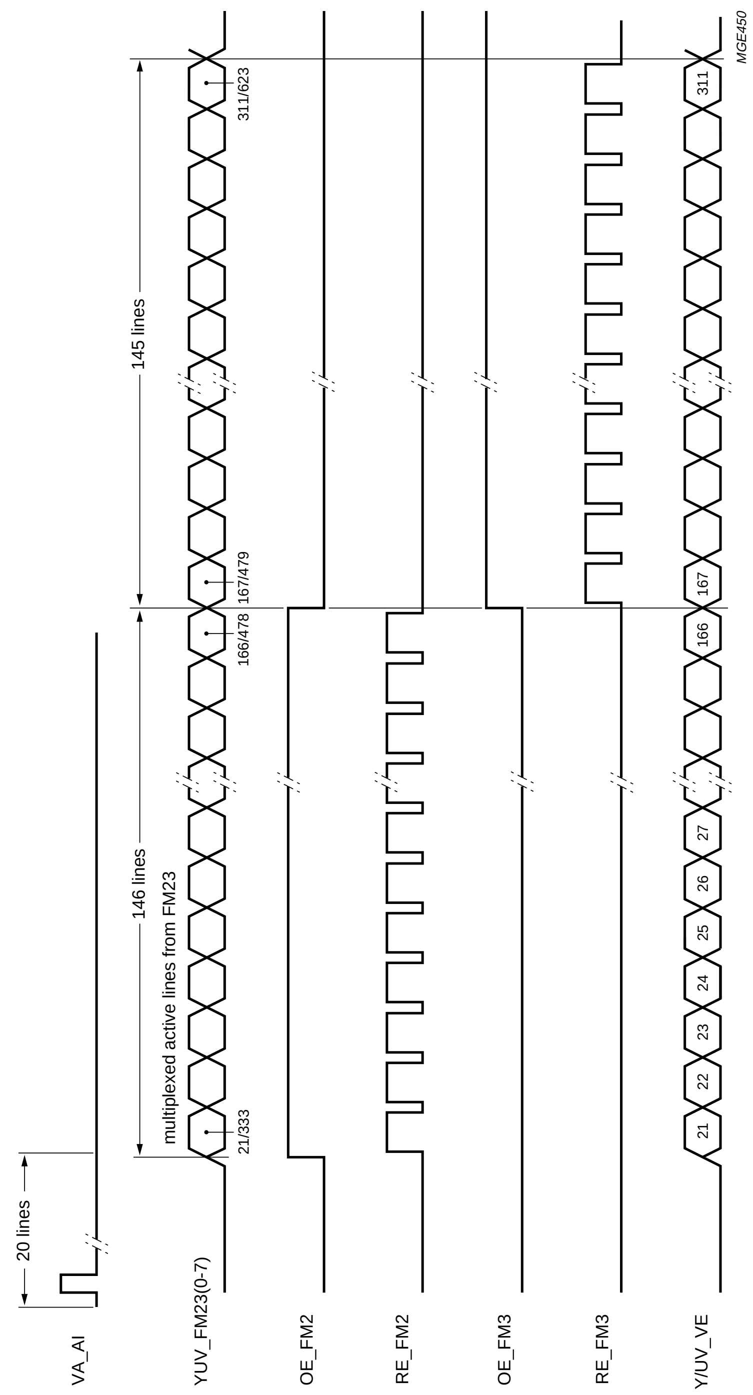


Fig.9 Line read timing FM2/3 bypass mode standard signal, first field.

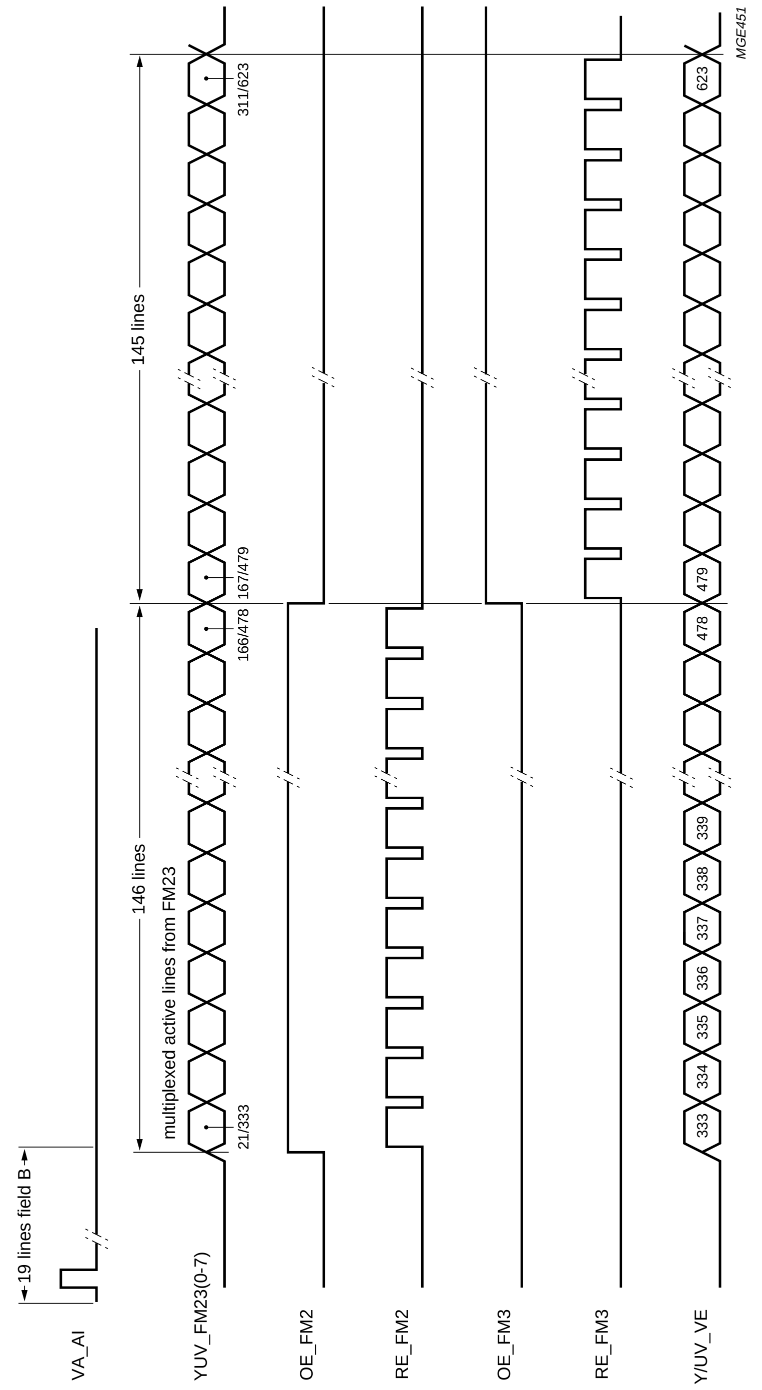
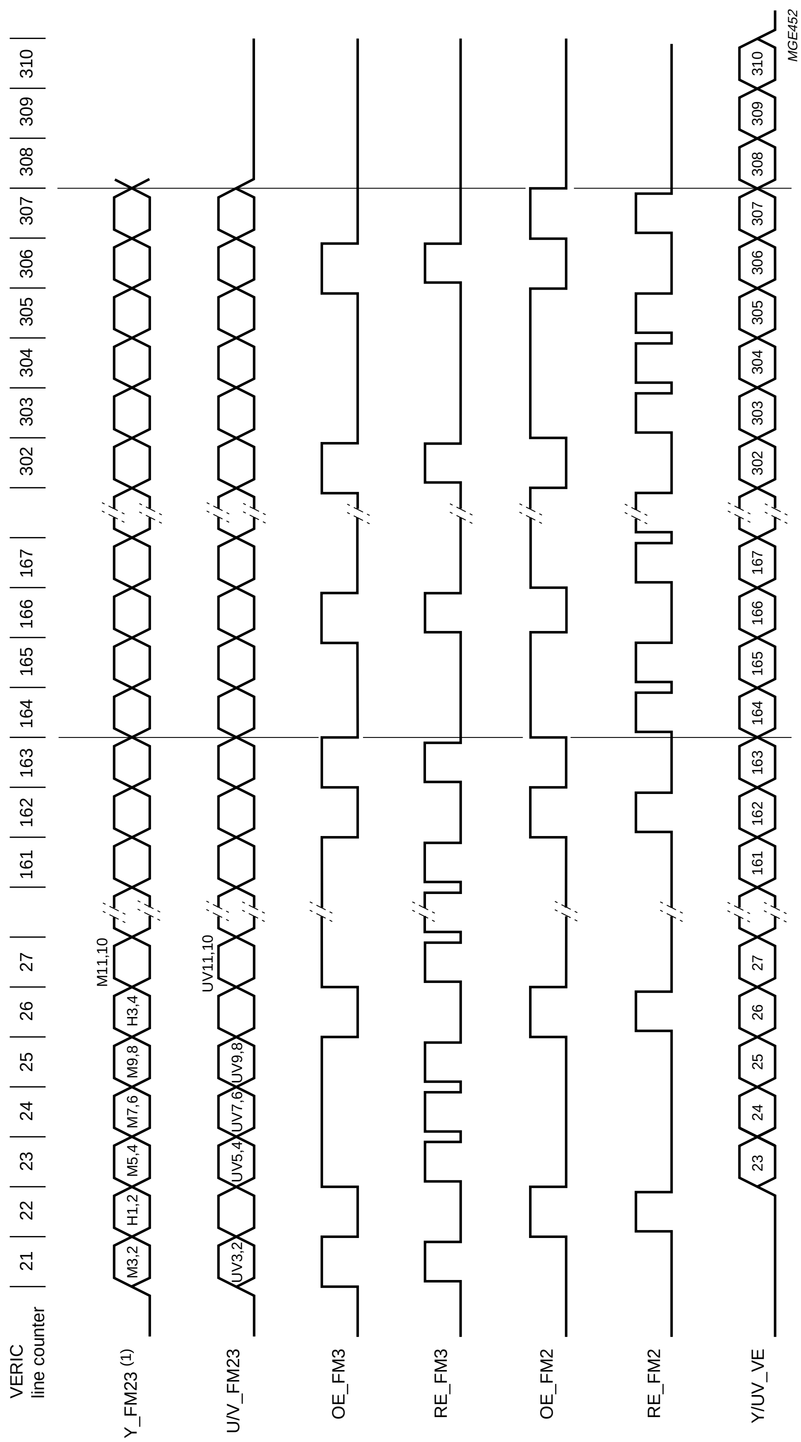


Fig.10 Line read timing FM2/3 bypass mode standard signal, second field.



(1) M = main line and H = helper line.

Fig.11 Line read timing FM2/3 CAMERA mode, first field.

VErtical Reconstruction IC (VERIC) for PALplus

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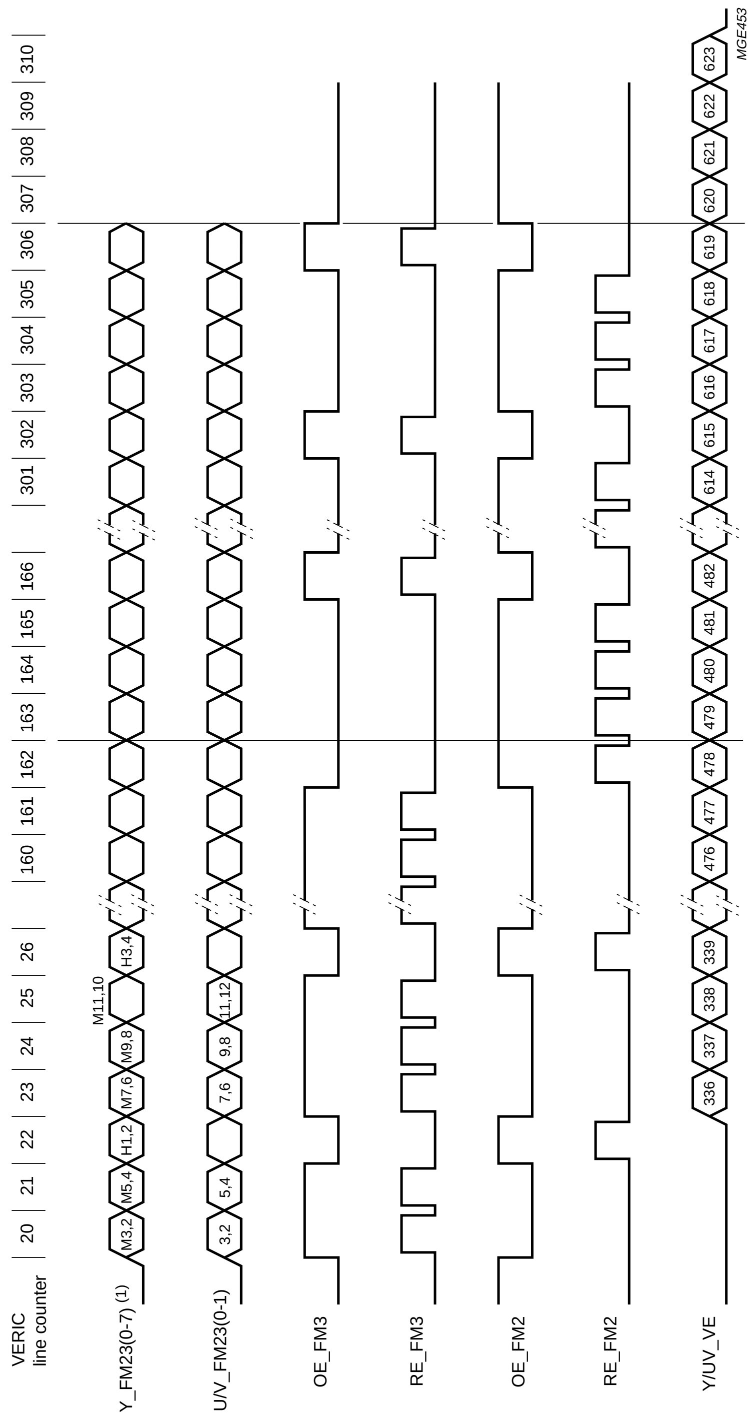
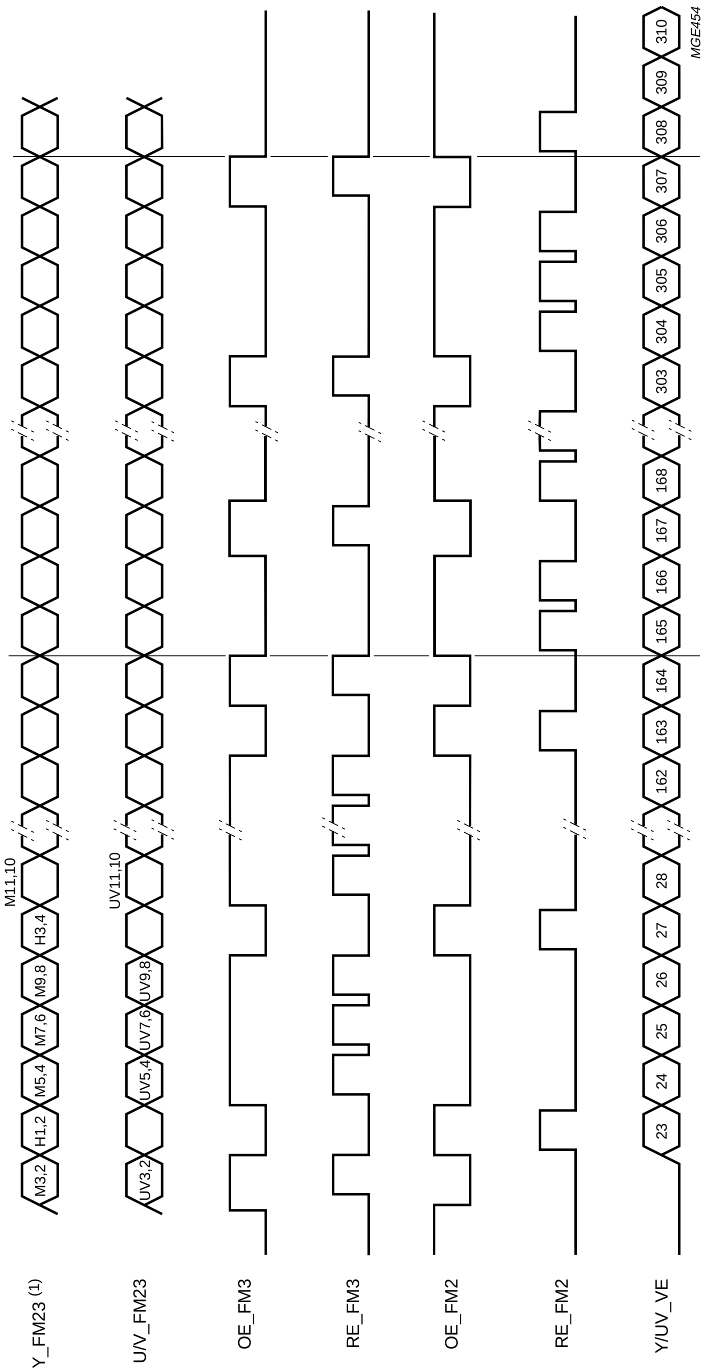


(1) M = main line and H = helper line.

Fig.12 Line read timing FM2/3 CAMERA mode, second field.



(1) M = main line and H = helper line.

Fig.13 Line read timing FM2/3 FILM mode, first field.

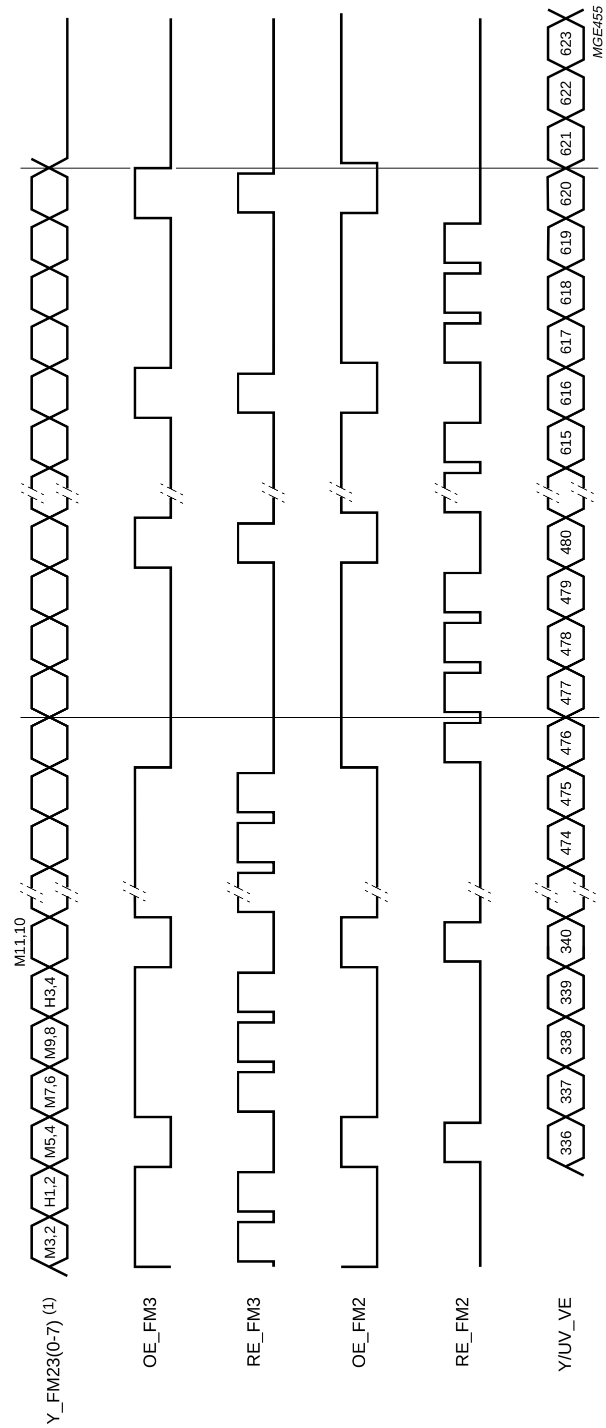
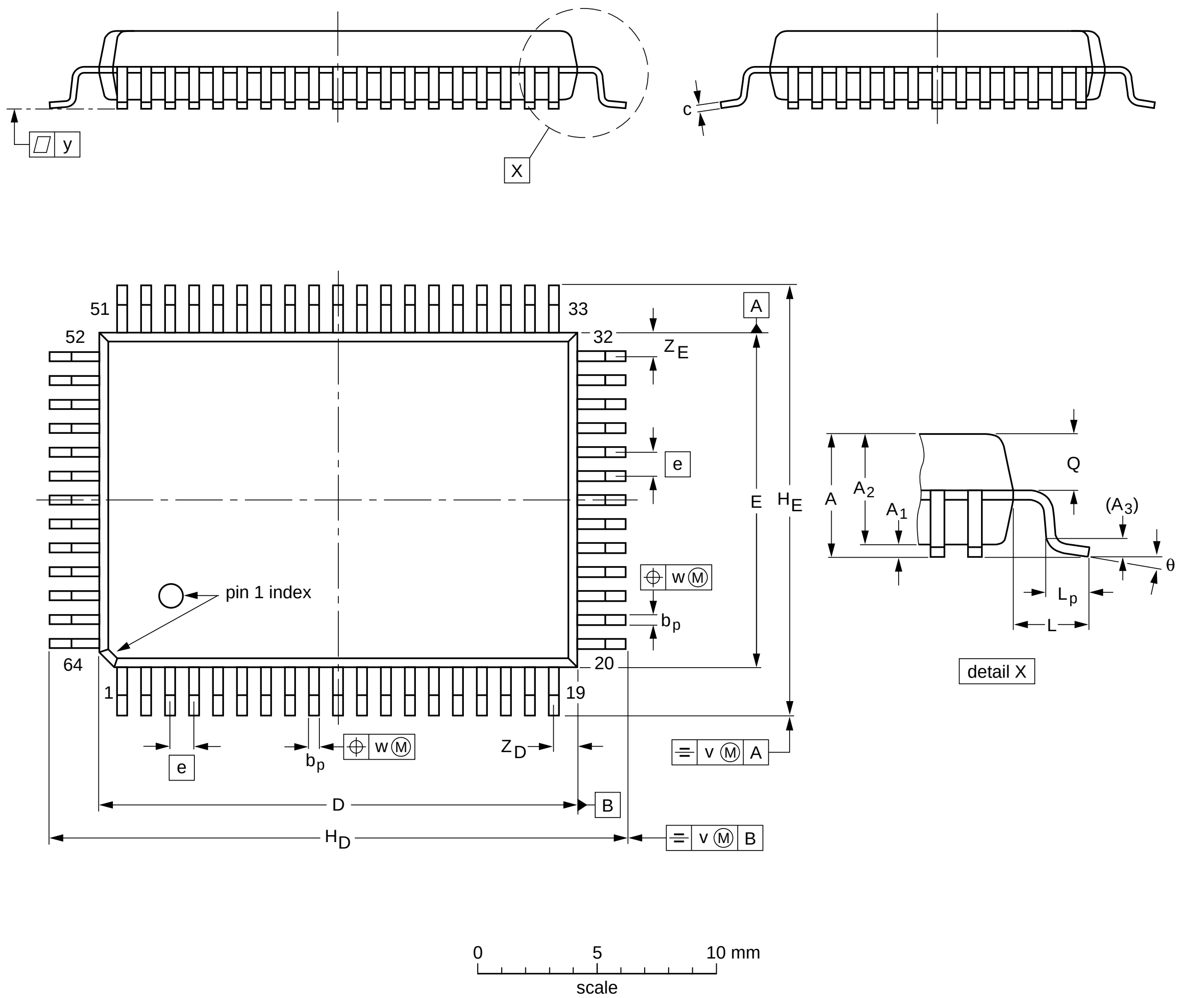


Fig.14 Line read timing FM2/3 FILM mode, second field.

(1) M = main line and H = helper line.

PACKAGE OUTLINE

QFP64: plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm **SOT319-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.20	0.25 0.05	2.90 2.65	0.25	0.50 0.35	0.25 0.14	20.1 19.9	14.1 13.9	1	24.2 23.6	18.2 17.6	1.95	1.0 0.6	1.4 1.2	0.2	0.2	0.1	1.2 0.8	1.2 0.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT319-2						~~92-11-17~~ 95-02-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9398 510 63011).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

NOTES

NOTES

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