M36LLR8760T1, M36LLR8760D1
M36LLR8760M1, M36LLR8760B1

256 + 128 Mbit (Multiple Bank, Multi-Level, Burst) Flash Memory
64 Mbit (Burst) PSRAM, 1.8V Supply, Multi-Chip Package

TARGET SPECIFICATION

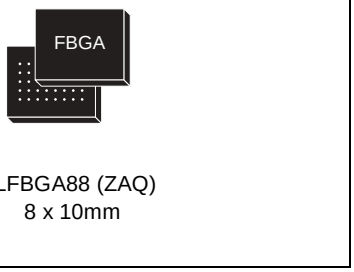
FEATURES SUMMARY

- MULTI-CHIP PACKAGE
  - 1 die of 256 Mbit (16Mb x16, Multiple Bank, Multi-level, Burst) Flash Memory
  - 1 die of 128 Mbit (8Mb x16, Multiple Bank, Multi-Level, Burst) Flash Memory
  - 1 die of 64 Mbit (4Mb x16) Pseudo SRAM
- SUPPLY VOLTAGE
  - $V_{DDF1} = V_{DDF2} = V_{CCP} = V_{DDQF}$ = 1.7 to 1.95V
  - V_{PPF} = 9V for fast program (12V tolerant)
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 20h
  - Top Configuration (Top + Top) M36LLR8760T1: 880Dh + 88C4h
  - Mixed Configuration (Bottom + Top) M36LLR8760D1: 880Eh + 88C4h
  - Mixed Configuration (Top + Bottom) M36LLR8760M1: 880Dh + 88C5h
  - Bottom Configuration (Bottom + Bottom) M36LLR8760B1: 880Eh + 88C5h
- PACKAGE
  - Compliant with Lead-Free Soldering Processes
  - Lead-Free Versions

FLASH MEMORIES

- SYNCHRONOUS / ASYNCHRONOUS READ
  - Synchronous Burst Read mode: 54MHz
  - Asynchronous Page Read mode
  - Random Access: 85ns
- SYNCHRONOUS BURST READ SUSPEND
- PROGRAMMING TIME
  - 10µs typical Word program time using Buffer Enhanced Factory Program command
- MEMORY ORGANIZATION
  - Multiple Bank Memory Array: 16 Mbit Banks for the 256 Mbit Memory 8 Mbit Banks for the 128 Mbit Memory
  - Parameter Blocks (at Top or Bottom)

Figure 1. Package



LFBGA88 (ZAQ)
8 x 10mm

- COMMON FLASH INTERFACE (CFI)
- 100,000 PROGRAM/ERASE CYCLES per BLOCK
- DUAL OPERATIONS
  - program/erase in one Bank while read in others
  - No delay between read and write operations
- SECURITY
  - 64 bit unique device number
  - 2112 bit user programmable OTP Cells
- BLOCK LOCKING
  - All blocks locked at power-up
  - Any combination of blocks can be locked with zero latency
  - $\overline{WP}_F$ for Block Lock-Down
  - Absolute Write Protection with $V_{PPF} = V_{SS}$

PSRAM

- ACCESS TIME: 70ns
- ASYNCHRONOUS PAGE READ
  - Page Size: 16 words
  - Subsequent read within page: 20ns
- LOW POWER FEATURES
  - Temperature Compensated Refresh (TCR)
  - Partial Array Refresh (PAR)
  - Deep Power-Down (DPD) Mode
- SYNCHRONOUS BURST READ/WRITE

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SUMMARY DESCRIPTION

The M36LLR8760T1, M36LLR8760D1, M36LLR8760M1 and M36LLR8760B1 combine three memory devices in a Multi-Chip Package:

- a 256-Mbit, Multiple Bank Flash memory, the M30L0R8000(T/B)0 (Flash 1)
- a 128-Mbit, Multiple Bank Flash memory, the M58LR128GT/B (Flash 2)
- a 64-Mbit PseudoSRAM, the M69KB096AA.

For detailed information on how to use the memory components, refer to the M30L0R8000(T/B)0, M58LR128GT/B and M69KB096AA datasheets which are available from your local STMicroelectronics distributor and should be read in conjunction with the M36LLR8760x1 datasheet.

What differs between the M36LLR8760T1, M36LLR8760D1 and M36LLR8760B1 is the configuration of the two Flash memories:

- in the M36LLR8760T1, Flash 1 and Flash 2 both have a Top Configuration (Parameter Blocks located at the top of the address space).
- in the M36LLR8760D1, Flash 1 has a Bottom Configuration (Parameter Blocks at the bottom of the address space) and Flash 2 has a Top Configuration.
- In the M36LLR8760M1, Flash 1 has a Top Configuration and Flash 2 has a Bottom Configuration.
- In the M36LLR8760B1, both Flash 1 and Flash 2 have a Bottom Configuration.

Recommended operating conditions do not allow more than one memory to be active at the same time.

The memories are offered in a Stacked LFBGA88 (8 x 10mm, 8x10 ball array, 0.8mm pitch) package.

In addition to the standard version, the package is also available in Lead-free version, in compliance with JEDEC Std J-STD-020B, the ST ECOPACK 7191395 Specification, and the RoHS (Restriction of Hazardous Substances) directive. All packages are compliant with Lead-free soldering processes.

The memory is supplied with all the bits erased (set to '1').

Figure 2. Logic Diagram

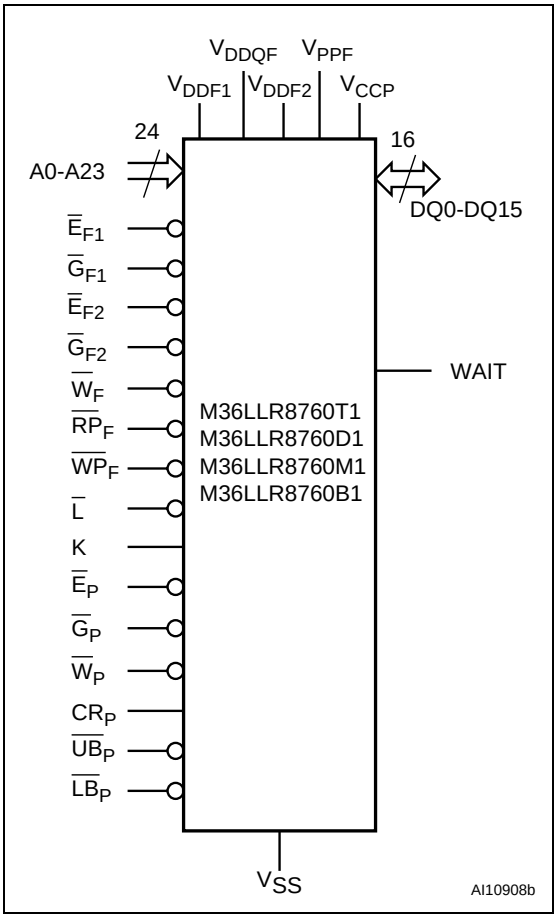
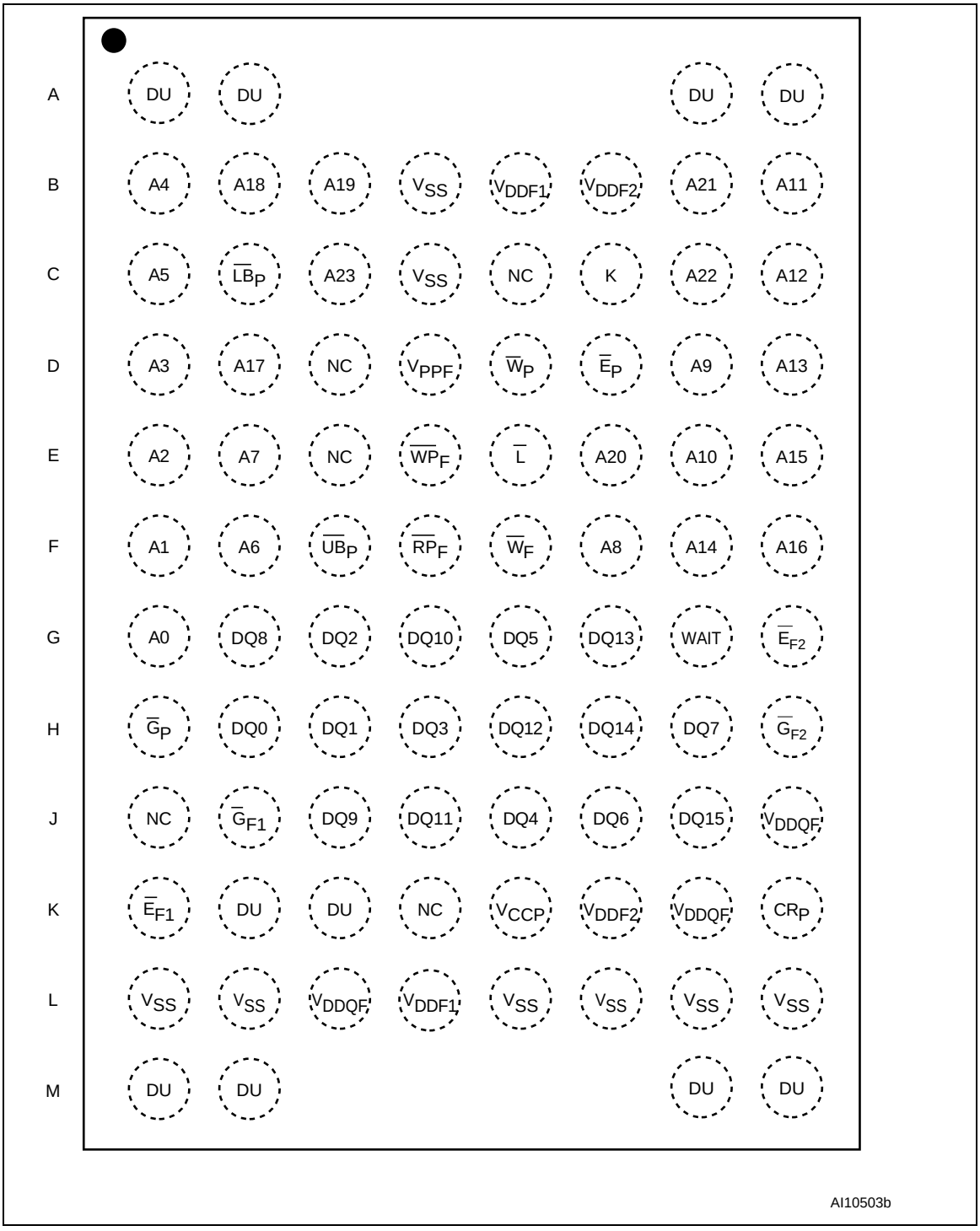


Table 1. Signal Names

A0-A23(1)	Address Inputs
DQ0-DQ15	Common Data Input/Output
$\overline{L}$	Common Flash and PSRAM Latch Enable Input
K	Common Flash and PSRAM Burst Clock
WAIT	Wait Data in Burst Mode for both Flash memories and PSRAM
V_{DDF1}	Flash 1 Power Supply
V_{DDF2}	Flash 2 Power Supply
V_{DDQF}	Common Flash Supply for I/O Buffers
V_{PPF}	Common Flash Optional Supply Voltage for Fast Program & Erase
V_{SS}	Common, Ground
V_{CCP}	PSRAM Power Supply
NC	Not Connected Internally
DU	Do Not Use as Internally Connected
Flash Memory Signals	
$\overline{E}_{F1}$	Flash 1 Chip Enable Input
$\overline{G}_{F1}$	Flash 1 Output Enable Input
$\overline{E}_{F2}$	Flash 2 Chip Enable Input
$\overline{G}_{F2}$	Flash 2 Output Enable Input
$\overline{W}_F$	Common Flash Memory Write Enable Input
$\overline{RP}_F$	Common Flash Memory Reset input
$\overline{WP}_F$	Common Flash Memory Write Protect Input
PSRAM Signals	
$\overline{E}_P$	Chip Enable Input
$\overline{G}_P$	Output Enable Input
$\overline{W}_P$	Write Enable Input
CR_P	Configuration Register Enable Input
$\overline{UB}_P$	Upper Byte Enable Input
$\overline{LB}_P$	Lower Byte Enable Input

Note: 1. A22 is an Address Input for the two Flash memories only. A23 is for the 256Mb Flash memory component only.

Figure 3. LFBGA Connections (Top view through package)



Note: A22 is an Address Input for the two Flash memories only. A23 is for the 256Mb Flash memory component only.

SIGNAL DESCRIPTIONS

See Figure 2., Logic Diagram and Table 1., Signal Names, for a brief overview of the signals connected to this device.

Address Inputs (A0-A23). Addresses A0-A21 are common inputs for the Flash memory and PSRAM components. A22 is common to the two Flash memory components whereas A23 is an address input for the 256 Mbit Flash memory component only.

The Address Inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the Command Interface of the internal state machine. The Flash memories are accessed through the Chip Enable signal ($\overline{E}_F$) and through the Write Enable signal (W_F), while the PSRAM is accessed through the Chip Enable signal ($\overline{E}_P$) and the Write Enable signal (W_P).

It is not allowed to have $\overline{E}_F$ Low, and $\overline{E}_P$ Low at the same time.

Data Input/Output (DQ0-DQ15). The Data I/O output the data stored at the selected address during a Bus Read operation or input a command or the data to be programmed during a Bus Write operation.

For the PSRAM component, the upper Byte Data Inputs/Outputs (DQ8-DQ15) carry the data to or from the upper part of the selected address when Upper Byte Enable (UB_P) is driven Low. The lower Byte Data Inputs/Outputs (DQ0-DQ7) carry the data to or from the lower part of the selected address when Lower Byte Enable (LB_P) is driven Low. When both UB_P and LB_P are disabled, the Data Inputs/ Outputs are high impedance.

Latch Enable ($\overline{L}$). The Latch Enable pin is common to the Flash memory and PSRAM components.

For details of how the Latch Enable signal behaves, please refer to the datasheets of the respective memory components: M69KB096AA for the PSRAM and M30L0R8000(T/B)0 and M58LR128GT/B for Flash 1 and Flash 2, respectively.

Clock (K). The Clock input pin is common to the Flash memory and PSRAM components.

For details of how the Clock signal behaves, please refer to the datasheets of the respective memory components: M69KB096AA for the PSRAM and M30L0R8000(T/B)0 and M58LR128GT/B for Flash 1 and Flash 2, respectively.

Wait (WAIT). WAIT is an output pin common to the Flash memory and PSRAM components. However the WAIT signal does not behave in the same way for the PSRAM and the Flash memories.

For details of how it behaves, please refer to the M69KB096AA datasheet for the PSRAM and to the M30L0R8000T/B0 and M58LR128GT/B datasheets for Flash 1 and Flash 2, respectively.

Flash Chip Enable Inputs ($\overline{E}_{F1}$, $\overline{E}_{F2}$). The Flash Chip Enable inputs activate the control logic, input buffers, decoders and sense amplifiers of the Flash memory component selected ($\overline{E}_{F1}$ is used to select Flash 1, $\overline{E}_{F2}$ is used to select Flash 2). When Chip Enable is Low, V_{IL}, and Reset is High, V_{IH}, the device is in active mode. When Chip Enable is at V_{IH} the corresponding Flash memory are deselected, the outputs are high impedance and the power consumption is reduced to the standby level.

It is not allowed to have $\overline{E}_{F1}$ at V_{IL}, $\overline{E}_{F2}$ at V_{IL} and $\overline{E}_P$ at V_{IL} at the same time. Only one memory component can be enabled at a time.

Flash Output Enable Inputs ($\overline{G}_{F1}$, $\overline{G}_{F2}$). The Output Enable pins control the data outputs during Flash memory Bus Read operations.

Flash Write Enable ($\overline{W}_F$). The Write Enable controls the Bus Write operation of the Flash memories' Command Interface. The data and address inputs are latched on the rising edge of Chip Enable or Write Enable whichever occurs first.

Flash Write Protect ($\overline{WP}_F$). Write Protect is an input that gives an additional hardware protection for each block. When Write Protect is Low, V_{IL}, Lock-Down is enabled and the protection status of the Locked-Down blocks cannot be changed. When Write Protect is at High, V_{IH}, Lock-Down is disabled and the Locked-Down blocks can be locked or unlocked. (See the Lock Status Table in the M30L0R8000(T/B)0 and M58LR128GT/B datasheets).

Flash Reset ($\overline{RP}_F$). The Reset input provides a hardware reset of the Flash memories. When Reset is at V_{IL}, the memory is in Reset mode: the outputs are high impedance and the current consumption is reduced to the Reset Supply Current I_{DD2}. Refer to Table 6., Flash 1 DC Characteristics - Currents, for the value of I_{DD2}. After Reset all blocks are in the Locked state and the Configuration Register is reset. When Reset is at V_{IH}, the device is in normal operation. Exiting Reset mode the device enters Asynchronous Read mode, but

a negative transition of Chip Enable or Latch Enable is required to ensure valid data outputs.

The Reset pin can be interfaced with 3V logic without any additional circuitry. It can be tied to V_{RPH} (refer to Table 8., Flash 1 and Flash 2 DC Characteristics - Voltages).

PSRAM Chip Enable input ($\overline{E}_P$). The Chip Enable input activates the PSRAM when driven Low (asserted). When deasserted (V_{IH}), the device is disabled, and goes automatically in low-power Standby mode or Deep Power-down mode.

PSRAM Write Enable ($\overline{W}_P$). Write Enable, $\overline{W}_P$, controls the Bus Write operation of the PSRAM. When asserted (V_{IL}), the device is in Write mode and Write operations can be performed either to the configuration registers or to the memory array.

PSRAM Output Enable ($\overline{G}_P$). Output Enable, $\overline{G}_P$, provides a high speed tri-state control, allowing fast read/write cycles to be achieved with the common I/O data bus.

PSRAM Upper Byte Enable ($\overline{UB}_P$). The Upper Byte En-able, $\overline{UB}_P$, gates the data on the Upper Byte Data Inputs/Outputs (DQ8-DQ15) to or from the upper part of the selected address during a Write or Read operation.

PSRAM Lower Byte Enable ($\overline{LB}_P$). The Lower Byte Enable, $\overline{LB}_P$, gates the data on the Lower Byte Data Inputs/Outputs (DQ0-DQ7) to or from the lower part of the selected address during a Write or Read operation.

If both $\overline{LB}_P$ and $\overline{UB}_P$ are disabled (High) during an operation, the device will disable the data bus from receiving or transmitting data. Although the device will seem to be deselected, it remains in an active mode as long as $\overline{E}_P$ remains Low.

PSRAM Configuration Register Enable (CR_P). When this signal is driven High, V_{IH}, Write operations load either the value of the Refresh Configuration Register (RCR) or the Bus configuration register (BCR).

V_{DDF1}/V_{DDF2} Supply Voltages. V_{DDF1} and V_{DDF2} provide the power supply to the internal cores of Flash 1 and Flash 2, respectively. It is the main power supply for all Flash memory operations (Read, Program and Erase).

V_{CCP} Supply Voltage. V_{CCP} provides the power supply to the internal core of the PSRAM device. It is the main power supply for all PSRAM operations.

V_{DDQF} Supply Voltage. V_{DDQF} provides the power supply for the Flash memory. This allows all Outputs to be powered independently of the Flash memory and SRAM core power supplies, V_{DDF} and V_{CCP}.

V_{PPF} Program Supply Voltage. V_{PPF} is both a control input and a power supply pin for the Flash memories. The two functions are selected by the voltage range applied to the pin.

If V_{PPF} is kept in a low voltage range (0V to V_{DDQF}) V_{PPF} is seen as a control input. In this case a voltage lower than V_{PPLK} gives an absolute protection against Program or Erase, while $V_{PPF} > V_{PP1}$ enables these functions (see Tables 6 and 8, DC Characteristics for the relevant values). V_{PPF} is only sampled at the beginning of a Program or Erase; a change in its value after the operation has started does not have any effect and Program or Erase operations continue.

If V_{PPF} is in the range of V_{PPH} it acts as a power supply pin. In this condition V_{PPF} must be stable until the Program/Erase algorithm is completed.

V_{SS} Ground. V_{SS} is the common ground reference for all voltage measurements in the Flash (core and I/O Buffers) and PSRAM chips. It must be connected to the system ground.

Note: Each Flash memory device in a system should have their supply voltage (V_{DDF}) and the program supply voltage V_{PPF} decoupled with a 0.1µF ceramic capacitor close to the pin (high frequency, inherently low inductance capacitors should be as close as possible to the package). See Figure 6., AC Measurement Load Circuit. The PCB track widths should be sufficient to carry the required V_{PPF} program and erase currents.

FUNCTIONAL DESCRIPTION

The PSRAM and Flash memory components have separate power supplies but share the same grounds. They are distinguished by three Chip Enable inputs: $\overline{E}_{F1}$ and $\overline{E}_{F2}$ for Flash 1 and Flash 2, respectively, and $\overline{E}_P$ for the PSRAM.

Recommended operating conditions do not allow more than one device to be active at a time. The most common example is simultaneous read operations on one of the Flash memories and the PSRAM which would result in a data bus contention. Therefore it is recommended to put the other devices in the high impedance state when reading the selected device.

Figure 4. Functional Block Diagram

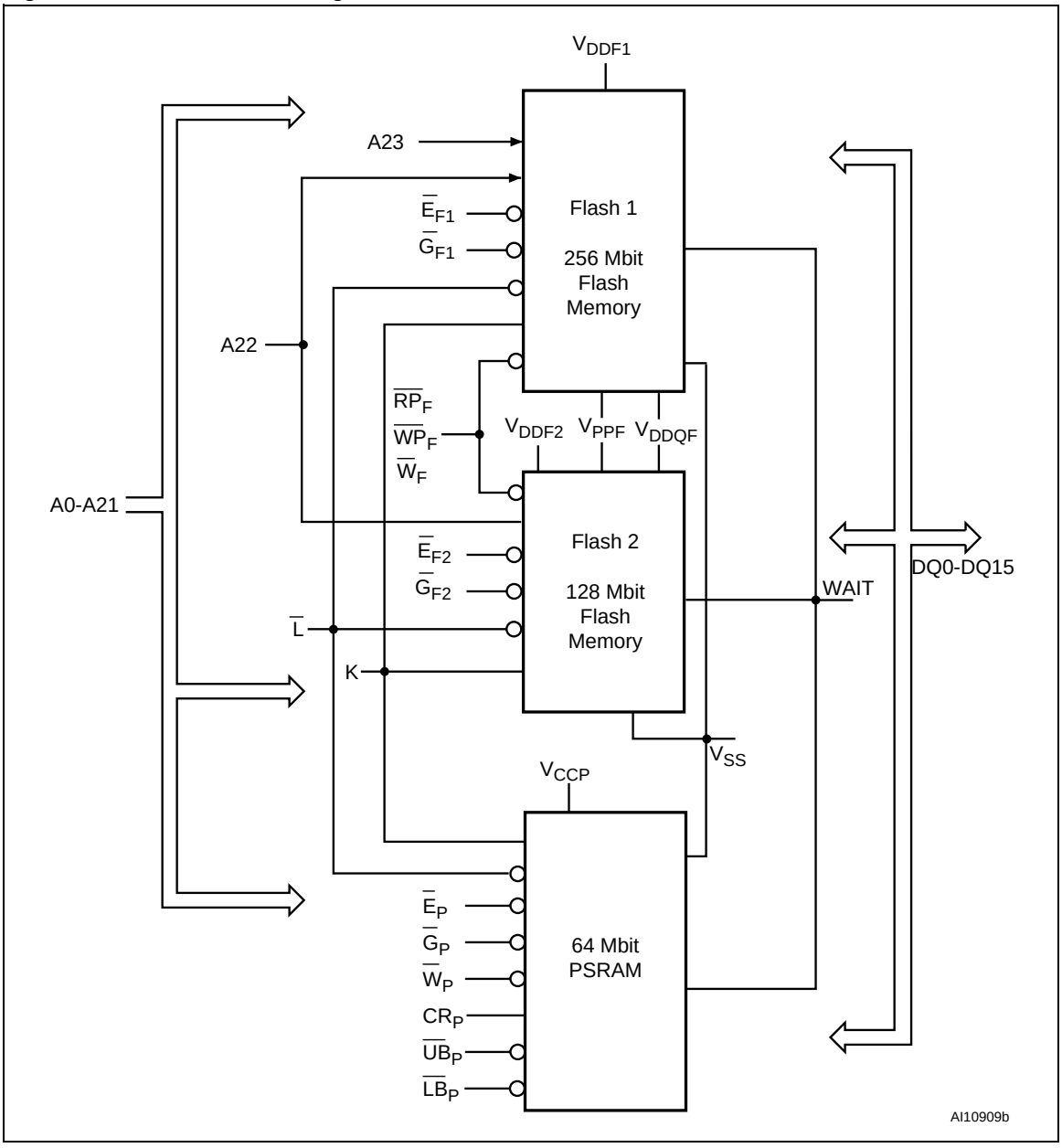


Table 2. Main Operating Modes

Operation	$\overline{E}_F$(5)	$\overline{G}_F$(5)	$\overline{W}_F$	$\overline{L}_F$	$\overline{RP}_F$	WAIT$_F$(4)	$\overline{E}_P$	CR$_P$	$\overline{G}_P$	$\overline{W}_P$	$\overline{LB}_P$,$\overline{UB}_P$	DQ15-DQ0
Flash Read	V_{IL}	V_{IL}	V_{IH}	V_{IL}(2)	V_{IH}		PSRAM must be disabled. Only one Flash memory can be enabled at a time.					Flash Data Out
Flash Write	V_{IL}	V_{IH}	V_{IL}	V_{IL}(2)	V_{IH}							Flash Data In
Flash Address Latch	V_{IL}	X	V_{IH}	V_{IL}	V_{IH}							Flash Data Out or Hi-Z (3)
Flash Output Disable	V_{IL}	V_{IH}	V_{IH}	X	V_{IH}		Any PSRAM mode is allowed. Both Flash memories must be disabled.					Hi-Z
Flash Standby	V_{IH}	X	X	X	V_{IH}	Hi-Z						Hi-Z
Flash Reset	X	X	X	X	V_{IL}	Hi-Z						Hi-Z
PSRAM Read	Both Flash memories must be disabled						V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	PSRAM data out
PSRAM Write							V_{IL}	V_{IL}	X	V_{IL}	V_{IL}	PSRAM data in
PSRAM Write Configuration Register							V_{IL}	V_{IH}	V_{IH}	V_{IL}	X	PSRAM data in
PSRAM Standby	Any Flash memory mode is allowed. Only one Flash memory can be enabled at a time						V_{IH}	V_{IL}	X	X	X	Hi-Z
PSRAM Deep Power-Down							V_{IH}	X	X	X	X	Hi-Z

Note: 1. X = Don't care.
2. $\overline{L}_F$ can be tied to V_{IH} if the valid address has been previously latched.
3. Depends on $\overline{G}_F$.
4. WAIT signal polarity is configured using the Set Configuration Register command. See the M30L0R8000(T/B)0 and M30L0R8000(T/B)0 datasheets for details.
5. $\overline{E}_F$ is either $\overline{E}_{F1}$ or $\overline{E}_{F2}$, and $\overline{G}_F$ is either $\overline{G}_{F1}$ or $\overline{G}_{F2}$ according to the Flash memory enabled. Only one Flash memory can be enabled at a time.

MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_A	Ambient Operating Temperature	–25	85	°C
T_{BIAS}	Temperature Under Bias	–25	85	°C
T_{STG}	Storage Temperature	–65	125	°C
T_{LEAD}	Lead Temperature During Soldering		(1)	°C
V_{IO}	Input or Output Voltage	–0.5	3.6	V
V_{DDF1}, V_{DDF2}, V_{DDQF}, V_{CCP}	Core and Input/Output Supply Voltages	–0.2	2.45	V
V_{PPF}	Flash Program Voltage	–0.2	12.6	V
I_O	Output Short Circuit Current		100	mA
t_{VPPFH}	Time for V_{PPF} at V_{PPFH}		100	hours

Note: 1. Compliant with the JEDEC Std J-STD-020B (for small body, Sn-Pb or Pb assembly), the ST ECOPACK ® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.

DC AND AC PARAMETERS

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in Table 4., Operating and AC Measurement Conditions. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 4. Operating and AC Measurement Conditions

Parameter	Flash Memories		PSRAM		Unit
	Min	Max	Min	Max	
V_{DDF1}/V_{DDF2} Supply Voltages	1.7	1.95	–	–	V
V_{CCP} Supply Voltage	–	–	1.7	1.95	V
V_{DDQF} Supply Voltage	1.7	1.95	–	–	V
V_{PPF} Supply Voltage (Factory environment)	8.5	9.5	–	–	V
V_{PPF} Supply Voltage (Application environment)	–0.4	V_{DDQF} +0.4	–	–	V
Ambient Operating Temperature	–25	85	–25	85	°C
Load Capacitance (C_L)	30		30		pF
Output Circuit Resistors (R_1, R_2)	16.7		16.7		kΩ
Input Rise and Fall Times		5			ns
Input Pulse Voltages	0 to V_{DDQF}		0 to V_{DDQF}		V
Input and Output Timing Ref. Voltages	V_{DDQF}/2		V_{DDQF}/2		V

Figure 5. AC Measurement I/O Waveform

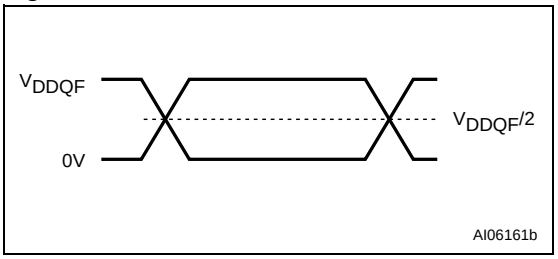


Figure 6. AC Measurement Load Circuit

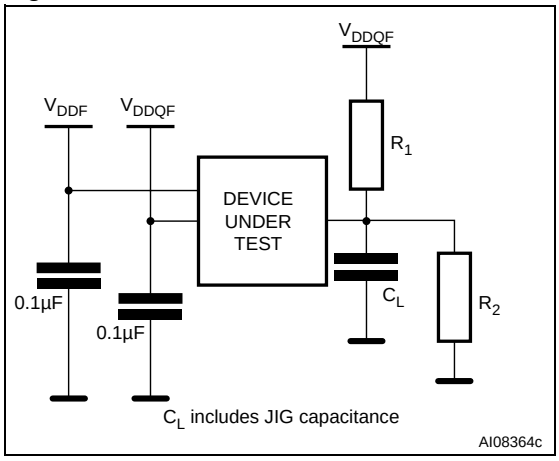


Table 5. Device Capacitance

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		14	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		18	pF

Note: Sampled only, not 100% tested.

Table 6. Flash 1 DC Characteristics - Currents

Symbol	Parameter	Test Condition	Typ	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{DDQF}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{DDQF}$		±1	µA
I_{DD1}	Supply Current Asynchronous Read (f=5MHz)	$\overline{E}_{F1} = V_{IL}$, $\overline{G}_{F1} = V_{IH}$	13	15	mA
	Supply Current Synchronous Read (f=54MHz)	4 Word	16	18	mA
		8 Word	18	20	mA
		16 Word	23	25	mA
		Continuous	25	27	mA
I_{DD2}	Supply Current (Reset)	$\overline{RP}_F = V_{SS} \pm 0.2V$	50	110	µA
I_{DD3}	Supply Current (Standby)	$\overline{E}_{F1} = V_{DDF1} \pm 0.2V$	50	110	µA
I_{DD4}	Supply Current (Automatic Standby)	$\overline{E}_{F1} = V_{IL}$, $\overline{G}_{F1} = V_{IH}$	50	110	µA
I_{DD5} (1)	Supply Current (Program)	$V_{PPF} = V_{PPH}$	8	20	mA
		$V_{PPF} = V_{DDF1}$	10	25	mA
	Supply Current (Erase)	$V_{PPF} = V_{PPH}$	8	20	mA
		$V_{PPF} = V_{DDF1}$	10	25	mA
I_{DD6} (1,2)	Supply Current (Dual Operations)	Program/Erase in one Bank, Asynchronous Read in another Bank	23	40	mA
		Program/Erase in one Bank, Synchronous Read (Continuous f=54MHz) in another Bank	35	52	mA
I_{DD7}(1)	Supply Current Program/ Erase Suspended (Standby)	$\overline{E}_{F1} = V_{DDF1} \pm 0.2V$	50	110	µA
I_{PP1}(1)	V_{PPF} Supply Current (Program)	$V_{PPF} = V_{PPH}$	2	5	mA
		$V_{PPF} = V_{DDF1}$	0.2	5	µA
	V_{PPF} Supply Current (Erase)	$V_{PPF} = V_{PPH}$	2	5	mA
		$V_{PPF} = V_{DDF1}$	0.2	5	µA
I_{PP2}	V_{PPF} Supply Current (Read)	$V_{PPF} \le V_{DDF1}$	0.2	5	µA
I_{PP3}(1)	V_{PPF} Supply Current (Standby)	$V_{PPF} \le V_{DDF1}$	0.2	5	µA

Note: 1. Sampled only, not 100% tested.
2. V_{DDF1} Dual Operation current is the sum of read and program or erase currents.

Table 7. Flash 2 DC Characteristics - Currents

Symbol	Parameter	Test Condition	Typ	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{DDQF}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{DDQF}$		±1	µA
I_{DD1}	Supply Current Asynchronous Read (f=5MHz)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$	13	15	mA
	Supply Current Synchronous Read (f=54MHz)	4 Word	16	18	mA
		8 Word	18	20	mA
		16 Word	23	25	mA
		Continuous	25	27	mA
I_{DD2}	Supply Current (Reset)	$\overline{RP} = V_{SS} \pm 0.2V$	25	70	µA
I_{DD3}	Supply Current (Standby)	$\overline{E} = V_{DDQF} \pm 0.2V$ K=V_{SS}	25	70	µA
I_{DD4}	Supply Current (Automatic Standby)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$	25	70	µA
I_{DD5} (1)	Supply Current (Program)	$V_{PP} = V_{PPH}$	8	20	mA
		$V_{PP} = V_{DD}$	10	25	mA
	Supply Current (Erase)	$V_{PP} = V_{PPH}$	8	20	mA
		$V_{PP} = V_{DD}$	10	25	mA
I_{DD6} (1,2)	Supply Current (Dual Operations)	Program/Erase in one Bank, Asynchronous Read in another Bank	23	40	mA
		Program/Erase in one Bank, Synchronous Read (Continuous f=54MHz) in another Bank	35	52	mA
I_{DD7}(1)	Supply Current Program/ Erase Suspended (Standby)	$\overline{E} = V_{DDQF} \pm 0.2V$ K=V_{SS}	25	70	µA
I_{PP1}(1)	V_{PP} Supply Current (Program)	$V_{PP} = V_{PPH}$	2	5	mA
		$V_{PP} = V_{DD}$	0.2	5	µA
	V_{PP} Supply Current (Erase)	$V_{PP} = V_{PPH}$	2	5	mA
		$V_{PP} = V_{DD}$	0.2	5	µA
I_{PP2}	V_{PP} Supply Current (Read)	$V_{PP} \le V_{DD}$	0.2	5	µA
I_{PP3}(1)	V_{PP} Supply Current (Standby)	$V_{PP} \le V_{DD}$	0.2	5	µA

Note: 1. Sampled only, not 100% tested.
2. V_{DDF2} Dual Operation current is the sum of read and program or erase currents.

Table 8. Flash 1 and Flash 2 DC Characteristics - Voltages

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage		0		0.4	V
V_{IH}	Input High Voltage		V_{DDQF} – 0.4		V_{DDQF} + 0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 100µA			0.1	V
V_{OH}	Output High Voltage	I_{OH} = –100µA	V_{DDQF} – 0.1			V
V_{PP1}	V_{PPF} Program Voltage-Logic	Program, Erase	1.1	1.8	3.3	V
V_{PPH}	V_{PPF} Program Voltage Factory	Program, Erase	8.5	9.0	9.5	V
V_{PPLK}	Program or Erase Lockout				0.4	V
V_{LKO}	$V_{DDF1/F2}$ Lock Voltage				1	V
V_{RPH}	$\overline{RP}_F$ pin Extended High Voltage				3.3	V

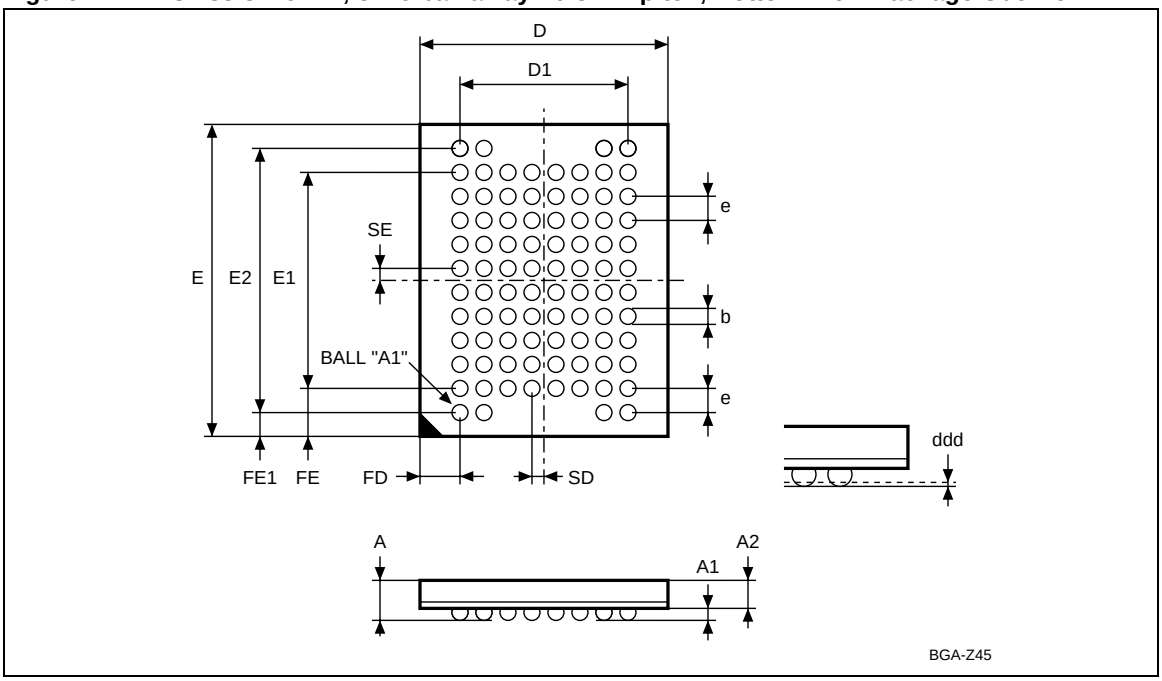
Table 9. PSRAM DC Characteristics

Symbol	Parameter	Test Condition		Min.	Typ	Max.	Unit
I_{CC1} (1)	Operating Current: Asynchronous Random Read/Write	V_{CC}=V_{IH} or V_{IL}, $\overline{E}$ = V_{IL}, I_{OUT} = 0mA	70ns			25	mA
I_{CC1P} (1)	Operating Current: Asynchronous Page Read		70ns			15	mA
I_{CC2} (1)	Operating Current: Initial Access, Burst Read/Write		80MHz			35	mA
			66MHz			30	mA
I_{CC3R}(1)	Operating Current: Continuous Burst Read		80MHz			18	mA
			66MHz			15	mA
I_{CC3W}(1)	Operating Current: Continuous Burst Write		80MHz			35	mA
			66MHz			30	mA
I_{SB}(2)	V_{CC} Standby Current	V_{CC} = V_{CCQ} or 0V, $\overline{E}$ = V_{IH}				120	µA
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}				1	µA
I_{LO}	Output Leakage Current	$\overline{G}$ = V_{IH} or $\overline{E}$ = V_{IH}				1	µA
I_{ZZ}	Deep-Power Down Current	V_{IN} = V_{IH} or V_{IL}			10		µA
V_{IH}	Input High Voltage			1.4		V_{CCQ} + 0.2	V
V_{IL}	Input Low Voltage			–0.2		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –0.2mA		0.8V_{CCQ}			V
V_{OL}	Output Low Voltage	I_{OL} = 0.2mA				0.2V_{CCQ}	V

Note: 1. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add the current required to drive the output capacitance expected in the actual system.
2. I_{SB}(Max) values are measured with RCR2 to RCR0 bits set to '000' (full array refresh) and RCR6 to RCR5 bits set to '11' (temperature compensated refresh threshold at +85°C). In order to achieve low standby current, all inputs must be driven either to V_{CCQ} or V_{SS}.
3. The Operating Temperature is +25°C.

PACKAGE MECHANICAL

Figure 7. LFBGA88 8x10mm, 8x10 ball array - 0.8mm pitch, Bottom View Package Outline



Note: Drawing is not to scale.

Table 10. Stacked LFBGA88 8x10mm - 8x10 active ball array, 0.8mm pitch, Package Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.400			0.0551
A1		0.200			0.0079	
A2	1.000			0.0394		
b	0.350	0.300	0.400	0.0138	0.0118	0.0157
D	8.000	7.900	8.100	0.3150	0.3110	0.3189
D1	5.600	–	–	0.2205	–	–
ddd			0.100			0.0039
E	10.000	9.900	10.100	0.3937	0.3898	0.3976
E1	7.200	–	–	0.2835	–	–
E2	8.800	–	–	0.3465	–	–
e	0.800	–	–	0.0315	–	–
FD	1.200	–	–	0.0472	–	–
FE	1.400	–	–	0.0551	–	–
SD	0.400	–	–	0.0157	–	–
SE	0.400	–	–	0.0157	–	–
FE1	0.600	–	–	0.0236	–	–

PART NUMBERING

Table 11. Ordering Information Scheme

Example: M36 L L R 8 7 6 0 T 1 ZAQ T

Device Type
M36 = Multi-Chip Package (Multiple Flash + RAM)

Flash 1 Architecture
L = Multi-Level, Multiple Bank, Burst mode

Flash 2 Architecture
L = Multi-Level, Multiple Bank, Burst mode

Operating Voltage
R = V_{DDF} = V_{CCP} = V_{DDQF} = 1.7 to 1.95V

Flash 1 Density
8 = 256 Mbits

Flash 2 Density
7 = 128 Mbits

RAM 1 Density
6 = 64 Mbits

RAM 0 Density
0 = No Die

Parameter Blocks Location
T = Top Boot Block Flash
B = Bottom Boot Block Flash
D = Mixed (Flash 1 Bottom, Flash 2 Top)
M = Mixed (Flash 1 Top, Flash 2 Bottom)

Product Version
1 = 0.13µm Flash technology (2 Chip Enable inputs, one for each Flash memory), 85ns speed; 0.11µm PSRAM, 70ns speed, burst mode

Package
ZAQ = Stacked LFBGA88 8x10mm - 8x10 active ball array, 0.8mm pitch

Option
Blank = Standard Packing
T = Tape & Reel Packing
E = Lead-free and RoHS Standard packing
F = Lead-free and RoHS Tape & Reel packing

Devices are shipped from the factory with the memory content bits erased to '1'. For a list of available options (Speed, Package, etc.) or for further information on any aspect of this device, please contact the ST-Microelectronics Sales Office nearest to you.

REVISION HISTORY

Table 12. Document Revision History

Date	Version	Revision Details
29-Apr-2004	0.1	First Issue
01-Feb-2005	0.2	Part Number M69KB096A changed to M69KB096AA throughout document.
13-July-2005	0.3	V_{DDQ} changed to V_{DDQF} throughout the document. Table 6., Table 7., Table 8. and Table 9. modified.