MAAPSM0008

1-Watt Power Amplifier
5 - 6 GHz

V 1.1

MAAPSM0008

Features

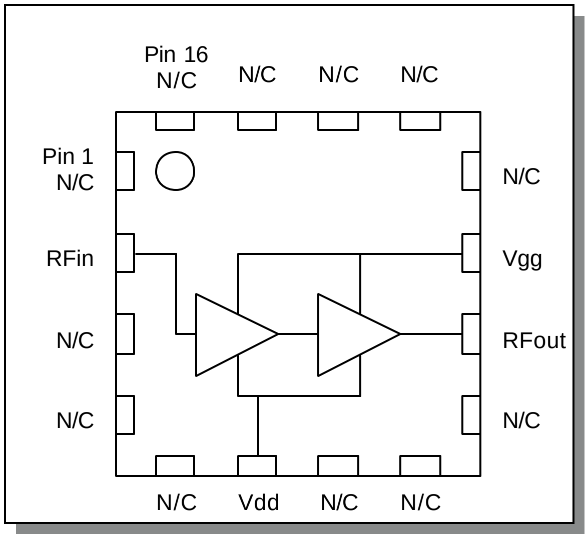
- U-NII and Hiperlan Applications
- Saturated Output Power 30.5 dBm at +7.0 V
- Power Added Efficiency 40 Percent
- No External RF Matching
- 4-mm FQFP-N, 16-Lead Package

Description

The MAAPSM0008 is a two-stage power amplifier mounted in a standard outline, 16-lead, 4-mm FQFP-N plastic package, designed specifically for the U-NII, MMAC, and Hiperlan bands. The MAAPSM0008 has fully matched 50 ohms input and output, eliminating the need for external RF tuning components.

M/A-COM fabricates the MAAPSM0008 using a self-aligned gate MESFET process to realize high power efficiency and small size. The process features full passivation for performance and reliability.

Functional Schematic



Pin Configuration

Pin	Function	Descriptions
1, 3, 4 ,5 ,7, 8, 9, 12, 13, 14, 15, 16	NC	No connection
2	RF_{IN}	RF input to the amplifier. DC block on-chip. 50 ohm input.
6	V_{dd}	Positive voltage supply to both stages
10	RF_{OUT}	RF output of the amplifier. DC block on-chip. 50 Ohm output.
11	V_{gg}	Negative voltage supply to the gates of both stages
Pad	GND	RF & DC ground

Ordering Information

Part Number	Package
MAAPSM0008TR	MAAPSM0008 on 7-inch, 1000-piece reel
MAAPSM0008TR-3000	MAAPSM0008 on 13 inch, 3000-piece reel
MAAPSM0008SMB	MAAPSM0008 Sample Test Board

Specifications subject to change without notice.

- **North America:** Tel. (800) 366-2266, Fax (800) 618-8883
- **Asia/Pacific:** Tel.+81-44-844-8296, Fax +81-44-844-8298
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Visit www.macom.com for additional data sheets and product information.

Electrical Specifications: T_C = 40 °C, V_{DD} = 7.0 V, I_{DQ} = 360 mA
(unless otherwise specified)

Parameter	Test Conditions	Units	Min.	Typ.	Max.	Typ. @ V_{DD} + 5 V
Frequency		GHz	5.0		6.0	
Input VSWR	F = 5.825 GHz, Pin = +14 dBm			1.5:1	2.0:1	1.5:1
Gain	F = 5.825 GHz, Pin = 0 dBm	dB	18.0	19.5		19.0
P1dB	F = 5.825 GHz	dBm		29.5		28.0
Saturated Power	F = 5.825 GHz, Pin = +14 dBm	dBm	29.5	30.5		29.0
Drain Current at Psat	F = 5.825 GHz, Pin = +14 dBm	mA		500	600	500
Harmonics 2f 3f	Output Power = 30.5 dBm	dBc dBc		-40 -70		-40 -70
Thermal resistance		°C/W		31		31
Third-Order Intercept Point		dBm		40		38
Stability	+3.0 V < V_{DD} < +10.0 V, P_{OUT} < +15 dBm, VSWR < 6:1, -25 ºC < T_C < 70 ºC, RBW = 3 MHz max. hold		All spurs < -70 dBc			

Recommended Operating Conditions [1]

Characteristic	Symbol	Unit	Min	Typ	Max
Drain Voltage	V_{DD}	V	4.5	7.0	8.0
Gate Voltage [2]	V_{GG}	V	-2.5	-2.0	-1.0
Input Power	P_{IN}	dBm		—	15
Gate Current	I_{GG}	mA	-4	1	+4
Case Temperature	T_C	°C	-40	25	70

1. Operation outside of these ranges may reduce product reliability.
2. A 100 E-Series resistor should be used in the gate voltage line.

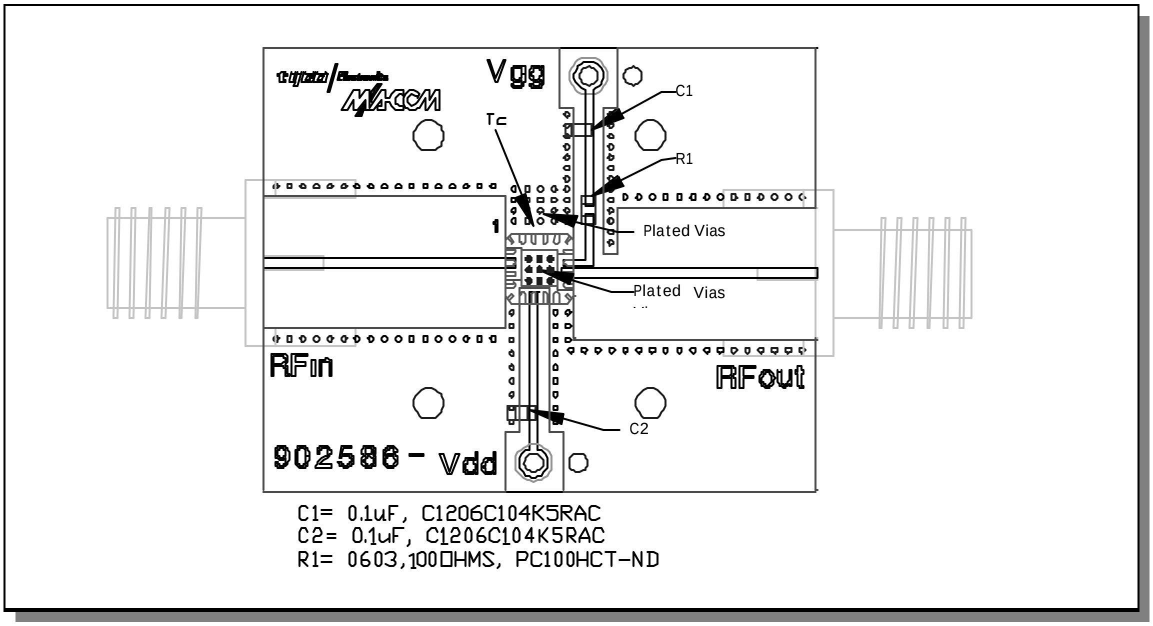
Operating The MAAPSM0008

The MAAPSM0008 is static sensitive. Please handle with care. To operate the device, follow these steps.

1. Apply V_{GG} = -2 V, V_{DD}= 0 V.
2. Ramp V_{DD} to desired voltage, typically 5 to 7 V.
3. Adjust V_{GG} to set I_{DQ}, (approximately –2 V).
4. Set RF input.
5. Power down sequence in reverse. Turn gate voltage off last.

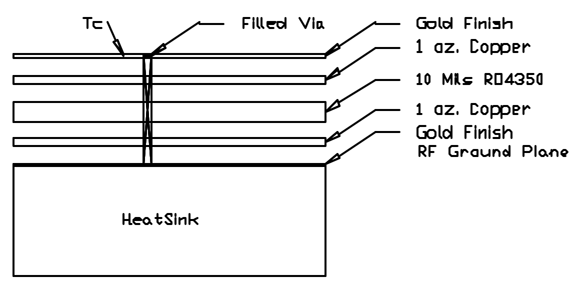
Application Information

Sample Board



Notes on board design

1. Sample board uses RO4350 e_r = 3.48 as dielectric for circuit board. Dielectric thickness is not critical but RFin and RFout transmission lines should be 50 ohms (w = 22 mil for thickness = 10 mil).
2. Solder the exposed paddle on the back of the package to the board. Proper attachment of the exposed paddle is essential for RF and DC ground in addition to providing a low thermal resistance.
3. Case temperature (Tc) is measured as shown on the application board drawing on the top circuit board metal as close to the body of the package as possible.
4. The board must provide adequate heat sinking to accommodate the 2.5 W typically dissipated under small signal conditions. Sample board uses vias in the vicinity of the ground pad to provide a suitable heat sink connected to the ground plane of the board as shown above (recommend $theta_{CA}$ = 5 °C/W max).
5. Placement of C1, C2 and R1 are not critical but use of 1206 for the bypass caps (C1 and C2) is critical.



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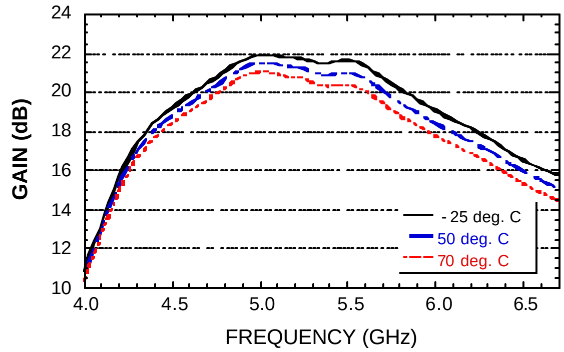
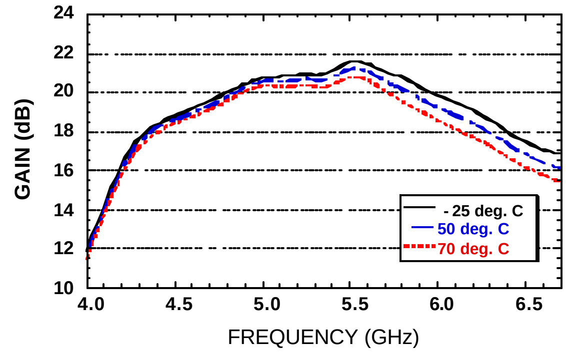
Typical Performance Curves

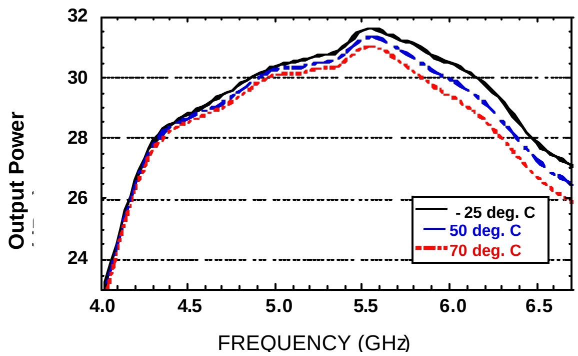
Gain Vs. Frequency
P_{IN} = + 6 dBm, V_{DD} = 7 V



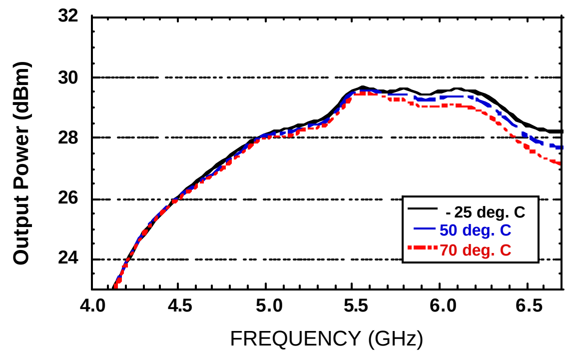
Gain Vs. Frequency
P_{IN} = + 6 dBm, V_{DD} = 5 V



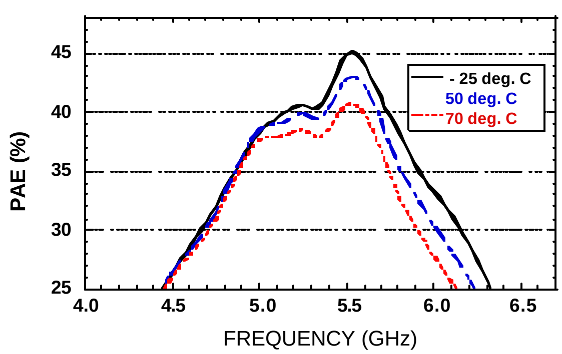
Output Power Vs. Frequency
P_{IN} = + 12 dBm, V_{DD} = 7 V



Output Power Vs. Frequency
P_{IN} = + 12 dBm, V_{DD} = 5 V



PAE Vs. Frequency
P_{IN} = + 12 dBm, V_{DD} = 7 V



PAE Vs. Frequency
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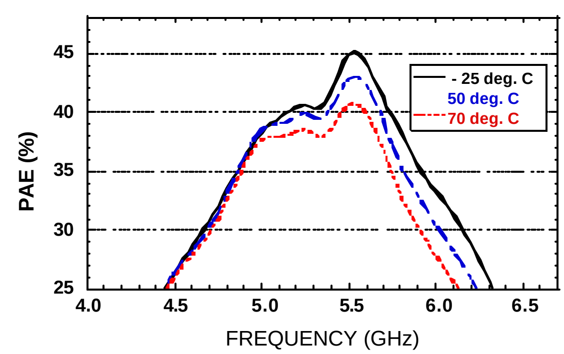

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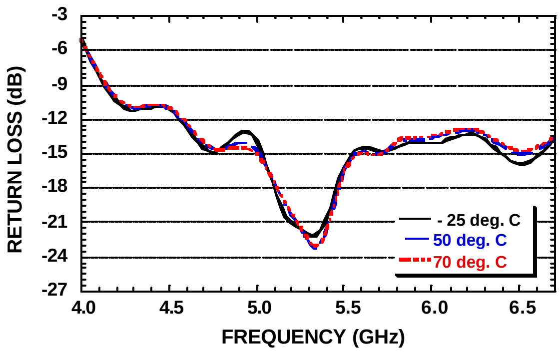
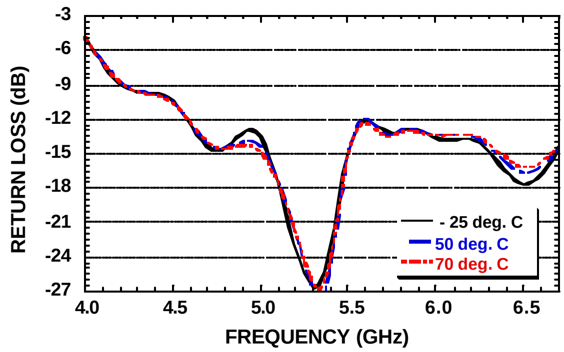
Typical Performance Curves

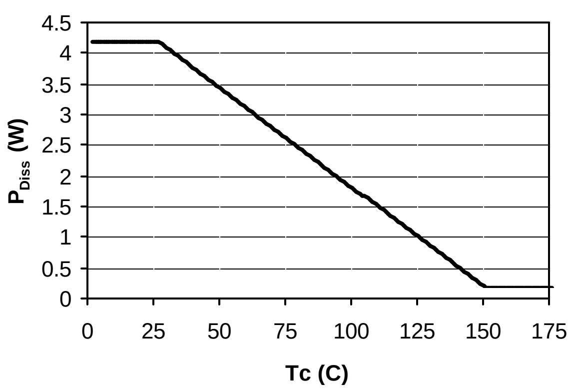
Input Return Loss Vs. Frequency
P_{IN} = + 12 dBm, V_{DD} = 7 V



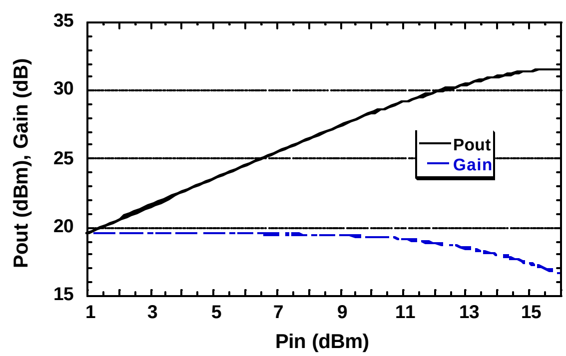
Input Return Loss Vs. Frequency
P_{IN} = + 12 dBm, V_{DD} = 5 V



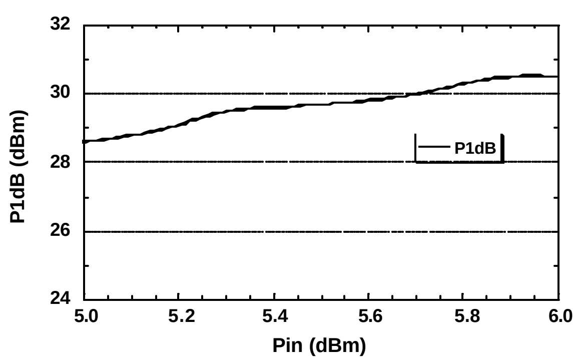
Dissipated Power vs. Case Temperature



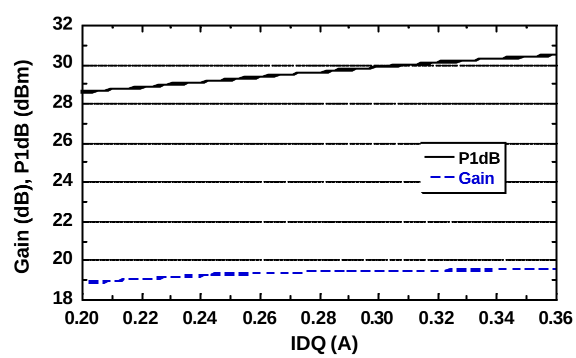
Output Power & Gain Vs. Input Power
Freq = 5.80 GHz, V_{DD} = 7 V



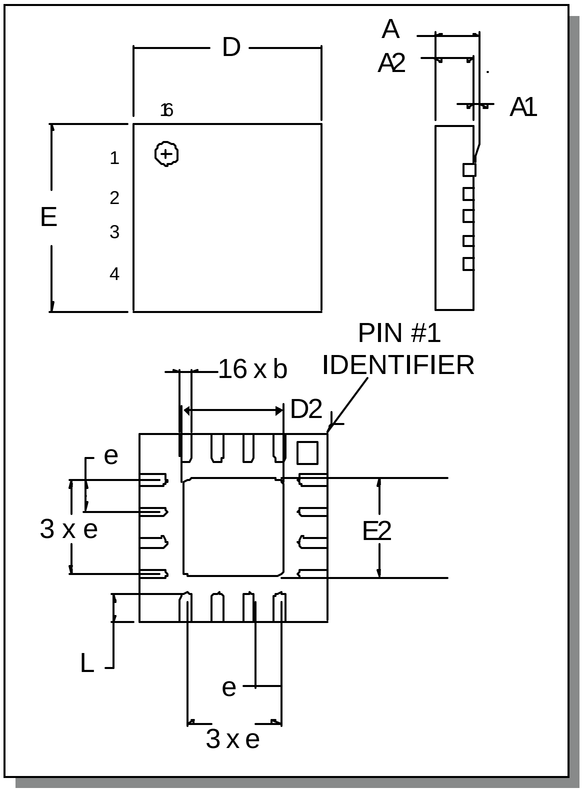
1-dB Compression Vs. Frequency
V_{DD} = 7 V, I_{Dq} = 0.360 A



P1dB, Gain Vs. Quiescent Bias
V_{DD} = 7 V, Freq = 5.8 GHz



4-mm FQFP-N, 16-Lead (MLP) Package, Saw Singulated



Dim	Measurement (mm)		
	Min.	Nom.	Max.
A	0.80	0.90	1.00
A1	0	0.02	0.05
A2	0.80	0.88	1.00
b	0.23	0.30	0.38
D	-	4.00 basic	-
D2	2.05	2.15	2.25
e		0.65 basic	
E	-	4.00 basic	-
E2	2.05	2.15	2.25
L	0.45 typ.	0.55 typ.	0.65 typ.

Note: See JEDEC MO-220A VGGC Issue B for additional dimensional and tolerance information.

Handling Procedures

Please observe the following precautions to avoid damage to the MAAPSM0008:

Static Sensitivity

Gallium arsenide integrated circuits are ESD sensitive and can be damaged by static electricity. Use proper ESD precautions when handling these devices.

Absolute Maximum Ratings[1]

Parameter	Absolute Maximum
Max Input Power (5 - 6 GHz)	+ 15 dBm
Operating Voltages	+10 volts
Operating Temperature	-40 °C to +70 °C
Channel Temperature	+150 °C
Storage Temperature	-40 °C to +150 °C

1. Exceeding any one or combination of these limits may cause permanent damage.