# M36L0T7050T0
# M36L0T7050B0

## 128Mbit (Multiple Bank, Multi-Level, Burst) Flash Memory
## 32Mbit (2M x16) PSRAM, Multi-Chip Package

## FEATURES SUMMARY

■ MULTI-CHIP PACKAGE
   – 1 die of 128Mbit (8Mx16, Multiple Bank, Multi-level, Burst) Flash Memory
   – 1 die of 32Mbit (2Mx16) Pseudo SRAM

■ SUPPLY VOLTAGE
   – $V_{DDF}$ = 1.7 to 2V
   – $V_{DDP}$ = $V_{DDQ}$ = 2.7 to 3.3V
   – $V_{PP}$ = 9V for fast program (12V tolerant)

■ ELECTRONIC SIGNATURE
   – Manufacturer Code: 20h
   – Device Code (Top Flash Configuration) M36L0T7050T0: 88C4h
   – Device Code (Bottom Flash Configuration) M36L0T7050B0: 88C5h

■ PACKAGE
   – Compliant with Lead-Free Soldering Processes
   – Lead-Free Versions

### FLASH MEMORY

■ SYNCHRONOUS / ASYNCHRONOUS READ
   – Synchronous Burst Read mode: 50MHz
   – Asynchronous Page Read mode
   – Random Access: 90ns

■ SYNCHRONOUS BURST READ SUSPEND

■ PROGRAMMING TIME
   – 10µs typical Word program time using Write to Buffer and Program

■ MEMORY ORGANIZATION
   – Multiple Bank Memory Array: 8 Mbit Banks
   – Parameter Blocks (Top or Bottom location)

■ DUAL OPERATIONS
   – program/erase in one Bank while read in others
   – No delay between read and write operations

■ SECURITY
   – 64 bit unique device number
   – 2112 bit user programmable OTP Cells

### Figure 1. Package



TFBGA88 (ZAQ)
8 x 10mm
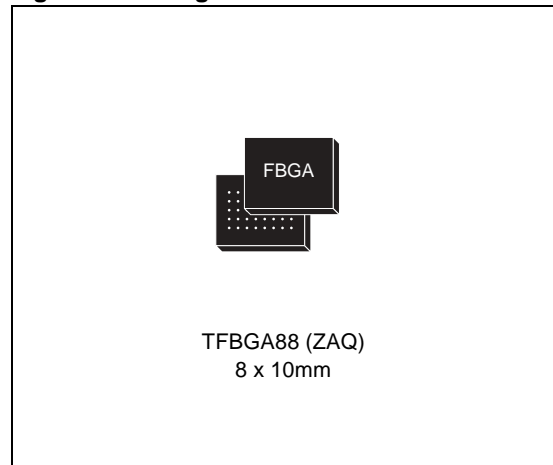
■ BLOCK LOCKING
   – All blocks locked at power-up
   – Any combination of blocks can be locked with zero latency
   – $\overline{WP}$ for Block Lock-Down
   – Absolute Write Protection with $V_{PP} = V_{SS}$

■ COMMON FLASH INTERFACE (CFI)

■ 100,000 PROGRAM/ERASE CYCLES per BLOCK

### PSRAM

■ ACCESS TIME: 70ns

■ LOW STANDBY CURRENT: 100µA

■ DEEP POWER-DOWN CURRENT: 10µA

■ BYTE CONTROL: $\overline{UB_P}/\overline{LB_P}$

■ PROGRAMMABLE PARTIAL ARRAY

■ 8 WORD PAGE ACCESS CAPABILITY: 18ns

■ POWER-DOWN MODES
   – Deep Power-Down
   – 4 Mbit Partial Array Refresh
   – 8 Mbit Partial Array Refresh
   – 16 Mbit Partial Array Refresh

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## SUMMARY DESCRIPTION

The M36L0T7050T0 and M36L0T7050B0 combine two memory devices in a Multi-Chip Package: a 128-Mbit, Multiple Bank Flash memory, the M30L0T7000T0 or M30L0T7000B0, and a 32-Mbit PseudoSRAM, the M69AW048B. Recommended operating conditions do not allow more than one memory to be active at the same time.

The memory is offered in a Stacked TFBGA88 (8x10mm, 8x10 ball array, 0.8mm pitch) package.

In addition to the standard version, the packages are also available in Lead-free version, in compliance with JEDEC Std J-STD-020B, the ST ECO-PACK 7191395 Specification, and the RoHS (Restriction of Hazardous Substances) directive.

All packages are compliant with Lead-free soldering processes.

The memory is supplied with all the bits erased (set to '1').

**Figure 2. Logic Diagram**



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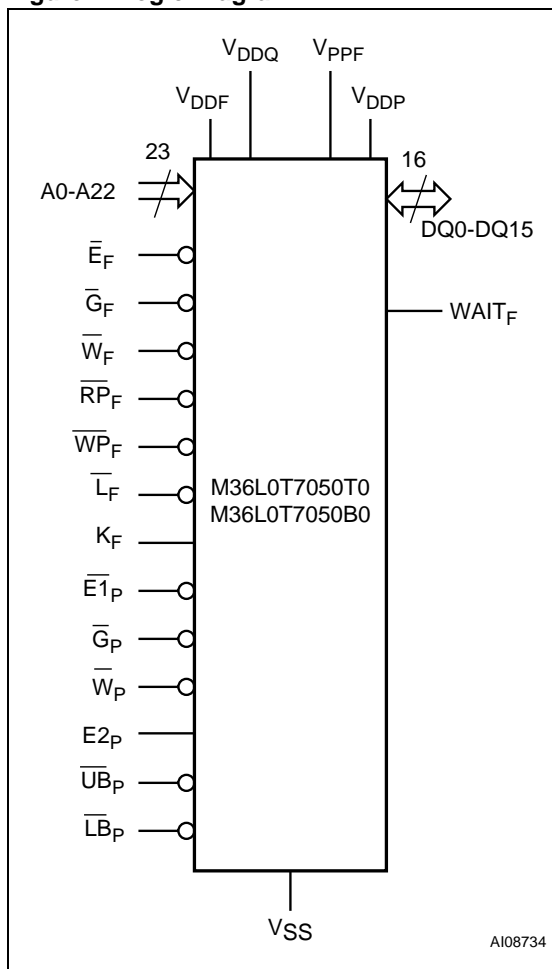
**Table 1. Signal Names**

| A0-A22 [1] | Address Inputs |
|---|---|
| DQ0-DQ15 | Common Data Input/Output |
| $V_{DDF}$ | Power Supply for Flash Memory |
| $V_{DDQ}$ | Flash Memory Power Supply for I/O Buffers |
| $V_{PPF}$ | Flash Optional Supply Voltage for Fast Program and Erase |
| $V_{SS}$ | Ground |
| $V_{DDP}$ | PSRAM Power Supply |
| NC | Not Connected Internally |
| DU | Do Not Use as Internally Connected |
| **Flash Memory Signals** | |
| $\overline{L}_F$ | Latch Enable Input |
| $\overline{E}_F$ | Chip Enable Input |
| $\overline{G}_F$ | Output Enable Input |
| $\overline{W}_F$ | Write Enable Input |
| $\overline{RP}_F$ | Reset Input |
| $\overline{WP}_F$ | Write Protect Input |
| $K_F$ | Burst Clock |
| $WAIT_F$ | Wait Data in Burst Mode |
| **PSRAM Signals** | |
| $\overline{E1}_P$ | Chip Enable Input |
| $\overline{G}_P$ | Output Enable Input |
| $\overline{W}_P$ | Write Enable Input |
| $E2_P$ | Power-down Input |
| $\overline{UB}_P$ | Upper Byte Enable Input |
| $\overline{LB}_P$ | Lower Byte Enable Input |

Note: 1. A22-A21 are not connected to the PSRAM component.

**Figure 3. TFBGA Connections (Top view through package)**

|   | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| A | DU | DU |  |  |  |  | DU | DU |
| B | A4 | A18 | A19 | $V_{SS}$ | $V_{DDF}$ | NC | A21 | A11 |
| C | A5 | $\overline{LB}_P$ | NC | $V_{SS}$ | NC | $K_F$ | A22 | A12 |
| D | A3 | A17 | NC | $V_{PPF}$ | $\overline{W}_P$ | $\overline{E}_P$ | A9 | A13 |
| E | A2 | A7 | NC | $\overline{WP}_F$ | $\overline{L}_F$ | A20 | A10 | A15 |
| F | A1 | A6 | $\overline{UB}_P$ | $\overline{RP}_F$ | $\overline{W}_F$ | A8 | A14 | A16 |
| G | A0 | DQ8 | DQ2 | DQ10 | DQ5 | DQ13 | $WAIT_F$ | NC |
| H | $\overline{G}_P$ | DQ0 | DQ1 | DQ3 | DQ12 | DQ14 | DQ7 | NC |
| J | NC | $\overline{G}_F$ | DQ9 | DQ11 | DQ4 | DQ6 | DQ15 | $V_{DDQ}$ |
| K | $\overline{E}_F$ | DU | DU | NC | $V_{DDP}$ | NC | $V_{DDQ}$ | $E2_P$ |
| L | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | $V_{DDF}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ |
| M | DU | DU |  |  |  |  | DU | DU |

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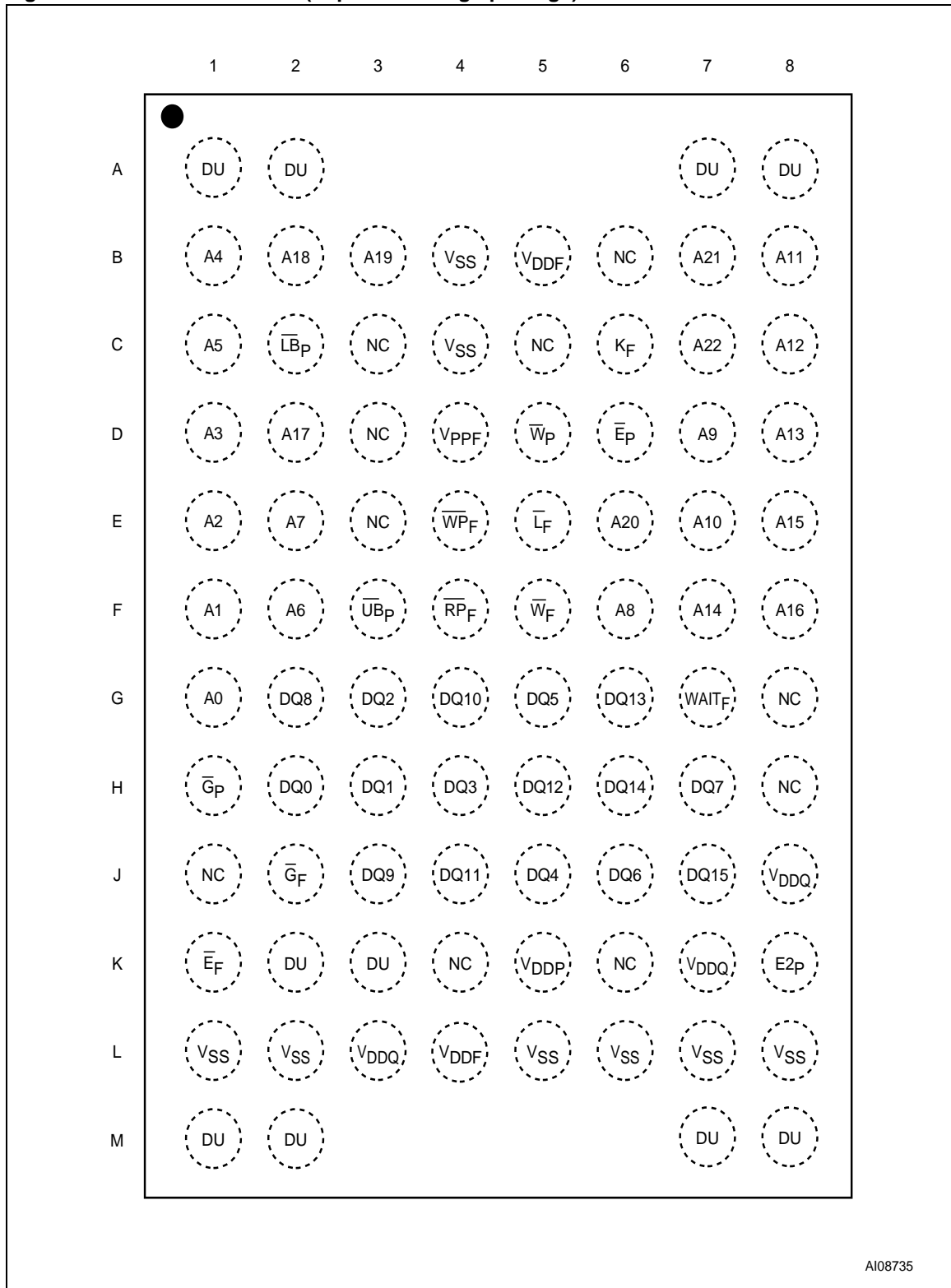
# SIGNAL DESCRIPTIONS

See Figure 2., Logic Diagram and Table 1., Signal Names, for a brief overview of the signals connected to this device.

**Address Inputs (A0-A22).** Addresses A0-A20 are common inputs for the Flash Memory and the PSRAM components. The other lines (A21-A22) are inputs for the Flash Memory component only.

The Address Inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the Command Interface of the Flash memory Program/Erase Controller or they select the cells to access in the PSRAM.

The Flash memory component is accessed through the Chip Enable signal ($\overline{E}_F$) and through the Write Enable ($\overline{W}_F$) signal, while the PSRAM is accessed through two Chip Enable signals (E1$_P$ and E2$_P$) and the Write Enable signal ($\overline{W}_P$).

**Data Input/Output (DQ0-DQ15).** In the Flash memory the Data I/O output the data stored at the selected address during a Bus Read operation or input a command or the data to be programmed during a Write Bus operation.

In the PSRAM the Upper Byte Data Inputs/Outputs, DQ8-DQ15, carry the data to or from the upper part of the selected address during a Write or Read operation, when Upper Byte Enable ($\overline{UB}_P$) is driven Low.

The Lower Byte Data Inputs/Outputs, DQ0-DQ7, carry the data to or from the lower part of the selected address during a Write or Read operation, when Lower Byte Enable ($\overline{LB}_P$) is driven Low.

**Flash Chip Enable ($\overline{E}_F$).** The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is Low, $V_{IL}$, and Reset is High, $V_{IH}$, the device is in active mode. When Chip Enable is at $V_{IH}$ the Flash memory is deselected, the outputs are high impedance and the power consumption is reduced to the standby level.

**Flash Output Enable ($\overline{G}_F$).** The Output Enable input controls data output during Flash memory Bus Read operations.

**Flash Write Enable ($\overline{W}_F$).** The Write Enable controls the Bus Write operation of the Flash memories' Command Interface. The data and address inputs are latched on the rising edge of Chip Enable or Write Enable whichever occurs first.

**Flash Write Protect ($\overline{WP}_F$).** Write Protect is an input that gives an additional hardware protection for each block. When Write Protect is Low, $V_{IL}$, Lock-Down is enabled and the protection status of the Locked-Down blocks cannot be changed. When Write Protect is at High, $V_{IH}$, Lock-Down is disabled and the Locked-Down blocks can be locked or unlocked. (See the Lock Status Table in the M30L0T7000T0 datasheet).

**Flash Reset ($\overline{RP}_F$).** The Reset input provides a hardware reset of the memory. When Reset is at $V_{IL}$, the memory is in Reset mode: the outputs are high impedance and the current consumption is reduced to the Reset Supply Current I$_{DD2}$. Refer to Table 7., Flash DC Characteristics - Currents, for the value of I$_{DD2}$. After Reset all blocks are in the Locked state and the Configuration Register is reset. When Reset is at $V_{IH}$, the device is in normal operation. Exiting Reset mode the device enters Asynchronous Read mode, but a negative transition of Chip Enable or Latch Enable is required to ensure valid data outputs.

The Reset pin can be interfaced with 3V logic without any additional circuitry. It can be tied to $V_{RPH}$ (refer to Table 8., Flash Memory DC Characteristics - Voltages).

**Flash Latch Enable ($\overline{L}_F$).** Latch Enable latches the address bits on its rising edge. The address latch is transparent when Latch Enable is Low, $V_{IL}$, and it is inhibited when Latch Enable is High, $V_{IH}$. Latch Enable can be kept Low (also at board level) when the Latch Enable function is not required or supported.

**Flash Clock (K$_F$).** The Clock input synchronizes the Flash memory to the microcontroller during synchronous read operations; the address is latched on a Clock edge (rising or falling, according to the configuration settings) when Latch Enable is at $V_{IL}$. Clock is don't care during Asynchronous Read and in write operations.

**Flash Wait (WAIT$_F$).** WAIT is a Flash output signal used during Synchronous Read to indicate whether the data on the output bus are valid. This output is high impedance when Flash Chip Enable is at $V_{IH}$ or Flash Reset is at $V_{IL}$. It can be configured to be active during the wait cycle or one clock cycle in advance. The WAIT$_F$ signal is not gated by Output Enable.

**Chip Enable ($\overline{E1}_P$).** When asserted (Low), the Chip Enable, $\overline{E1}_P$, activates the memory state machine, address buffers and decoders, allowing Read and Write operations to be performed. When de-asserted (High), all other pins are ignored, and the device is put, automatically, in low-power Standby mode.

**Chip Enable (E2$_P$).** The Chip Enable, E2$_P$, puts the device in Power-down mode (Deep Power-Down, PAR and Standby) when it is driven Low. One of these, Deep Power-Down mode, is the lowest power mode.

**Output Enable ($\overline{G}_P$).** The Output Enable, $\overline{G}_P$, provides a high speed tri-state control, allowing

fast read/write cycles to be achieved with the common I/O data bus.

**Write Enable ($\overline{W}_P$).** The Write Enable, $\overline{W}_P$, controls the Bus Write operation of the memory.

**Upper Byte Enable ($\overline{UB}_P$).** The Upper Byte Enable, UB$_P$, gates the data on the Upper Byte Data Inputs/Outputs (DQ8-DQ15) to or from the upper part of the selected address during a Write or Read operation.

**Lower Byte Enable ($\overline{LB}_P$).** The Lower Byte Enable, LB$_P$, gates the data on the Lower Byte Data Inputs/Outputs (DQ0-DQ7) to or from the lower part of the selected address during a Write or Read operation.

**V$_{DDF}$ Supply Voltage.** V$_{DDF}$ provides the power supply to the internal cores of the Flash memory component. It is the main power supply for all Flash operations (Read, Program and Erase).

**V$_{DDP}$ Supply Voltage.** The V$_{DDP}$ Supply Voltage supplies the power for all operations (Read, Write, etc.) and for driving the refresh logic, even when the device is not being accessed.

**V$_{DDQ}$ Supply Voltage.** V$_{DDQ}$ provides the power supply for the Flash Memory I/O pins. This allows all Outputs to be powered independently of the Flash Memory core power supply, V$_{DDF}$.

**V$_{PPF}$ Program Supply Voltage.** V$_{PPF}$ is both a Flash control input and a Flash power supply pin.

The two functions are selected by the voltage range applied to the pin.

If V$_{PPF}$ is kept in a low voltage range (0V to V$_{DDQ}$) V$_{PPF}$ is seen as a control input. In this case a voltage lower than V$_{PPLKF}$ gives an absolute protection against Program or Erase, while V$_{PPF}$ > V$_{PP1F}$ enables these functions (see Tables 7 and 8, DC Characteristics for the relevant values). V$_{PPF}$ is only sampled at the beginning of a Program or Erase; a change in its value after the operation has started does not have any effect and Program or Erase operations continue.

If V$_{PPF}$ is in the range of V$_{PPHF}$ it acts as a power supply pin. In this condition V$_{PPF}$ must be stable until the Program/Erase algorithm is completed.

**V$_{SS}$ Ground.** V$_{SS}$ is the common ground reference for all voltage measurements in the Flash (core and I/O Buffers) and PSRAM chips.

**Note: Each Flash memory device in a system should have their supply voltage (V$_{DDF1}$ and V$_{DDF2}$) and the program supply voltage V$_{PPF}$ decoupled with a 0.1μF ceramic capacitor close to the pin (high frequency, inherently low inductance capacitors should be as close as possible to the package). See Figure 6., AC Measurement Load Circuit. The PCB track widths should be sufficient to carry the required V$_{PPF}$ program and erase currents.**

## FUNCTIONAL DESCRIPTION

The PSRAM and Flash memory components have separate power supplies but share the same grounds. They are distinguished by three Chip Enable inputs: $\overline{E}_F$ for the Flash memory and $\overline{E1}_P$ and E2$_P$ for the PSRAM.

Recommended operating conditions do not allow more than one device to be active at a time. The most common example is simultaneous read operations in the Flash memory and the PSRAM which would result in a data bus contention. Therefore it is recommended to put the other device in the high impedance state when reading the selected device.

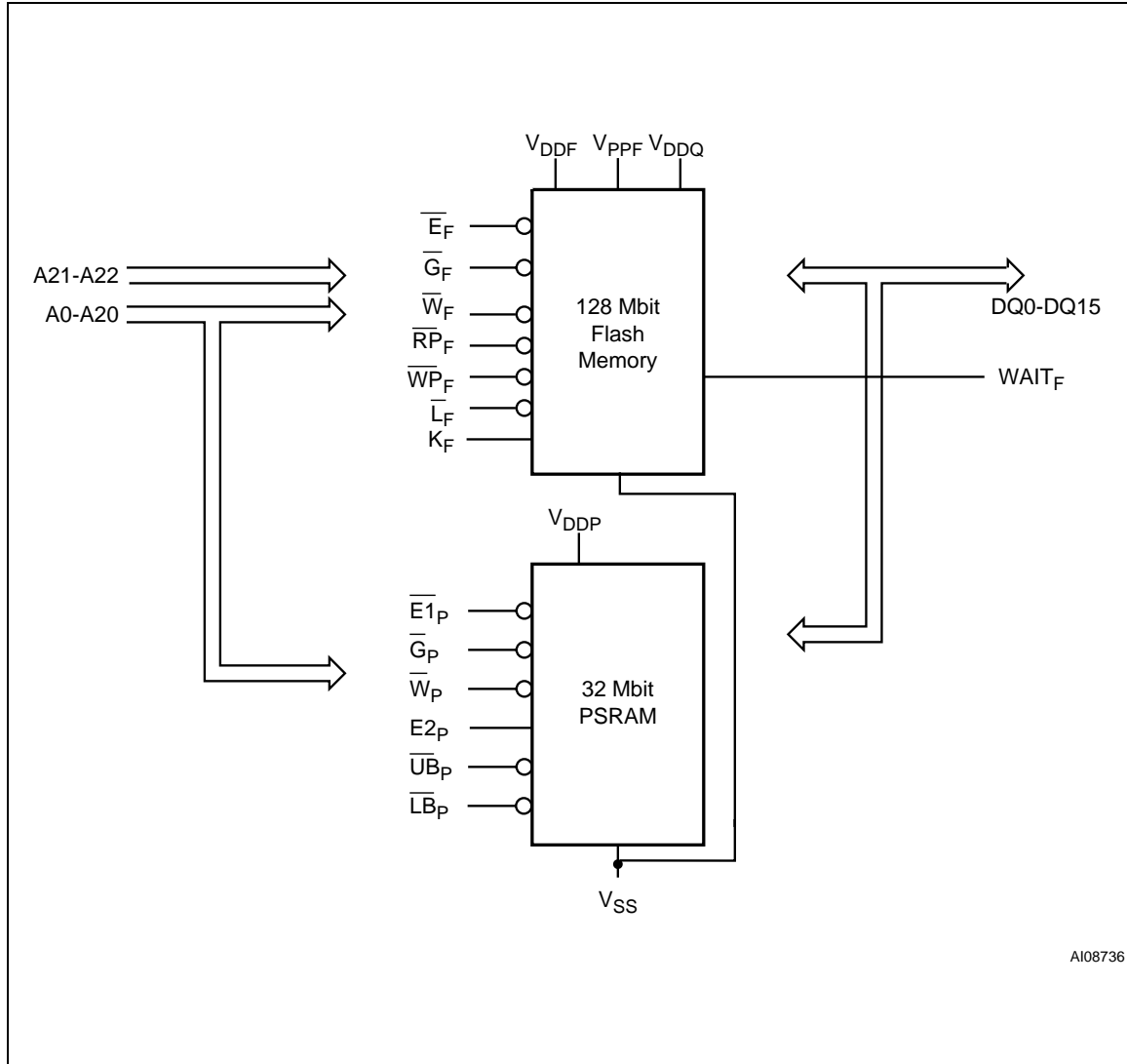**Figure 4. Functional Block Diagram**

**Table 2. Main Operating Modes**

| Operation | $\overline{E}_F$ | $\overline{G}_F$ | $\overline{W}_F$ | $\overline{L}_F$ | $\overline{RP}_F$ | WAIT$_F$[4] | E1$_P$ | $\overline{E2}_P$ | $\overline{G}_P$ | $\overline{W}_P$ | $\overline{LB}_P,\overline{UB}_P$ | DQ15-DQ0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Flash Read | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{IL}$[2] | $V_{IH}$ | | | | | | | Flash Data Out |
| Flash Write | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $V_{IL}$[2] | $V_{IH}$ | | PSRAM must be disabled | | | | | Flash Data In |
| Flash Address Latch | $V_{IL}$ | X | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | | | | | | | Flash Data Out or Hi-Z [3] |
| Flash Output Disable | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | X | $V_{IH}$ | | | | | | | Hi-Z |
| Flash Standby | $V_{IH}$ | X | X | X | $V_{IH}$ | Hi-Z | Any PSRAM mode is allowed | | | | | Hi-Z |
| Flash Reset | X | X | X | X | $V_{IL}$ | Hi-Z | | | | | | Hi-Z |
| PSRAM Read | | | | | | | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | PSRAM data out |
| PSRAM Write | Flash Memory must be disabled | | | | | | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | $V_{IL}$ | $V_{IL}$ | PSRAM data in |
| Output Disable | | | | | | | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | $V_{IH}$ | X | Hi-Z |
| PSRAM Standby | Any Flash mode is allowed | | | | | | $V_{IH}$ | $V_{IH}$ | X | X | X | Hi-Z |
| PSRAM Deep Power-Down | | | | | | | X | $V_{IL}$ | X | X | X | Hi-Z |

Note: 1. $\underline{X}$ = Don't care.
2. $\overline{L}_F$ can be tied to $V_{IH}$ if the valid address has been previously latched.
3. Depends on $\overline{G}_F$.
4. WAIT signal polarity is configured using the Set Configuration Register command. See the M30L0T7000T0 datasheet for details.

## FLASH MEMORY DEVICE

The M36L0T7050T0 and M36L0T7050B0 contain a 128 Mbit Flash memory. For detailed information on how to use the devices, see the M30L0T7000(T/B)0 datasheet which is available from your local STMicroelectronics distributor.

## PSRAM DEVICE

The M36L0T7050T0 and M36L0T7050B0 contain a 32 Mbit PSRAM. This device can be placed in a number of sleep and partial sleep modes (see Table 3.). For detailed information on how to use the device, see the M69AW048B datasheet which is available from the internet site *http://www.st.com* or from your local STMicroelectronics distributor.

**Table 3. Power-Down Configuration Data**

| Power-Down Modes | Power-Down Configuration Data | | | |
|---|---|---|---|---|
| | DQ15–DQ9 | DQ8-DQ2 | DQ1 | DQ0 |
| Deep Power-Down (default) | 0 | 0 | 1 | 1 |
| 4Mb PAR | 0 | 0 | 1 | 0 |
| 8Mb PAR | 0 | 0 | 0 | 1 |
| 16Mb PAR | 0 | 0 | 0 | 0 |

## MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not im-

plied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

**Table 4. Absolute Maximum Ratings**

| Symbol | Parameter | Value | | Unit |
|--------|-----------|-------|-----|------|
| | | Min | Max | |
| $T_A$ | Ambient Operating Temperature | −25 | 85 | °C |
| $T_{BIAS}$ | Temperature Under Bias | −25 | 85 | °C |
| $T_{STG}$ | Storage Temperature | −55 | 125 | °C |
| $T_{LEAD}$ | Lead Temperature during Soldering | | (1) | °C |
| $V_{IO}$ | Input or Output Voltage | −0.5 | 3.6 | V |
| $V_{DDF}$ | Flash Memory Core Supply Voltage | −0.2 | 2.5 | V |
| $V_{DDQ}$, $V_{DDP}$ | PSRAM and Input/Output Supply Voltages | −0.2 | 3.6 | V |
| $V_{PPF}$ | Flash Program Voltage | −0.2 | 14 | V |
| $I_O$ | Output Short Circuit Current | | 100 | mA |
| $t_{VPPFH}$ | Time for $V_{PPF}$ at $V_{PPFH}$ | | 100 | hours |

Note: 1. Compliant with the JEDEC Std J-STD-020B (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.
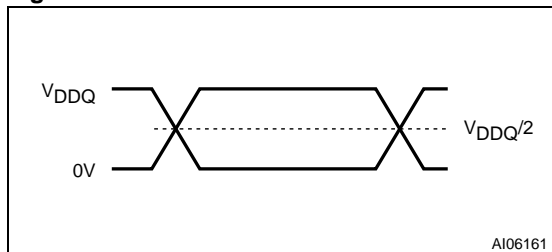
## DC AND AC PARAMETERS

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in Table 5., Operating and AC Measurement Conditions. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.
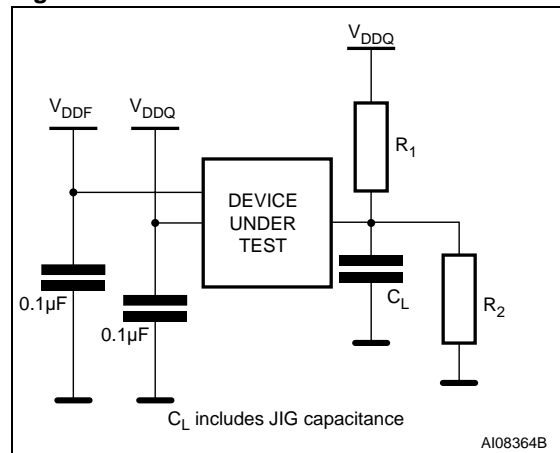
**Table 5. Operating and AC Measurement Conditions**

| Parameter | Flash Memory | | PSRAM | | Unit |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| $V_{DDF}$ Supply Voltage | 1.7 | 2.0 | – | – | V |
| $V_{DDP}$ Supply Voltage | – | – | 2.7 | 3.3 | V |
| $V_{DDQF}$ Supply Voltage | 2.7 | 3.3 | – | – | V |
| $V_{PPF}$ Supply Voltage (Factory environment) | 8.5 | 12.6 | – | – | V |
| $V_{PPF}$ Supply Voltage (Application environment) | −0.4 | $V_{DDQ}$ +0.4 | – | – | V |
| Ambient Operating Temperature | −25 | 85 | −30 | 85 | °C |
| Load Capacitance ($C_L$) | 30 | | 50 | | pF |
| Output Circuit Resistors ($R_1$, $R_2$) | 22 | | 22 | | kΩ |
| Input Rise and Fall Times | | 5 | 5 | | ns |
| Input Pulse Voltages | 0 to $V_{DDQ}$ | | 0 to $V_{DDQ}$ | | V |
| Input and Output Timing Ref. Voltages | $V_{DDQ}$/2 | | $V_{DDQ}$/2 | | V |

**Figure 5. AC Measurement I/O Waveform**



$V_{DDQ}$

0V

$V_{DDQ}$/2

AI06161

**Figure 6. AC Measurement Load Circuit**



$V_{DDQ}$

$V_{DDF}$  $V_{DDQ}$

$R_1$

DEVICE UNDER TEST

$C_L$  $R_2$

0.1µF

0.1µF

$C_L$ includes JIG capacitance

AI08364B

**Table 6. Device Capacitance**

| Symbol | Parameter | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | | 12 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | | 15 | pF |

Note: Sampled only, not 100% tested.

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**Table 7. Flash DC Characteristics - Currents**

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current | $0V \leq V_{IN} \leq V_{DDQ}$ | | | ±2 | µA |
| $I_{LO}$ | Output Leakage Current | $0V \leq V_{OUT} \leq V_{DDQ}$ | | | ±10 | µA |
| $I_{DD1}$ | Supply Current Asynchronous Read (f=6MHz) | $\overline{E}_F = V_{IL}, \overline{G}_F = V_{IH}$ | | 14 | 16 | mA |
| | Supply Current Synchronous Read (f=40MHz) | 4 Word | | 13 | 17 | mA |
| | | 8 Word | | 15 | 19 | mA |
| | | 16 Word | | 17 | 21 | mA |
| | | Continuous | | 21 | 26 | mA |
| | Supply Current Synchronous Read (f=50MHz) | 4 Word | | 16 | 19 | mA |
| | | 8 Word | | 19 | 23 | mA |
| | | 16 Word | | 22 | 26 | mA |
| | | Continuous | | 23 | 28 | mA |
| $I_{DD2}$ | Supply Current (Reset) | $\overline{RP}_F = V_{SS} \pm 0.2V$ | | 25 | 75 | µA |
| $I_{DD3}$ | Supply Current (Standby) | $\overline{E}_F = V_{DDF} \pm 0.2V$ | | 25 | 75 | µA |
| $I_{DD4}$ | Supply Current (Automatic Standby) | $\overline{E}_F = V_{IL}, \overline{G}_F = V_{IH}$ | | 25 | 75 | µA |
| $I_{DD5}$ [1] | Supply Current (Program) | $V_{PPF} = V_{PPH}$ | | 8 | 15 | mA |
| | | $V_{PPF} = V_{DDF}$ | | 10 | 20 | mA |
| | Supply Current (Erase) | $V_{PPF} = V_{PPH}$ | | 8 | 15 | mA |
| | | $V_{PPF} = V_{DDF}$ | | 10 | 20 | mA |
| $I_{DD6}$ [1,2] | Supply Current (Dual Operations) | Program/Erase in one Bank, Asynchronous Read in another Bank | | 24 | 36 | mA |
| | | Program/Erase in one Bank, Synchronous Read in another Bank | | 40 | 55 | mA |
| $I_{DD7}$ [1] | Supply Current Program/ Erase Suspended (Standby) | $\overline{E} = V_{DD} \pm 0.2V$ | | 25 | 75 | µA |
| $I_{PP1}$ [1] | $V_{PPF}$ Supply Current (Program) | $V_{PPF} = V_{PPH}$ | | 2 | 5 | mA |
| | | $V_{PPF} = V_{DDF}$ | | 0.2 | 5 | µA |
| | $V_{PPF}$ Supply Current (Erase) | $V_{PPF} = V_{PPH}$ | | 2 | 5 | mA |
| | | $V_{PPF} = V_{DDF}$ | | 0.2 | 5 | µA |
| $I_{PP2}$ | $V_{PPF}$ Supply Current (Read) | $V_{PPF} \leq V_{DDF}$ | | 0.2 | 5 | µA |
| $I_{PP3}$ [1] | $V_{PPF}$ Supply Current (Standby) | $V_{PPF} \leq V_{DDF}$ | | 0.2 | 5 | µA |

Note: 1. Sampled only, not 100% tested.
  2. $V_{DD}$ Dual Operation current is the sum of read and program or erase currents.

### Table 8. Flash Memory DC Characteristics - Voltages

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|--------|-----------|----------------|-----|-----|-----|------|
| $V_{IL}$ | Input Low Voltage | | −0.5 | | 0.4 | V |
| $V_{IH}$ | Input High Voltage | | $V_{DDQ}$ −0.4 | | $V_{DDQ}$ + 0.4 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 100μA | | | 0.1 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = −100μA | $V_{DDQ}$ −0.1 | | | V |
| $V_{PP1}$ | $V_{PPF}$ Program Voltage-Logic | Program, Erase | 1.1 | 1.8 | 3.3 | V |
| $V_{PPH}$ | $V_{PPF}$ Program Voltage Factory | Program, Erase | 8.5 | 9.0 | 12.6 | V |
| $V_{PPLK}$ | Program or Erase Lockout | | | | 0.4 | V |
| $V_{LKO}$ | $V_{DDF}$ Lock Voltage | | 1 | | | V |
| $V_{RPH}$ | $\overline{RP}_F$ pin Extended High Voltage | | | | 3.3 | V |

### Table 9. PSRAM DC Characteristics

| Symbol | Parameter | Test Condition | | Min | Max | Unit |
|--------|-----------|----------------|---|-----|-----|------|
| $I_{CC1}$ | $V_{DDP}$ Active Current | $V_{DDP}$ = 3.3V, $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $\overline{E1}_P$ = $V_{IL}$ and $E2_P$ = $V_{IH}$, $I_{OUT}$ = 0mA | $t_{RC}$ / $t_{WC}$ = minimum | | 30 | mA |
| $I_{CC2}$ | | | $t_{RC}$ / $t_{WC}$ = 1 μs | | 3 | mA |
| $I_{CC3}$ | $V_{DDP}$ Page Read Current | $V_{DDP}$ = 3.3V, $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $\overline{E1}_P$ = $V_{IL}$ and $E2_P$ = $V_{IH}$, $I_{OUT}$ = 0mA, $t_{PRC}$ = min. | | | 10 | mA |
| $I_{CCPD}$ | $V_{DDP}$ Power Down Current | $V_{DDP}$ = 3.3V, $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $E2_P \leq$ 0.2V | Deep Power-Down | | 10 | μA |
| $I_{CCP4}$ | | | 4 Mb PAR | | 40 | μA |
| $I_{CCP8}$ | | | 8 Mb PAR | | 50 | μA |
| $I_{CCP16}$ | | | 16 Mb PAR | | 65 | μA |
| $I_{LI}$ | Input Leakage Current | 0V ≤ $V_{IN}$ ≤ $V_{DDP}$ | | −1 | 1 | μA |
| $I_{LO}$ | Output Leakage Current | 0V ≤ $V_{OUT}$ ≤ $V_{DDP}$ | | −1 | 1 | μA |
| $I_{SB}$ | Standby Supply Current CMOS | $V_{DDP}$ = 3.3V, $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{DDP}$ −0.2V, $\overline{E1}_P$ = $E2_P \geq V_{DDP}$ −0.2V | | | 100 | μA |
| $V_{IH}$ [(1)] | Input High Voltage | | | 0.8$V_{DDP}$ | $V_{DDP}$ + 0.2 | V |
| $V_{IL}$ [(2)] | Input Low Voltage | | | −0.3 | 0.2$V_{DDP}$ | V |
| $V_{OH}$ | Output High Voltage | $V_{DDP}$ = 2.7V, $I_{OH}$ = −0.5mA | | 2.4 | | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 1mA | | | 0.4 | V |

Note: 1. Maximum DC voltage on input and I/O pins is $V_{DDP}$ + 0.2V.
During voltage transitions, input may positive overshoot to $V_{DDP}$ + 1.0V for a period of up to 5ns.
2. Minimum DC voltage on input or I/O pins is −0.3V.
During voltage transitions, input may positive overshoot to $V_{SS}$ + 1.0V for a period of up to 5ns.

## PACKAGE MECHANICAL

**Figure 7. Stacked TFBGA88 8x10mm - 8x10 active ball array, 0.8mm pitch, Bottom View Outline**
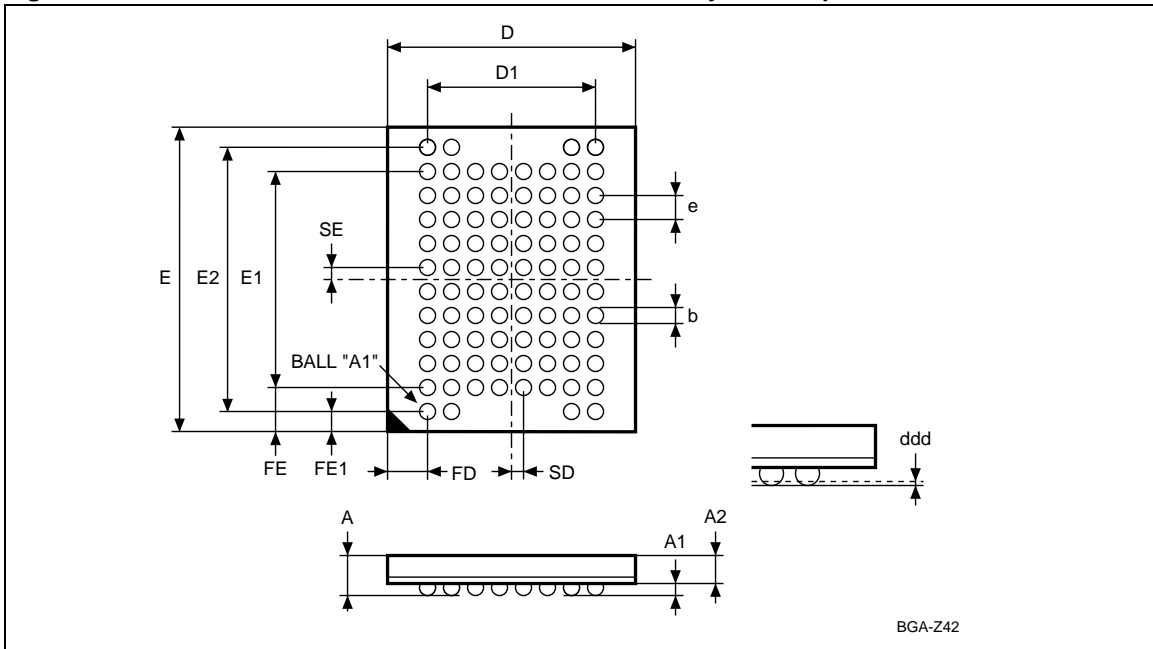


Note: Drawing is not to scale.

**Table 10. Stacked TFBGA88 8x10mm - 8x10 active ball array, 0.8mm pitch, Package Data**

| Symbol | millimeters | | | inches | | |
|---|---|---|---|---|---|---|
| | **Typ** | **Min** | **Max** | **Typ** | **Min** | **Max** |
| A | | | 1.200 | | | 0.0472 |
| A1 | | 0.200 | | | 0.0079 | |
| A2 | 0.850 | | | 0.0335 | | |
| b | 0.350 | 0.300 | 0.400 | 0.0138 | 0.0118 | 0.0157 |
| D | 8.000 | 7.900 | 8.100 | 0.3150 | 0.3110 | 0.3189 |
| D1 | 5.600 | | | 0.2205 | | |
| ddd | | | 0.100 | | | 0.0039 |
| E | 10.000 | 9.900 | 10.100 | 0.3937 | 0.3898 | 0.3976 |
| E1 | 7.200 | | | 0.2835 | | |
| E2 | 8.800 | | | 0.3465 | | |
| e | 0.800 | – | – | 0.0315 | – | – |
| FD | 1.200 | | | 0.0472 | | |
| FE | 1.400 | | | 0.0551 | | |
| FE1 | 0.600 | | | 0.0236 | | |
| SD | 0.400 | | | 0.0157 | | |
| SE | 0.400 | | | 0.0157 | | |

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## PART NUMBERING

**Table 11. Ordering Information Scheme**

Example:                                        M36  L  0  T  7  0  5  0  T  0  ZAQ  T

**Device Type**

M36 = Multi-Chip Package (Flash + RAM)

**Flash 1 Architecture**

L = Multilevel, Multiple Bank, Burst mode

**Flash 2 Architecture**

0 = No Die

**Operating Voltage**

T = $V_{DDF}$ = 1.7 to 2V; $V_{DDQ}$ = $V_{DDP}$ = 2.7 to 3.3V

**Flash 1 Density**

7 = 128 Mbit

**Flash 2 Density**

0 = No Die

**RAM 1 Density**

5 = 32 Mbit

**RAM 0 Density**

0 = No Die

**Parameter Blocks Location**

T = Top Boot Block Flash
B = Bottom Boot Block Flash

**Product Version**

0 = 0.13µm Flash technology, 90ns speeds;
0.18µm RAM, 70ns speed

**Package**

ZAQ = Stacked TFBGA88 8x10mm - 8x10 active ball array, 0.8mm pitch

**Option**

Blank = Standard Packing
T = Tape & Reel Packing
E= lead-free and RoHS package, standard packing
F= lead-free and RoHS package, tape and reel packing

Devices are shipped from the factory with the memory content bits erased to '1'. For a list of available options (Speed, Package, etc.) or for further information on any aspect of this device, please contact the ST-Microelectronics Sales Office nearest to you.

## REVISION HISTORY

**Table 12. Document Revision History**

| Date | Version | Revision Details |
|------|---------|------------------|
| 29-Jul-2003 | 0.1 | First Issue |
| 10-Dec-2004 | 1.0 | Document status promoted from Target Specification to full Datasheet.<br>TFBGA88 package specifications updated, package fully compliant with the ST ECOPACK specification.<br>Flash memory and PSRAM data updated to the version 0.2 of the M30L0T7000x0 datasheet and to the version 5.0 of the M69AW048B datasheet. |

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