HI-3282

ARINC 429 SERIAL TRANSMITTER AND DUAL RECEIVER

GENERAL DESCRIPTION

The HI-3282 is a silicon gate CMOS device for interfacing the ARINC 429 serial data bus to a 16-bit parallel data bus. Two receivers and an independent transmitter are provided. The receiver input circuitry and logic are designed to meet the ARINC 429 specifications for loading, level detection, timing, and protocol. The transmitter section provides the ARINC 429 communication protocol. Additional interface circuitry such as the Holt HI-8382 or HI-8585 are required to translate the 5 volt logic outputs to ARINC 429 drive levels.

The 16-bit parallel data bus exchanges the 32-bit ARINC data word in two steps when either loading the transmitter or interrogating the receivers. The data bus interfaces with CMOS and TTL.

Timing of all the circuitry begins with the master clock input, CLK. For ARINC 429 applications, the master clock frequency is 1 MHz.

Each independent receiver monitors the data stream with a sampling rate 10 times the data rate. The sampling rate is software selectable at either 1MHz or 125KHz. The results of a parity check are available as the 32nd ARINC bit.

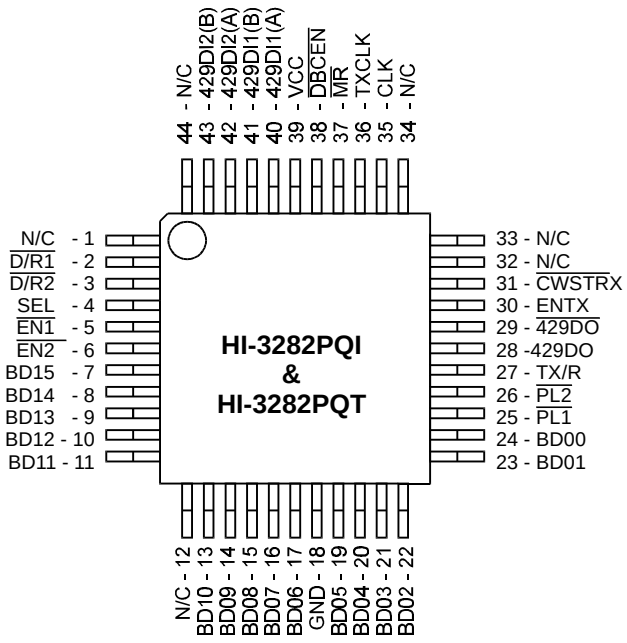
The transmitter has a First In, First Out (FIFO) memory to store 8 ARINC words for transmission. The data rate of the transmitter is software selectable by dividing the master clock, CLK, by either 10 or 80. The master clock is used to set the timing of the ARINC transmission within the required resolution.

APPLICATIONS

- Avionics data communication
- Serial to parallel conversion
- Parallel to serial conversion

FEATURES

- ARINC specification 429 compatible
- Compatible with Industry-standard alternate Parts
- Small footprint 44 PQFP package option
- 16-Bit parallel data bus
- Direct receiver interface to ARINC bus
- Timing control 10 times the data rate
- Selectable data clocks
- Automatic transmitter data timing
- Self test mode
- Parity functions
- Low power, single 5 volt supply
- Industrial & full military temperature ranges



44-Pin Plastic Quad Flat Pack (PQFP)

PIN DESCRIPTION

SYMBOL	FUNCTION	DESCRIPTION
VCC	POWER	+5V ±5%
429DI1 (A)	INPUT	ARINC receiver 1 positive input
429DI1 (B)	INPUT	ARINC receiver 1 negative input
429DI2 (A)	INPUT	ARINC receiver 2 positive input
429DI2 (B)	INPUT	ARINC receiver 2 negative input
$\overline{D/R1}$	OUTPUT	Receiver 1 data ready flag
$\overline{D/R2}$	OUTPUT	Receiver 2 data ready flag
SEL	INPUT	Receiver data byte selection (0 = BYTE 1) (1 = BYTE 2)
$\overline{EN1}$	INPUT	Data Bus control, enables receiver 1 data to outputs
$\overline{EN2}$	INPUT	Data Bus control, enables receiver 2 data to outputs if $\overline{EN1}$ is high
BD15	I/O	Data Bus
BD14	I/O	Data Bus
BD13	I/O	Data Bus
BD12	I/O	Data Bus
BD11	I/O	Data Bus
BD10	I/O	Data Bus
BD09	I/O	Data Bus
BD08	I/O	Data Bus
BD07	I/O	Data Bus
BD06	I/O	Data Bus
GND	POWER	0 V
BD05	I/O	Data Bus
BD04	I/O	Data Bus
BD03	I/O	Data Bus
BD02	I/O	Data Bus
BD01	I/O	Data Bus
BD00	I/O	Data Bus
$\overline{PL1}$	INPUT	Latch enable for byte 1 entered from data bus to transmitter FIFO.
$\overline{PL2}$	INPUT	Latch enable for byte 2 entered from data bus to transmitter FIFO. Must follow $\overline{PL1}$.
TX/R	OUTPUT	Transmitter ready flag. Goes low when ARINC word loaded into FIFO. Goes high after transmission and FIFO empty.
429DO	OUTPUT	"ONES" data output from transmitter.
$\overline{429DO}$	OUTPUT	"ZEROES" data output from transmitter.
ENTX	INPUT	Enable Transmission
$\overline{CWSTR}$	INPUT	Clock for control word register
CLK	INPUT	Master Clock input
TX CLK	OUTPUT	Transmitter Clock equal to Master Clock (CLK), divided by either 10 or 80.
$\overline{MR}$	INPUT	Master Reset, active low
$\overline{DBCEN}$	INPUT	Data bit control Enable. (Active low, with internal pull up to VDD).

FUNCTIONAL DESCRIPTION

CONTROL WORD REGISTER

The HI-3282 contains 11 data flip flops whose D inputs are connected to the data bus and clocks connected to $\overline{\text{CWSTR}}$. Each flip flop provides options to the user as follows:

DATA BUS PIN	FUNCTION	CONTROL	DESCRIPTION
BD04	PAREN		Enables parity bit insertion into Transmitter data bit 32
BDO5	SELF TEST	0 = ENABLE	If enabled, an internal connection is made passing 429DO and $\overline{429DO}$ to the receiver logic inputs
BDO6	RECEIVER 1 DECODER	1 = ENABLE	If enabled, ARINC bits 9 and, 10 must match the next two control word bits
BDO7	-	-	If Receiver 1 Decoder is enabled, the ARINC bit 9 must match this bit
BDO8	-	-	If Receiver 1 Decoder is enabled, the ARINC bit 10 must match this bit
BDO9	RECEIVER 2 DECODER	1 = ENABLE	If enabled, ARINC bits 9 and 10 must match the next two control word bits
BD10	-	-	If Receiver 2 Decoder is enabled, then ARINC bit 9 must match this bit
BD11	-	-	If Receiver 2 Decoder is enabled, then ARINC bit 10 must match this bit
BD12	INVERT XMTR PARITY	1 = ENABLE	Logic 0 enables normal odd parity and Logic 1 enables even parity output in transmitter 32nd bit
BD13	XMTR DATA CLK SELECT	0 = ÷10 1 = ÷80	CLK is divided either by 10 or 80 to obtain XMTR data clock
BD14	RCVR DTA CLK SELECT	0 = ÷10 1 = ÷80	CLK is divided either by 10 or 80 to obtain RCVR data clock

ARINC 429 DATA FORMAT

The following table shows the bit positions in exchanging data with the receiver or the transmitter. ARINC bit 1 is the first bit transmitted or received.

BYTE 1																
DATA BUS	BD 15	BD 14	BD 13	BD 12	BD 11	BD 10	BD 09	BD 08	BD 07	BD 06	BD 05	BD 04	BD 03	BD 02	BD 01	BD 00
ARINC BIT	13	12	11	10	9	31	30	32	1	2	3	4	5	6	7	8

BYTE 2																
DATA BUS	BD 15	BD 14	BD 13	BD 12	BD 11	BD 10	BD 09	BD 08	BD 07	BD 06	BD 05	BD 04	BD 03	BD 02	BD 01	BD 00
ARINC BIT	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14

THE RECEIVERS

ARINC BUS INTERFACE

Figure 1 shows the input circuit for each receiver. The ARINC 429 specification requires the following detection levels:

STATE	DIFFERENTIAL VOLTAGE
ONE	+6.5 Volts to +13 Volts
NULL	+2.5 Volts to -2.5 Volts
ZERO	-6.5 Volts to -13 Volts

The HI-8382 guarantees recognition of these levels with a common mode Voltage with respect to GND less than ±5V for the worst case condition (4.75V supply and 13V signal level).

The tolerances in the design guarantee detection of the above levels, so the actual acceptance ranges are slightly larger. If the ARINC signal is out of the actual acceptance ranges, including the nulls, the chip rejects the data.

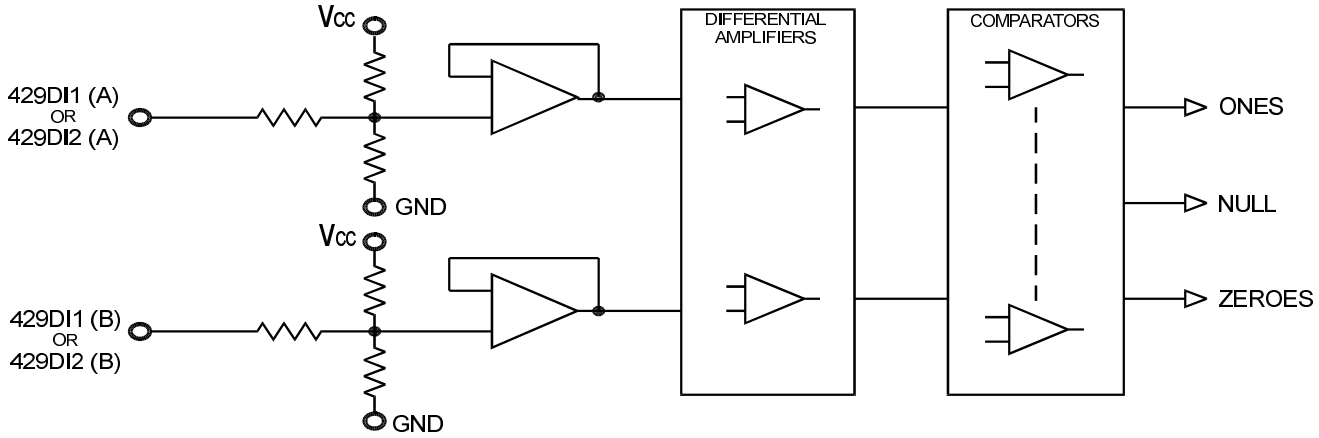


FIGURE 1. **ARINC RECEIVER INPUT**

FUNCTIONAL DESCRIPTION (con't)

RECEIVER LOGIC OPERATION

Figure 2 shows a block diagram of the logic section of each receiver.

BIT TIMING

The ARINC 429 specification contains the following timing specification for the received data:

	HIGH SPEED	LOW SPEED
BIT RATE	100K BPS ± 1%	12K -14.5K BPS
PULSE RISE TIME	1.5 ± 0.5 µsec	10 ± 5 µsec
PULSE FALL TIME	1.5 ± 0.5 µsec	10 ± 5 µsec
PULSEWIDTH	5 µsec ± 5%	34.5 to 41.7 µsec

RECEIVER PARITY

The receiver parity circuit counts Ones received, including the parity bit, ARINC bit 32. If the result is odd, then "0" will appear in the 32nd bit.

RETRIEVING DATA

Once 32 valid bits are recognized, the receiver logic generates an End of Sequence (EOS). If the receiver decoder is enabled and the 9th and 10th ARINC bits match the control word program bits or if the receiver decoder is disabled, then EOS clocks the data ready flag flip flop to a "1", $\overline{D/R1}$ or $\overline{D/R2}$ (or both) will go low. The data flag for a receiver will remain low until after both ARINC bytes from that receiver are retrieved. This is accomplished by activating $\overline{EN}$ with SEL, the byte selector, low to retrieve the first byte and activating $\overline{EN}$ with SEL high to retrieve the second byte. $\overline{EN1}$ retrieves data from receiver 1 and $\overline{EN2}$ retrieves data from receiver 2.

If another ARINC word is received, and a new EOS occurs before the two bytes are retrieved, the data is overwritten by the new word.

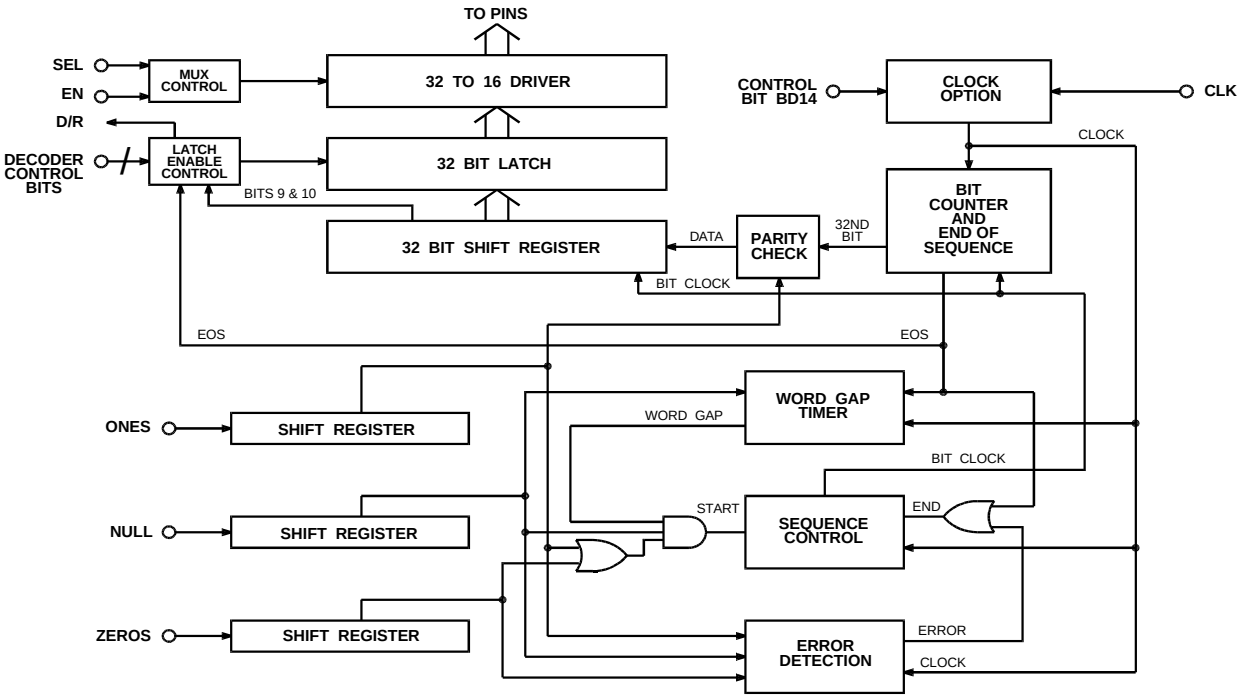


FIGURE 2. **RECEIVER BLOCK DIAGRAM**

FUNCTIONAL DESCRIPTION (con't)

TRANSMITTER

A block diagram of the transmitter section is shown in Figure 3.

FIFO OPERATION

The FIFO is loaded sequentially by first pulsing $\overline{PL1}$ to load byte 1 and then $\overline{PL2}$ to load byte 2. The control logic automatically loads the 31 bit word in the next available position of the FIFO. If TX/R, the transmitter ready flag is high (FIFO empty), then 8 words, each 31 bits long, may be loaded. If TX/R is low, then only the available positions may be loaded. If all 8 positions are full, the FIFO ignores further attempts to load data.

DATA TRANSMISSION

When ENTX goes high, enabling transmission, the FIFO positions are incremented with the top register loading into the data transmission shift register. Within 2.5 data clocks the first data bit appears at either 429DO or $\overline{429DO}$. The 31 bits in the data transmission shift register are presented sequentially to the outputs in the ARINC 429 format with the following timing:

	HIGH SPEED	LOW SPEED
ARINC DATA BIT TIME	10 Clocks	80 Clocks
DATA BIT TIME	5 Clocks	40 Clocks
NULL BIT TIME	5 Clocks	40 Clocks
WORD GAP TIME	40 Clocks	320 Clocks

The word counter detects when all loaded positions are transmitted and sets the transmitter ready flag, TX/R, high.

TRANSMITTER PARITY

Control register bit BD04 (PAREN) enables parity bit insertion into transmitter data bit 32. Parity is always inserted if DBCEN is open or high. If DBCEN is low, logic 0 on PAREN inserts data on bit 32, and logic 1 on PAREN inserts parity on bit 32.

The parity generator counts the ONES in the 31-bit word. If the BD12 control word bit is set low, the 32nd bit transmitted will make parity odd. If the control bit is high the parity is even.

SELF TEST

If the BD05 control word bit is set low, 429DO or $\overline{429DO}$ become inputs to the receivers bypassing the interface circuitry. 429DO and $\overline{429DO}$ outputs remain active during self test.

SYSTEM OPERATION

The two receivers are independent of the transmitter. Therefore, control of data exchanges are strictly at the option of the user. The only restrictions are:

1. The received data may be overwritten if not retrieved within one ARINC word cycle.

2. The FIFO can store 8 words maximum and ignores attempts to load addition data if full.

3. Byte 1 of the transmitter data must be loaded first.

4. Either byte of the received data may be retrieved first. Both bytes must be retrieved to clear the data ready flag.

5. After ENTX, transmission enable, goes high it cannot go low until TX/R, transmitter readyflag, goes high. Otherwise, one ARINC word is lost during transmission.

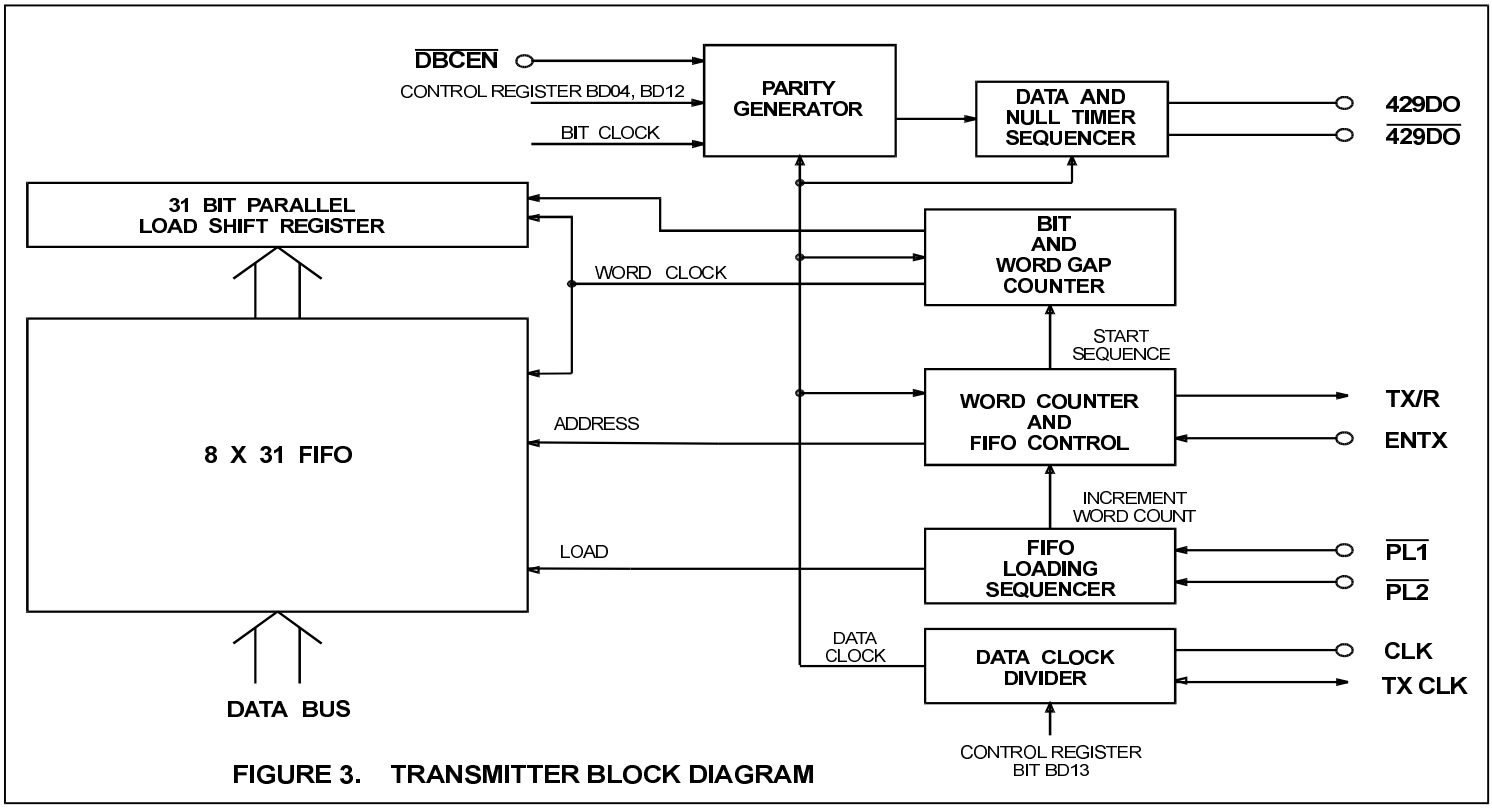


FIGURE 3. TRANSMITTER BLOCK DIAGRAM

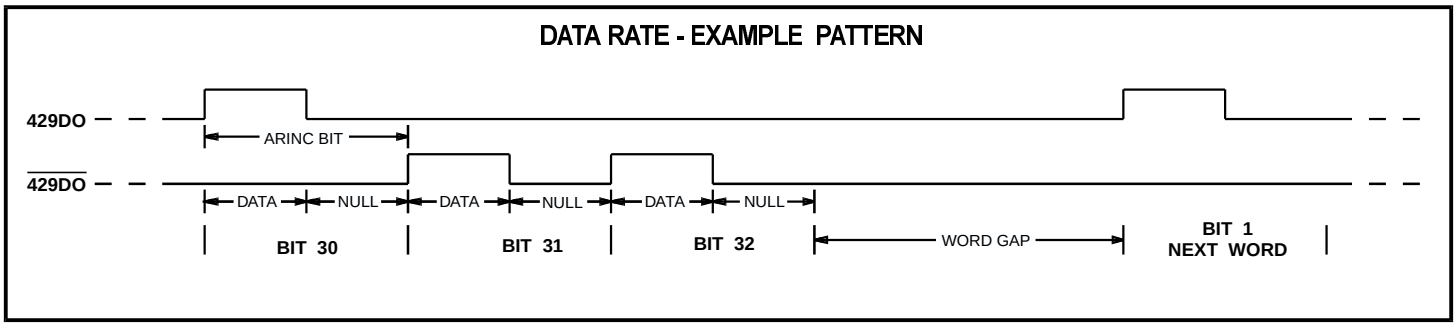
FUNCTIONAL DESCRIPTION (con't)

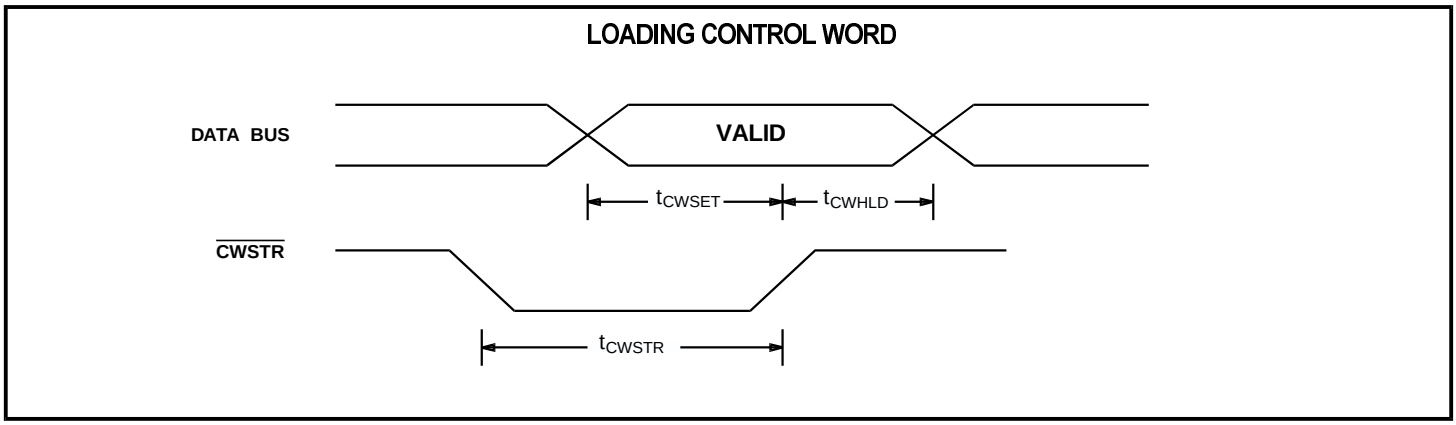
REPEATER OPERATION

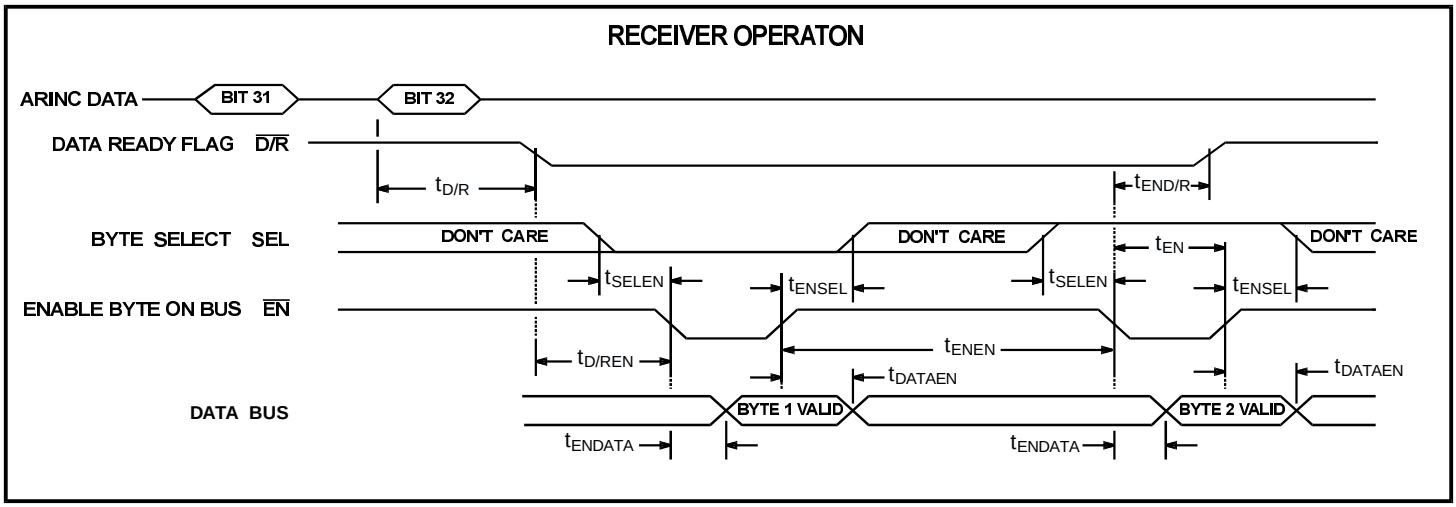
The repeater mode of operation allows a data word that has been received by the HI-3282 to be placed directly into its FIFO for transmission. After a 32-bit word has been shifted into the receiver shift register, the $\overline{D/R}$ flag will go low. A logic "0" is placed on the SEL line and $\overline{EN}$ is strobed. This is the same procedure as for normal receiver operation and it places the lower byte (16) of the data word on the data bus. By strobing $\overline{PL1}$ at the same time as $\overline{EN}$, the byte will also be placed into the transmitter FIFO. SEL is then taken high and $\overline{EN}$ is strobed again to place the upper byte of the data word on the data bus. By strobing $\overline{PL2}$ at the same time as $\overline{EN}$, the second byte will also be placed into the FIFO. The data word is now ready to be transmitted according to the parity programmed into the control word register.

In normal operation, either byte of a received data word may be read from the receiver latches first by use of SEL input. During repeater operation however, the lower byte of the data word must be read first. This is necessary because, as the data is being read, it is also being loaded into the FIFO and the transmitter FIFO is always loaded with the lower byte of the data word first.

TIMING DIAGRAMS

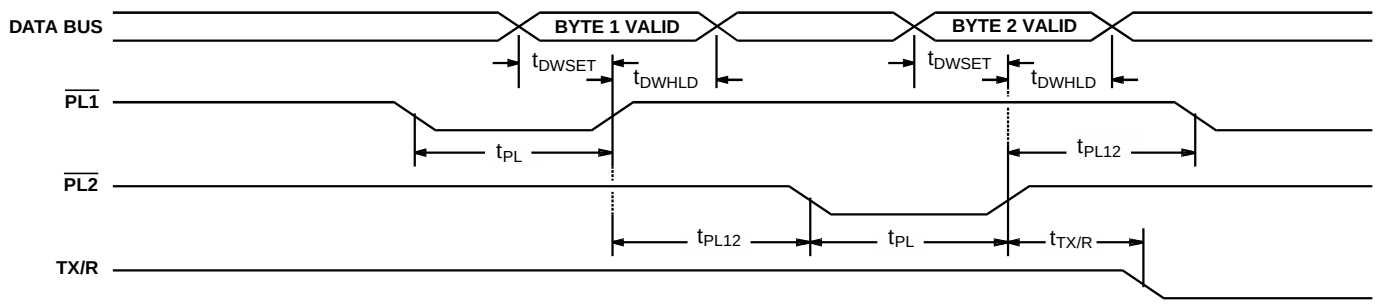




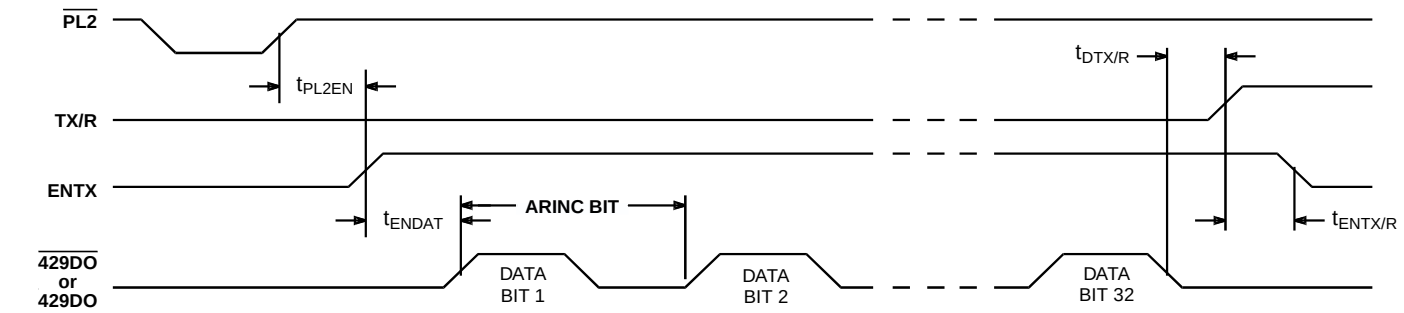


TIMING DIAGRAMS (con't)

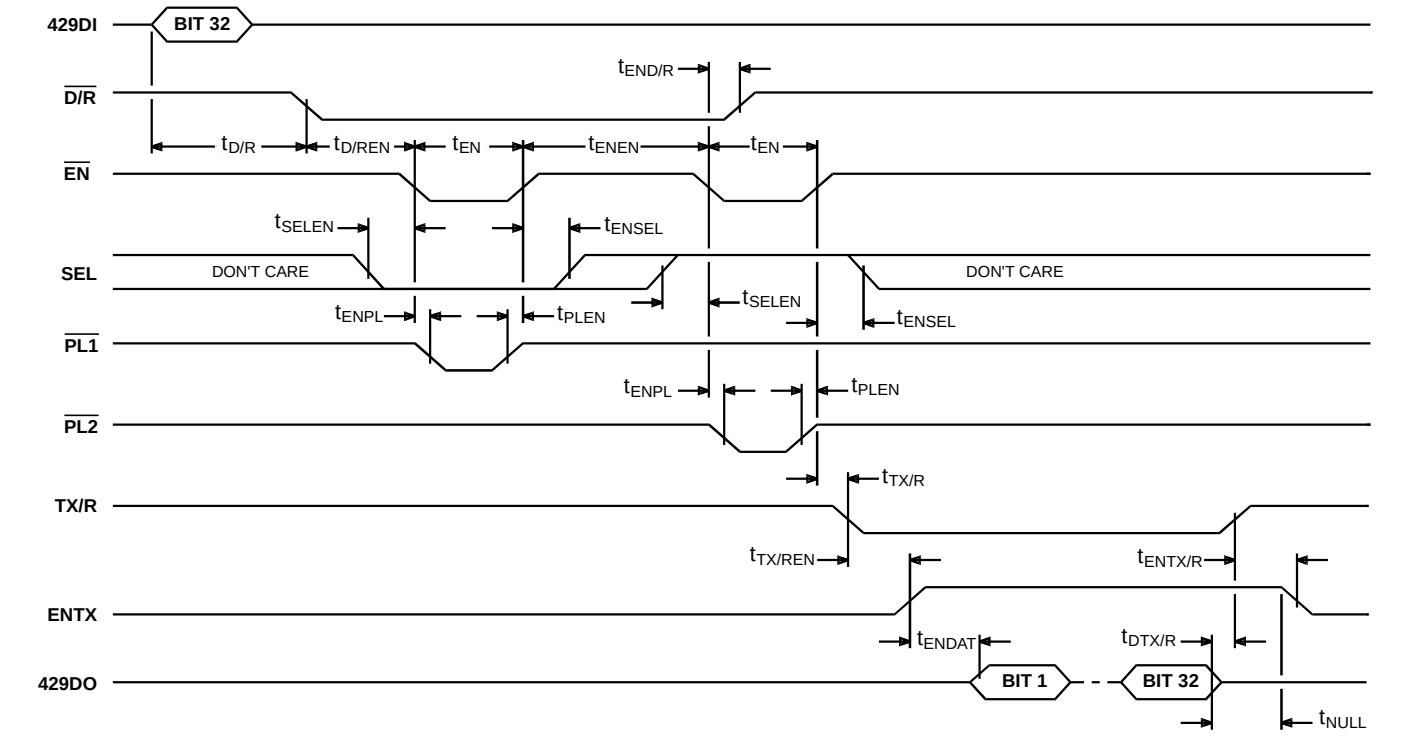
TRANSMITTER OPERATION



TRANSMITTING DATA



REPEATER OPERATION TIMING



ABSOLUTE MAXIMUM RATINGS

Supply Voltage Vcc ..... -0.5V to +7V	Power Dissipation 500mW
Voltage at pins 2, 3, 4 & 5 ..... -29V to +29V	Operating Temperature Range: (Industrial) ..... -40°C to +85°C
Voltage at any other pin ..... -1.5V to Vcc +1.5V	(Military) ..... -55°C to +125°C
DC Current Drain per input pin 10mA	Storage Temperature Range: ..... -65°C to +150°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Vcc = 5V ±5%, GND = 0V, TA = Operating Temperature Range (unless otherwise specified).

PARAMETER		SYMBOL	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
ARINC INPUTS - Pins: 429DI1(A), 429DI1(B), 429DI2(A), 429DI2(B)							
Differential Input Voltage:	ONE ZERO NULL	V_{IH} V_{IL} V_{NUL}	Common mode voltage less than ±5V with respect to GND	6.5 -13.0 -2.5	10.0 -10.0 0	13.0 -6.5 2.5	V V V
Input Resistance:	Differential To GND To Vcc	R_I R_G R_H		12 12 12	 27 27	 	KΩ KΩ kΩ
Input Current:	Input Sink Input Source	I_{IH} I_{IL}		 -450	 	200 	µA µA
Input Capacitance: (Guaranteed but not tested)	Differential To GND To Vcc	C_I C_G C_H		 	 	20 20 20	pF pF pF
BI-DIRECTIONAL INPUTS - Pins:BD00-BD15							
Input Voltage:	Input Voltage HI Input Voltage LO	V_{IH} V_{IL}		2.0 	 	 0.8	V V
Input Current:	Input Sink Input Source	I_{IH} I_{IL}		 -1.5	 	1.5 	µA µA
ALL OTHER INPUTS							
Input Voltage:	Input Voltage HI Input Voltage LO	V_{IH} V_{IL}		2.0 	 	 0.8	V V
Input Current:	Input Sink Input Source Pull-up Current ($\overline{DCBEN}$ Pin)	I_{IH} I_{IL} I_{PU}		 -10 -150	 	10 -50	µA µA µA
OUTPUTS							
Output Voltage:	Logic "1" Output Voltage Logic "0" Output Voltage	V_{OH} V_{OL}	I_{OH} = -1.5mA I_{OL} = 1.6mA	2.7 	 	 0.4	V V
Output Current: (Bi-directional Pins)	Output Sink Output Source	I_{OL} I_{OH}	V_{OUT} = 0.4V V_{OUT} = V_{CC} - 0.4V	1.6 	 	 -1.0	mA mA
Output Current: (All Other Outputs)	Output Sink Output Source	I_{OL} I_{OH}	V_{OUT} = 0.4V V_{OUT} = V_{CC} - 0.4V	1.6 	 	 -1.0	mA mA
Output Capacitance:		C_O			15		pF
SUPPLY INPUT							
Standby Supply Current:		I_{CC1}				10	mA
Operating Supply Current:		I_{CC2}				10	mA

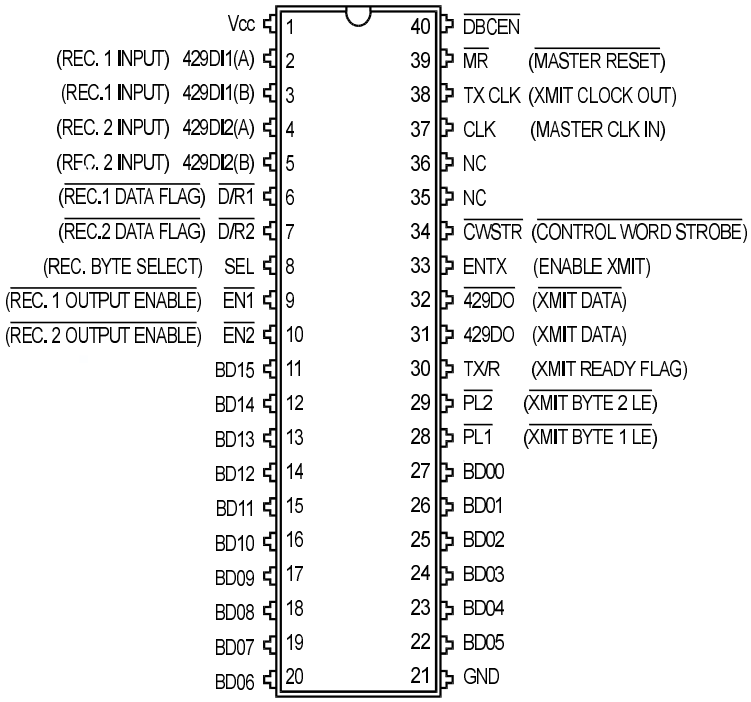
AC ELECTRICAL CHARACTERISTICS

Vcc = 5V, GND = 0V, TA = Operating Temperature Range and fclk = 1mhz ±0.1% with 60/40 duty cycle

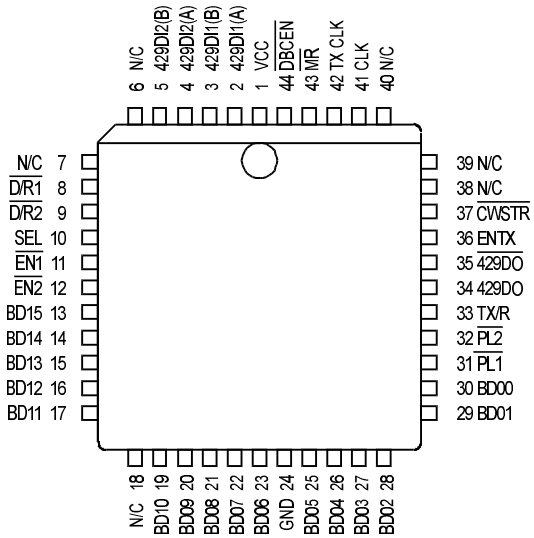
PARAMETER	SYMBOL	LIMITS			UNITS
		MIN	TYP	MAX	
CONTROL WORD TIMING					
Pulse Width - $\overline{CWSTR}$	t_{CWSTR}	50			ns
Setup - DATA BUS Valid to $\overline{CWSTR}$ HIGH	t_{CWSET}	50			ns
Hold - $\overline{CWSTR}$ HIGH to DATA BUS Hi-Z	t_{CWHLD}	0			ns
RECEIVER TIMING					
Delay - Start ARINC 32nd Bit to $\overline{D/R}$ LOW: High Speed	$t_{D/R}$			16	µs
Low Speed	$t_{D/R}$			128	µs
Delay - $\overline{D/R}$ LOW to $\overline{EN}$ L0W	$t_{D/REN}$	0			ns
Delay - $\overline{EN}$ LOW to $\overline{D/R}$ HIGH	$t_{END/R}$			200	ns
Setup - SEL to $\overline{EN}$ L0W	t_{SELEN}	0			ns
Hold - SEL to $\overline{EN}$ HIGH	t_{ENSEL}	0			ns
Delay - $\overline{EN}$ L0W to DATA BUS Valid	t_{ENDATA}		50	80	ns
Delay - $\overline{EN}$ HIGH to DATA BUS Hi-Z	t_{DATAEN}			30	ns
Pulse Width - $\overline{EN1}$ or $\overline{EN2}$	t_{EN}	80	50		ns
Spacing - $\overline{EN}$ HIGH to next $\overline{EN}$ L0W	t_{ENEN}	50			ns
FIFO TIMING					
Pulse Width - $\overline{PL1}$ or $\overline{PL2}$	t_{PL}	50			ns
Setup - DATA BUS Valid to $\overline{PL}$ HIGH	t_{DWSET}	50			ns
Hold - $\overline{PL}$ HIGH to DATA BUS Hi-Z	t_{DWHLD}	0			ns
Spacing - $\overline{PL1}$ or $\overline{PL2}$	t_{PL12}	0			ns
Delay - $\overline{PL2}$ HIGH to TX/R LOW	$t_{TX/R}$			840	ns
TRANSMISSION TIMING					
Spacing - $\overline{PL2}$ HIGH to ENTX HIGH	t_{PL2EN}	0			µs
Delay - ENTX HIGH to 429DO or $\overline{429D0}$: High Speed	t_{ENDAT}			25	µs
Delay - ENTX HIGH to 429DO or $\overline{429D0}$: Low Speed	t_{ENDAT}			200	µs
Delay - 32nd ARINC Bit to TX/R HIGH	$t_{DTX/R}$			50	ns
Spacing - TX/R HIGH to ENTX L0W	$t_{ENTX/R}$	0			ns
REPEATER OPERATION TIMING					
Delay - $\overline{EN}$ LOW to $\overline{PL}$ LOW	t_{ENPL}	0			ns
Hold - $\overline{PL}$ HIGH to $\overline{EN}$ HIGH	t_{PLEN}	0			ns
Delay - TX/R LOW to ENTX HIGH	$t_{TX/REN}$	0			ns
Master Reset Pulse Width	t_{MR}	50			ns
ARINC Data Rate and Bit Timing				± 1%	

ADDITIONAL HI-3282 PIN CONFIGURATIONS (See page 1 for the 44-pin Plastic QFP)

PIN CONFIGURATION (Top View)



HI-3282CDI, HI-3282CDT, HI-3282CDM
40-PIN CERAMIC SIDE-BRAZED DIP



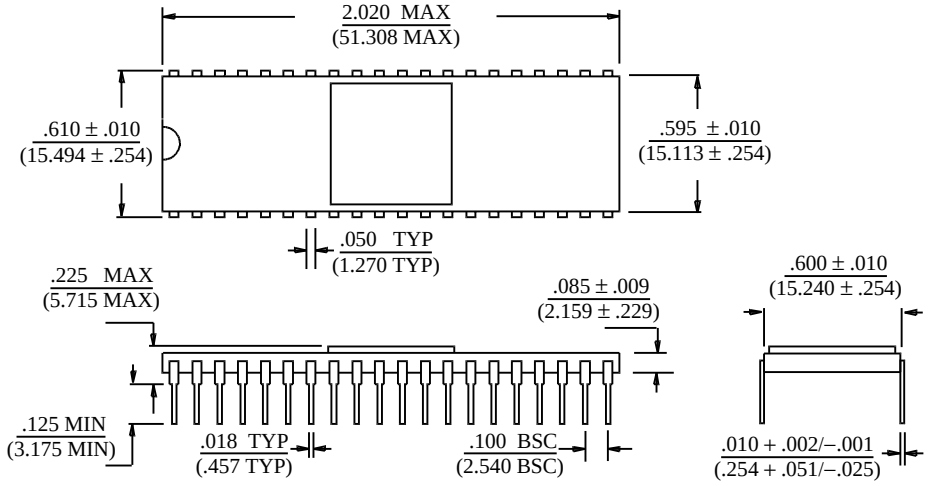
HI-3282PJI / HI-3282PJT
44-Pin J-Lead PLCC

ORDERING INFORMATION

PART NUMBER	PACKAGE DESCRIPTION	TEMPERATURE RANGE	FLOW	BURN IN	LEAD FINISH
HI-3282PQI	44 PIN PLASTIC QUAD FLATPACK (PQFP)	-40°C TO +85°C	I	NO	SOLDER
HI-3282PQT	44 PIN PLASTIC QUAD FLATPACK (PQFP)	-55°C TO +125°C	T	NO	SOLDER
HI-3282PJI	44 PIN PLASTIC J-LEAD PLCC	-40°C TO +85°C	I	NO	SOLDER
HI-3282PJT	44 PIN PLASTIC J-LEAD PLCC	-55°C TO +125°C	T	NO	SOLDER
HI-3282CDI	40 PIN CERAMIC SIDE-BRAZED DIP	-40°C TO +85°C	I	NO	GOLD
HI-3282CDT	40 PIN CERAMIC SIDE-BRAZED DIP	-55°C TO +125°C	T	NO	GOLD
HI-3282CDM	40 PIN CERAMIC SIDE-BRAZED DIP	-55°C TO +125°C	M	YES	SOLDER

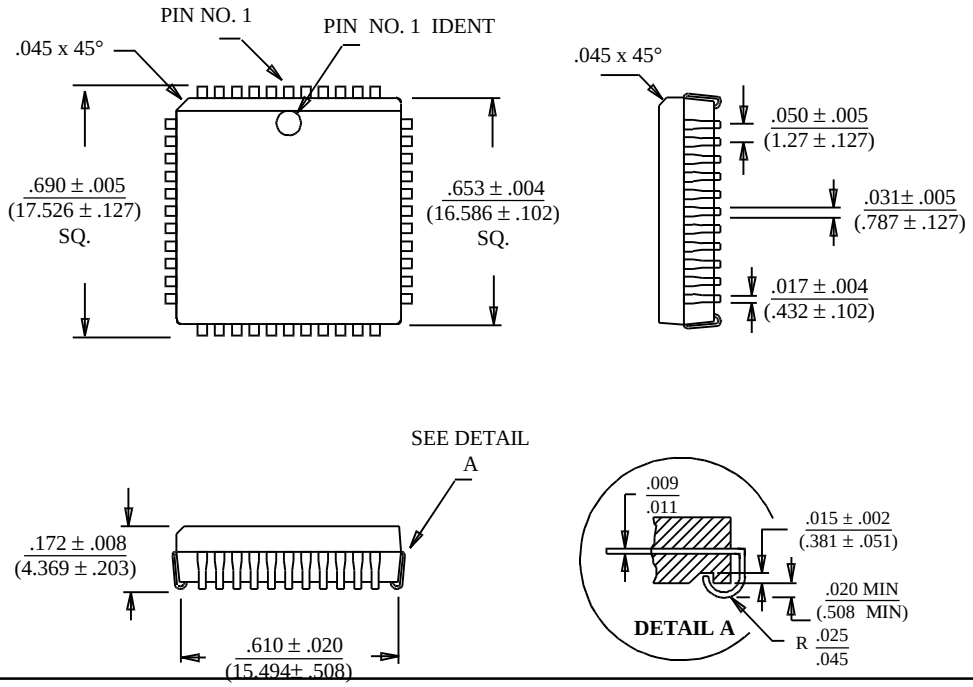
40-PIN CERAMIC SIDE-BRAZED DIP

Package Type: 40C



44-PIN PLASTIC PLCC

Package Type: 44J



44-PIN PLASTIC QUAD FLAT PACK (PQFP)

Package Type: 44PQS