

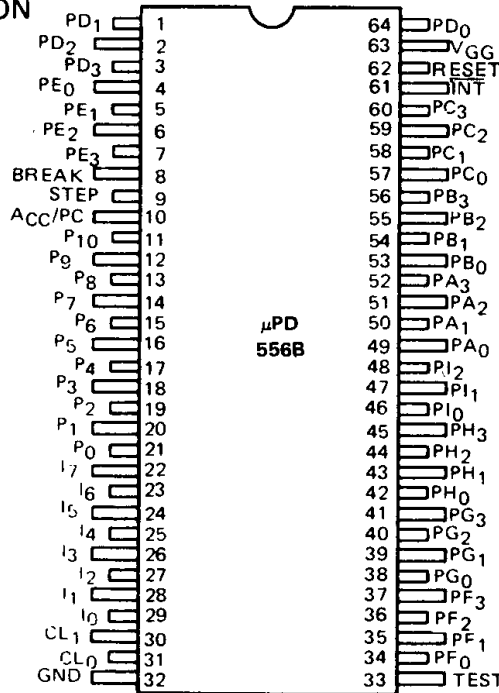
μCOM-4 4-BIT SINGLE CHIP ROM-LESS EVALUATION CHIP

DESCRIPTION The μPD556B is the ROM-less evaluation chip for the μCOM-4 4-bit single chip micro-computer family. The μPD556B is used in conjunction with an external 2048 x 8-bit program memory, such as the μPD2716 UV EPROM, to emulate each of the 14 different μCOM-4 single chip microcomputers.

The μPD556B contains a 96 x 4-bit RAM, which includes six working registers and the Flag register. It has a level-triggered hardware interrupt, a three-level stack, and a programmable 6-bit timer. The μPD556B executes all 80 instructions of the extended μCOM-4 family instruction set.

The μPD556B provides 35 I/O lines organized into the 4-bit input Ports A and B, the 4-bit I/O Ports C and D, the 4-bit output Ports E, F, G, and H, and the 3-bit output Port I. It typically executes its instructions with a 10μs instruction cycle time. The μPD556B is manufactured with a standard PMOS process, allowing use of a single -10V power supply, and is available in a 64-pin quad-in-line ceramic package.

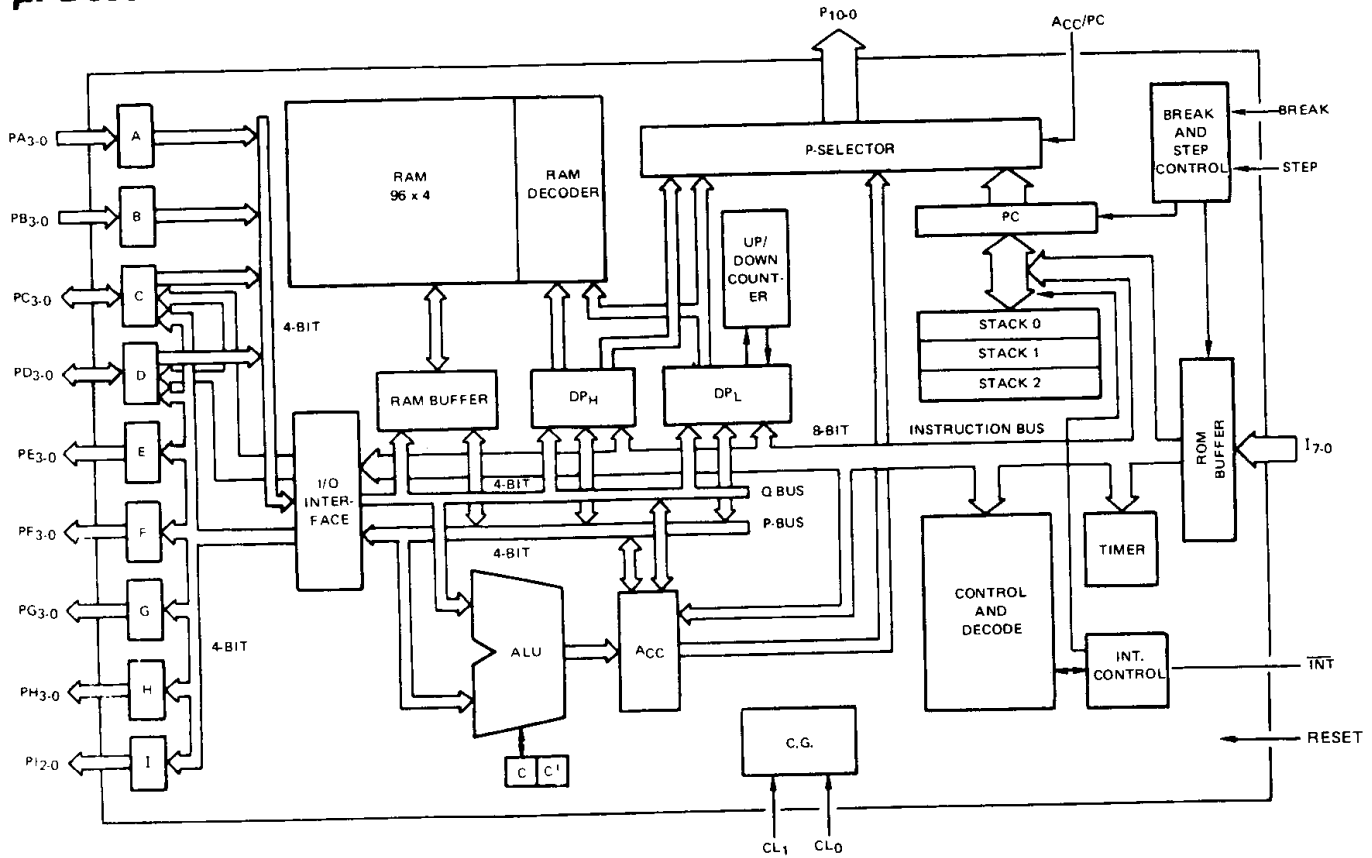
PIN CONFIGURATION



PIN NAMES

| | |
|----------------------------------|---|
| PA ₀ -PA ₃ | Input Port A |
| PB ₀ -PB ₃ | Input Port B |
| PC ₀ -PC ₃ | Input/Output Port C |
| PD ₀ -PD ₃ | Input/Output Port D |
| PE ₀ -PE ₃ | Output Port E |
| PF ₀ -PF ₃ | Output Port F |
| PG ₀ -PG ₃ | Output Port G |
| PH ₀ -PH ₃ | Output Port H |
| PI ₀ -PI ₂ | Output Port I |
| $\overline{\text{INT}}$ | Interrupt Input |
| I ₀₋₇ | Instruction Input |
| PC ₀₋₁₀ | Program Counter Output |
| ACC/PC | Accumulator/Program Counter Select |
| BREAK | Break Input |
| STEP | Single Step Input |
| CL ₀ -CL ₁ | External Clock Source |
| RESET | Reset |
| V _{GG} | Power Supply Negative |
| V _{SS} | Power Supply Positive |
| TEST | Factory Test Pin (Connect to V _{SS}) |

6



| | | |
|-----------------------------------|-----------------|----------------------------------|
| Operating Temperature | -10°C to +70°C | ABSOLUTE MAXIMUM RATINGS* |
| Storage Temperature | -40°C to +125°C | |
| Supply Voltage, V _{GG} | -15V to +0.3V | |
| All Input Voltages | -15V to +0.3V | |
| All Output Voltages | -15V to +0.3V | |
| Output Current (total, all ports) | -4 mA | |

T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = -10°C to +70°C; V_{GG} = -10V ± 10%, V_{SS} = 0V

| PARAMETER | SYMBOL | LIMITS | | | UNIT | TEST CONDITIONS |
|----------------------------|------------------|--------|-----|-----------------|------|--|
| | | MIN | TYP | MAX | | |
| Input High Voltage | V _{IH} | 0 | | -2.0 | V | Ports A to D, I _{7,0} BREAK, STEP, INT, RESET, and ACC/PC |
| Input Low Voltage | V _{IL} | -4.3 | | V _{GG} | V | Ports A to D, I _{7,0} BREAK, STEP, INT, RESET, and ACC/PC |
| Clock High Voltage | V _{φH} | 0 | | -0.8 | V | CL ₀ Input, External Clock |
| Clock Low Voltage | V _{φL} | -6.0 | | V _{GG} | V | CL ₀ Input, External Clock |
| Input Leakage Current High | I _{LIH} | | | +10 | μA | Ports A and B, I _{7,0} INT, RESET, BREAK, STEP, ACC/PC, V _I = -1V |
| | | | | +10 | μA | Ports C and D, V _I = -1V |
| Input Leakage Current Low | I _{LIL} | | | -10 | μA | Ports A and B, I _{7,0} INT, RESET, BREAK, STEP, ACC/PC, V _I = -11V |
| | | | | -10 | μA | Ports C and D, V _I = -11V |
| Clock Input Leakage High | I _{LφH} | | | +200 | μA | CL ₀ Input, External Clock, V _{φH} = 0V |
| Clock Input Leakage Low | I _{LφL} | | | -200 | μA | CL ₀ Input, External Clock, V _{φL} = -11V |
| Output High Voltage | V _{OH1} | | | -1.0 | V | Ports C to I, P _{10,0} I _{OH} = -1.0 mA |
| | V _{OH2} | | | -2.3 | V | Ports C to I, P _{10,0} I _{OH} = -3.3 mA |
| Output Leakage Current Low | I _{LOL} | | | -30 | μA | Ports C to I, P _{10,0} V _O = -11V |
| Supply Current | I _{GG} | | -30 | -50 | mA | |

AC CHARACTERISTICS

T_a = -10°C to +70°C, V_{GG} = -10V ± 10%

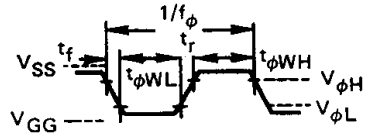
| PARAMETER | SYMBOL | LIMITS | | | UNIT | TEST CONDITIONS |
|----------------------------------|---------------------------------|--------|-----|-----|------|--------------------------|
| | | MIN | TYP | MAX | | |
| Frequency | f _φ | 150 | | 440 | KHz | |
| Clock Rise and Fall Times | t _r , t _f | 0 | | 0.3 | μs | |
| Clock Pulse Width High | t _{φWH} | 0.5 | | 5.6 | μs | |
| Clock Pulse Width Low | t _{φWL} | 0.5 | | 5.6 | μs | |
| Input Setup Time | t _{IS} | | | 5 | μs | |
| Input Hold Time | t _{IH} | 0 | | | μs | |
| BREAK to STEP Interval | t _{BS} | 200 | | | μs | f = 400 KHz, "1" Written |
| STEP to RUN Interval | t _{SB} | 200 | | | μs | f = 400 KHz, "1" Written |
| STEP Pulse Width | t _{WS} | 30 | | | μs | f = 400 KHz, "1" Written |
| BREAK to ACC Interval | t _{BA} | 200 | | | μs | f = 400 KHz, "1" Written |
| ACC/PC Pulse Width | t _{WA} | 30 | | | μs | f = 400 KHz, "1" Written |
| STEP to ACC Interval | t _{SA1} | 200 | | | μs | f = 400 KHz, "1" Written |
| PC to STEP Overlap | t _{SA2} | | | 5 | μs | f = 400 KHz, "1" Written |
| PC to RUN Interval | t _{AB} | 0 | | | μs | f = 400 KHz, "1" Written |
| ACC/PC - P _{10,0} Delay | t _{DAP1} | | | 15 | μs | f = 400 KHz, "1" Written |
| | t _{DAP2} | | | 15 | μs | f = 400 KHz, "1" Written |

CAPACITANCE

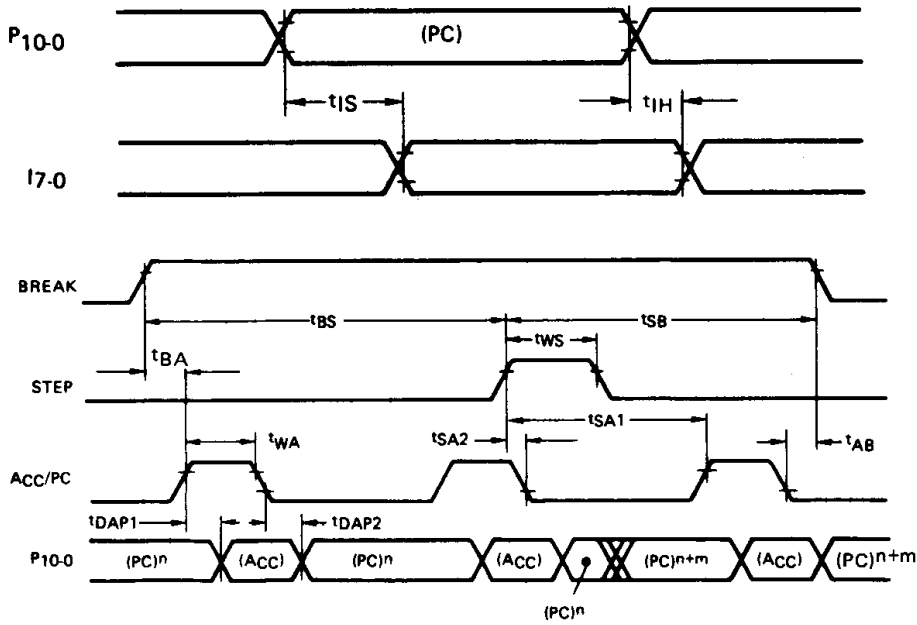
T_a = 25°C

| PARAMETER | SYMBOL | LIMITS | | | UNIT | TEST CONDITIONS |
|--------------------------|-----------------|--------|-----|-----|------|-----------------|
| | | MIN | TYP | MAX | | |
| Input Capacitance | C _I | | | 15 | pf | f = 1 MHz |
| Output Capacitance | C _O | | | 15 | pf | |
| Input/Output Capacitance | C _{IO} | | | 15 | pf | |

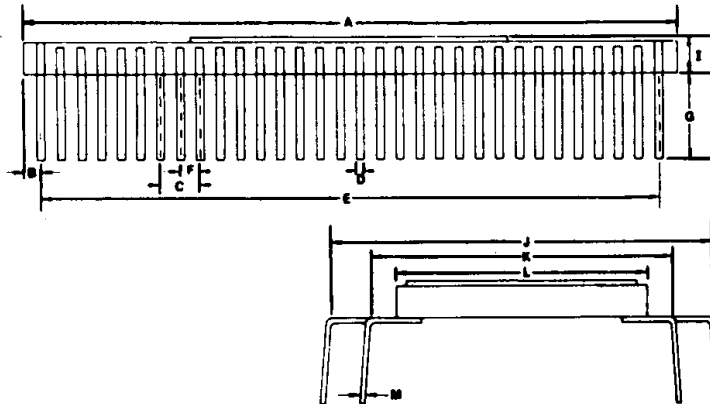
CLOCK WAVEFORM



TIMING WAVEFORMS



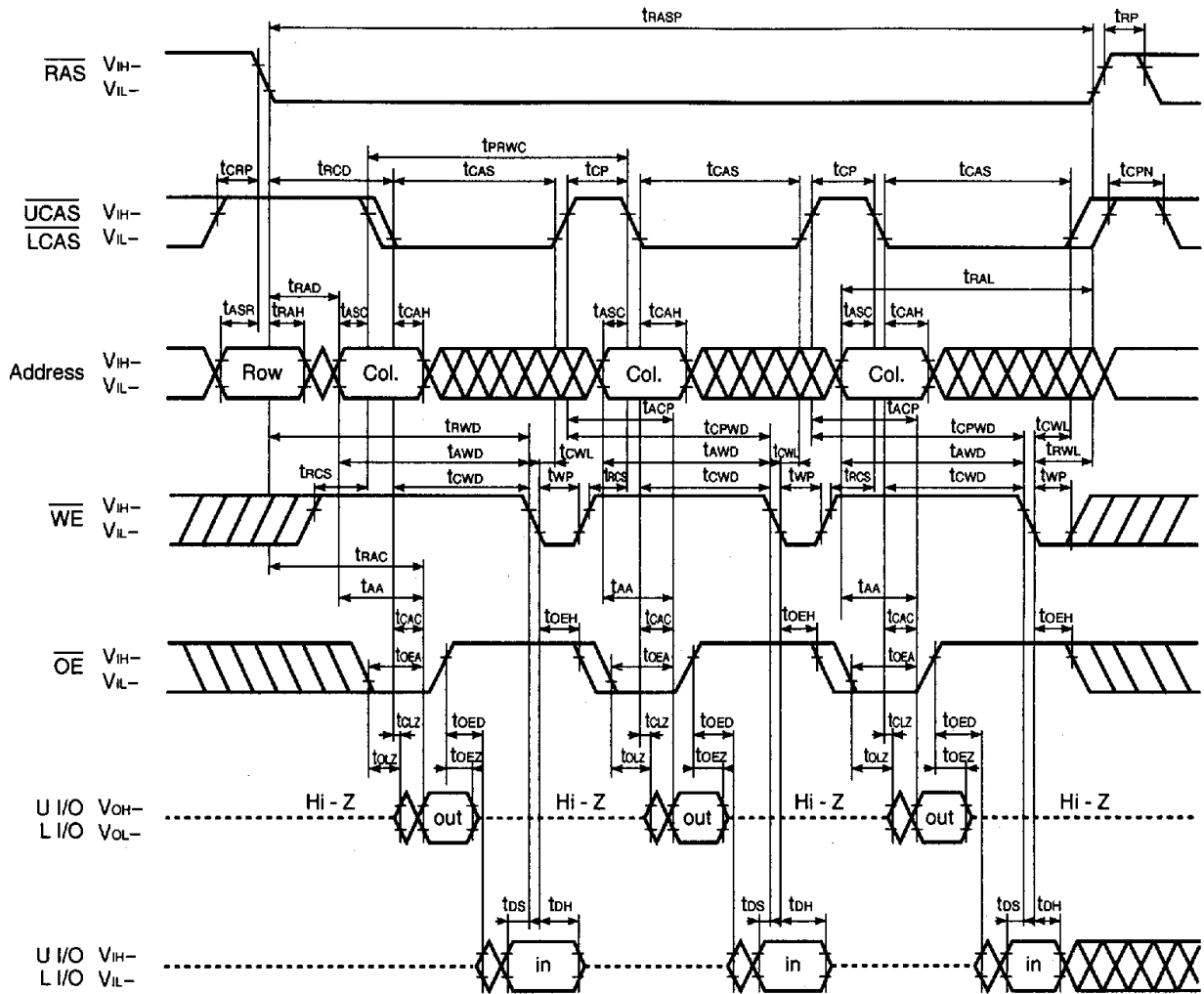
**PACKAGE OUTLINE
μPD556B**



CERAMIC

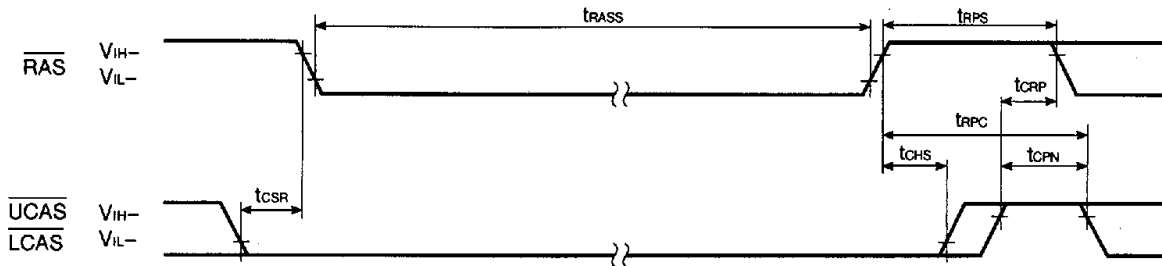
| ITEM | MILLIMETERS | INCHES |
|------|-------------|--------------|
| A | 41.5 | 1.634 MAX |
| B | 1.05 | 0.042 |
| C | 2.54 | 0.1 |
| D | 0.5 ± 0.1 | 0.2 ± 0.004 |
| E | 39.4 | 1.55 |
| F | 1.27 | 0.05 |
| G | 5.4 MIN | 0.21 MIN |
| I | 2.35 MAX | 0.13 MAX |
| J | 24.13 | 0.95 |
| K | 19.05 | 0.75 |
| L | 15.9 | 0.626 |
| M | 0.25 ± 0.05 | 0.01 ± 0.002 |

Fast Page Mode Read Modify Write Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self Refresh Cycle (Only for the μ PD42S18160)



Remark Address, $\overline{\text{WE}}$, $\overline{\text{OE}}$: Don't care L I/O, U I/O: Hi-Z

Cautions on Use of $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self Refresh

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh can be used independently when used in combination with distributed $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh; However, when used in combination with burst $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh or with long $\overline{\text{RAS}}$ only refresh (both distributed and burst), the following cautions must be observed.

- (1) **Normal Combined Use of $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self Refresh and Burst $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Long Refresh**
When $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh and burst $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ long refresh are used in combination, please perform $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh as follows just before and after setting $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh.

μ PD42S18160: 1,024 times within a 16 ms interval

- (2) **Normal Combined Use of $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Self Refresh and Long $\overline{\text{RAS}}$ Only Refresh**
When $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh and $\overline{\text{RAS}}$ only refresh are used in combination, please perform $\overline{\text{RAS}}$ only refresh as follows just before and after setting $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh.

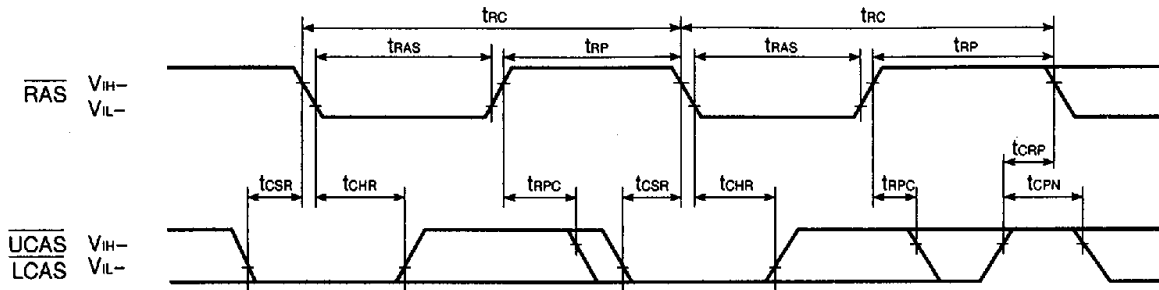
μ PD42S18160: 1,024 times within a 16 ms interval

- (3) If $t_{\text{RASS (MIN.)}}$ is not satisfied at the beginning of $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh cycles ($t_{\text{RAS}} < 100 \mu\text{s}$), $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles will be executed one time.
If $10 \mu\text{s} < t_{\text{RAS}} < 100 \mu\text{s}$, $\overline{\text{RAS}}$ precharge time for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh (t_{RPS}) is applied.
And refresh cycles as follows should be met.

μ PD42S18160: 1,024 times within a 128 ms interval

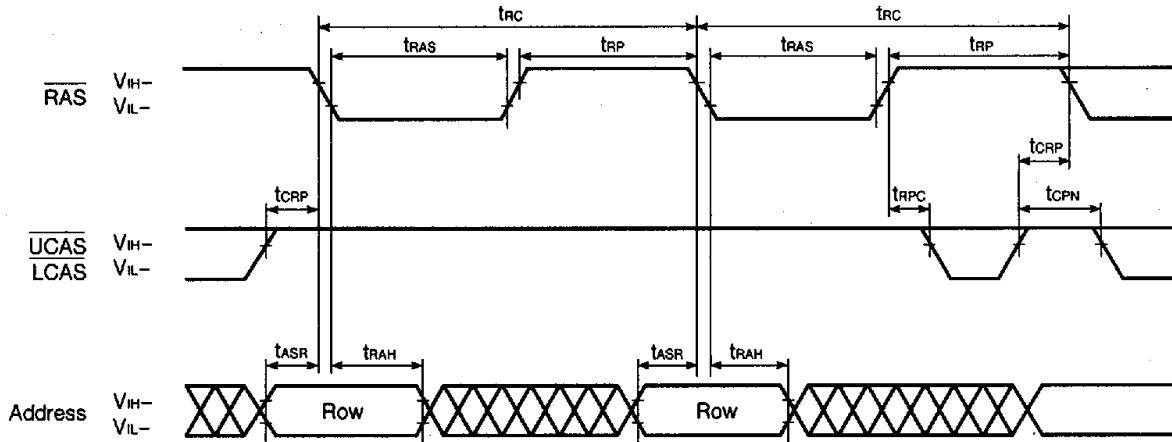
For details, please refer to **How to use DRAM User's Manual**.

CAS Before RAS Refresh Cycle



Remark Address, \overline{WE} , \overline{OE} : Don't care L I/O, U I/O: Hi-Z

RAS Only Refresh Cycle



Remark \overline{WE} , \overline{OE} : Don't care L I/O, U I/O: Hi-Z

Hidden Refresh Cycle (Read)

