HIP0051

0.25A/50V Octal Low Side Power Driver with Serial Bus Control

June 1996

Features

- **Eight Open Drain - NDMOS Low Side Drivers Each Capable of 250mA**
- **High Voltage Power BiMOS with Low Idle and Standby Current**
- **Over-Voltage Clamp Protection**
  - **Each Output . . . . . 50V Typical**
- **Serial Data Input, Parallel Output Power Drive**
- **Common Enable for Output Drivers and Data Storage Register**
- **-40°C to 85°C Operating Range**

Applications

- **Automotive and Industrial Systems**
- **Solenoids, Relays and Lamp Drivers**
- **Logic and µP Controlled Drivers**
- **Robotic Controls**

Description

The HIP0051 is a logic controlled, eight channel Octal Low Side Power Driver. As shown in the Block Diagram, the outputs are controlled via the serial data interface which allows the data to be shifted out, allowing control of other cascaded serial devices.

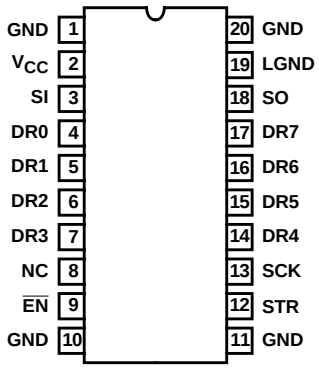
The HIP0051 is fabricated in a Power BiMOS IC process, and is intended for use in automotive and other applications having a wide range of temperature and electrical stress conditions. It is particularly suited for driving lamps, displays, relays, and solenoids in applications where low operating power, high breakdown voltage, and high output current at high temperature is required.

Ordering Information

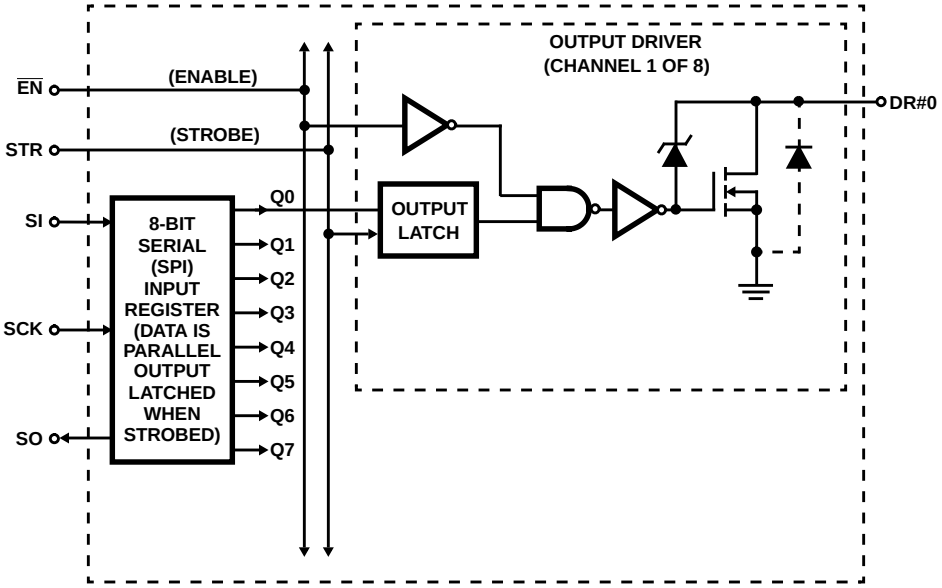
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HIP0051IB	-40 to 85	20 Ld SOIC	M20.3

Pinout

HIP0051
(SOIC)
TOP VIEW



Block Diagram



File Number **4155**

Absolute Maximum Ratings

Output Voltage, V_{OUT} (Note 1) . . . . . -0.3V to 40V
Input Voltage, V_{IN} . . . . . -0.3V to V_{CC} + 0.3V
Logic Supply Voltage, V_{CC} . . . . . -0.3V to +7V
Output Clamp Energy, 25°C (5ms Pulse) 75mJ
Continuous Output Load Current, I_{LOAD} (Each Output) 0.25A
Continuous Output Current, I_{LOAD} (All Outputs ON, Note 2) . . 1.69A
Peak Output Current
  Each Output, Other Outputs OFF . . . . . ±2A
  Peak Avalanche Current (3ms duration) 1A

Operating Conditions

Operating Ambient Temperature Range, T_A . . . . . -40°C to 85°C
Operating Logic Supply Voltage Range, V_{CC} . . . . . +4.5V to +5.5V
Power Output Driver Voltage Range . . . . . 0 to V_{OC}
Max. Supply Current, with 100mA each Output 100µA
Max. Supply Current, with No Load, Outputs OFF 100µA
Logic Input High Voltage . . . . . .0.7xV_{CC}
Logic Input Low Voltage . . . . . .0.2xV_{CC}
Typical Output R_{DSON} Channel Resistance 2Ω
Typical Output Rise Time 4µs
Typical Output Fall Time 10µs

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)
SOIC Package	100

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range, T_{STG} . . . . -55°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. The MOSFET Output Drain is internally clamped with a Drain-to-Gate zener diode that turns-on the MOSFET; holding the Drain at the Output Clamp voltage V_{OC}.
2. The maximum continuous current with all outputs on is limited by package dissipation. At 25°C ambient temperature, the maximum equal current with all outputs ON is 211mA in each output for a total of 1.69A. At a maximum ambient temperature of T_A = 85°C and r_{DSON}(Max) = 3.5Ω, each output is limited to 152mA and the total current for all 8 outputs ON is 8 x 152mA = 1.22A.
3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V_{CC} = 4.5V to 5.5V, V_{BATT} = 8V to 16V, T_A = -40°C to 85°C, Unless Otherwise Specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUTS DRIVERS (DR0 TO DR7)						
Output Channel Resistance	$r_{DS(ON)}$	Output Current = 200mA, T_A = 85°C		2	3.5	Ω
Output Clamping Voltage	V_{OC}	Outputs OFF	42	50	58	V
Output Clamping Energy	E_{OC}	5ms Pulse, T_A = 25°C	75	190		mJ
Peak Output Load Currents, Short Duration	I_{PEAK}	100µs Duration, Each Output, all Outputs ON, Duty Cycle ≤ 2%	0.85	-	-	A
Cold Start-up Lamp Currents	I_{LAMP}	5ms Duration, Each Output, all Outputs ON, Duty Cycle ≤ 17%	0.3	-	-	A
Output OFF Leakage Current	I_{OFF}	Output Voltage = 40V, T_A = 85°C	-	-0.2	10	µA
Output Rise Time	t_{rise}	Load = 75Ω, 0.01µF (RC in Parallel), V_{BATT} = 18V	0.5	4	30	µs
Output Fall Time	t_{fall}		0.5	10	30	µs
Output Delay from Strobe, High to Low Output Transition	t_{DHL}		1	4	10	µs
Output Delay from Strobe, Low to High Output Transition	t_{DLH}		0.2	2.6	10	µs
LOGIC SUPPLY						
Logic Supply Current, Loaded	I_{CC}	All Outputs ON, 200mA Load at each Output	-	-	100	µA
Logic Supply Current, No Load	I_{CC}	All Outputs OFF	-	-	100	µA

Electrical Specifications V_{CC} = 4.5V to 5.5V, V_{BATT} = 8V to 16V, T_A = -40°C to 85°C, Unless Otherwise Specified. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS ($\overline{EN}$, SI, SCK, STR)						
Threshold Voltage at Falling Edge	V_{T-}	V_{CC} = 5V ± 10%	0.2V_{CC}	0.3V_{CC}	-	V
Threshold Voltage at Rising Edge	V_{T+}	V_{CC} = 5V ± 10%	-	0.6V_{CC}	0.7V_{CC}	V
Hysteresis Voltage	V_H	V_{T+} - V_{T-}	0.85	1.4	2.25	V
Leakage Current	I_{LIN}	V_{CC} = 5V	-10	-0.2	10	µA
Leakage Current	I_{LIN}	V_{CC} = 0V	-10	-0.1	10	µA
SERIAL DATA CLOCK (SCK)						
Frequency	f_{SCK}		-	-	1.6	MHz
Pulse Width High	$t_{W(CKH)}$		175	27	-	ns
Pulse Width Low	$t_{W(CKL)}$		175	27	-	ns
SERIAL DATA IN (SI)						
Input Setup Time	t_{SUI}		-	1.1	75	ns
Input Hold Time	T_{HI}		-	1.5	75	ns
STROBE (STR)						
Strobe Pulse Width	$t_{W(S)}$		150	12	-	ns
Min. Clock to Strobe Delay	$t_{D(CS)}$		75	5	-	ns
SERIAL DATA OUT (SO)						
Low Level Output Voltage	V_{OL}	Sink Current = 1.6mA	-	0.2	0.4	V
High Level Output Voltage	V_{OH}	Source Current = -1.6mA	3.7	4.4	-	V
Propagation Delay	$t_{P(CD)}$		75	260	-	ns

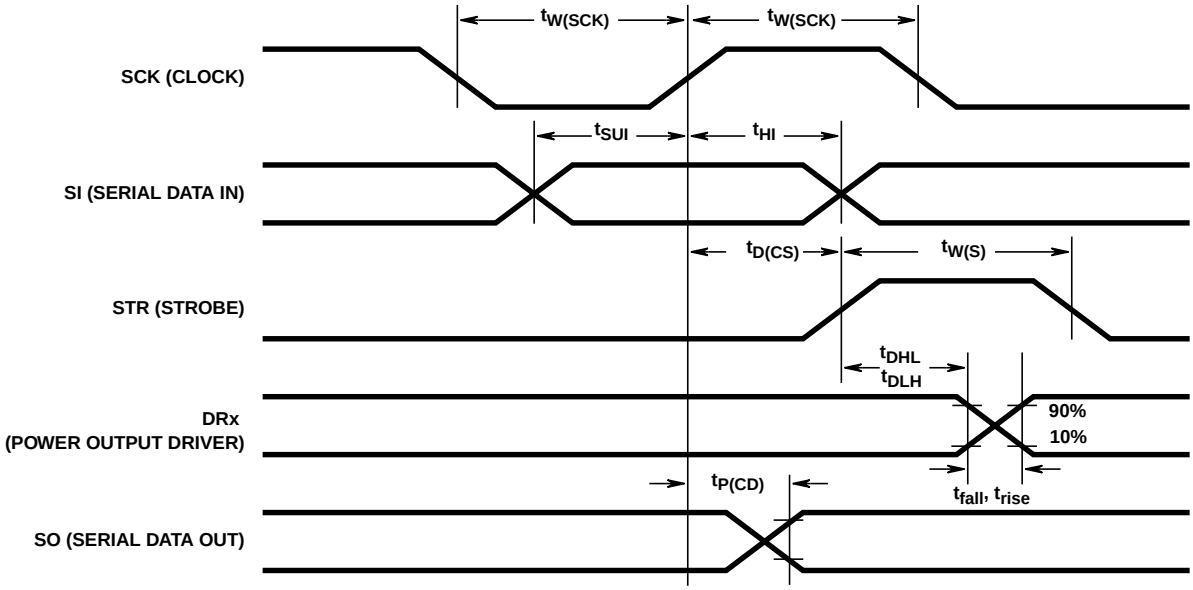


FIGURE 1. LOGIC TIMING CONTROL SPECIFICATIONS

Pin Descriptions

V_{CC} - Logic Power Supply

The V_{CC} pin is the positive 5V logic voltage supply input for the IC. The normal operating voltage range is 4.5 to 5.5V. When switched on, the POR forces all outputs off.

SCK - Serial Clock

SCK is the clock input for the SPI interface. Output ON/OFF control data is clocked into an eight stage shift register on the rising edge of an external clock. This input has a Schmitt trigger.

SI - Serial Data In

SI is the Serial Data Input pin for the SPI interface. The eight Power Outputs are controlled by the serial data via the Output Data Buffer. This input has a Schmitt trigger.

STR - Strobe for the SPI Interface

When the STR pin is high, data from the 8-bit shift register is passed into the Output Data Buffers where it controls the ON-OFF state of each output driver. The data is latched in the Output Data Buffers on the trailing edge of the STR pulse. This input has a Schmitt trigger.

SO - Serial Data Out

The Serial Data Out allows other ICs to be serially cascaded. For example, a 10-bit LED driver may be located behind the HIP0051. A controlling microprocessor may then clock out 18 bits of information and simultaneously strobe both parts. The cascaded ICs may be the same or different from the HIP0051.

DR0 to DR7 - Outputs 0 Thru 7

The Drain Output pins of the DMOS Power Drivers are capable of sinking 250mA.

$\overline{EN}$ - Enable

The Enable pin is an active low enable function for all eight output drivers. When $\overline{EN}$ is high, drive from the Output Data Buffer is held low and all output drivers are disabled. When $\overline{EN}$ is low, the output drivers are enabled and data in the 8-bit shift register is transparent to the Output Data Buffer. This input has a Schmitt trigger.

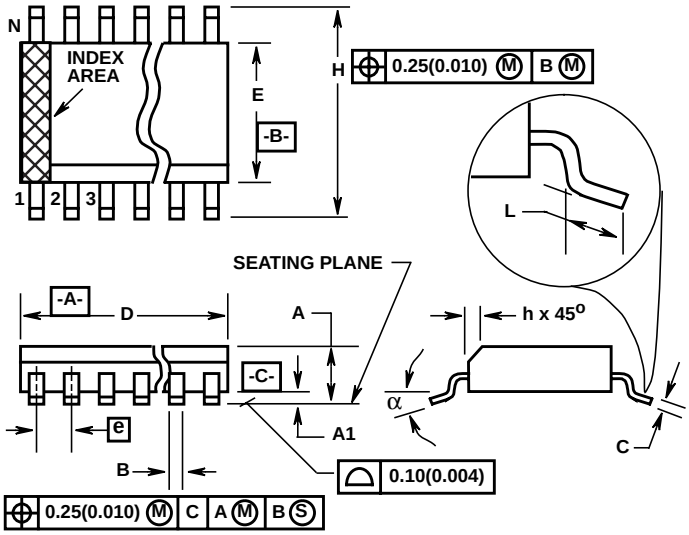
LGND and GND - Ground

LGND is the logic input power supply ground pin. The GND pins are common grounds for the Power Output Drivers. The power supplies for the logic and power circuits require a common ground. To minimize ground bounce at the logic input, the external ground return path for the GND pin should be separate from the LGND pin. LGND and GND have common substrate ground connections on the chip.

OUTPUT CONTROL TABLE

STROBE	8-BIT SERIAL DATA (LATCHED)								OUTPUT							
⎍	D1	D2	D3	D4	D5	D6	D7	D8	DR1	DR2	DR3	DR4	DR5	DR6	DR7	DR8
⎍	0	0	0	0	0	0	0	0	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
⎍	1	0	0	0	0	0	0	0	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
⎍	1	1	0	0	0	0	0	0	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF
⎍	1	1	1	0	0	0	0	0	ON	ON	ON	OFF	OFF	OFF	OFF	OFF
⎍	1	1	1	1	0	0	0	0	ON	ON	ON	ON	OFF	OFF	OFF	OFF
⎍	0	0	0	0	1	1	1	1	OFF	OFF	OFF	OFF	ON	ON	ON	ON
⎍	1	1	1	1	1	1	1	1	ON	ON	ON	ON	ON	ON	ON	ON

Small Outline Plastic Packages (SOIC)



M20.3 (JEDEC MS-013-AC ISSUE C)
20 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4961	0.5118	12.60	13.00	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
α	0^o	8^o	0^o	8^o	-

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NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.