82C435 ENHANCED GRAPHICS CONTROLLER
82A436 BUS INTERFACE

- **100% hardware and software compatible to IBM Enhanced Graphics Adapter™ card**
- **Backward compatible to IBM Color Graphics™, IBM Monochrome™ and Hercules™ adapters**
- **Reduces the chip-count for an EGA implementation to 13 standard components, including 256 Kbytes of display memory**
- **Hardware support for context switching in windowing and multi-tasking environments**
- **Smart Auto-Emulation adjusts automatically to display mode required by application software**
- **Improved CPU access to display memory, allowing up to two times faster performance over IBM EGA without software changes**
- **Supports 640 × 480 resolution. 38 MHz options supports 800 × 600 resolution**
- **BIOS and software drivers for 640 × 480 resolution and 800 × 600 resolution available**

The 82C435 Graphics Controller and 82A436 Bus Interface offer a complete, highly integrated solution for implementing an IBM Enhanced Graphics Adapter compatible controller, with backward compatibility to CGA, IBM Monochrome, and Hercules modes. A complete EGA, with backward compatibility can be implemented using a total of 13 off-the-shelf components, including 256K bytes of display memory.

82C435 Graphics Controller

The 82C435 single-chip graphics controller integrates the functions of the four-chip CS8240 CHIPSet (82C431 Graphics Controller, 82C432A Sequencer, 82C433 Attributes Controller, and 82C434A CRT Controller) with additional support logic and registers for backward compatibility to CGA, Hercules and IBM Monochrome modes.

The 83C435 is packaged in an 84-pin PLCC.

82A436 Bus Interface

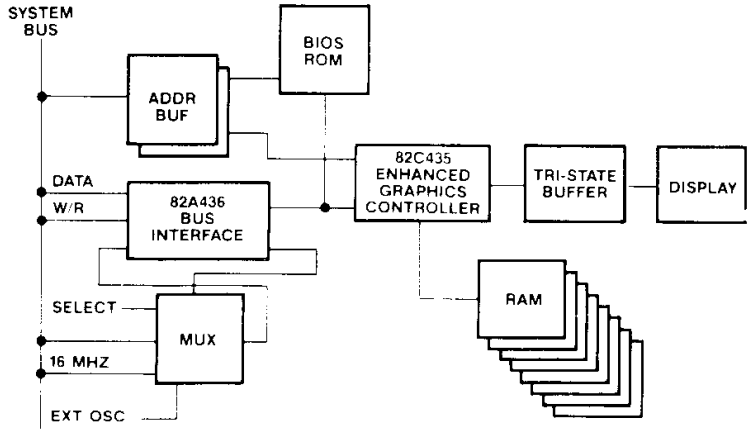
The 82A436 Bus Interface provides bus interface, memory select and I/O select logic functions. The 82A436 is a bipolar device and is packaged in a 68 pin PLCC.

Backward Compatibility/Smart Auto-Emulation

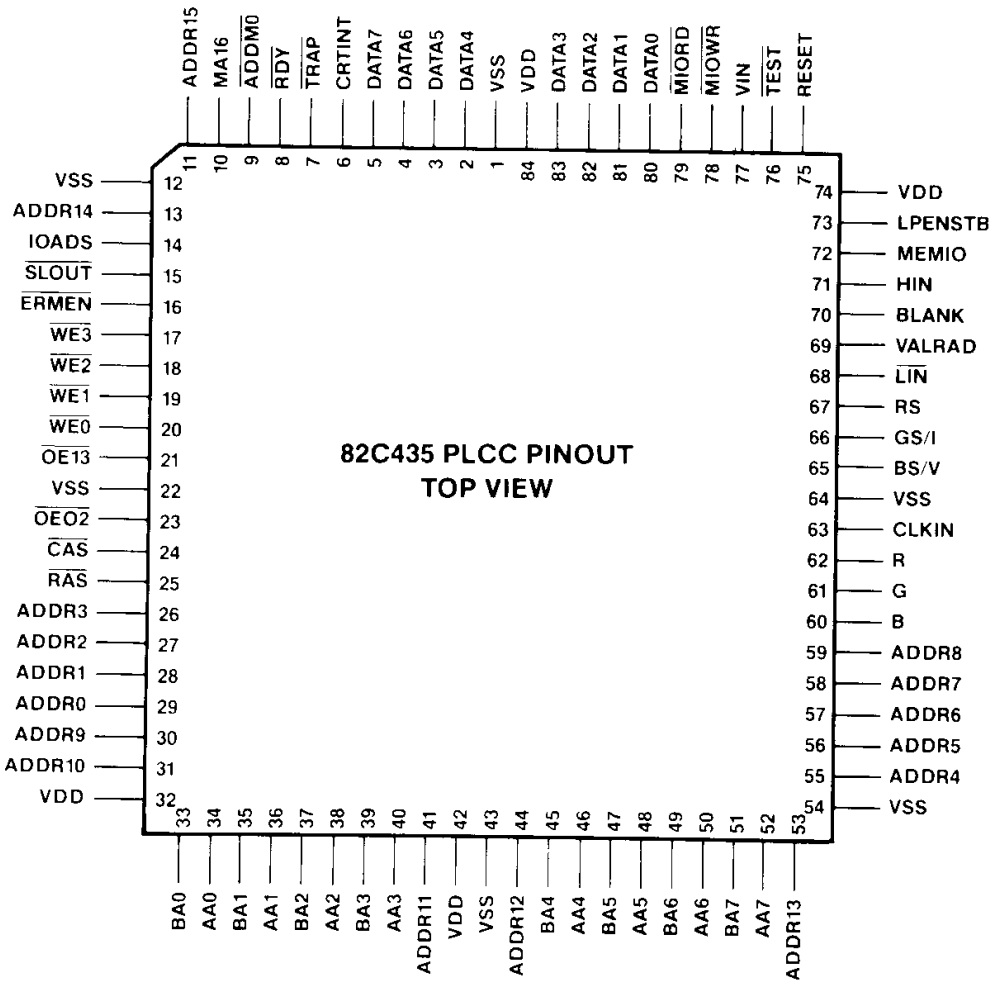
The 82C435 supports backward compatibility on-chip to CGA, IBM Monochrome and Hercules modes. It also supports Smart Auto-Emulation which automatically adjusts to the graphics mode required by the application software. The 82C435 provides enhanced performance to CGA modes by displaying CGA text in EGA resolution.

Hardware Support for Context Switching

For support of multitasking and windowing environments, the entire state of the 82C435/82A436 (most registers and latches in the 82C435/82A436) is readable and writable.



82C435/82A436 EGA System Diagram



82C435 Pin Description

Pin No. PLCC	Type	Symbol	Description
29	I	ADDR0	
28	19	I	ADDR2
26	I	ADDR1	
27	I	ADDR3	
55	I	ADDR4	
56	I	ADDR5	
57	I	ADDR6	
58	I	ADDR7	SYSTEM ADDRESS bits 0-15. These bits are used for addressing the display memory.
59	I	ADDR8	
30	I	ADDR9	
31	I	ADDR10	
41	I	ADDR11	
44	I	ADDR12	
53	I	ADDR13	
13	I	ADDR14	
11	I	ADDR15	
80	I/O	DATA0	
81	I/O	DATA1	
82	I/O	DATA2	SYSTEM DATA BUS bits 0-7. These bits are used to transfer data to and from the CPU data bus. These are open drain outputs and must have external pull up resistors.
83	I/O	DATA3	
2	I/O	DATA4	
3	I/O	DATA5	
4	I/O	DATA6	
5	I/O	DATA7	
10	I	MA16	Buffered MA16 input from the 82A436; derived from the CPU address.
63	I	CLKIN	DOT CLOCK INPUT. CLKIN is the clock input from an external multiplexer (LS153). CLKSEL0 and CLKSEL1 (bits 2 and 3 of the Miscellaneous Output Register) determine which frequency is used: 14.317 MHz, 16.25 MHz (up to 25MHz) external crystal or external oscillator (up to 25MHz).
9	I	$\overline{\text{ADDM0}}$	Active Low Decoded input (from the 82A436) for the three upper system address bus bits to address the display memory at locations AXXXX and BXXXX. Low when A19-A17 = 101.
79	I	$\overline{\text{MIORD}}$	MEMORY I/O READ. $\overline{\text{MIORD}}$ is an active low input from 82A436 for memory or I/O read operations.
78	I	$\overline{\text{MIOWR}}$	MEMORY I/O WRITE. $\overline{\text{MIOWR}}$ is an active low input from 82A436 for all memory or I/O write operations.
72	I	MEMIO	MEMORY I/O. MEMIO is a control signal from 82A436: 0 = memory; 1 = I/O.

82C435 Pin Description (Continued)

Pin No. PLCC	Type	Symbol	Description
75	I	RESET	RESET is an active high input from the system bus used to reset the CRT Controller Registers as follows: a. It initializes the horizontal and vertical polarity control to logical 0. b. Mode Register bits 4 and 7 are reset. c. All counters in the CRT Controller Registers are reset. d. Address Register bits 3 and 4 are reset. e. Hercules configuration switch (I/O address 3BF) bits 0 and 1 are reset. All other control registers remain unchanged. RESET must be active for at least 64 dot clocks.
73	I	LPENSTB	LIGHT PEN STROBE. LPENSTB is an input from the 82A436. It latches the current address being displayed into the light pen register on a low to high transition.
14	I	IOADS	I/O ADDRESS. IOADS selects the I/O address to the CRT Controller. 0 = 2XX, 1 = 3XX.
68	I	$\overline{\text{LIN}}$	LINEAR ADDRESSING INPUT. When $\overline{\text{LIN}}$ = 1, the 82C435 works in the normal mode (index addressing) for normal EGA operation. When $\overline{\text{LIN}}$ = 0, the address bus points to the register location and I/O writes and reads ($\overline{\text{MIOWR}}$ and $\overline{\text{MIORD}}$) can be performed in one operation.
76	I	$\overline{\text{TEST}}$	$\overline{\text{TEST}}$ = 0 sets the vertical retrace counter to the complement of the contents of the Vertical Retrace Start Register (CR10) at the end of the current scan line. $\overline{\text{TEST}}$ = 1 allows normal operation.
62 61 60 67 66 65	O O O O O O	R G B RS GS/I BS/V	R, G, B, RS, GS/I, BS/V are the 6 outputs that drive the monochrome or color monitor. R, G, and B are the Red, Green and Blue signals, respectively. The RS, GS/I, and BS/V are the Secondary Red, Secondary Green/Intensity Secondary Blue/Monochrome Video (display) signals.
71	O	HIN	HORIZONTAL SYNC OUTPUT. HIN is active high if horizontal polarity bit (bit 6 of the Miscellaneous Output Register (I/O address 3C2)) is low. It is active low if the horizontal polarity bit is high.
77	O	VIN	VERTICAL SYNC OUTPUT. VIN is active high if the vertical polarity bit (bit 7 of the Miscellaneous Output Register (I/O address 3C2)) is low. It is active low if the vertical polarity bit is high.
70	O	BLANK	BLANK is an active high output for blanking the screen during retrace periods.

82C435 Pin Description (Continued)

Pin No. PLCC	Type	Symbol	Description
15	O	$\overline{\text{SLOUT}}$	ATTRIBUTE SHIFT LOAD. $\overline{\text{SLOUT}}$ is an active low output on the features connector (pin 9). It is used internally by the Attributes Controller in text mode to load parallel data coming in from the display memory.
6	O	CRTINT	CRT INTERRUPT. CRTINT is an active high output signal to the system bus pin IRQ2 (IRQ9), used to signal the CPU that the CRT needs attention. CRTINT is enabled by bit 5 of the Vertical Retrace End Register. It can be cleared by programming bit 4 of the Vertical Retrace End Register to 0. When not active, the CRTINT output is in a tri-state condition.
8	O	$\overline{\text{RDY}}$	READY. $\overline{\text{RDY}}$ is an active low output used by the 82C435 to indicate to the CPU that a data transfer will be completed. $\overline{\text{RDY}}$ becomes inactive as soon as a memory read or a memory write operation is completed. When a read or write operation is completed, the $\overline{\text{RDY}}$ output goes high for one dot clock period, and then goes tri-state. $\overline{\text{RDY}}$ can directly drive the I/OCHRDY on the I/O bus.
7	I/O	$\overline{\text{TRAP}}$	$\overline{\text{TRAP}}$ can be programmed as an output or as an input. As an output this is active low and is used to inform an external processor that some assistance is needed in the Hercules or CGA emulation modes. This pin can directly drive the IOCHCHK line on the PC-AT bus. As an input, this pin when low forces all writes to go to plane 2 only (fonts).
34	I/O	AA0	Multiplexed data/address bus AA0-7 for memory planes 0 and 1.
36	I/O	AA1	
38	I/O	AA2	
40	I/O	AA3	
46	I/O	AA4	
48	I/O	AA5	
50	I/O	AA6	
52	I/O	AA7	
25	O	$\overline{\text{RAS}}$	ROW ADDRESS STROBE. $\overline{\text{RAS}}$ is an active low signal to the display memory. At the falling edge of $\overline{\text{RAS}}$, the row address is present on the AA and BA busses.
24	O	$\overline{\text{CAS}}$	COLUMN ADDRESS STROBE. $\overline{\text{CAS}}$ is an active low signal to the display memory. At the falling edge of $\overline{\text{CAS}}$, the column address is present on the AA and BA busses.
23	O	$\overline{\text{OE02}}$	OUTPUT ENABLE PLANES 0 AND 2. $\overline{\text{OE02}}$ is an active low signal which causes plane 0 and plane 2 data to be read by the 82C435. Plane 0 data is read over the AA bus and plane 2 data is read over the BA bus.
21	O	$\overline{\text{OE13}}$	OUTPUT ENABLE PLANES 1 AND 3. $\overline{\text{OE13}}$ is an active low signal which causes plane 1 and plane 3 data to be read by the 82C435. Plane 1 data is read over the AA bus and plane 3 data is read over the BA bus.

82C435 Pin Description (Continued)

Pin No. PLCC	Type	Symbol	Description
20	O	$\overline{WE0}$	WRITE ENABLE PLANE 0. $\overline{WE0}$ is an active low write enable to display memory plane 0 for memory write operations.
19	O	$\overline{WE1}$	WRITE ENABLE PLANE 1. $\overline{WE1}$ is an active low write enable to display memory plane 1 for memory write operations.
18	O	$\overline{WE2}$	WRITE ENABLE PLANE 2. $\overline{WE2}$ is an active low write enable to display memory plane 2 for memory write operations.
17	O	$\overline{WE3}$	WRITE ENABLE PLANE 3. $\overline{WE3}$ is an active low write enable to display memory plane 3 for memory write operations.
33	I/O	BA0	Multiplexed data/address bus BA0-7 for memory planes 2 and 3.
35	I/O	BA1	
37	I/O	BA2	
39	I/O	BA3	
45	I/O	BA4	
47	I/O	BA5	
49	I/O	BA6	
51	I/O	BA7	
16	O	$\overline{ERMEN}$	EARLY MEMORY ENABLE. $\overline{ERMEN}$ goes low one dot clock before the time slot for a CPU-to-memory read or write access.
69	O	VALRAD	VALID READ ADDRESS. VALRAD is active high when bit 1 (enable RAM) of the Miscellaneous Output Register (I/O address 3C2) is high and one of the following conditions is true: **Bits 3 2 — Valid Address Ranges** 0 0 A0000 for 128K bytes EGA mode 0 1 A0000 for 64K bytes EGA mode 1 0 B0000 for 32K bytes EGA mode, Hercules or Mono emulation for 4K bytes (small memory), or 64K bytes Hercules (large memory) 1 1 B8000 for 32K bytes EGA mode or CGA emulation for 32K bytes (large memory)

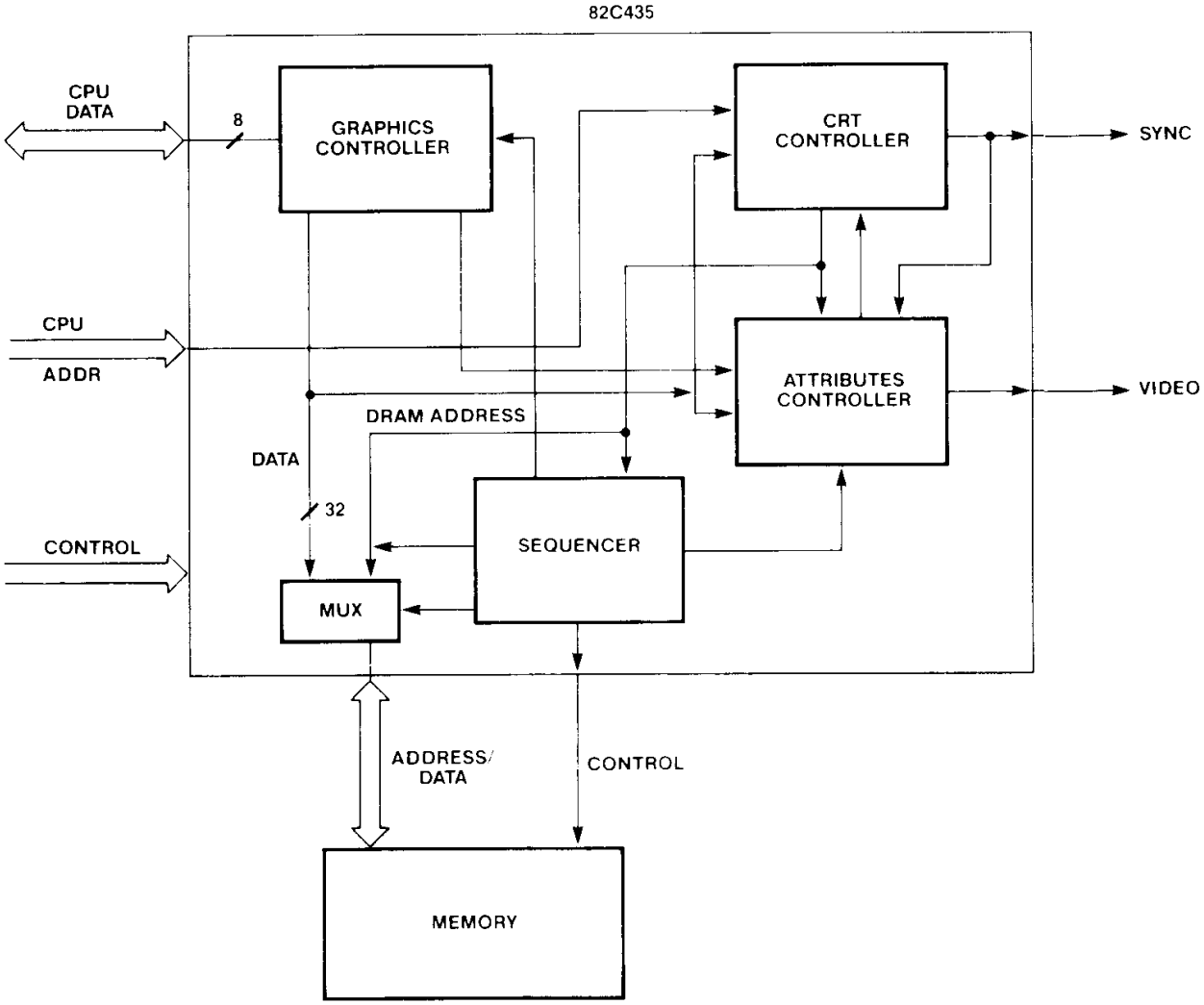


Figure 1. Enchanced Graphics Controller

82C435 FUNCTIONAL DESCRIPTION

The 82C435/82A436 is a complete implementation of the IBM Enhanced Graphics Adapter with improved features. All EGA functions are supported by the 82C435 Single Chip Enhanced Graphics Controller directly in hardware at the register level. The entire EGA display memory of 256 Kbytes is supported using 8 64k*4 DRAM chips. Additionally, the 82C435 allows the CPU more frequent access into the display buffer (memory), which speeds up graphics intensive applications programs by up to two times. This high bandwidth feature is transparent to all applications programs that use the EGA in the standard resolutions of 640*200 or 640*350. No special software drivers are required to enable this feature.

For support of multitasking environments and context switching, the **entire state** of the 82C435/82A436 (most registers and latches in the 82C435/82A436) is readable and writable.

The 82A436 Bus Interface Chip integrates all the external logic required around the 82C435 to implement a EGA/CGA/MDA/ Hercules compatible graphics subsystem. The 82A436 internally decodes all memory and I/O (normal and alternate) addresses used by each of the graphics subsystems.

The 82C435 is an integration of four different modules. These modules are essentially the four chips in the CS8240 EGA CHIPSet 82C431, 82C432, 82C433 and 82C434 with extended functionality. Each of the four modules retains its identity within the 82C435. The four modules are:

a) **Graphics Controller** — The Graphics Controller interfaces the 8 bit CPU data bus to four planes of display memory. It supports different types of pixel/data mappings for read and write operations.

b) **Sequencer** — The Sequencer generates all the timing signals for the 82C435 and the memory control signals for the display memory.

c) **Attributes Controller** — The Attributes Controller generates the video data stream from the font pattern and attribute code in the text mode. Additionally, the Attributes Controller provides a 16/64 color palette (in both the text and graphics modes).

d) **CRT Controller** — The CRT Controller generates all the sync and timing signals for the monitor and also generates the multiplexed display memory row and column addresses for display refresh and CPU access to display memory.

GRAPHICS CONTROLLER

The Graphics Controller is responsible for directing data from the display memory to the Attributes Controller and the CPU. The Graphics Controller operates in two basic modes: Text (Alphanumeric) and Graphics. In the Text Mode, the Graphics Controller fetches the character code and attribute byte from memory, it then fetches the appropriate byte of the character font from the memory based character font table. The font pattern and the attribute byte are then sent to the Attributes Controller. In the Graphics Mode, the Graphics Controller, fetches data for 8 pixels (4 bits/pixel) from display memory and then serially sends each pixel data to the Attributes Controller.

The Graphics Controller formats the data for use in various compatible modes. The Graphics Controller also provides color comparators which can be used in color painting and filling operations. Data can be written to the display memory planes in 32 bit words to expedite fast color presetting of the display areas on the monitor. Logical functions on the chip allow for manipulation of the data before being written to the display memory, allowing the user to implement features such as transparency and overlaying.

The Graphics Controller has two major sections, Graphics A and Graphics B. The Graphics A section normally writes to the display memory planes 0 and 1, and the Graphics B section normally writes to the memory planes

2 and 3. The following description will refer to these two sections as Graphics A and Graphics B.

GRAPHICS CONTROLLER REGISTERS

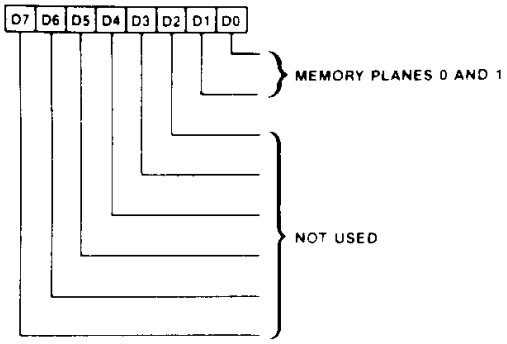
Most Graphics Controller registers are located at two byte addresses in the CPU I/O space. The registers are accessed by first writing a pointer to the actual data register into the Graphics Address Register and then accessing the Graphics Data Register. The Graphics Address Register is located at I/O address 3CEh, and the Graphics Data Registers are all located at I/O address 3CFh. The following table describes the Graphics Registers:

Register Number	Register Name	Address Pointer	Address
—	Graphics A Position	—	3CCh
—	Graphics B Position	—	3CAh
—	Graphics Address	—	3CEh
GR0	Set/Reset	00	3CFh
GR1	Enable Set/Reset	01	3CFh
GR2	Color Compare	02	3CFh
GR3	Data Rotate	03	3CFh
GR4	Read Map Select	04	3CFh
GR5	Graphics Mode	05	3CFh
GR6	Miscellaneous	06	3CFh
GR7	Color Don't Care	07	3CFh
GR8	Bit Mask	08	3CFh
GRF8	Processor Latch 0	F8h	3CFh
GRF9	Processor Latch 1	F9h	3CFh
GRFA	Processor Latch 2	FAh	3CFh
GRFB	Processor Latch 3	FBh	3CFh

REGISTER DESCRIPTION

GRAPHICS A POSITION REGISTER

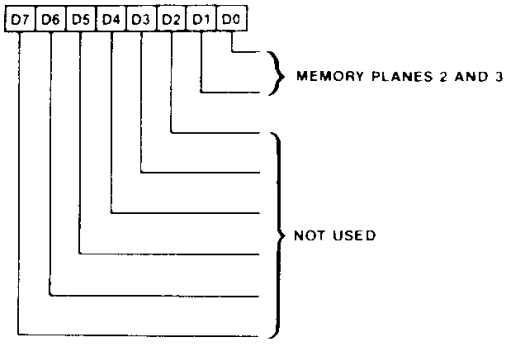
Read-Write Register
I/O Address: 3CCh



The Graphics A Position Register selects the CPU data bus signals and directs them to/from display memory planes 0 and 1. This register should normally be programmed to 00h to select D0 and D1 for display memory planes 0 and 1 respectively.

GRAPHICS B POSITION REGISTER

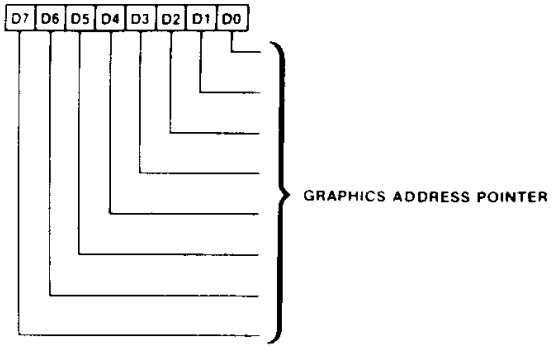
Read-Write Register
I/O Address: 3CAh



The Graphics B Position Register selects the CPU data bus signals and directs them to/from display memory planes 2 and 3. This register should normally be programmed to 01h to select D2 and D3 for display memory planes 2 and 3 respectively.

GRAPHICS ADDRESS REGISTER

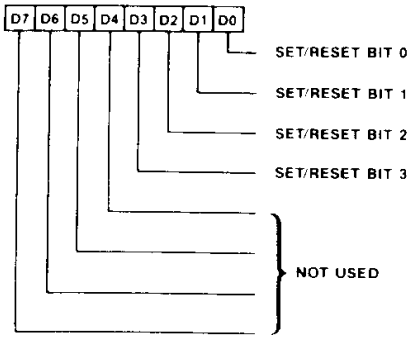
Read-Write Register
I/O Address: 3CEh



The Graphics Address Register is used to point to other registers in the Graphics Controller. The four least significant bits determine the register which will be pointed to in the next register write operation. When this register is read, D5, D6 and D7 are always '1'. D4 is '1' if D5, D6 and D7 were written as 1. D4 is '0' if D5, D6 or D7 were written as '0'.

SET/RESET REGISTER (GR0)

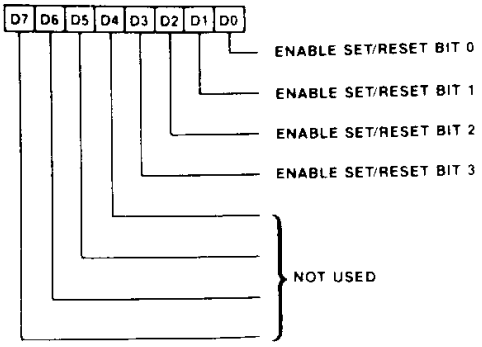
Read-Write Register
I/O Address: 3CFh
Address Pointer: 00



When the Graphics Mode Register selects write mode 0, and the Set/Reset mode is enabled through the Enable Set/Reset Register, bit 0 of this register is written to the entire addressed byte in display memory plane 0. Similarly bits 1, 2 and 3 determine the data to be written into display memory planes 1, 2 and 3 respectively.

ENABLE SET/RESET REGISTER (GR1)

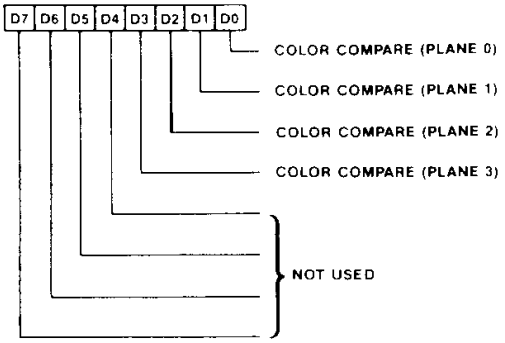
Read-Write Register
I/O Address: 3CFh
Address Pointer: 01



The Enable Set/Reset Register works in conjunction with the Set/Reset Register. If the Graphics Mode Register is programmed to write mode 0, and Set/Reset is enabled (=1), then the contents of the Set/Reset Register determine the data to be written to the respective display memory planes. If write mode 0 is selected and Set/Reset is not enabled (= 0) on a plane, the plane is written with the data from the CPU data bus.

COLOR COMPARE REGISTER (GR2)

Read-Write Register
I/O Address: 3CFh
Address Pointer: 02



If the Graphics Mode Register is set to Read Mode 1, each bit of data read from the display memory planes 0-3 is compared to bits D0 through D3 programmed in the Color Compare Register and the Color Don't Care Register. A match between the memory data and the Color Compare Register (for the bits as specified in the Color Don't Care Register) results in a logical 1 being output on the corresponding data bus bit. Following is an example to illustrate the mechanism:

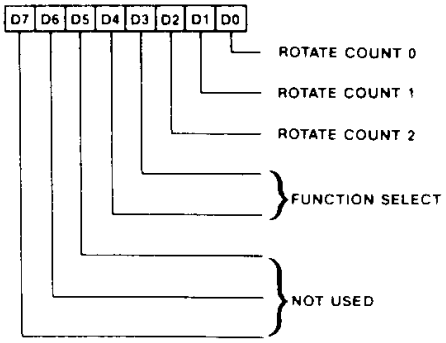
If Color Compare Register = 0011, Color Don't Care = 1111, and:

Plane 0 has data = 11111111
Plane 1 has data = 00000001
Plane 2 has data = 11111110
Plane 3 has data = 00000000

then the data bus D7-D0 will have 00000001, indicating that a match occurred on the bit D0 only.

DATA ROTATE REGISTER (GR3)

Read-Write Register
I/O Address: 3CFh
Address Pointer: 03



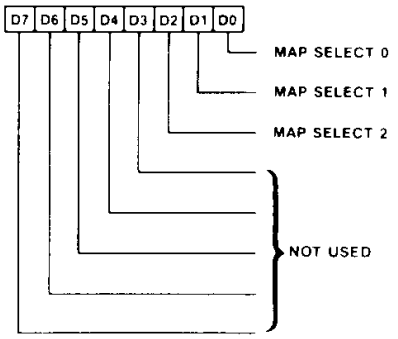
The Data Rotate Register is used to perform a rotate function on the data written by the CPU. If the Graphics Mode Register is programmed for write mode 0, then the value in the Rotate Count Field represents the number of bits the CPU data will be rotated (right) during the CPU write cycles. The CPU data bits are first rotated and then subject to the logical operation as specified in the Function Select Field.

The Function Select bits allow the contents of the processor latches to operate logically upon the CPU data being written into the EGA memory. The bits operate as follows:

D4	D3	
0	0	No change to the Data
0	1	Logical 'AND' between Data and latched data.
1	0	Logical 'OR' between Data and latched data.
1	1	Logical 'XOR' between Data and latched data.

READ MAP SELECT REGISTER (GR4)

Read-Write Register
I/O Address: 3CFh
Address Pointer: 04

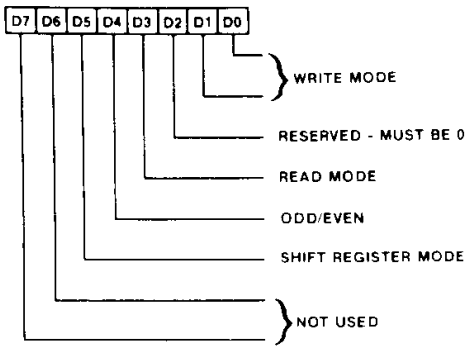


The contents of the Read Map Select Register represent the memory plane from which the CPU reads the data in read mode 0. This register does not effect the read operation performed through the Color Compare Register (read mode 1). The four memory maps are selected as follows:

D2	D1	D0	
0	0	0	Map 0
0	0	1	Map 1
0	1	0	Map 2
0	1	1	Map 3

GRAPHICS MODE REGISTER (GR5)

Read-Write Register
I/O Address: 3CFh
Address Pointer: 05



The function of the bits is as follows:

Write Mode (D0,D1)—Figure 2

D1	D0	
0	0	Each of the four display memory planes is written with the CPU data rotated by the number of counts in the Rotate Register, except when the Set/Reset Register is enabled for any of the four planes. When the Set/Reset Register is enabled, the corresponding plane is written with the data stored in the Set/Reset Register.
0	1	Each of the four display memory planes is written with the data previously loaded in the processor latches. These latches are loaded during all read operations.
1	0	All planes (0-3) in the addressed byte are set to the value of data bus (D0-D3). The data bits are treated as the color value to be written into the eight pixels in the addressed byte. For example, memory plane 0 is set to the value of data bit D0, memory plane 1 is set to the value of data bus bit D1, etc. Individual pixels (all planes) in the addressed byte can be prevented from being updated by appropriately programming the Bit Mask Register.
1	1	Illegal

The operations specified above will also work in conjunction with the Function Select options available through Data Rotate Register.

Read Mode (D3)—Figure 3

D3	
0	When D3 = 0, the CPU reads the data from one of the display memory planes. The exact plane is selected through the Read Map Select Register.
1	When D3 = 1, the CPU reads the result of the logical comparison between the four display memory planes data and the contents of the Color Compare and Color Don't Care Registers.

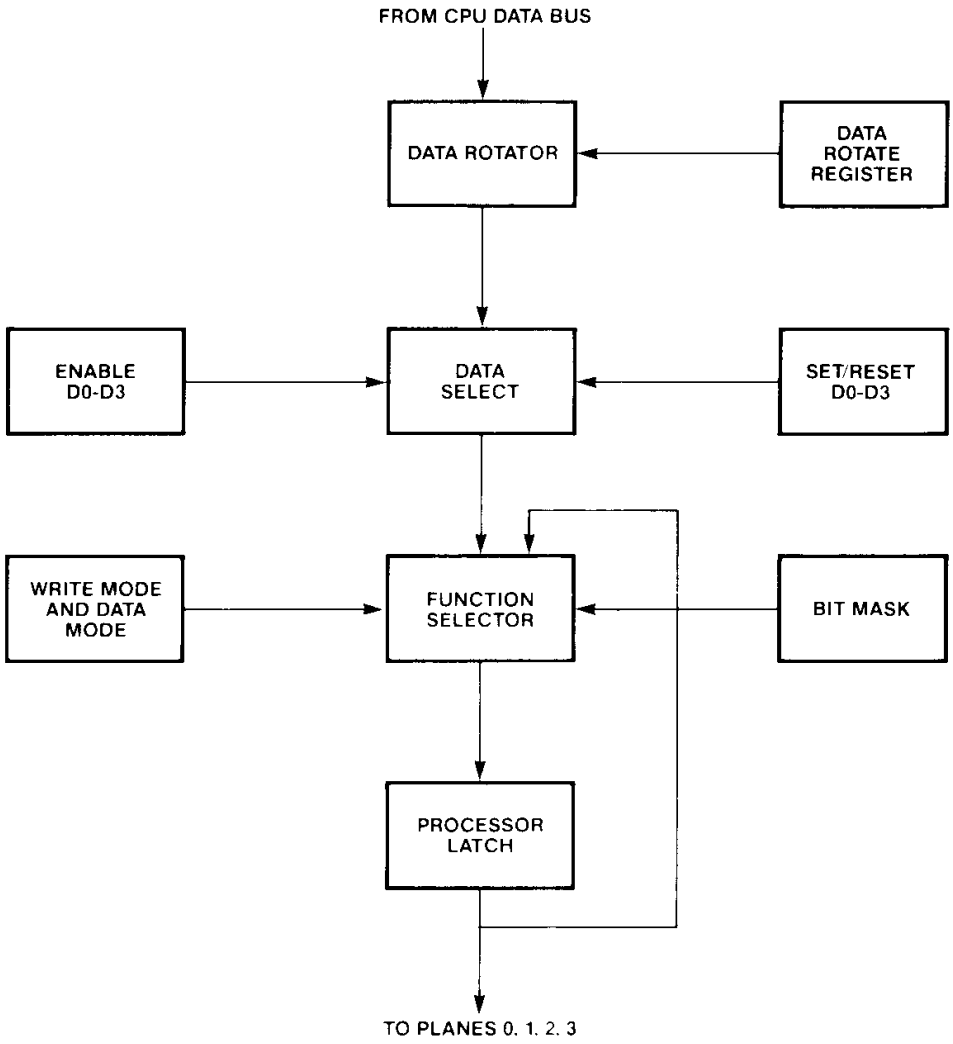


Fig. 2

Odd/Even (D4)

D4 = 1 will put the Graphics Controller in the Odd/Even addressing mode. In this mode, even CPU addresses access planes 0 and 2 while odd CPU addresses access planes 1 and 3. This option is useful for IBM Color Graphics Adapter compatible memory organization. The value of this bit should be the complement of the value programmed in D2 of the Sequencer Memory Mode Register.

Shift Register (D5)

The data bits in the memory planes 0-3 are represented as M0D0-M0D7, M1D0-M1D7, M2D0-M2D7, and M3D0-M3D7, respectively. When D5 = 1, the data in the 4 serial shift registers will be formatted as follows:

MSB							LSB	Output to:
M1D0	M1D2	M1D4	M1D6	M0D0	M0D2	M0D4	M0D6	Bit0
M1D1	M1D3	M1D5	M1D7	M0D1	M0D3	M0D5	M0D7	Bit1
M3D0	M3D2	M3D4	M3D6	M2D0	M2D2	M2D4	M2D6	Bit2
M3D1	M3D3	M3D5	M3D7	M2D1	M2D3	M2D5	M2D7	Bit3

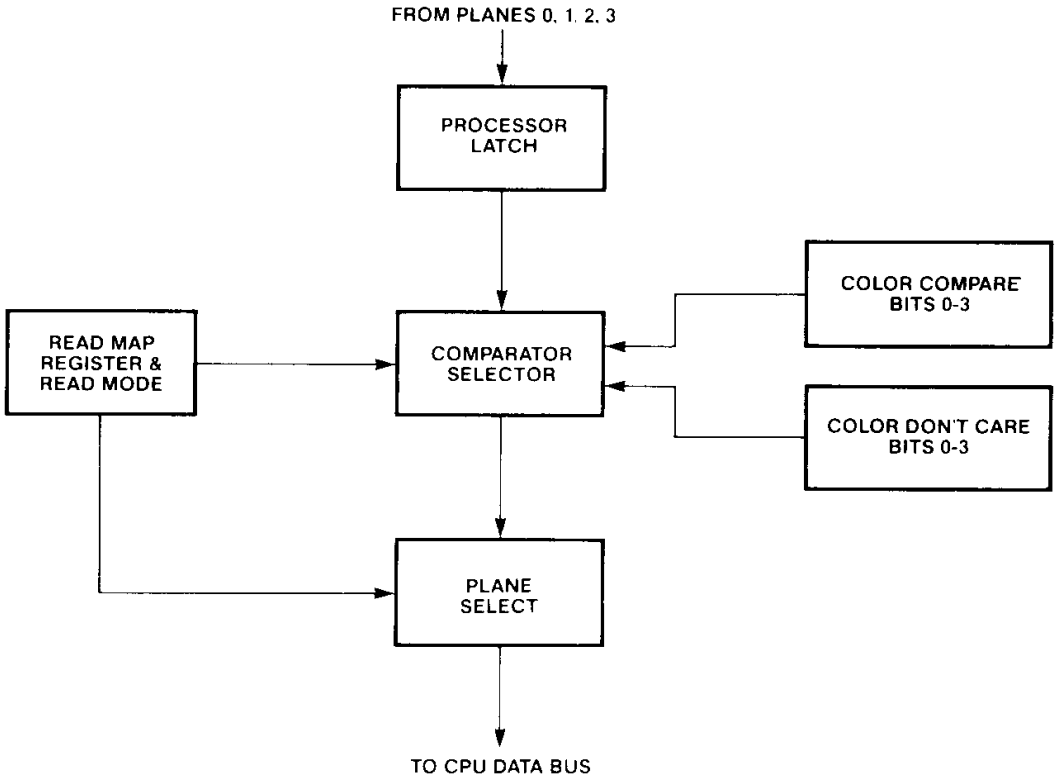


Fig. 3

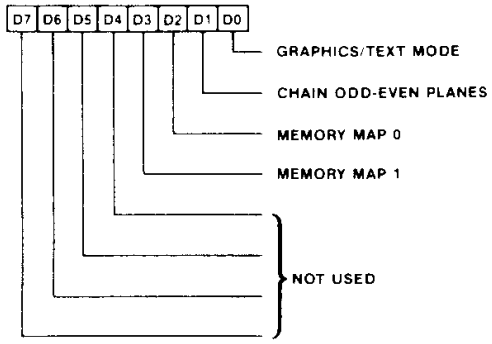
The Least Significant Bit (LSB) is shifted out first. The first two registers correspond to the Graphics A shift registers, while the following two correspond to the Graphics B shift registers. This is normally used for CGA compatible 320*200, 4 color graphics mode.

When D5 = 0, then M0D7-M0D0, M1D7-M1D0, M2D7-M2D0 and M3D7-M3D0 are shifted out with the bit D7 going out first in all cases.

MSB							LSB	Output to:
M0D0	M1D1	M1D2	M1D3	M0D4	M0D5	M0D6	M0D7	Bit0
M1D0	M1D1	M1D2	M1D3	M1D4	M1D5	M1D6	M1D7	Bit1
M2D0	M2D1	M2D2	M2D3	M2D4	M2D5	M2D6	M2D7	Bit2
M3D0	M3D1	M3D2	M3D3	M3D4	M3D5	M3D6	M3D7	Bit3

MISCELLANEOUS REGISTER (GR6)

Read-Write Register
I/O Address: 3CFh
Address Pointer: 06



Graphics/Text Mode

D0 = 1 selects the graphics mode. D0 = 0 selects the text mode.

Chain Odd-Even Planes

When D1 = 1, the CPU address bit A0 is replaced by a higher order address bit. The

contents of A0 determine which memory plane is to be selected. A '0' will select planes 0 and 2, and a '1' will select planes 1 and 3. This mode can be used to have a 128 k byte long display buffer with 2 bits/pixel (monochrome graphics mode).

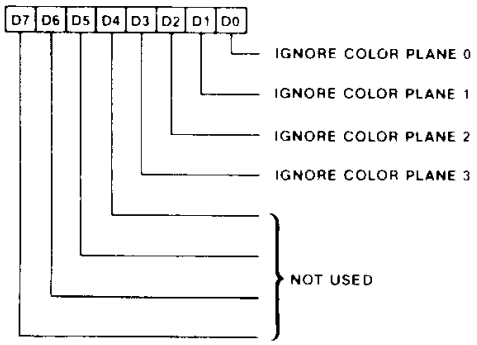
Memory Maps 0 and 1

These bits control the mapping of the display memory buffers into the CPU address space. Bits D3 and D2 are output as CDSEL1 and CDSEL0 signals from the 82C435 (flat pack only). Normally, CDSEL0 and CDSEL1 are not used externally to the 82C435 (in all modes).

D3	D2	
0	0	Address A0000h-BFFFFh
0	1	Address A0000h-AFFFFh
1	0	Address B0000h-B7FFFh/BFFFFh-used in Hercules emulation
1	1	Address B8000h-BFFFFh-used in CGA emulation

COLOR DON'T CARE REGISTER (GR7)

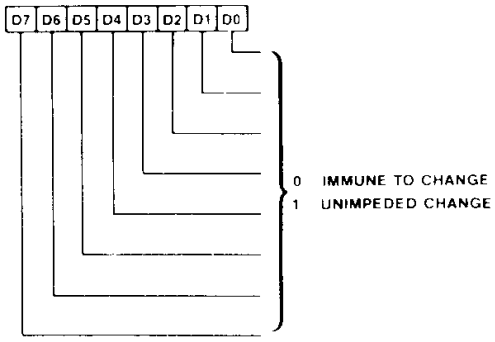
Read-Write Register
I/O Address: 3CFh
Address Pointer: 07



Any bit in the Color Don't Care Register that is set to 0 indicates that the corresponding bit in the Color Compare Register is a don't care in read mode 1. Any bit set to 1 enables the corresponding bit in the Color Compare Register.

BIT MASK REGISTER (GR8)

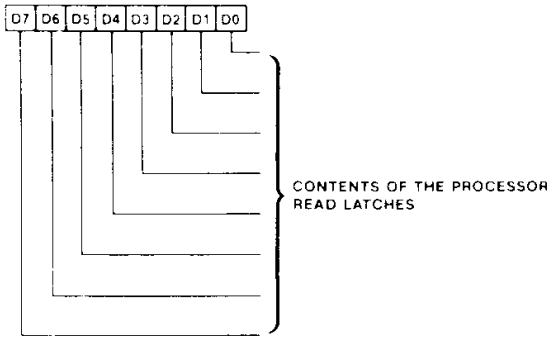
Read-Write Register
I/O Address: 3CFh
Address Pointer: 08



Any bit programmed to 0 in the Bit Mask Register will cause the corresponding bit in each of the four memory planes to be immune to change. The data written into these memory bits is the data stored in the processor latches on the chip. Any bit programmed to 1 will allow unrestricted manipulation of the corresponding bit in each of the four memory planes. The bit mask is applicable to any data written by the CPU, including rotate, logical functions (AND, OR, XOR), Set/Reset and No Change. The data to be preserved using the bit mask must be latched by reading the addressed byte. In order to execute a proper read-modify-write cycle into memory, each byte must first be read, the Bit Mask Register set and the new data is then written. The bit mask applies to all the four planes simultaneously.

PROCESSOR LATCH REGISTERS (GRF8-GRFB)

Read Only Register
I/O Address: 3CFh
Address Pointer: F8h-FBh



There are four byte-wide latches inside the 82C435. These latches are set whenever the CPU reads the display memory. The contents of these latches are subsequently used for the logical operations in the CPU write cycles. In order to completely determine the context of the 82C435, these latches can be read by the CPU as four byte-wide registers in the Graphics Controller address space. The registers at offset F8h-FBh reflect the contents of the latches for planes 0-3 respectively. In order to restore the processor latches, the CPU should first transfer the old contents of the processor latches to some address in memory and then read the same address.

SEQUENCER

The Sequencer generates memory timings for the display RAMs and the character clock

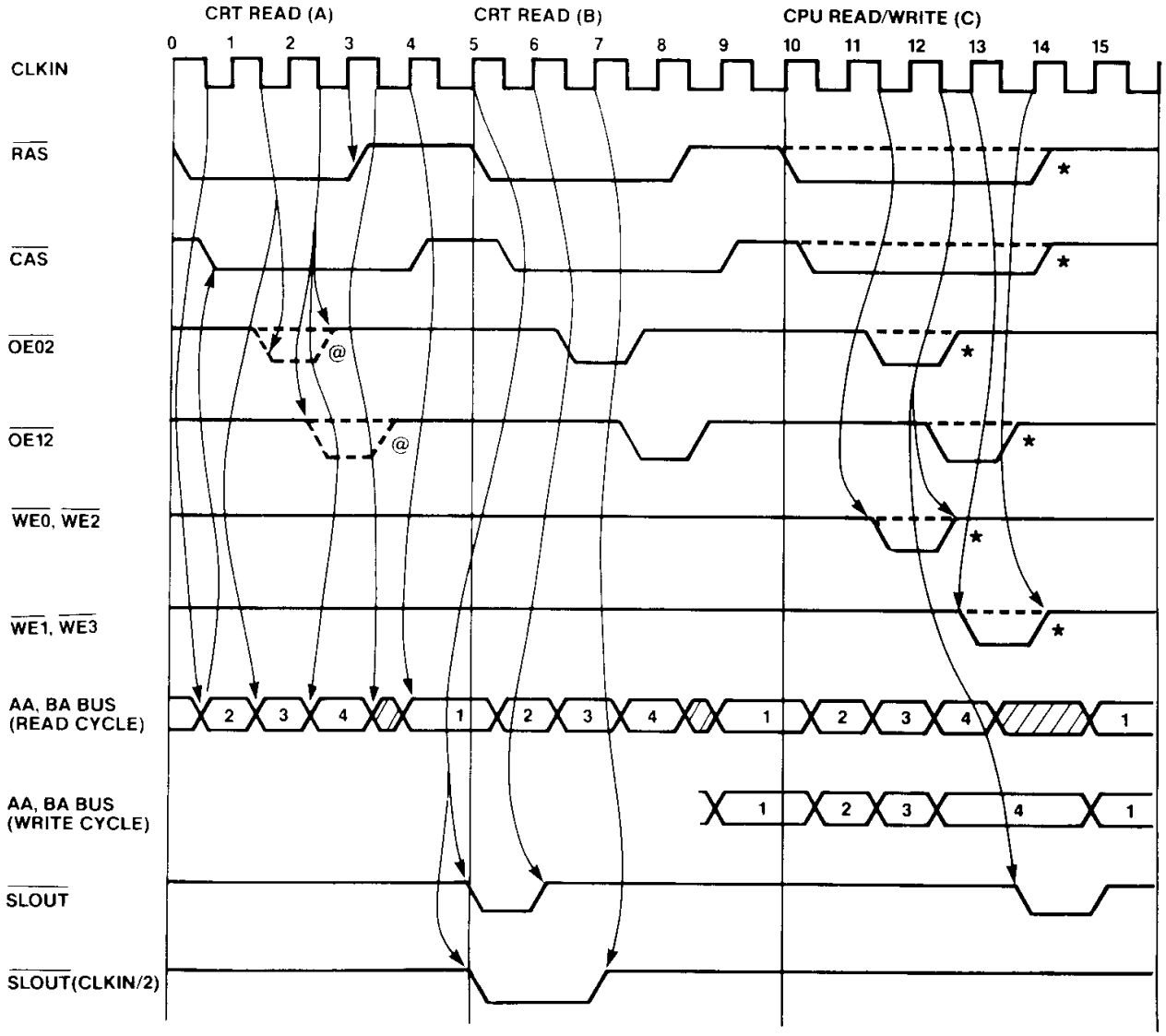
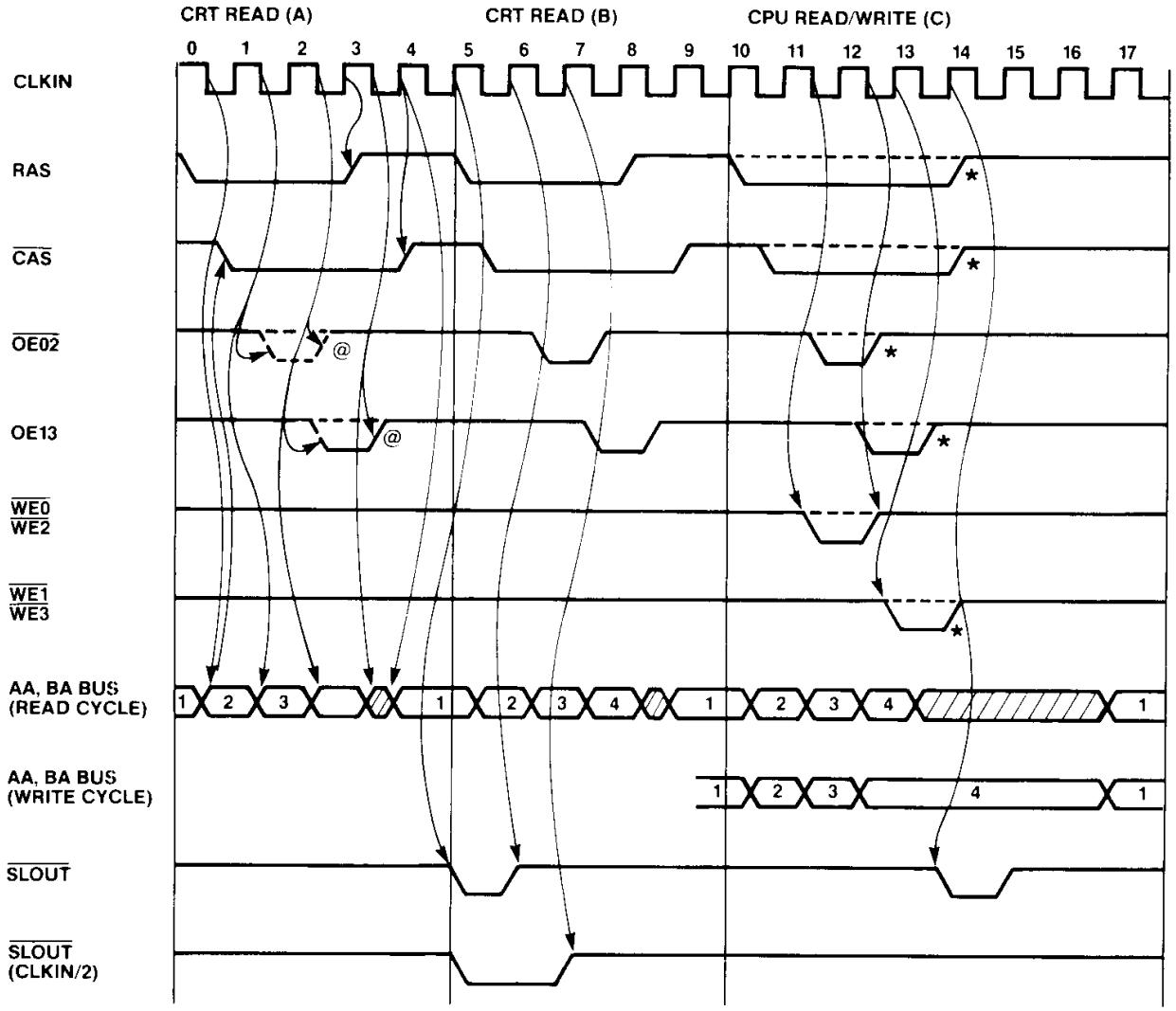


Figure 4. Memory Cycle Division for High CPU Bandwidth Mode (SR1-D5=0), 8 Dots/Character



@ NOE_x ACTIVE DURING CRT READ CYCLE A ONLY FOR HIGH CRT BANDWIDTH MODE (SR0-D1=0)
★ONLY ACTIVE FOR VALID CPU/MEMORY READ/WRITE CYCLES

1. RAS ADDRESS
2. CAS ADDRESS
3. DATA 0, 2
4. DATA 1, 3

Figure 5. Memory Cycle Division for High CPU Bandwidth Mode (SR1-D5=0), 9 Dots/Character

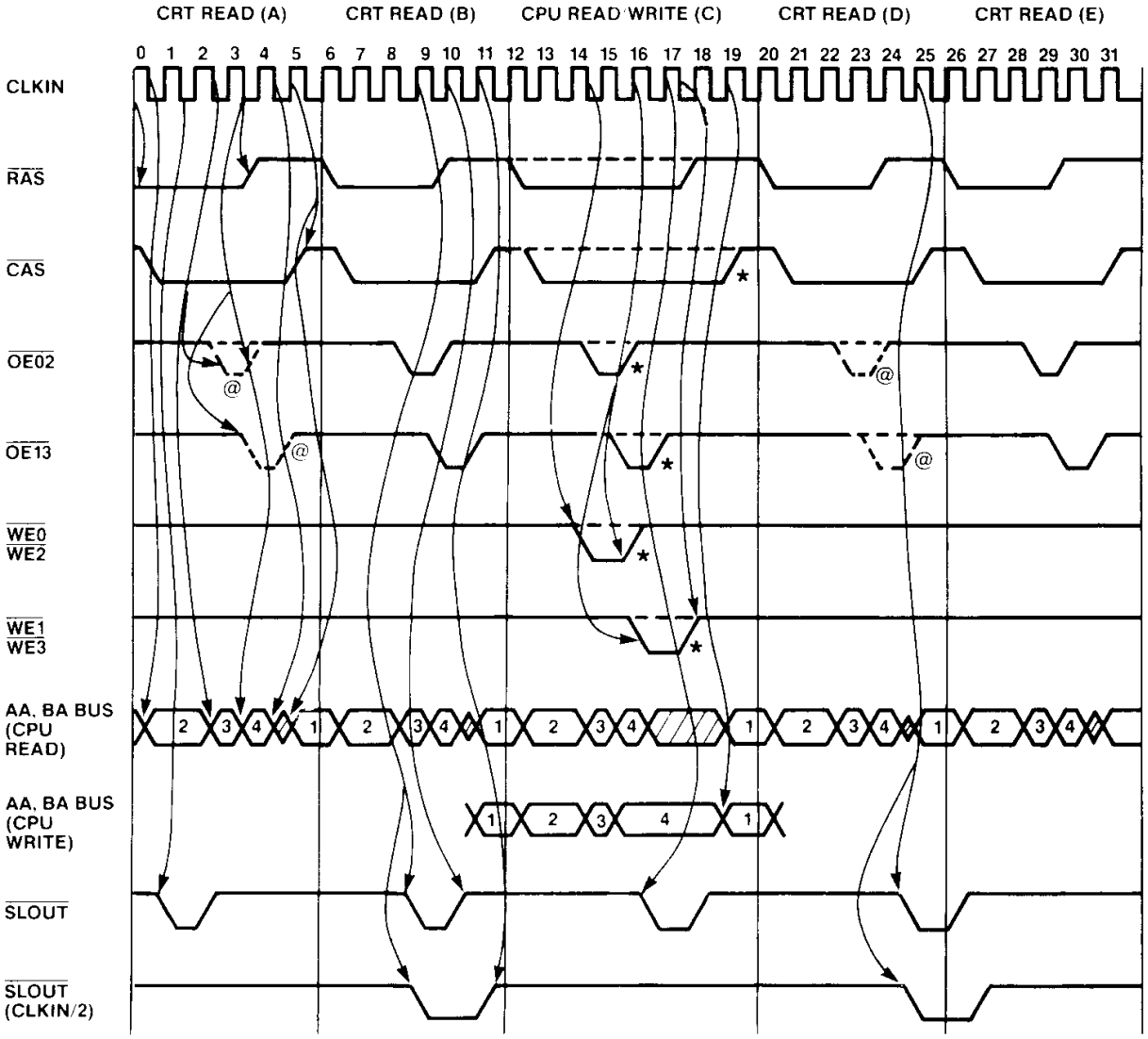
for controlling the regenerative memory fetches. The Sequencer provides control signals for other modules in the 82C435. It also allows the CPU to access memory during active display intervals by inserting dedicated CPU memory cycles. Figures 4, 5, 6 and 7 illustrate various memory cycles for different configurations. As shown in the figures, the memory cycle selection allows different screen resolutions. The Sequencer also protects the entire memory from being altered, by selectively masking out planes through the configurable Mask Register. Figure 8 shows the memory control signals for the four memory planes.

SEQUENCER REGISTERS

The Sequencer Registers are all located at two byte addresses in the CPU I/O space. The registers are accessed by first writing a pointer to the actual data register into the

Sequencer Address Register and then accessing the Sequencer Data Register. The Sequencer Address Register is located at I/O address 3C4h. The Sequencer Data Registers are all located at I/O address 3C5h. The following table describes the Sequencer Registers:

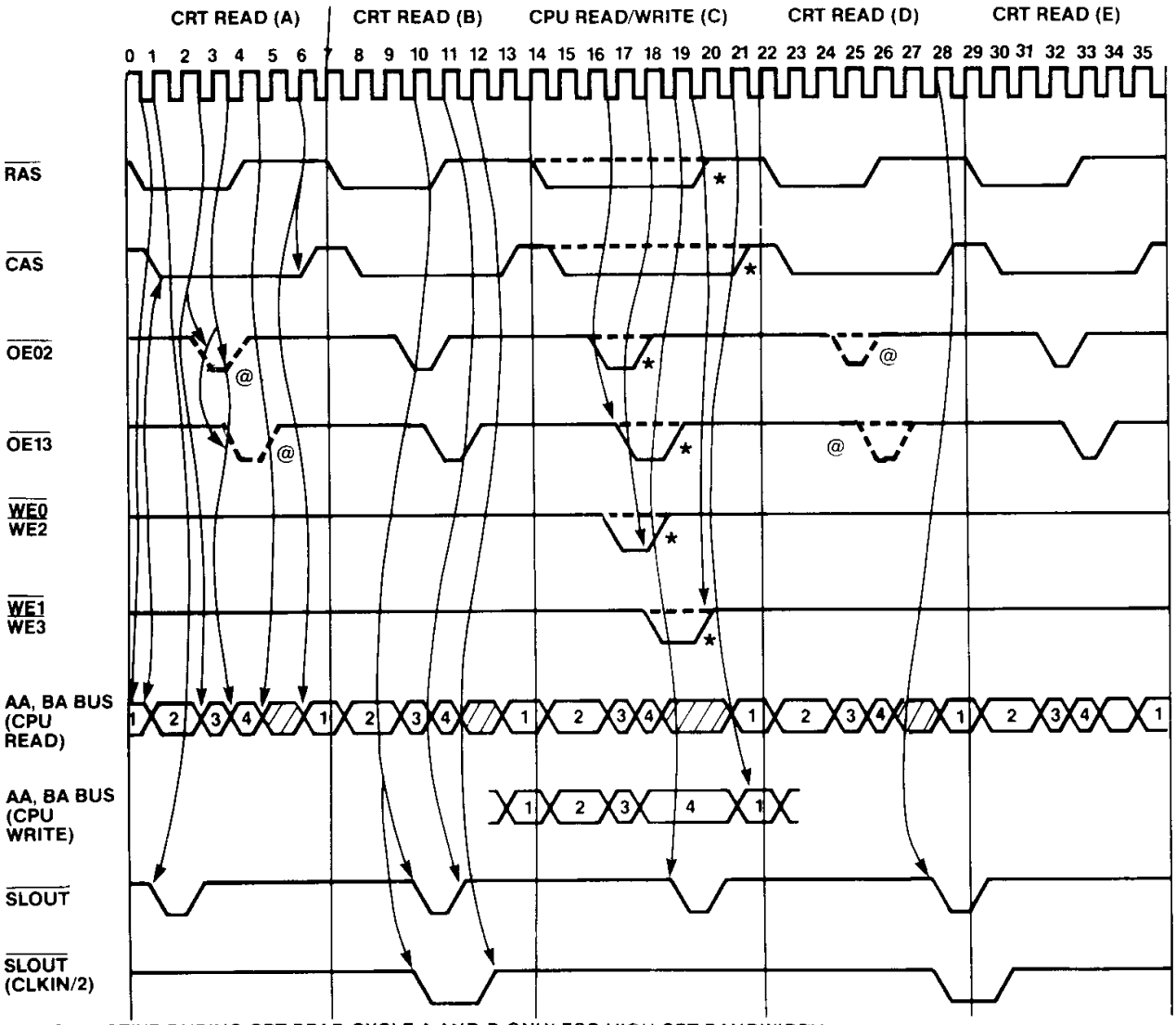
Register Number	Register Name	Address Pointer	Address
	Address	—	3C4h
SR0	Reset	00	3C5h
SR1	Sequencer Clocking Mode	01	3C5h
SR2	Plane Mask (Map Mask)	02	3C5h
SR3	Character Map Select	03	3C5h
SR4	Sequencer Memory Mode	04	3C5h



@ NOE_x ACTIVE DURING CRT READ CYCLE A AND D ONLY FOR HIGH CRT BANDWIDTH MODE (SR0-D1 0)
★ ONLY ACTIVE FOR VALID CPU/MEMORY READ/WRITE CYCLES

1. RAS ADDRESS
2. CAS ADDRESS
3. DATA 0, 2
4. DATA 1, 3

Figure 6. Memory Cycle Division for Low CPU Bandwidth Mode (SR1-D5=0), 8 Dots/Character



@ NOE$_x$ ACTIVE DURING CRT READ CYCLE A AND D ONLY FOR HIGH CRT BANDWIDTH MODE (SR0-D1=0)
★ONLY ACTIVE FOR VALID CPU/MEMORY READ/WRITE CYCLES

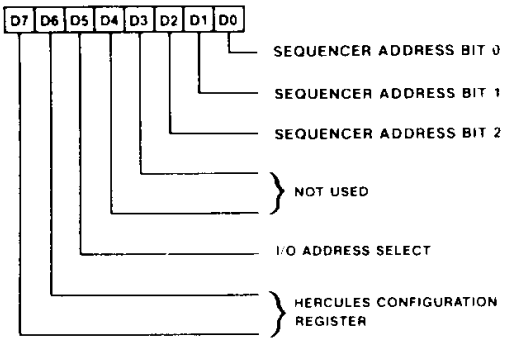
1. RAS ADDRESS
2. CAS ADDRESS
3. DATA 0, 2
4. DATA 1, 3

Figure 7. Memory Cycle Division for Low CRT Bandwidth Mode (SR1-D5=0), 9 Dots/Character

SEQUENCER REGISTER DESCRIPTION

ADDRESS REGISTER

Read-Write Register
I/O Address: 3C4h



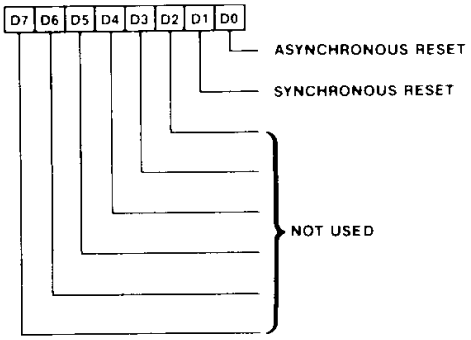
The Address Register is a three bit write-only register. When loaded with a binary value (pointer), it points to the data register where data is to be accessed.

D5 is a secondary read location for the I/O address select bit of the EGA Miscellaneous Output Register (I/O address 3C2h).

D6 and D7 are the read locations for the Hercules Configuration Register (bits D0 and D1 at I/O address 3BFh).

RESET REGISTER (SR0)

Read-Write Register
I/O Address: 3C5h
Address Pointer: 00



Asynchronous Reset

D0=0 causes the Sequencer to clear asynchronously and halt. It also places all the outputs (except R, G, B, RS, GS/I, BS/V) in a high impedance state. D0=1 causes the Sequencer to run unless D1=0 (Synchronous Reset). Asynchronous Reset can cause data loss in the dynamic display RAMs.

Synchronous Reset

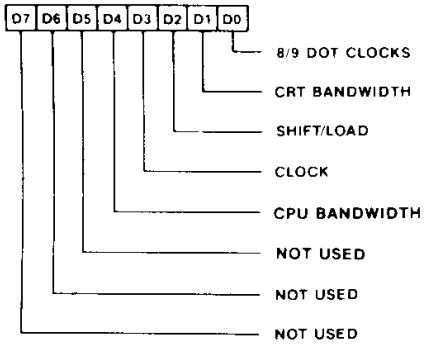
D1=0 causes the Sequencer to clear synchronously and halt. D1=1 causes the Sequencer to run unless D0 (Asynchronous Reset) is cleared to zero.

Before changing the Clocking Mode Register, the Sequencer should be reset with this bit. This will preserve the memory contents.

Both the Reset bits must be a logical 1 to allow the Sequencer to operate.

SEQUENCER CLOCKING MODE REGISTER (SR1)

Read-Write Register
I/O Address: 3C5h
Address Pointer: 01



The description for the individual bit fields is as follows:

D0 8/9 Dot Clocks: D0=0 causes the Sequencer to generate character clocks which are 9 dots wide. D0=1 causes the Sequencer to generate character clocks which are 8 dots wide. The only mode that uses 9 dots wide character clocks is the monochrome text mode. The resolution for this mode is 720 x 350. All other modes use 8 dots wide character clocks.

D1 CRT Bandwidth: D1=1 makes CRT memory accesses for the low resolution modes (horizontal resolution of 320 pixels). D1=0 must be programmed for all higher resolution modes (horizontal resolution of 640 or 720 pixels).

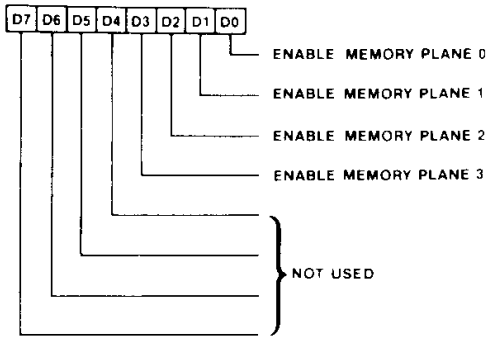
D2 Shift/Load: D2=0 causes the display serializers in the Graphics Controller to

be reloaded every character clock. D2=1 causes the display serializers to be reloaded every other character clock. This mode is useful when 16 bits are fetched every memory cycle and chained together in the shift registers. This bit is only set for APA (all-points-addressable) graphics modes.

D3 Dot Clock: D3=0 selects the Sequencer master clock input to be output on the Dot Clock output pin. D3=1 causes the master clock to be divided by 2 to generate the dot clock. As the Dot Clock is the primary clock used by the 82C435, all other timings will be stretched as they are derived from the Dot Clock. Dot Clock divided by 2 is used for 320 x 200 modes.

D4 CPU Bandwidth: D4=0 allows two CPU accesses into display memory for every four CRTC accesses. This effectively doubles the memory bandwidth available to the CPU. This high speed mode can be used for video clocks up to 20 MHz. Therefore at normal EGA operation (16 MHz video clock), the CPU can update the screen at up to twice the normal speed. At higher video rates, D4 must be set to one, resulting in the normal EGA mode of one CPU memory access for every four CRTC memory accesses. CPU Bandwidth is independent of the CRT Bandwidth (bit D1) of this register.

PLANE MASK REGISTER
(MAP MASK REGISTER SR2)
Read-Write Register
I/O Address: 3C5h
Address Pointer: 02

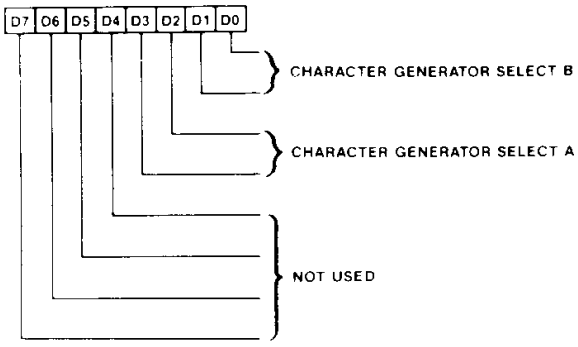


The Plane Mask Register is also referred to in some cases as Map Mask Register. A logical 1 in any of the bits 0 through 3 enables the CPU to write to the corresponding memory planes 0 through 3. A logical 0 in any of the bits disables the CPU to write to the corresponding memory planes by suppressing the $\overline{WE}$ signal to that memory plane. When this register is loaded with 0FH, the CPU can perform a 32-bit write operation in one memory cycle. This substantially reduces the CPU overhead in the CPU in graphics drawing and filling operations.

When odd/even modes are selected (by clearing bit 2 of the Sequencer Memory Mode Register) planes 0, 1 and planes 2, 3 should have the same plane mask value.

In Graphics modes, each pixel consists of four bits. Planes 0-3 contain one bit each from the four bit pixel information. In the Text mode, plane 0 contains the character codes, plane 1 contains the corresponding attribute byte, plane 2 contains the character font (up to four fonts can be stored in plane 2) and plane 3 is not used. Figure 8 represents the memory organization in the two modes.

CHARACTER MAP SELECT REGISTER (SR3)
Read-Write Register
I/O Address: 3C5h
Address Pointer: 03



Character Generator Select B

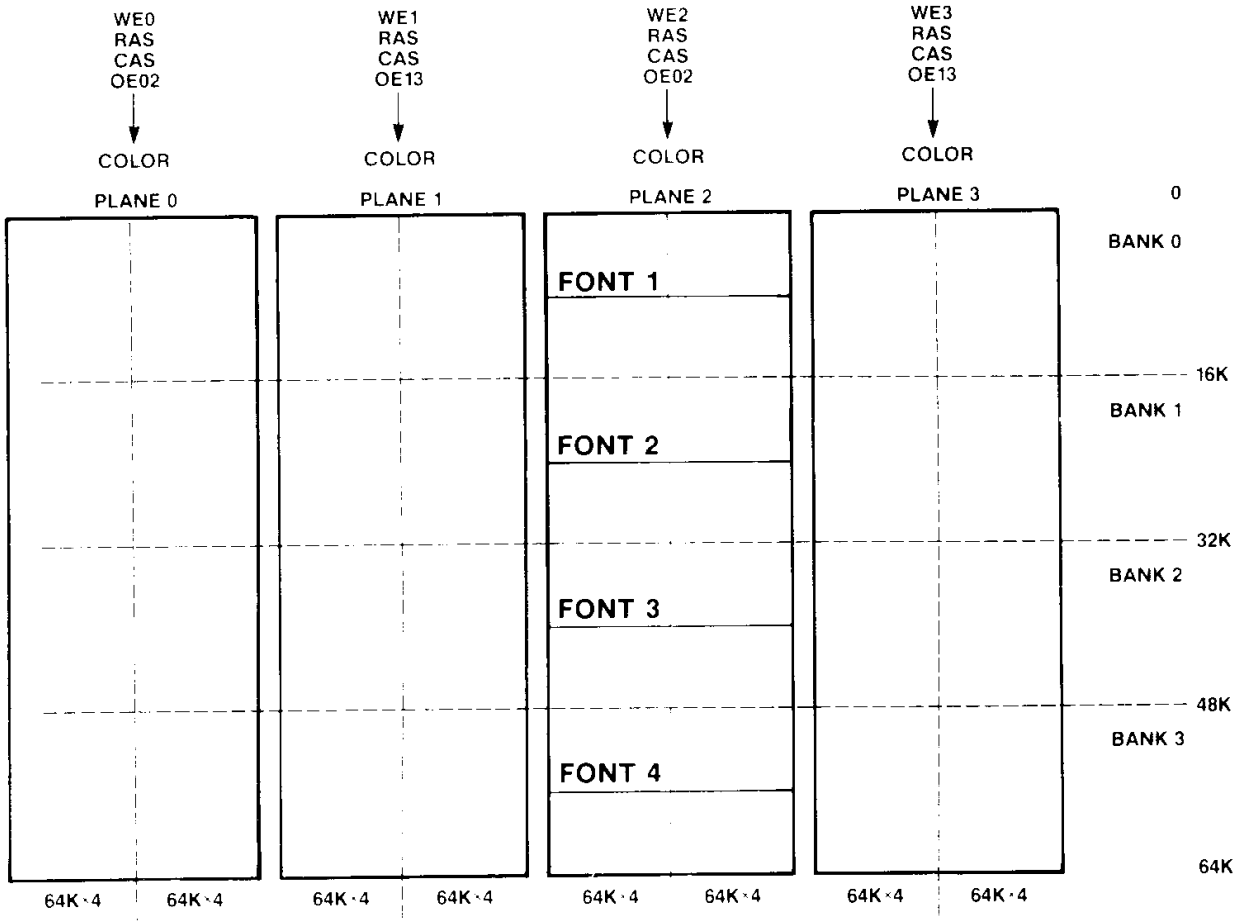
D1-D0 select the character generator used to generate alphanumeric characters when attribute bit 3 is 0 (display memory bit M1D3) according to the following table:

D1	D0	Character Generator	Table Location
0	0	0	First 8K of Plane 2 Bank 0
0	1	1	First 8K of Plane 2 Bank 1
1	0	2	First 8K of Plane 2 Bank 2
1	1	3	First 8K of Plane 2 Bank 3

Character Generator Select A

D3-D2 select the character generator used to generate alphanumeric characters when attribute bit 3 is a 1, according to the following table:

D3	D2	Character Generator	Table Location
0	0	0	First 8K of Plane 2 Bank 0
0	1	1	First 8K of Plane 2 Bank 1
1	0	2	First 8K of Plane 2 Bank 2
1	1	3	First 8K of Plane 2 Bank 3



IN GRAPHICS MODE: PLANES 0-3 CONTAIN 1 BIT EACH OF A 4 BIT PIXEL. A TOTAL OF 64K PIXELS CAN BE STORED IN MEMORY IN THIS MODE.

IN THE ALPHANUMERIC MODE: PLANE 0 HAS ADDRESS DATA
PLANE 1 HAS ATTRIBUTE DATA
PLANE 2 HAS CHARACTER FONT
PLANE 3 NOT USED

EACH FONT SUPPORTS 256 CHARACTERS UP TO 32 SCAN LINES HIGH AND REQUIRES 8K BYTES OF MEMORY. THE FONT IS RESIDENT IN THE UPPER 8K BYTE POSITION OF EVERY 16K BYTE BLOCK OF PLANE 2.

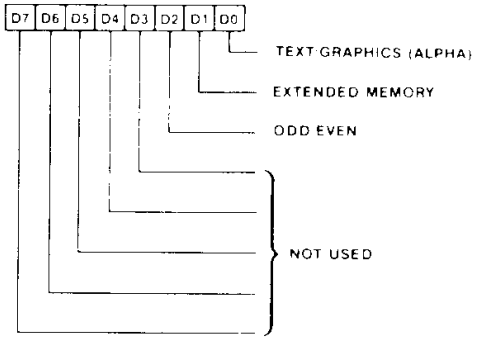
Figure 8. Enhanced Graphics Display Memory Organization

In text modes, bit 3 of the attribute bit D3 normally turns the foreground intensity on or off. This bit may be redefined to be a switch between character sets. This function is enabled when there is a difference in the values of Character Map Select A and Character Map Select B bits. Whenever the two values are the same, the character select function is disabled and attribute bit D3 turns the foreground intensity on or off. 256K bytes of memory support 4 character sets.

Asynchronous Reset (Reset Register bit 0) clears the Character Map Select Register to 0. This should only be done during a system reset.

SEQUENCER MEMORY MODE REGISTER (SR4)

Read-Write Register
I/O Address: 3C5h
Address Pointer: 04



Text/Graphics (D0)

D0=0 indicates that a graphics mode is active. This forces the same address on the multiplexed memory address bus AAx and BAx. D0=1 indicates that the text mode is active and forces the display buffer address on memory address bus AAx and the character generator address on memory address bus BAx.

Extended Memory (D1)

In EGA modes this bit must be programmed to 1. The 82C435 does not support 16k*4 DRAMs. Only 64k*4 DRAMs are supported, for 256 Kbytes of display memory. In CGA/Hercules modes this bit must be programmed to 0. In CGA mode, the memory is restricted to 16 Kbytes while in the Monochrome (Hercules) Text mode the memory is restricted to 4 Kbytes.

Odd/Even (D2)

D2 = 0 puts the Sequencer in the Odd/Even addressing mode. In this mode, even CPU addresses access planes 0 and 2, while odd CPU addresses access planes 1 and 3. This option is useful for IBM Color Graphics Adapter (text and graphics mode) compatible memory organization. The value of this bit should be the complement of the value programmed in D4 of the Graphics Controller Mode Register (GR5).

ATTRIBUTES CONTROLLER

The Attributes Controller provides a palette of 16 colors selectable from a possible 64, each one of which may be specified separately. Six color outputs, Red (R), Green (G), Blue (B), Secondary Red (RS), Secondary Green/Intensity (GS/I) and Secondary Blue/Monochrome (BS/V) are available as outputs. The Attributes Controller also controls blinking and underline operations.

The Attributes Controller formats data from the display memory for display on the screen. It also provides the horizontal pixel panning capability in both text and graphics modes.

In the text mode, the attribute bits are decoded to select one of the 16 color palette registers. The color palette, which consists of 16 registers, each 6-bit wide, can be loaded with any color combination. Thus it is possible to display the characters in any one of the 16 colors out of a possible of 64 (6-bit wide registers).

In the graphics mode, the color information is stored in the display memory as 1, 2 or 4 bits per pixel. The pixel bit pattern is used to select one of the 2, 4 or 16 color registers. The six bit contents of the respective color register determines the color on the screen for each individual pixel.

ATTRIBUTES CONTROLLER REGISTERS

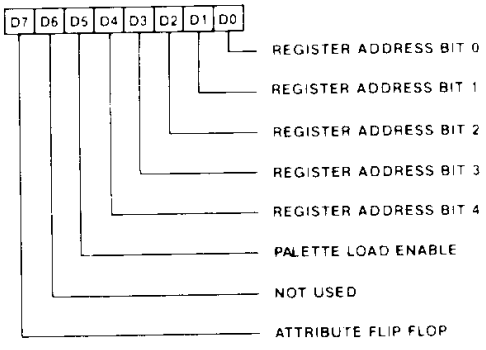
The Attributes Controller registers are all located at a single byte address in the CPU I/O space. The registers are accessed by first writing a pointer to the actual data register

into the Attributes Address Register and then accessing the Attributes Data Register. Both the Attributes Address and Data Registers are located at I/O address 3C0h. Both registers can also be accessed at I/O address 3C1h. An internal flip-flop controls the selection of the Attributes Address and Data Registers. To select the Address Register, an IO Read is executed to address 3BAh/3DAh to clear this flip-flop. After the Address Register has been loaded by an IO Write to address 3C0h, this flip-flop toggles, and the 82C435 is ready to have Data Register (pointed to by the Address Register) loaded. Every IO Write to address 3C0h toggles this flip-flop. The following table describes the Attributes Registers:

Register Number	Register Name	Address Pointer	Address
-	Address Register	—	3C0h
AR0-ARF	Palette Registers	00h-0Fh	3C0h
AR10	Attributes Mode Control	10h	3C0h
AR11	Overscan Color	11h	3C0h
AR12	Color Plane Enable	12h	3C0h
AR13	Horizontal Pixel Panning	13h	3C0h

ATTRIBUTES ADDRESS REGISTER

Read-Write Register
I/O Address: 3C0h



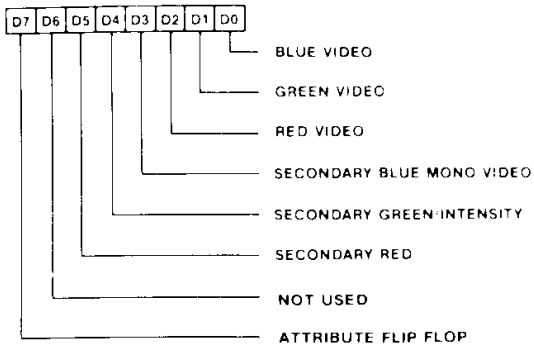
D0-D4 are used to point to the internal data registers in the Attributes Controller.

D5=0 disables the color palette and video to allow access to the color registers. D5=1 enables the video and normal palette function of color translation. This bit must be 0 to load the palette registers (AR0-ARF). After the palette registers have been loaded, this bit must be set to 1 to enable the video data.

D7 indicates the current state of the Attributes flip-flop that toggles between the Attributes Address and Data Registers. D7 = 0 when the Attributes Address Register is read and D7 = 1 when any of the Attributes Data Registers is read. This bit is a read-only bit. To set this bit to a desired value, you need to reset the flip-flop as described earlier and then it can be toggled to the right state.

PALETTE REGISTERS (AR0-ARF)

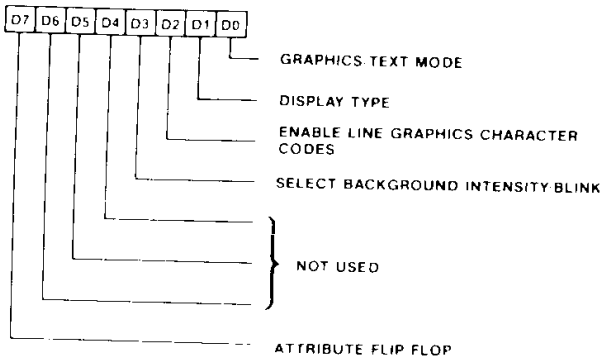
Read-Write Registers
I/O Address: 3C0h
Address Pointer: 00-0Fh



These six bit registers allow a dynamic mapping between the text attribute or graphic color input and the display color on the CRT screen. The six bits, D0-D5 are output as B,G,R,BS,GS/I, and RS/V respectively. A logical 1 in a bit selects the corresponding color for that bit while a 0 de-selects it. The maximum number of possible displayable colors is 64 for monitors with six color inputs. Monitors with three color inputs allow a maximum of eight displayable colors, while monitors which also have an intensity input allow a maximum of sixteen displayable colors.

ATTRIBUTES MODE CONTROL REGISTER (AR10)

Read-Write Register
I/O Address: 3C0h
Address Pointer: 10h



Graphics/Text Mode (D0)

D0=0 selects text mode. D0=1 selects graphics mode.

Monochrome/Color Display (D1)

D1=0 selects color display attributes. D1=1 selects IBM Monochrome display attributes.

Enable Line Graphics Character Codes (D2)

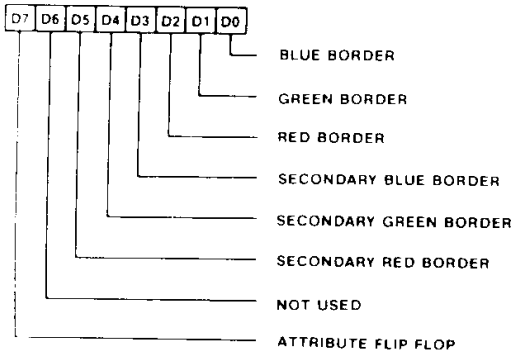
D2=0 makes the ninth dot the same as the background. This enables compatibility with the IBM Monochrome display adapter, which uses 9 dots per character. D2=1 enables the special line graphics character codes for the IBM Monochrome Display Adapter. When this bit is set, it forces the ninth dot of a line graphics character to be identical to the eighth dot of the character. The line graphics character codes for the Monochrome Display Adapter are C0H through DFH. When a Line Graphics character is to be displayed, the Attributes Controller will force the ninth dot bit of a line graphics character to be identical to the eighth dot of the character.

Enable Blink/Select Background Intensity (D3)

D3=0 selects the background intensity for the attribute input. This is required for Monochrome and Color Graphics Adapter compatibility. D3=1 enables the blink attribute in text and graphics modes. The blinking counter operates off the Vertical Sync signal. It divides the VRTC period by 32. For text and graphics modes, the blink is ON for 16 VRTC periods and OFF for 16 VRTC periods. In the text mode, blink is usually used only in Monochrome display modes. In this case , the blink affect displays the character for 16 frames and blanks the screen for 16 frames. In the graphics mode, when blink is activated, the most significant color bit (bit 3) for each pixel is inverted alternately, thus allowing two different colors to be displayed for 16 CRT frames each. When the CURSOR is displayed in the text mode, the 'characters' are blinked at the rate of 16 frames ON and 16 frames OFF. The CURSOR, however, is blinked at a rate of ON for 8 frames and OFF for 8 frames.

OVERSCAN COLOR REGISTER (AR11)

Read-Write Register
I/O Address: 3C0h
Address Pointer: 11h

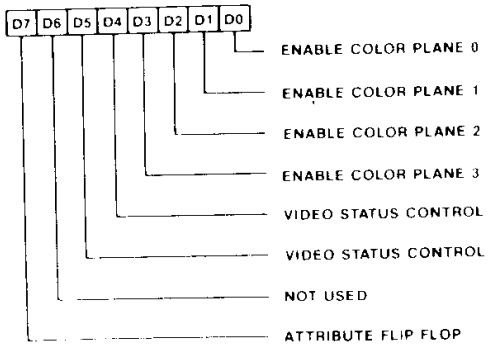


Overscan Color

This six-bit register defines the overscan or border color displayed on the CRT screen. For monochrome displays, this register should be cleared to logical 0. A logical 1 selects the corresponding color. The border color is displayed in the interval after Display Enable End and before Blank Start and between Blank End and Display Enable Start (the beginning).

COLOR PLANE ENABLE REGISTER (AR12)

Read-Write Register
I/O Address: 3C0h
Address Pointer: 12h



Enable Color Plane (D0-D3):

A logical 1 in any of the bits D0-D3 enables the respective color bits for each pixel. If any bit is set to zero, the corresponding bit of the pixel data from memory is forced to zero before accessing the palette.

Display Status MUX (D4-D5):

Bits D4 and D5 select two of the six color outputs to the CRT screen, which are 2 outputs of the 4 status bits. The output color combinations available on the status bits are listed in the following table:

COLOR PLANE ENABLE REGISTER		EGA STATUS REGISTER I OUTPUTS	
D5	**D4**	**Bit5**	**Bit4**
0	0	Red	Blue
0	1	Secondary Red	Secondary Green
1	0	Secondary Blue	Green
1	1	Not Used	Not Used

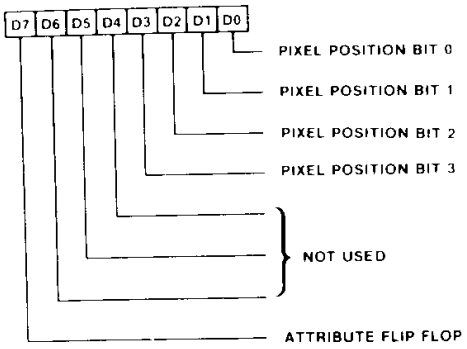
This capability can be used to run diagnostics on the color sub-system card.

D4 = 1 will also:

— Tri-state the color monitor outputs, R, G, B, RS, GS/I and BS/V and,
— Clear the cursor blink counter. D4 must be cleared to logical 0 for the cursor blink counter to function.

HORIZONTAL PIXEL PANNING REGISTER (AR13)

Read-Write Register
I/O Address: 3C0h
Address Pointer: 13h



Horizontal Pixel (Pel) Panning

Bits D0-D3 select the number of pixels to shift the display data horizontally to the left. Pixel panning is available in both text and graphics modes. In monochrome text mode the output can be shifted a maximum of 9 pixels, whereas in all other modes a maximum shift of 8 pixels is possible. The Start Address Register specifies the byte of the upper left corner of the screen display, and pixel panning gives pixel resolution to the left end of the display.

CRT CONTROLLER

The CRT Controller provides the synchronization signals for the display monitor. The CRT Controller contains various CPU accessible I/O registers, that allow flexible configuration options. These options include user configurable horizontal and vertical timings and polarity, cursor type and position, horizontal scan lines, and several other display related characteristics. The CRT Controller also provides split screen capability, soft scrolling and a light pen interface.

I/O address bits A1 and A2 are ignored when the CRTC registers are accessed. The CRTC registers can therefore be accessed at I/O addresses 3X0/1h, 3X2/3h, 3X4/5h and 3X6/7h (X=B in monochrome mode and X=D in color mode).

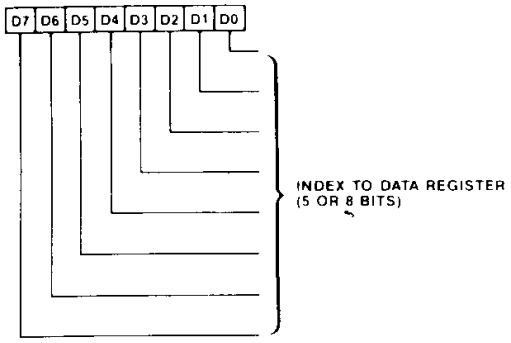
CRT CONTROLLER REGISTERS

Register Number	Register Name	Address Pointer	Address
—	Address Register	—	3B4h/3D4h
CR0	Horizontal Total	00	3B5h/3D5h
CR1	Horizontal Display Enable End	01	3B5h/3D5h
CR2	Start Horizontal Blanking	02	3B5h/3D5h
CR3	End Horizontal Blanking	03	3B5h/3D5h
CR4	Start Horizontal Retrace Pulse	04	3B5h/3D5h
CR5	End Horizontal Retrace Pulse	05	3B5h/3D5h
CR6	Vertical Total	06	3B5h/3D5h
CR7	CRT Controller Overflow	07	3B5h/3D5h
CR8	Preset Row Scan	08	3B5h/3D5h
CR9	Maximum Scan Line	09	3B5h/3D5h
CRA	Cursor Start Scan Line	0Ah	3B5h/3D5h
CRB	Cursor End Scan Line	0Bh	3B5h/3D5h
CRC	Start Address High	0Ch	3B5h/3D5h
CRD	Start Address Low	0Dh	3B5h/3D5h
CRE	Cursor Location High	0Eh	3B5h/3D5h
CRF	Cursor Location Low	0Fh	3B5h/3D5h
CR10	Vertical Retrace Start	10h	3B5h/3D5h
CR10	Light Pen High	10h	3B5h/3D5h
CR11	Vertical Retrace End	11h	3B5h/3D5h
CR11	Light Pen Low	11h	3B5h/3D5h
CR12	Vertical Display Enable End	12h	3B5h/3D5h
CR13	Offset	13h	3B5h/3D5h
CR14	Underline Location	14h	3B5h/3D5h
CR15	Start Vertical Blanking	15h	3B5h/3D5h
CR16	End Vertical Blanking	16h	3B5h/3D5h
CR17	CRT Mode Control	17h	3B5h/3D5h
CR18	Line Compare	18h	3B5h/3D5h
CRF7	Tag Register 0[2]	F7h	3B5h/3D5h
CRF8	Tag Register 1[2]	F8h	3B5h/3D5h
CRF9	400 Line Register[2]	F9h	3B5h/3D5h
CRFA	Temporary Storage 0[1,2]	FAh	3B5h/3D5h
CRFB	Temporary Storage 1[1,2]	FBh	3B5h/3D5h
CRFC	Temporary Storage 2[1,2]	FCh	3B5h/3D5h
CRFD	Temporary Storage 3[1,2]	FDh	3B5h/3D5h
CRFE	Temporary Storage 4[1,2]	FEh	3B5h/3D5h
CRFF	Emulation Mode Register[2]	FFh	3B5h/3D5h

(1—in 82A436, 2—used in CRTC Extended Mode only)

ADDRESS REGISTER

Read-Write Register
I/O Address: 3B4h/3D4h

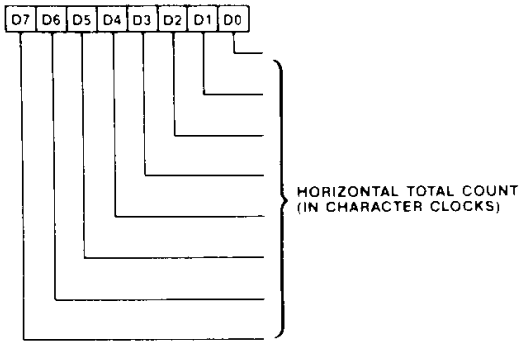


The CRT Controller Registers are all located at two byte addresses in the CPU I/O space. The registers are accessed by first writing a pointer to the actual data register into the CRT Controller Address Register and then accessing the CRT Controller Data Register. The Address Register is located at I/O address 3B4h/3D4h. The data registers are all located at I/O address 3B5h/3D5h. The exact address 3Bx/3Dx is selected thorough bit D0 of the EGA Misc. Output Register.

The Address Register is normally a 5 bit register with the upper 3 bits being ignored. When the CRTC Extended Mode Registers are enabled through register CR17, all 8 bits of the Address Register are used to point to the appropriate data register. When this register is read, D6 and D7 are always '1'. D5 is '1' if D6 and D7 were written as 1. D5 is '0' if D6 or D7 were written as 0.

HORIZONTAL TOTAL REGISTER (CR0)

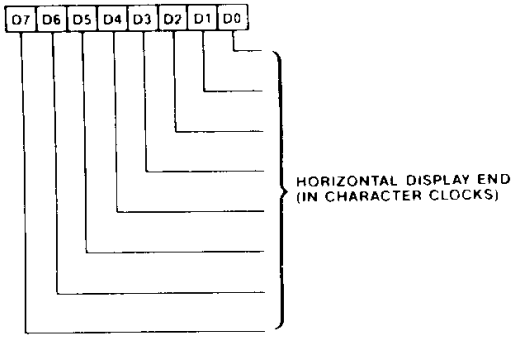
Read-Write Register
I/O Address: 3B5h/3D5h
Address Pointer: 00h



The Horizontal Total Register defines the total number of characters in a horizontal scan line, including the retrace time. This defines the horizontal sweep rate. The character clock is derived from the dot clock as defined by the Sequencer Clocking Mode Register. The actual number of character clocks per horizontal scan is two more than the value programmed in this register.

HORIZONTAL DISPLAY ENABLE END REGISTER (CR1)

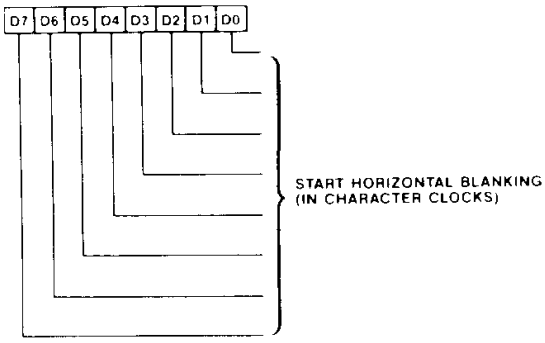
Read-Write Register
I/O Address: 3B5h/3D5h
Address Pointer: 01h



The Horizontal Display Enable End Register defines the number of characters to be displayed per horizontal line. The actual characters displayed per horizontal line is one more than the contents of this register.

START HORIZONTAL BLANKING REGISTER (CR2)

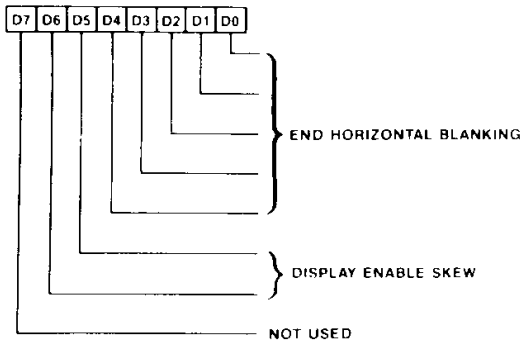
Read-Write Register
I/O Address: 3B5h/3D5h
Address Pointer: 02h



The contents of the Start Horizontal Blanking Register define the time when the horizontal

blanking will start. The register is defined in terms of the number of horizontal character clocks. The period between horizontal display enable end and horizontal blanking start is the right side border on the screen.

END HORIZONTAL BLANKING REGISTER (CR3)
Read-Write Register
I/O Address: 3B5h/3D5h
Address Pointer: 03h



The contents of the End Horizontal Blanking Register define the time when the horizontal blanking will terminate. The register is defined in terms of the number of character clocks.

D0-D4 End Horizontal Blanking: The horizontal blanking signal width, W, is determined as follows:

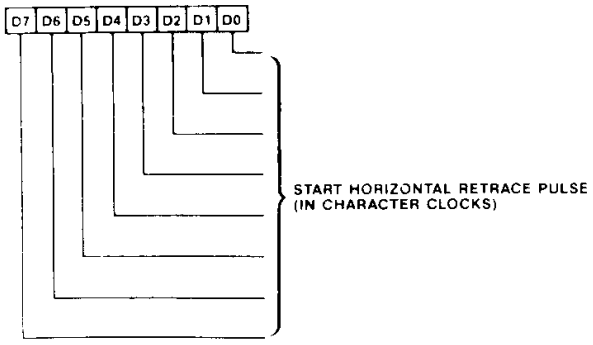
Value in Start Blanking Register + W = 5-bit value to be programmed in End Horizontal Blanking Register.

The five least significant bits of the horizontal character counter are compared with the contents of this register. When a match occurs, the horizontal blanking pulse becomes inactive. Note that the five bits of this register limit the length of the blanking pulse to 31 character clocks.

D5-D6 Display Enable Skew Control: Prior to displaying data on the screen, the 82C435 has to fetch the character and attribute code, then access the character generator font and finally read the Pixel Panning Register in the Attributes Controller. Each one of these accesses require the display enable signal to be skewed by one character clock to allow for synchronization with the horizontal and vertical retrace pulses. The display enable skew bits in this register allow for this skew. The skew can be programmed from 0-3 character clocks as follows:

D6	D5	Skew in character clocks
0	0	0
0	1	1
1	0	2
1	1	3

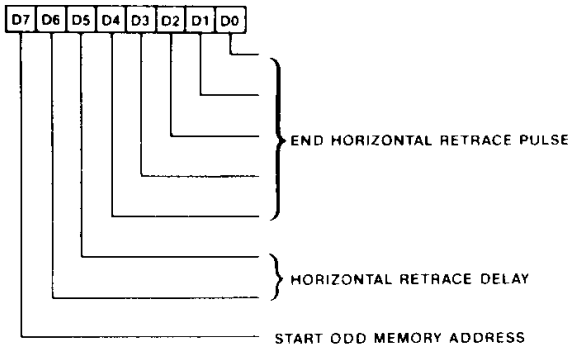
START HORIZONTAL RETRACE PULSE REGISTER (CR4)
Read-Write Register
I/O Address: 3B5h/3D5h
Address Pointer: 04h



The Start Horizontal Retrace Pulse Register defines the character position at which the Horizontal Retrace Pulse becomes active. It is used to center the monitor screen horizontally. The value in the register is the character count at which the Horizontal Retrace Pulse becomes active.

END HORIZONTAL RETRACE PULSE REGISTER (CR5)

Read-Write Register
I/O Address: 3B5h/3D5h
Address Pointer: 05h



The contents of the End Horizontal Retrace Register define the character count at which the Horizontal Retrace Pulse becomes inactive.

D0-D4 End Horizontal Retrace: The horizontal retrace signal becomes inactive after the character count becomes equal to the count in these bits. The width, W, of the retrace signal (in character clocks) is determined as follows:

Value in Horizontal Retrace Start Register + W = 5-bit result to be programmed in End Horizontal Retrace Register.

The five least significant bits of the horizontal character counter are compared to the contents of this register. When a match occurs, the horizontal retrace pulse becomes inactive. Note that the 5 bit register limits the length of the retrace signal to 31 character clocks maximum.

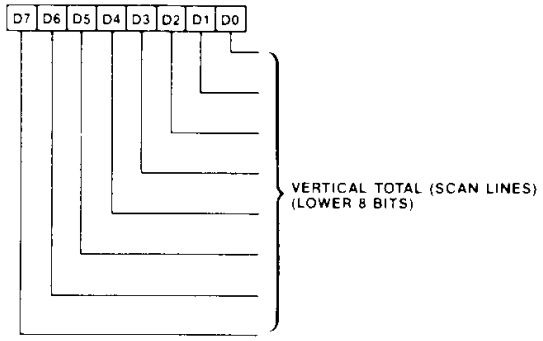
D5-D6 Horizontal Retrace Delay: The skew of the horizontal retrace signal is controlled by these bits. For some monitors, it is necessary to provide a horizontal retrace signal that takes up the entire blanking period. The horizontal retrace signal also triggers some internal timings on the falling edge of the signal. To ensure that the signals are latched properly, the retrace signal is started before the end of the display enable signal. It is then skewed several character clocks to provide the proper screen centering.

D6	D5	Skew in character clocks
0	0	0
0	1	1
1	0	2
1	1	3

D7 Start Odd/Even Memory Address: This bit determines the CRT memory address after a horizontal retrace. D7 = 0 selects an even address, and D7 = 1 selects an odd address. In most cases this bit should be set to '0'. The bit is useful in applications where horizontal pixel panning is required.

VERTICAL TOTAL REGISTER (CR6)

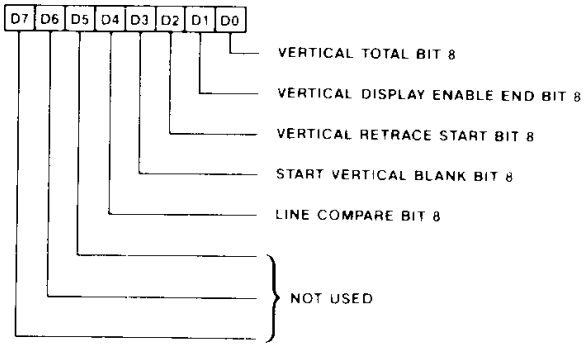
Read-Write Register
I/O Address: 3B5h/3D5h
Address Pointer: 06h



The Vertical Total Register contains the 8 low-order bits of a 9 bit register. The ninth bit is located in the CRT Controller Overflow Register. The Vertical Total Register defines the total number of scan lines (horizontal retrace periods) per frame.

CRT CONTROLLER OVERFLOW REGISTER (CR7)

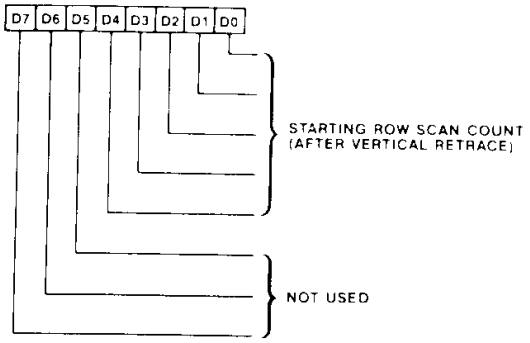
Read-Write Register
I/O Address: 3B5h/3D5h
Address Pointer: 07h



The CRT Controller Overflow Register contains the ninth bit (D8) of Vertical Total, Vertical Retrace Start, Start Vertical Blanking and Line Compare Registers.

PRESET ROW SCAN REGISTER (CR8)

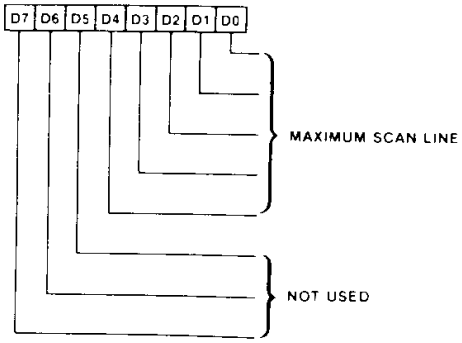
Read-Write Register
I/O Address: 3B5h/3D5h
Address Pointer: 08h



D0-D4 of the Preset Row Scan Register specify the starting row scan count after a vertical retrace. Each horizontal retrace increments the character row scan line counter. The horizontal row scan counter is cleared at maximum row scan count, which is programmed through register CR9. This register is used for soft scrolling in text modes and in the Hercules Graphics or CGA graphics modes.

MAXIMUM SCAN LINE REGISTER (CR9)

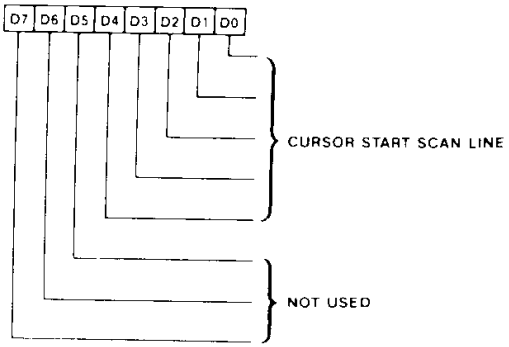
Read-Write Register
I/O Address: 3B5h/3D5h
Address Pointer: 09h



The contents of the Maximum Scan Line Register specifies the number of scan lines per character row. This actual number of scan lines per row is the contents of this register plus one.

CURSOR START SCAN LINE REGISTER (CRA)

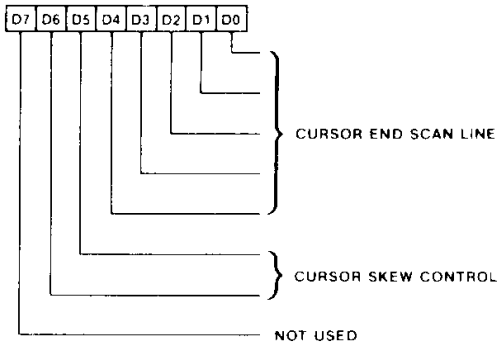
Read-Write Register
I/O Address: 3B5h/3D5h
Address Pointer: 0Ah



The Cursor Start Register defines the scan line within a character row where the cursor block is to begin. The first scan line for the cursor is the contents of this register.

CURSOR END SCAN LINE REGISTER (CRB)

Read-Write Register
I/O Address: 3B5h/3D5h
Address Pointer: 0Bh



The Cursor End Register defines the scan line within a character row where the cursor block is to end. It also controls the cursor skew as described below:

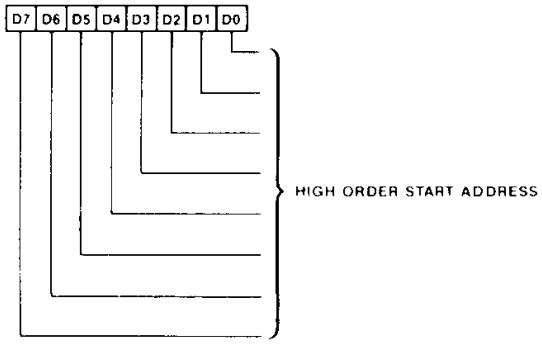
D0-D4 the last scan line for the block cursor is the contents of this field, minus one.

D5-D6 The cursor skew is controlled by these two bits. The bits control the skew as follows:

D6	D5	Skew
0	0	One character skew
0	1	One character skew
1	0	Two character skew
1	1	Three character skew

START ADDRESS HIGH REGISTER (CRC)

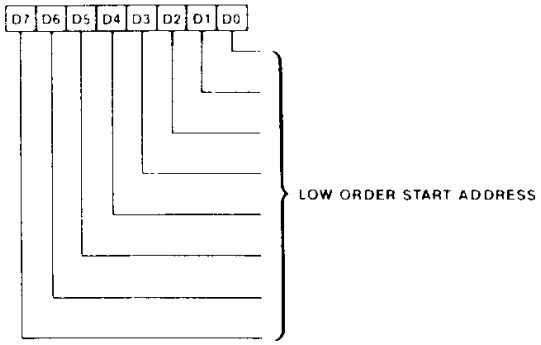
Read-Write Register
I/O Address: 3B5h/3D5h
Address Pointer: 0Ch



The Start Address is a 16-bit value which specifies the first word address in the display buffer for the screen refresh process. This display buffer address is mapped to the upper left corner of the screen. The Start Address High Register contains 8 high order bits of the address, while the Start Address Low Register specifies the other 8 low order bits. Byte resolution on this address can be achieved through the Extended Mode Register (CRF9 - bit D1).

START ADDRESS LOW REGISTER (CRD)

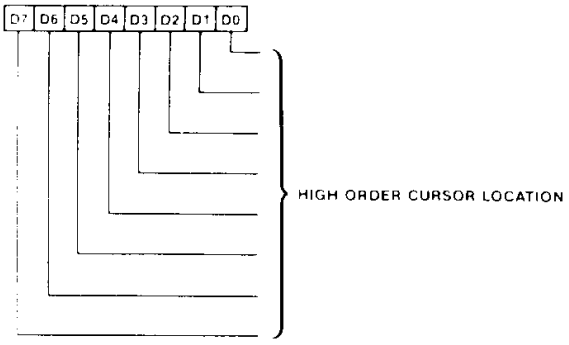
Read-Write Register
I/O Address: 3B5h/3D5h
Address Pointer: 0Dh



The Start Address Low Register contains the 8 low order bits of the Start Address (word address).

CURSOR LOCATION HIGH REGISTER (CRE)

Read-Write Register
I/O Address: 3B5h/3D5h
Address Pointer: 0Eh

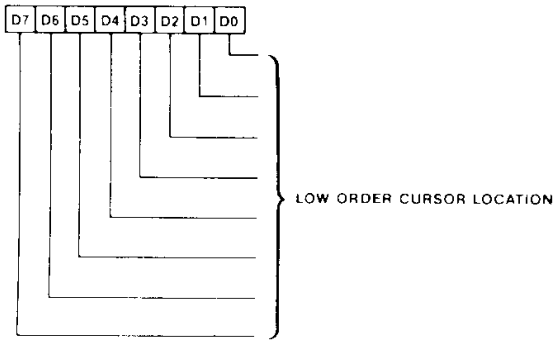


The Cursor Location address is a 16-bit value. The 8 high order bits are programmed in the Cursor Location High Register. The other 8

low order bits are programmed in the Cursor Location Low Register. The 16-bit word address defines the memory adddress for the character which should have the cursor superimposed on it.

CURSOR LOCATION LOW REGISTER (CRF)

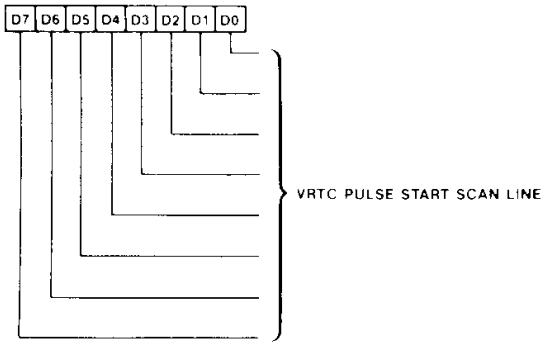
Read-Write Register
I/O Address: 3B5h/3D5h
Address Pointer: 0Fh



In conjunction with the Cursor Location High Register, the Cursor Location Low Register defines the low order 8 bits of the cursor location.

VERTICAL RETRACE START REGISTER (CR10)

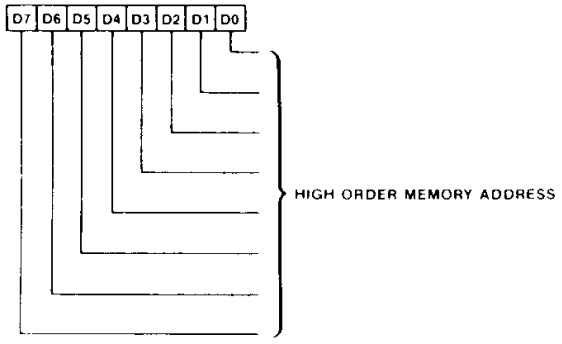
Read-Write Register
I/O Address: 3B5h/3D5h
Address Pointer: 10h



The Vertical Retrace Start Register is a 9-bit address which defines the scan line position of the VRTC pulse. The low order 8 bits are programmed through this register, while the high order ninth bit is programmed through the Overflow Register, CR7.

LIGHT PEN HIGH REGISTER (CR10)

Read only Register
I/O Address: 3B5h/3D5h
Address Pointer: 10h

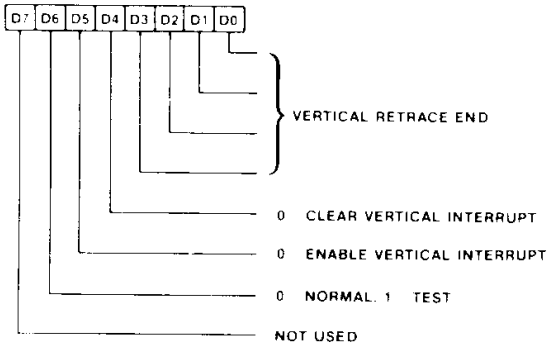


The Light Pen High Register contains the 8 high order bits of the memory address that was displayed when the light pen strobe signal was triggered. The low order 8 bits are stored in the Light Pen Low Register (CR11).

Normally all write operations to Data Register CR10 access the Vertical Retrace Start Register and read operations access the Light Pen High Register. Using the Extended Mode Registers of the 82C435, it is also possible to read the Vertical Retrace Start Register.

VERTICAL RETRACE END REGISTER (CR11)

Read-Write Register
I/O Address: 3B5h/3D5h
Address Pointer: 11h



The Vertical Retrace End Register performs multiple functions, as described below:

D3-D0 Vertical Retrace End: These four bits specify the scan line count at which

the vertical retrace output pulse becomes inactive. The four bits are compared with the four least significant bits of the scan line counter. When the four counter bits are equal to the contents in this register, the vertical retrace is terminated. The maximum retrace pulse width can only be 15 scan lines. The width, W, of the vertical retrace pulse can be determined as follows:

Value of Start Vertical Retrace Register + W = four bit value to be programmed into the End Vertical Retrace Register.

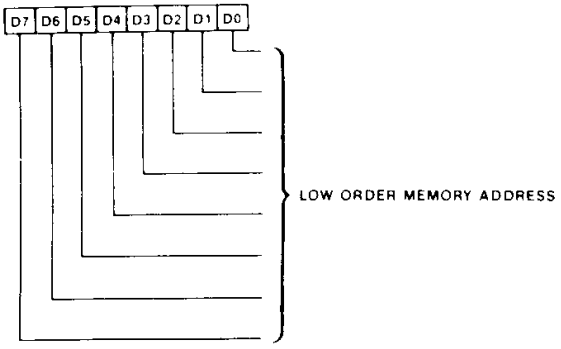
D4 Clear Vertical Interrupt: This bit is used to clear the vertical interrupt generated on the CRTINT output. A logical 0 will clear the interrupt.

D5 Enable Vertical Interrupt: A logical 0 will enable the vertical interrupt of the CRT Controller.

D6 Test: For normal operation this bit must be set to logical 0.

LIGHT PEN LOW REGISTER (CR11)

Read only Register
I/O Address: 3B5h/3D5h
Address Pointer: 011h

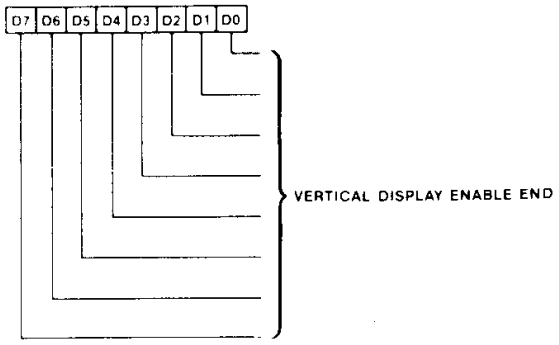


The Light Pen Low Register contains the 8 low order bits of the memory address displayed when the light pen strobe signal was triggered. The high order 8 bits are stored in the Light Pen High Register (CR10).

Normally all write operations to Data Register CR11 access the Vertical Retrace End Register and read operations access the Light Pen Low Register. Using the Extended Mode Registers of the 82C435, it is also possible to read the Vertical Retrace End Register.

VERTICAL DISPLAY ENABLE END REGISTER (CR12)

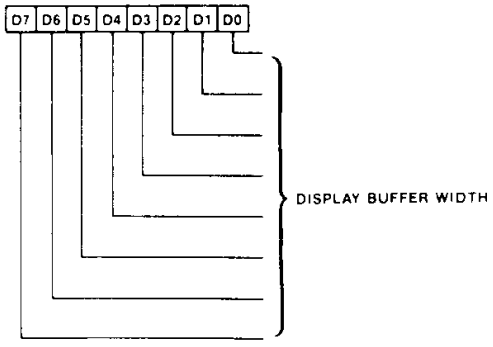
Read-Write Register
I/O Address: 3B5h/3D5h
Address Pointer: 12h



The Vertical Display Enable End Register defines 8 bits of the 9-bits address which specifies the scan line position where the display on the screen ends. The ninth bit is located in the Overflow Register CR7.

OFFSET REGISTER (CR13)

Read-Write Register
I/O Address: 3B5h/3D5h
Address Pointer: 13h



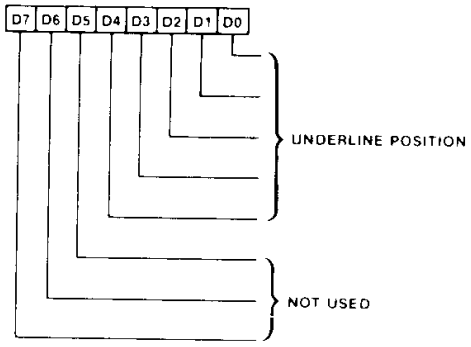
The Offset Register contents define the width of the Display Buffer currently used. This register is used to compute the memory starting address for the next display row (or scan line in graphics modes). The byte starting address of the next display row is computed as follows:

Byte Start Address for next row = Byte Start Address for current row + K*Contents of Offset Register (where K = 2 in Byte Mode and K = 4 in Word Mode).

The byte or word mode for the memory address counter is selected by the CRT Mode Control Register CR17, bit 6. In the CRTC Extended Mode, the 400 Line Register (CRF9) bit D2 allows byte/word resolution to the Display Buffer Width.

UNDERLINE LOCATION REGISTER (CR14)

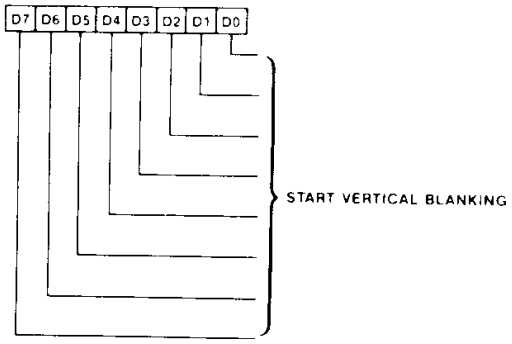
Read-Write Register
I/O Address: 3B5h/3D5h
Address Pointer: 14h



The Underline Location Register specifies the scan line within a character row at which the underline will appear for underlined characters. The value in the register should be one less than the desired scan line number.

START VERTICAL BLANKING REGISTER (CR15)

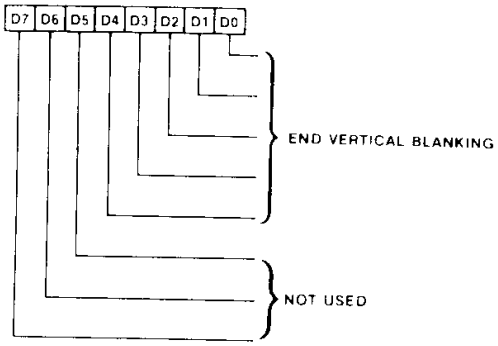
Read-Write Register
I/O Address: 3B5h/3D5h
Address Pointer: 15h



The Start Vertical Blanking Register contains the low order 8 bits of the scan line count at which vertical blanking becomes effective. The ninth bit is located in the Overflow Register CR7.

END VERTICAL BLANKING REGISTER (CR16)

Read-Write Register
I/O Address: 3B5h/3D5h
Address Pointer: 16h



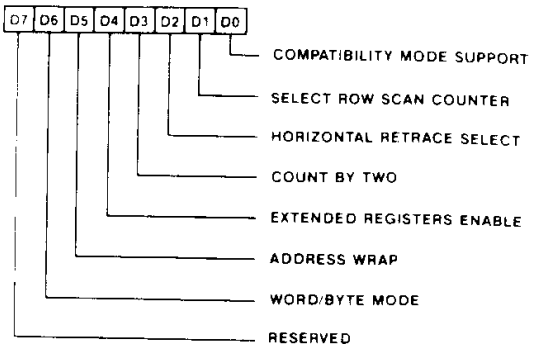
The End Vertical Blanking Register specifies the scan line count at which vertical blanking becomes inactive. The vertical blanking width, W, is determined as follows:

Value of Start Vertical Register + W = 5-bit value to be programmed into the End Vertical Blanking Register.

The five least significant bits of the result are programmed into this register. When the five least significant bits of the horizontal scan line counter are equal to the value in this register, Vertical Blanking is terminated. Note that the maximum width of the vertical blanking is limited to 31 scan lines.

CRT MODE CONTROL REGISTER (CR17)

Read-Write Register
I/O Address: 3B5h/3D5h
Address Pointer: 17h



The CRT Mode Control Register is a multi-function register, with each bit defining a different option. Following is a description of these bits:

D0 Compatibility Mode Support: This bit allows compatibility with the IBM Color Graphics Adapter. When D0=0, the character row scan line counter bit 0 is substituted for memory address bit 13 during active display time. When D0=1, no such substitution takes place.

D1 Select Row Scan Counter: This bit allows compatibility with the Hercules graphics card and with any other 4-bank graphics system. When D1=0, the row scan line counter bit 1 is substituted for memory address bit 14 during active display time. When D1=1, no such substitution takes place.

D2 Horizontal Retrace Select: This bit controls the vertical resolution capability of the CRT Controller. The vertical counter has a maximum resolution of 512 scan lines as defined by the Vertical Total Register. If the vertical retrace counter is clocked with the horizontal retrace clock divided by 2, then the vertical resolution is doubled to 1024 horizontal scan lines. D2=0 selects the horizontal retrace clock, and D2=1 selects the horizontal retrace clock divided by 2.

D3 Count By Two: This bit selects the character clock as the clock input or character clock divided by 2 as the character clock. This bit defines whether the contents of the Offset Register are a word or a double word value. When D3=0, the memory address counter is clocked by the character clock input. When D3=1, the memory address is clocked by the character clock input divided by 2. This bit is also used to create either a byte or word refresh address for the display memory.

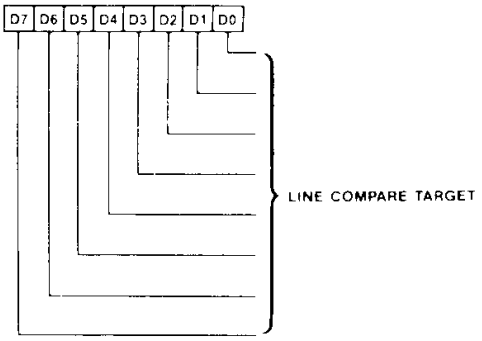
D4 Extended Register Enable: D4 = 0 is the default on reset. In this case the 82C435 behaves exactly as an EGA. When D4= 1, then all the Extended Mode Registers in the 82C435 become enabled. These registers are used for compatibility with CGA/MDA/Hercules graphics card and to save/restore the context of the 82C435. All extended register functionality is gated with this bit. The extended registers can always be read or written regardless of this bit.

D5 Address Wrap: Since the 82C435 does not support 64 Kbytes of display memory (it requires 256 Kbytes), this bit must always be one for all EGA modes. In the CGA mode, this bit must be set to 0.

D6 Word Mode or Byte Mode: When D6=0, Word Mode is selected. This mode causes the display memory address counter bits to shift down one bit, and the most significant bit of the counter appears on the least significant bit of the memory address output. D6 =1 selects the Byte Mode.

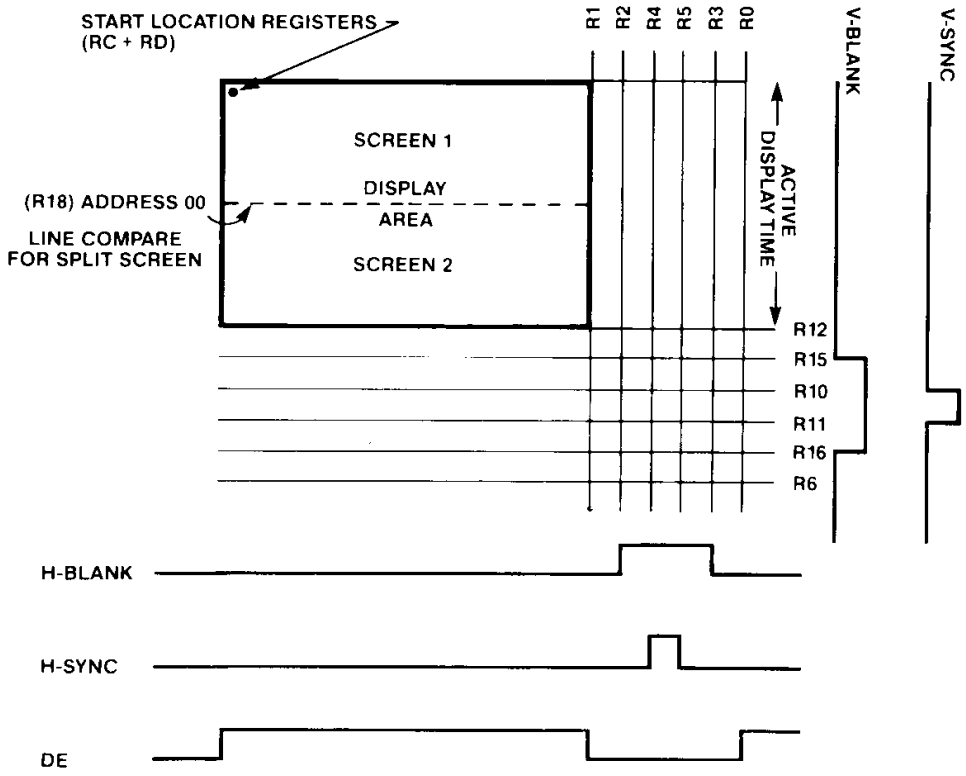
LINE COMPARE REGISTER (CR18)

Read-Write Register
I/O Address: 3B5h/3D5h
Address Pointer: 18h



The Line Compare Register is used to implement a split screen function. When the scan line counter value is equal to the contents of this register, the memory address generator is cleared to 0. The display buffer address generator then sequentially addresses the display buffer starting at address 0. Each subsequent row address is generated by the addition of Offset Register contents.

This feature allows a given area on the screen to be immune to scrolling. The scrolling operation utilizes the Start Address High and Low Registers, and the split screen screen capability will allow scrolling through some areas of the screen while the remaining screen remains immune to it. The CRT Controller provides all the timing and control signals for the display monitor. Figure 9 shows a graphic illustration of how the contents of these registers control the display screen. The horizontal blanking signal is controlled by the contents of CR2 and CR3 registers. Similarly, the contents of CR15 and CR16 determine the location and length of the vertical blanking signal. The screen blanking signal BLANK is a logical 'OR' of HBLANK and VBLANK as programmed in the respective registers. The horizontal retrace start location and width are controlled by the contents of the CR4 and CR5 registers, while the vertical retrace start location and width are controlled by the CR10 and CR11 registers. CR0 controls the total number of characters in the horizontal scan interval, including the retrace time. The total number of scan lines on one raster are determined by the vertical total register CR6. CR1 and CR12 define the effective display area on the screen by specifying the horizontal and vertical display enable positions, respectively.



R0: HORIZONTAL TOTAL
R1: HORIZONTAL DISPLAY END
R2: START HORIZONTAL BLANK
R3: END HORIZONTAL BLANK
R4: START HORIZONTAL RETRACE
R5: END HORIZONTAL RETRACE
R6: VERTICAL TOTAL
RC: START ADDRESS HIGH

RD: START ADDRESS LOW
R10: VERTICAL RETRACE START
R11: VERTICAL RETRACE END
R12: VERTICAL DISPLAY END
R15: START VERTICAL BLANK
R16: END VERTICAL BLANK
R18: LINE COMPARE

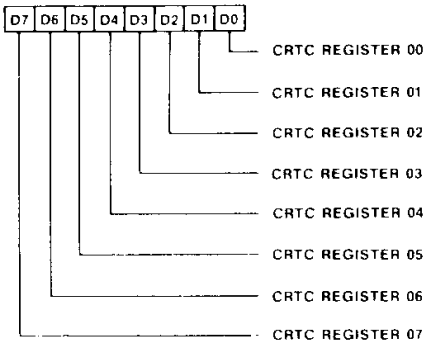
Fig. 9

CRTC EXTENDED REGISTERS

The CRTC Extended Registers are located in the CRT Controller address space (Address Pointer at 3B4h/3D4h and Data Register at 3B5h/3D5h). These registers are functional only after bit D4 of the CRTC Register is set.

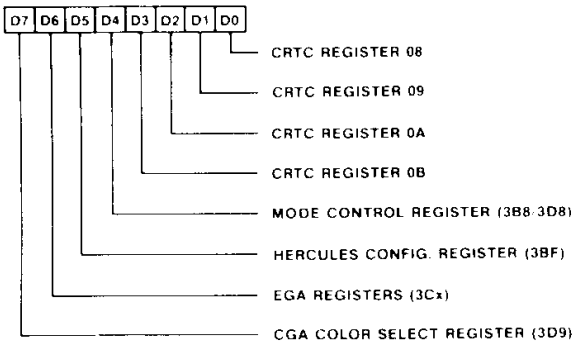
TAG REGISTER 0 (CRF7)

Read-Clear Register
I/O Address: 3B5h/3D5h
Address Pointer: F7h



TAG REGISTER 1 (CRF8)

Read-Clear Register
I/O Address: 3B5h/3D5h
Address Pointer: F8h

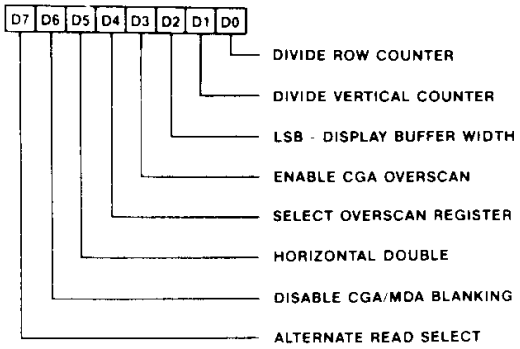


Tag Registers 0 and 1 are located at offset 0F7h (Tag Register 0) and 0F8h (Tag Register 1) in the CRT Controller. They can be accessed by first writing 0F7h/0F8h in the CRTC Address Register (I/O address 3B4h/3D4h) and then accessing the CRTC Data Register (I/O address 3B5h/3D5h).

A bit in these registers is set whenever the corresponding register is written into. When traps are enabled, then any bit set in the two Tag Registers will cause a trap. When emulation is in progress, then the emulation software can read these registers to determine which register access caused the trap resulting in the emulation software being invoked. Reading these registers clears the registers, serving as a trap acknowledge.

400 LINE REGISTER (CRF9)

Read-Write Register
I/O Address: 3B5h/3D5h
Address Pointer: F9h



The 400 Line Register is located at offset 0F9h in the CRT Controller. This register can be accessed by first writing 0F9h in the CRTC Address Register (I/O address 3B4h/3D4h) and then accessing the CRTC Data Register (I/O address 3B5h/3D5h).

The description for the individual bit fields is as follows:

D0 — Divide Row Counter: D0=0 causes the scan line (in a row) counter to be incremented every scan line. D0=1 causes this counter to be incremented every two scan lines. This bit should be set to 1 when it is desired to double each scan line (running 200 scan line software on a 400 scan line monitor). Power-on reset clears this bit.

D1 — Divide Vertical Counter: D1=0 causes the vertical counters to be incremented every scan line. D1=1 causes the vertical counters to be incremented every two scan lines. This bit should be set to 1 when it is desired to double each scan line (running 200 scan line software on a 400 scan line monitor). Power-on reset clears this bit.

D2 LSB - Display Buffer Width: This is the complement of the least significant bit for the Display Buffer Width (CRTC Offset Register CR13). This allows byte resolution on the Display Buffer Width.

D3 Enable CGA Overscan: D3=0 disables the CGA overscan (border) feature. This is useful when running CGA software on a 21.8 KHz monitor, when it may be desirable to disable the borders. D3=1 enables this feature. This bit is effective only in 80 column text mode.

D4 Select Overscan Register: D4=0 selects the CGA Color Select Register (hardware palette) as the source for the border color. D4=1 selects the Attribute Controller Overscan Color Register as the source for the border color. This bit is ignored in the EGA mode.

D5 Horizontal Double: D5=0 causes the CRTC to generate a 640*200 display when programmed for a 320*200 display. D5=0 generates a 320*200 display. When emulating the 640*200 CGA mode, it is easiest to algorithmically translate the 6845 parameters to EGA CRTC parameters in the 320*200 mode. Setting this bit to 0 results in a 640*200 display. This bit is used only when emulating 640*200*1 CGA graphics mode. For all other modes, this bit must be programmed high.

D6 Disable CGA/MDA Blanking: D6 = 1, disables the functionality of the Display Blanking feature of the CGA and MDA Mode Control Register—bit D3 of MDA CRT Control Register (I/O address 3B8h) and bit D3 of CGA Mode Control Register (I/O address 3D8h). D6 = 0 enables this functionality.

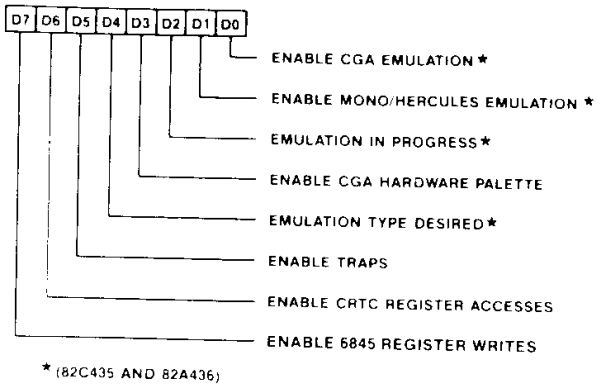
D7 Alternate Read Select: D7=0 returns the contents of the EGA Miscellaneous Output Register, EGA Feature Control Register, and Vertical Retrace Start and End Registers when reading CRTC Registers CRE, CRF, CR10 and CR11 respectively. D7=1 returns the contents of the Cursor Location High and Low Registers, and Light Pen High and Low Registers when reading CRTC Registers CRE, CRF, CR10 and CR11 respectively. On reset, this bit is set to 1.

TEMPORARY STORAGE REGISTERS

There are five byte wide temporary storage read-write registers in the 82A436. These registers are located at offset 0FAh-0FEh in the CRT Controller data register space. These registers can be accessed by first writing 0FAh/0FBh/0FCh/0FDh/0FEh in the CRTC Address Register (I/O address 3B4h/3D4h) and then accessing the CRTC Data Register (I/O address 3B5h/3D5h). These registers can be used as working registers.

EMULATION MODE REGISTER (CRFF)

Read-Write Register
I/O Address: 3B5h/3D5h
Address Pointer: FFh



The Emulation Mode Register is located at offset 0FFh in the CRT Controller. This register can be accessed by first writing 0FFh in the CRTC Address Register (I/O address 3B4h/3D4h) and then accessing the CRTC Data Register (I/O address 3B5h/3D5h).

The description for the individual bit fields is as follows:

D0 Enable CGA Emulation: This bit determines if CGA Emulation is to be enabled (=1) or disabled (=0).

D1 Enable Mono/Hercules Emulation: This bit determines if Monochrome/ Hercules Emulation is to be enabled (=1) or disabled (=0).

To automatically allow switching between EGA, CGA and Hercules emulation modes, CRFF bits D0 and D1 must be set as follows:

D1	D0	Switching between modes
0	0	Lock into EGA mode only.
0	1	Allow auto-emulation between EGA and CGA mode only.
1	0	Allow auto-emulation between EGA and Hercules modes only.
1	1	Allow auto-emulation between EGA, CGA and Hercules modes.

D2 Emulation in Progress: This bit determines if the 82C435 is currently in the CGA or Hercules emulation mode (=1) or in the normal EGA mode (=0). This bit must be set while CGA/MDA/Hercules emulation is in progress.

D3 Enable CGA Hardware Palette: A one in this bit selects the CGA Color Select Register (at I/O address 3D9h) to generate the colors to be displayed. A zero in this bit causes colors to be selected from the EGA Attribute Controller Palette. When this bit is set to 1, then TAG Register 1 bit 7 (CGA Color Select Register is disabled).

D4 Emulation Type: This is a read only bit that indicates what type of emulation is desired by the application software. If CGA emulation is enabled (D0 of this register) then any access to I/O address 3D8h will cause this bit to be set to zero indicating that CGA emulation is desired. If Mono/Hercules emulation is enabled (D1 of this register) then any access to I/O address 3B8h causes this bit to be set to one indicating that Monochrome/ Hercules emulation is desired.

D5 Enable Traps: A one in this bit generates a trap indicating processor support required for emulation whenever emulation is enabled and software desires a change in mode. A zero in this bit disables the traps.

A trap is generated under any one of the following conditions:

a) Write to I/O address 3BFh when Emulation Mode Register bit D1=1 (Hercules emulation enabled and access to Hercules Configuration Register).

b) Write to I/O address 3B8h when Emulation Mode Register bit D1=1 and bit D2= 0 (Currently in EGA mode, Hercules emulation enabled and access to Hercules Mode Control Register).

c) Write to I/O address 3B8h when Emulation Mode Register bit D1=1, bit D2=1 and bit D4=0 (Currently emulating CGA and access to Hercules Mode Control Register).

d) Write to I/O address 3B8h when Emulation Mode Register bit D1=1, bit D2=1, bit D4=1, Hercules Mode Control Register bit D3=1 and bit D1 toggles (currently emulating Hercules, video enabled and switch between text and graphics modes).

e) Write to I/O address 3D8h when Emulation Mode Register bit D0=1 and bit D2= 0 (Currently in EGA mode, CGA emulation enabled and access to CGA Mode Control Register).

f) Write to I/O address 3D8h when Emulation Mode Register bit D0=1, bit D2=1 and bit D4=1 (Currently emulating Hercules and access to CGA Mode Control Register).

g) Write to I/O address 3D8h when Emulation Mode Register bit D0=1, bit D2=1, bit D4=0, CGA Mode Control Register bit D3=1 and any one of bits D0,D1,D2 or D4 change state (currently emulating CGA, video enabled and mode switch).

h) Write to I/O address 3D9 when Emulation Mode Register bit D0=1 and bit D3=0 (CGA emulation enabled, CGA hardware palette disabled and access to CGA Color Select Register).

i) Write to any one of I/O addresses 3C0h, 3C2h, 3C4h, 3C5h, 3CAh, 3CCh, 3CEh or 3CFh when Emulation Mode Register bit D2=1 (currently emulating Hercules or CGA and access to any EGA only register).

j) Write to I/O address 3B5h when Emulation Mode Register bit D7 = 1, EGA Misc. Output Register bit D0 = 0 and CRTC Address Register = 00 through 0Bh (emulating Hercules/CGA and access to the Hercules 6845 Data Register).

k) Write to I/O address 3D5h when Emulation Mode Register bit D7 = 1, EGA Misc. Output Register bit D0 = 1 and CRTC Address Register = 00 through 0Bh (emulating Hercules/CGA and access to the CGA 6845 Data Register).

D6 Enable CRTC Registers: A one in this bit causes data writes to I/O address 3B5h/3D5h to be directed to the CRT Controller Registers. For data read operation at I/O address 3B5h/3D5h, D6=1 reads the CRTC registers and D6=0 reads the 6845 registers.

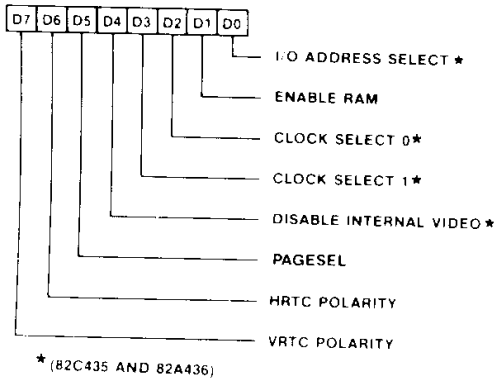
D7 Enable 6845 Registers: A one in this bit causes data writes to I/O address 3B5h/3D5h to be directed to the 6845 registers. Simultaneously setting D6 and D7=1 causes both the CRTC and 6845 registers to be written.

OTHER EGA REGISTERS

Register Name	Address
EGA Miscellaneous Output	3C2h
Feature Control Register	3BAh/3DAh
Input Status Register 0	3C2h
Input Status Register I	3BAh/3DAh

EGA MISCELLANEOUS OUTPUT REGISTER

Read/Write Register
I/O Address: 3C2h



The EGA Miscellaneous Output Register is normally a write only register. It can be read by setting the alternate read select bit in the 400 Line Register (CRF9 bit D7 = 0) and then reading CRTC Data Register at offset 0Fh. The I/O Address Select bit (D0) can also be read at bit D5 of the Sequencer Address Register (I/O address 3C4h). This register performs the following functions:

D0 This bit maps the CRT Controller address and data registers into the 3Bxh/3Dxh address space. This bit defaults to 0 on reset and is present

in both the 82C435 and 82A436. Setting this bit to 0 or 1 maps the registers as follows:

Register Name	I/O Address for D0=0	D0=1
CRTC Address Register (82C435/82A436)	3B4h	3D4h
CRTC Data Register (82C435/82A436)	3B5h	3D5h
Feature Control Register (82C435/82A436)	3BAh	3DAh
Input Status Register 1 (82C435/82A436)	3BAh	3DAh

D1 D1 = 0 prevents the CPU from accessing the EGA display memory. D1 = 1 allows such accesses.

D2-D3 D2-D3 bits are output on the CLKSEL0 and CLKSEL1 pins on the 82A436. Typically these are used to externally select the clock source for the 82C435. These bits are present in the 82C435 so that this register can be read correctly.

D4 Disable Internal Video: This bit is used in the 82A436. It is also present in the 82C435 so that this register can be read correctly.

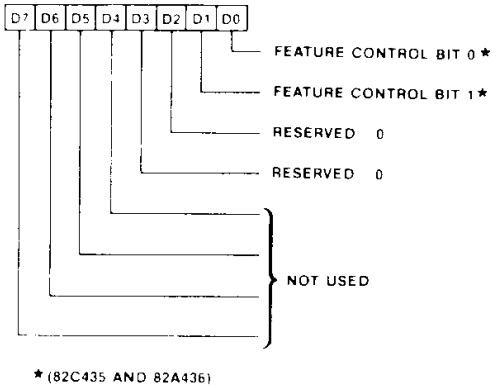
D5 Since the 82C435 does not support 64 Kbytes of display memory (it requires 256 Kbytes) this bit must always be 1.

D6 D6 selects the polarity for the Horizontal Sync pulse.
0 Positive horizontal sync pulse
1 Negative horizontal sync pulse

D7 D7 selects the polarity for the Vertical Sync pulse.
0 Positive vertical sync pulse
1 Negative vertical sync pulse

FEATURE CONTROL REGISTER

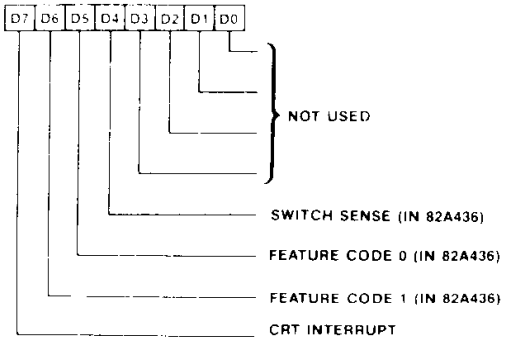
Read/Write Register
I/O Address: 3BAh/3DAh



The Feature Control Register exists in both the 82C435 and the 82A436. This is normally a write only register in the 82A436. It can be read (in the 82C435) by setting the alternate read select bit in the 400 Line Register (CRF9 bit D7= 0) and then reading the CRTC Data Register at offset 0Eh. Feature Control Bits 0 and 1 from this register are also output on 82A436 output pins FCOUT0 and FCOUT1 respectively. These pins are typically used to drive the EGA Features Connecter.

INPUT STATUS REGISTER 0

Read Only Register
I/O Address: 3C2h



Parts of the Input Status Register 0 exist in both the 82C435 and the 82A436. The data path to the CPU from the 82C435 always goes through the 82A436. When the CPU reads this register, the 82A436 reformats the status data put out by the 82C435 and passes the final status to the CPU.

Switch Sense (D4 - in 82A436)

This bit returns the current status of the 82A436 input pin SWITCH to the CPU. Typically, the CPU scans the state of the DIP switches on the EGA board through this bit.

Feature Code 0 and 1 (D5-D6 - in 82A436)

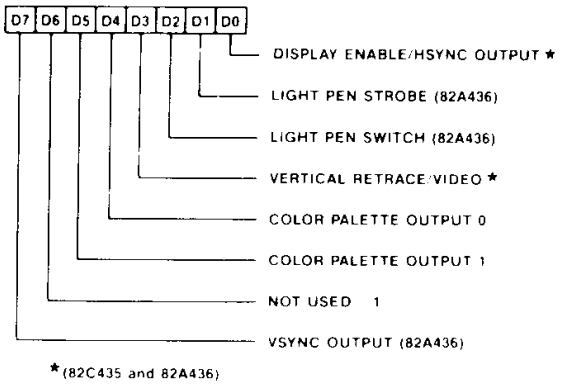
These two bits return the current status of the 82A436 input pins FEATIN0 and FEATIN1 respectively. These bits are typically used to read the status information from the EGA Board Feature Connecter.

CRT Interrupt (D7)

D7 is a reflection of the CRTINT output from the 82C435. This bit is 1 if the CRTINT pin is high. CRTINT is enabled through bit D5 of CR11. Once CRTINT goes active, it can only be reset through bit D4 of CR11.

INPUT STATUS REGISTER I (CGA/HERCULES STATUS REGISTER)

Read Only Register
I/O Address: 3BAh/3DAh



Parts of the Input Status Register I exist in both the 82C435 and the 82A436. The data path to the CPU from the 82C435 always goes through the 82A436. When the CPU reads this register, depending on the current emulation mode, the 82A436 reformats the status data output by the 82C435 and passes the final status to the CPU.

Display Enable/HSYNC Output (D0)

In EGA and CGA modes, D0 is an active low Display Enable signal generated by the 82C435. A logical 0 indicates the active display interval. This bit is returned high during the horizontal and vertical retrace interval. In Hercules emulation mode this bit is driven by the 82A436 and it indicates the current level of the 82C435 Horizontal Sync signal, HIN.

Light Pen Strobe (D1 - 82A436)

D1 is driven by the 82A436 and indicates the state of the Light Pen Latch. This latch is set whenever a valid Light Pen pulse is generated.

Light Pen Switch (D2 - 82A436)

D2 is driven by the 82A436 and indicates the state of the Light Pen Switch (on the Light Pen Connecter.)

Vertical Retrace/Video (D3)

In EGA mode, D3 is an active high vertical retrace signal, which is functionally the same as the active high Vertical Sync output (VIN) from the 82C435 (the polarity of this bit is always positive). In CGA emulation mode, D3 is driven by the 82A436 and is same as the Vertical Sync output from the 82C435. In Hercules emulation mode D3 is driven by the 82A436 and it indicates the current status of the Video (Secondary Blue) signal from the 82C435.

Color Palette Output (D4, D5)

D4 and D5 are two bits of the six bit video output from the color palette. Two of these 6 bits can be selectively read by the CPU through bits D4 and D5 of Input Status Register I. The two output signals to be multiplexed are determined by the contents of the Attributes Color Plane Enable Register (AR12). These bits are valid only in the EGA mode. In the CGA and Hercules modes, the 82A436 always drives these bits high.

Vertical Sync Output (D7)

This bit is valid only in the Hercules emulation mode. In this mode, D7 indicates the current level of the 82C435 Vertical Sync signal (to the monitor). In the EGA and CGA modes, this bit is always high.

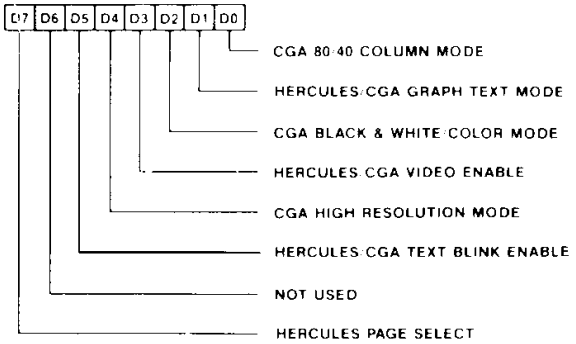
BACKWARD COMPATIBILITY REGISTERS

To complete the register description, there are some additional registers in the 82C435/82A436. These registers are:

I/O Address	Register
3B8h/3D8h	Hercules/CGA Mode Control Register (in 82C435)
3D9h	CGA Color Select Register (in 82C435)
3B9h/3DCh	Set Light Pen Latch (in 82A436)
3BBh/3DBh	Clear Light Pen Latch (in 82A436)
3BFh	Hercules Configuration Register (in 82C435)

HERCULES/CGA MODE CONTROL REGISTER

Read/Write Register
I/O Address: 3B8h/3D8h



All the bits in the Hercules/CGA Mode Control Register are effective only when emulation is in progress (CRFF bit D2 = 1). When CGA emulation is in progress (EGA Misc. Output Register bit D0 = 1), then this register functions as the CGA Mode Register and is located at I/O address 3D8h. When Hercules emulation is in progress (EGA Misc. Output Register bit D0 = 0), then this register functions as the Hercules Mode Register and is located at I/O address 3B8h.

D0 CGA 80/40 Column Mode: This bit is effective only when CGA emulation is in progress. D0 = 0 selects 40 column CGA text mode. D0 = 1 selects 80 column CGA text mode.

D1 Hercules/CGA Graphics/Text Mode: D1 = 0 selects the text mode and D1 = 1 selects the graphics mode. This is effective for both CGA and Hercules emulation modes.

D2 CGA Black & White/Color Mode: This bit is effective only when CGA emulation is in progress. D2 = 1 selects CGA Black & White mode, D2 = 0 selects CGA color mode.

D3 Hercules/CGA Video Enable: D3 = 1 enables the video signals. D3 = 0 blanks the screen. This is effective for both CGA and Hercules emulation modes.

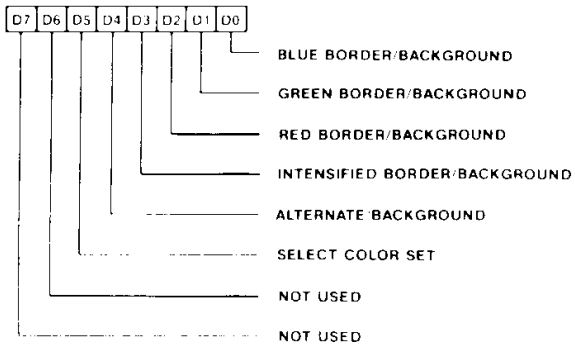
D4 CGA High Resolution Mode: This bit is effective only when CGA emulation is in progress. D4 = 0 selects the 320 * 200 CGA graphics mode, D4 = 1 selects 640 * 200 CGA graphics mode.

D5 Hercules/CGA Text Blink Enable: D5 = 1 enables the character blink attribute. D5 = 0 disables the character blink feature and the blink attribute bit is used to control background intensity. This is effective for both CGA and Hercules emulation modes.

D7 Hercules Page Select: This bit is effective only when Hercules emulation is in progress. D7 = 0 selects the lower part of memory (address B0000h onwards) in the Hercules Graphics Mode. D7 = 1 selects the upper part of the memory (address B8000h onwards).

CGA COLOR SELECT REGISTER

Read/Write Register
I/O Address: 3D9h



This registers serves as the CGA hardware palette register. This register is effective only when emulation is in progress (CRFF bit D2 = 1). This register can be disabled through the Emulation Mode Register (CRFF bit D3 = 0).

D0 Blue Border/Background: Selects blue border in 40*25 CGA text mode. Selects blue background in CGA 320*200 graphics mode. Selects blue foreground in CGA 640*200 graphics mode.

D1 Green Border/Background: Selects green border in 40*25 CGA text mode. Selects green background in CGA 320*200 graphics mode. Selects green foreground in CGA 640*200 graphics mode.

D2 Red Border/Background: Selects red border in 40*25 CGA text mode. Selects red background in CGA 320*200 graphics mode. Selects red foreground in CGA 640*200 graphics mode.

D3 Intensified Border/Background: Selects Intensified border in 40*25 CGA text mode. Selects intensified background in CGA 320*200 graphics mode. Selects Intensified foreground in CGA 640*200 graphics mode.

D4 Alternate/Background: Selects alternate intensified colors in CGA graphics mode. Selects background colors in CGA text modes.

D5 Select Color Set: Selects colors in CGA 320*200 graphics mode. The colors are generated as follows:

D5	Pixel Bit 1	Pixel Bit 0	Color
0	0	0	Background (=D0-D3)
0	0	1	Green
0	1	0	Red
0	1	1	Brown
1	0	0	Background (=D0-D3)
1	0	1	Cyan
1	1	0	Magenta
1	1	1	White

SET LIGHT PEN LATCH (in 82A436)

Write Only Register
I/O Address: 3DCh/3B9h

The Set Light Pen Register is used to trigger the Light Pen from software. In the EGA mode, this is done by an I/O Write to address 3DCh. In CGA mode, the Light Pen is triggered by an I/O Read or I/O Write to address 3DCh. In Hercules mode, this is done by an I/O Write to address 3B9h.

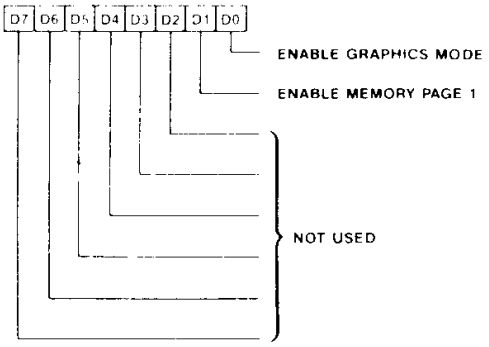
CLEAR LIGHT PEN LATCH (in 82A436)

Write Only Register
I/O Address: 3DBh/3BBh

The Clear Light Pen Register is used to clear the Light Pen Latch. In the EGA mode, this is done by an I/O Write to address 3DBh. In CGA mode, the Light Pen is triggered by an I/O Read or I/O Write to address 3DBh. In Hercules mode, this is done by an I/O Write to address 3BBh.

HERCULES CONFIGURATION REGISTER

Read/Write Register
I/O Address: 3BFh



The Hercules Configuration Register is effective only when Hercules emulation is in progress (CRFF bit D2 = 1) and EGA Misc Output Register bit D0 = 0. Bits D0 and D1 are read at bits D6 and D7 respectively in the Sequencer Address Register (I/O Address 3C4h).

D0 Enable Graphics Mode: D0 = 0 locks the 82C435 in the Hercules/MDA text mode. In this mode, the CPU has access to memory only in the address range B0000h-B0FFFh.

D1 Enable Memory Page 1: D0 = 0 prevents the setting of Page Select bit (D7 in Hercules Mode Control Register). This also restricts memory usage to address B0000h-B7FFFh. D0 = 1 allows setting of the Page Select bit and enables the use of the upper part of the display memory (address B8000h-BFFFFh).

MEMORY ADDRESS GENERATION

The 82C435 serves as a DRAM controller for the 256 Kbytes of display memory required by the EGA. The 82C435 is responsible for DRAM refresh, fetching of display data (text and graphics mode) from the display memory, and controlling CPU accesses to the display memory. All the DRAM control signals are generated by the 82C435. The 82C435 interfaces to the DRAMs using a multiplexed row address/column address/data bus. When the 82C435 accesses the display memory to fetch data to transfer to the screen, the DRAM addresses are generated as required by an internal 16-bit memory address counter (MA0-MA15). All DRAM refreshes are done during the horizontal blanking period. The refresh is done by reading the display memory. The refresh addresses are generated by an internal refresh counter. For CPU accesses to display memory, the 82C435 generates the DRAM row and column addresses as required by the CPU (A0-A16).

The DRAM row/column addresses are generated as follows:

ROW ADDRESSES FOR CPU ACCESS

AA7	**AA6**	**AA5**	**AA4**	**AA3**	**AA2**	**AA1**	**AA0**	
BA7	**BA6**	**BA5**	**BA4**	**BA3**	**BA2**	**BA1**	**BA0**	
A7	A6	A5	A4	A3	A2	A1	A0	No Chaining
A7	A6	A5	A4	A3	A2	A1	A16	Chained & CDSEL0,1=00
A7	A6	A5	A4	A3	A2	A1	PAGESEL	Chained & CDSEL0,1=01, 10,11

COLUMN ADDRESSES FOR CPU ACCESS

AA7	**AA6**	**AA5**	**AA4**	**AA3**	**AA2**	**AA1**	**AA0**
BA7	**BA6**	**BA5**	**BA4**	**BA3**	**BA2**	**BA1**	**BA0**
A15	A8	A13	A12	A11	A10	A9	A14

ROW ADDRESSES FOR CRT ACCESSES (GRAPHICS MODE)

AA7	**AA6**	**AA5**	**AA4**	**AA3**	**AA2**	**AA1**	**AA0**
BA7	**BA6**	**BA5**	**BA4**	**BA3**	**BA2**	**BA1**	**BA0**
MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0

COLUMN ADDRESSES FOR CRT ACCESSES (GRAPHICS MODE)

AA7	**AA6**	**AA5**	**AA4**	**AA3**	**AA2**	**AA1**	**AA0**
BA7	**BA6**	**BA5**	**BA4**	**BA3**	**BA2**	**BA1**	**BA0**
MA15	MA8	MA13	MA12	MA11	MA10	MA9	MA14

ROW ADDRESSES FOR CRT ACCESSES (TEXT MODE)

AA7	**AA6**	**AA5**	**AA4**	**AA3**	**AA2**	**AA1**	**AA0**
MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
BA7	**BA6**	**BA5**	**BA4**	**BA3**	**BA2**	**BA1**	**BA0**
CC2	CC1	CC0	RS4	RS3	RS2	RS1	RS0

COLUMN ADDRESSES FOR CRT ACCESSES (TEXT MODE)

AA7	**AA6**	**AA5**	**AA4**	**AA3**	**AA2**	**AA1**	**AA0**
MA15	MA8	MA13	MA12	MA11	MA10	MA9	MA14
BA7	**BA6**	**BA5**	**BA4**	**BA3**	**BA2**	**BA1**	**BA0**
FS1	CC3	0	CC7	CC6	CC5	CC4	FS0

AAx—Multiplexed Memory Address Bus A on 82C435
BAx—Multiplexed Memory Address Bus B on 82C435
RSx—Character Row Scan Line Counter Outputs
FSx—Font Select Codes as programmed in the Sequencer
MAx—Memory Address/Refresh Counter Outputs
CCx—Character Code

DISPLAY MEMORY REFRESH

The 82C435 automatically generates control signals to refresh the display memory. The refresh is performed using the horizontal blanking period. There is an internal eight bit refresh row address counter in the 82C435. Every horizontal blankng period, this counter is used to generate six read cycles with incrementng row addresses. The user should always program the horizontal parameters in the CRT Controller, so that six refresh cycles per horizontal blanking period is sufficient to meet the refresh specs for the DRAMs being used.

SPLIT SCREEN

The CRT Controller is capable of displaying split screens. Figure 9 shows a split screen display. The two screens, Screen 1 and Screen 2, are created by properly setting the Memory Address Registers (CRC and CRD) and the Line Compare Register (CR18). The CRC and CRD register contents specify the memory address for the first pixel to be displayed on the active screen. The start address for Screen 1 in figure 9 is determined by the contents of the registers CRC and CRD. Split screens are created with the use of Line Compare Register CR18. The internal display memory address counter is cleared when the absolute scan line counter reaches the value equal to the contents of CR18. Thus Screen 2 in figure 9 starts at display memory address 0000H. The linear address generator addresses the display buffer sequentially starting at 0000H. Each subsequent row address is determined by the Offset Register contents as described earlier under register description.

SOFT SCROLL

The CRT Controller offers soft scrolling capability by pre-setting a value in the Preset Scan Register, CR8. Figure 10 shows a typical example of how this can be achieved. As described in the CRT Controller section, the Start Address Registers CRC and CRD define the address of the first pixel that is displayed on the screen.

In the text mode, the start address is the address of the first character which will be displayed in the first row. The Preset Scan Row Register defines the top scan line for the first character row on the screen. By incrementing CR8, the screen will appear to scroll upwards one scan line at a time. When CR8 becomes equal to CR9 (maximum scan line), then CR8 should be reset to 0 and the Start Address Registers (CRC and CRD) should be updated to start with the next character row.

The Preset Scan Register should be set to zero for graphics modes. In this mode the vertical scrolling can be controlled by updating the Start Address Registers only.

CURSOR CONTROL

The height of the CURSOR is programmable through registers CRA and CRB. The memory address of the CURSOR is programmable through registers CRE and CRF. Figure 11 shows how the CURSOR height is controlled by setting the horizontal scan line equal to the contents of CRA and CRB registers.

VERTICAL INTERRUPT

The 82C435 generates an interrupt at the end of a vertical display. The Vertical Display End Register CR12 controls the time when the interrupt becomes active, if the interrupt enable bit was cleared in the Vertical Retrace End Register CR11. The interrupt can be used by the CPU to update the 82C435 during the vertical blanking interval.

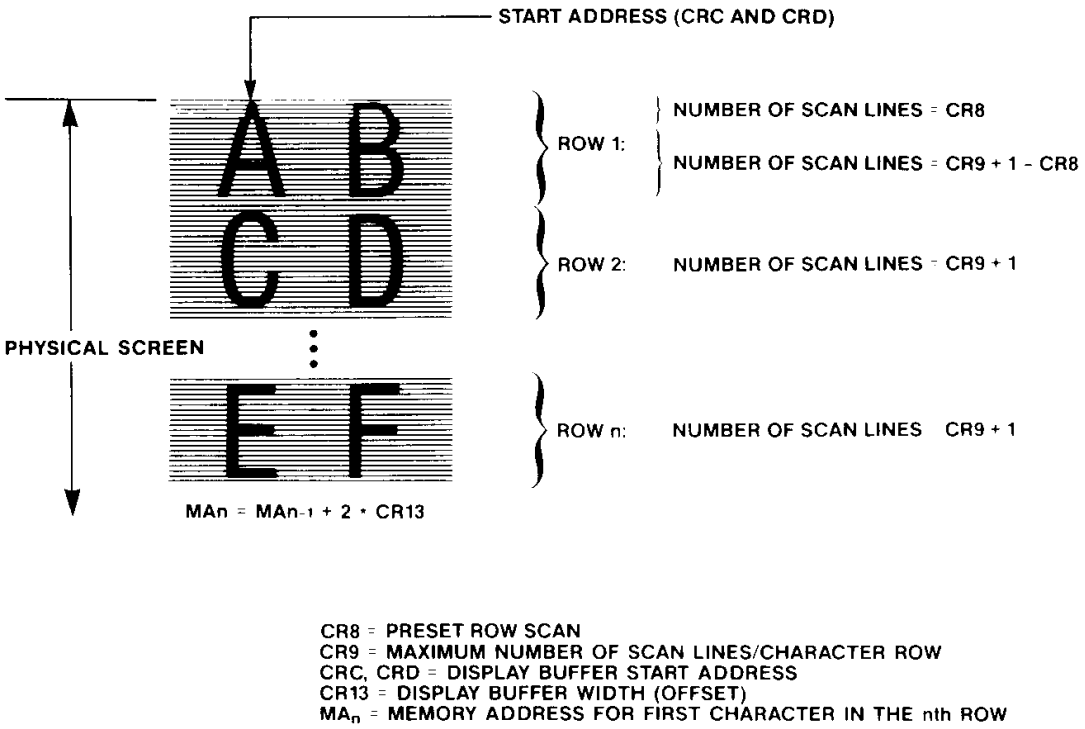


Figure 10. Soft Scrolling With 82C435; Increment CR8 To Move The Screen Up By One Scan Line

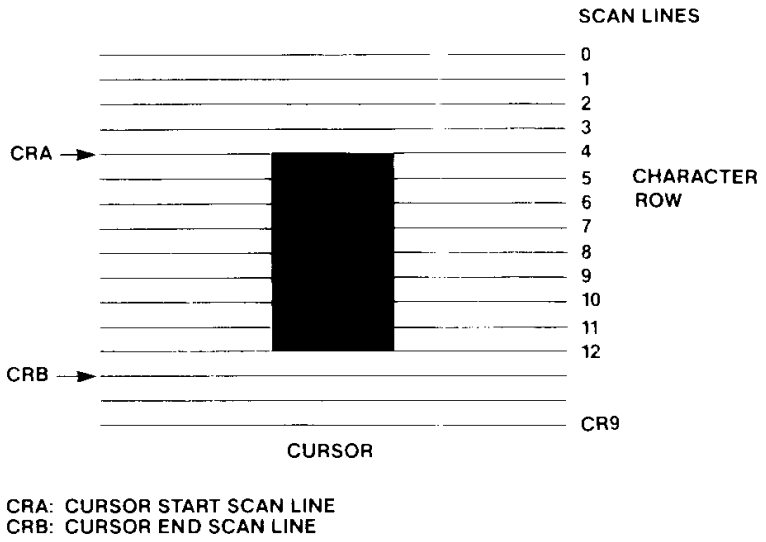


Figure 11. CRTC Cursor Control

CGA/MDA/HERCULES COMPATIBILITY

Compatibility with the CGA, MDA and Hercules display subsystems is required to be compatible with older software that does not support an EGA. There are two levels of compatibility:

a) Compatibility at memory interface and higher level mode selections,

b) Compatibility at direct register level

The 82C435/82A436 allow compatibility at both levels described above.

The memory interfaces required are:

CGA 40 Column Text Mode	16 Kbytes at address B8000h
CGA 80 Column Text Mode	16 Kbytes at address B8000h
CGA 160*100 Graphics Mode	16 Kbytes at address B8000h
CGA 320*200 Graphics Mode	16 Kbytes at address B8000h 2 scan bank format
CGA 640*200 Graphics Mode	16 Kbytes at address B8000h 2 scan bank format
MDA/Hercules Text Mode	4 Kbytes at address B0000h
Hercules Graphics Mode-Half	32 Kbytes at address B0000h 4 scan bank format
Hercules Graphics Mode-Full	64 Kbytes at address B0000h 4 scan bank format

The 82C435 supports text mode memory organizations required by the CGA and the Monochrome/Hercules boards.

From a software point of view, the accesses that the software makes to the hardware can be categorized as follows (in order of frequency of occurrences):

a) software access to display memory - this is done to update the character codes and attributes in the text mode and to set the pixel pattern in the graphics modes.

b) software access to certain hardware registers, these include the CGA Color Select Register (at I/O address 3D9h), the Status Register, the 6845 Cursor Position Registers (Registers 0Eh and 0Fh) and the 6845 Start Address Registers (Registers 0Ch and 0Dh).

c) software access to the other hardware registers, including the mode registers and the video timing (6845 internal) registers.

The 82C435/82A436 provide a direct hardware interface to the software at levels a) and b) described above. Software accesses to the registers at level c) described above are very infrequent. Typically most accesses to these registers is done through the BIOS and the BIOS on the display board should program the EGA registers properly to correspond to the CGA/MDA/Hercules display modes. In the event of some software that directly accesses these registers, the 82C435/82A436 require some assistance from the CPU.

Any software that is configured to run with a CGA/MDA/Hercules board that programs registers on the video boards directly, accesses the registers at I/O addresses 3B8/3D8h Mode Register, 3BFh Hercules Configuration Register, 3B4/3D4h - 6845 Index Register and 3B5/3D5h - 6845 Data Register.

The 6845 Index Register is present in hardware on the 82C435. The EGA CRT Controller registers are mapped to the same address space as the 6845 registers. Of the 18 registers in the 6845, 7 have a direct one-to-one correspondence with the registers on the EGA CRT Controller (Registers 0Ch-11h). The other registers on the 6845 however do not have a one to one correspondence with the EGA CRT Controller registers.

The CPU has to in this case transform the register contents of the 6845 registers and write them into the EGA CRT Controller. To assist in the transform process, the 82C435 has an alternate bank of 11 registers corresponding to 6845 Data Registers 0-08h, 0Ah and 0Bh. These registers are called 6845 Registers. In the emulation mode all CPU

accesses to I/O address 3B5h/3D5h (6845/ CRTC Data Register) are directed to the CRT Controller Register or the 6845 registers (or both) depending on the contents of the Emulation Mode Register in the 82C435. Whenever a 6845 register is written into, a trap to the CPU is generated in the form of a Non-Maskable Interrupt. The Emulation Mode Register also enables or disables such traps. On a write to a 6845 register, a bit is also set in one of two Tag Register in the 82C435. There is one bit in the Tag Registers for each of the 6845 registers, Mode Control Registers and the unique EGA-only Registers. On receipt of an NMI, the CPU should first read the TAG Registers which will indicate which register access generated the trap and requires emulation help. This can also be used to automatically switch from one emulation mode to another emulation mode or to the normal EGA mode. If none of the bits in the Tag Registers are set, it means that the NMI was not generated by the video board but by some other source (eg parity error). The CPU should then be directed to the old NMI handling routine. The emulation software when loaded, redirects the PC NMI vector to point to the emulation software. The old NMI vector can be stored in temporary storage registers in the 82A436 allowing for a safe way to store the old NMI vector.

Traps to the CPU can also be selectively enabled on accesses to the CGA/MDA/ Hercules Mode Registers, the CGA Color Palette and the unique EGA-only Registers. Thus it is possible to let the board automatically detect if software wants to use an EGA/CGA/MDA/Hercules modes on the board. It is also possible to disable all the emulation and lock the board in the 100% EGA mode. One advantage of using the NMI to trap CPU accesses to the 6845 is to allow CGA text mode emulation on the enhanced 350 scan line monitor. In this case although the software selects a 200 scan line display, the emulation software can still cause higher quality character to appear on the screen.

6845 REGISTERS

INDEX	REGISTER
0	bits 6-0 of Horizontal Total Register
1	bits 6-0 of Horizontal Displayed Register
2	bits 4-0 of Horizontal Sync Position Register
3	bits 7-0 of Horizontal Sync Width Register
4	bits 6-0 of Vertical Total Register
5	bits 4-0 of Vertical Total Adjust Register
6	bits 6-0 of Vertical Displayed Register
7	bits 6-0 of Vertical Sync Position Register
8	bits 5, 4, 1 and 0 of Interlace Mode Register
Ah	bits 6-0 of Cursor Start Register
Bh	bits 4-0 of Cursor End Register

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{DD}	—	7.0	V
Input Voltage	V_I	-0.5	V_{DD} + 0.5	V
Output Voltage	V_O	-0.5	V_{DD} + 0.5	V
Operating Temperature	T_{OP}	-25	85	C
Storage Temperature	T_{STG}	-40	125	C

82C435 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{DD}	4.75	5.25	V
Ambient Temperature	T_A	0	70	°C

82C435 DC Characteristics

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL1} = 2mA[1] I_{OL2} = 4mA[2] I_{OL3} = 8mA[3] I_{OL4} = 4mA[4]	V_{OL}		0.45	V
Output High Voltage I_{OH1} = 2mA[1] I_{OH2} = 4mA[2] I_{OH3} = 8mA[3]	V_{OH}	3.5		V
Input Leakage Current	I_{IL}	-100	+100	μA
Power Supply Current @ 25MHz CLKIN, 0C	I_{CC}		100	mA
Output High Impedence Leakage $0.45 < V_{PIN} < V_{DD}$	I_{OZ}	-100	+100	μA

NOTES:

1. 2 mA source and sink drive on pins ERMEN, CDSEL0-1, CCLK, DOTCLK, VALRAD
2. 4 mA source and sink drive on pins SLOUT, WE0-3, OE02, OE13, AA_{0-7}, BA_{0-7}, R, G, B, RS, BS/V, GS/I
3. 8 mA source and sink drive on pins CAS, RAS , BLANK, HIN, VIN, CRTINT, TRAP, RDY
4. 4 mA sink drive only (open drain) on pins $DATA_{0-7}$

82C435 AC Characteristics

(T_A = 0°C-70°C, V_{DD} = 5V ±5%)

CLKIN Timings

Parameter	Symbol	Min.(ns)
CLKIN Period	t_C	40
CLKIN High time	t_{ch}	t_c/2-5%
CLKIN Low time	t_{cl}	t_c/2-5%

Video Timings

Parameter	Symbol	Max.(ns)
VIN, BLANK delay from CLKIN	t_{vin}	150
HIN delay from CLKIN	t_{hin}	100
VIDEO delay from CLKIN	t_{vid}	66

Other Timings

Parameter	Symbol	Min.(ns)
LPENSTB Pulse Width	t19	100
RESET Pulse Width	t20	$64t_c$*

* In CLKIN/2 mode, t20 must be 128 t_c minimum.

I/O Bus Timings

Parameter	Symbol	Min.(ns)	Max.(ns)
$\overline{\text{MIORD}}$, $\overline{\text{MIOWR}}$ Pulse Width	t1	200	
$\overline{\text{MIORD}}$, $\overline{\text{MIOWR}}$ to $\overline{\text{RDY}}$ Low delay	t2		50
Address setup to $\overline{\text{MIOWR}}$ (I/O Write)	t3	80	
Address hold from $\overline{\text{MIOWR}}$ (I/O Write)	t4	80	
Address setup to $\overline{\text{MIORD}}$ (I/O Read)	t3	20	
Address hold from $\overline{\text{MIORD}}$ (I/O Read)	t4	20	
Address setup to $\overline{\text{MIORD}}$/$\overline{\text{MIOWR}}$ (Memory)	t3	20	
Address hold from $\overline{\text{RDY}}$ (Memory Read/Write)	t4a	0	
Trap delay from $\overline{\text{MIOWR}}$	t5		150
MEMIO setup to $\overline{\text{MIORD}}$/$\overline{\text{MIOWR}}$	t6	20	

I/O Bus Timings (Continued)

Parameter	Symbol	Min.(ns)	Max.(ns)
MEMIO hold from $\overline{MIORD}$/$\overline{MIOWR}$	t7	5	
I/O Write Data setup to $\overline{MIOWR}$	t8	45	
I/O Write Data hold from $\overline{MIOWR}$	t9	60	
I/O Read Data delay from $\overline{MIORD}$	t10		150
I/O Write Data hold from $\overline{MIORD}$	t11	5	90
$\overline{RDY}$ high time	t12	$0.5t_c$	
Memory Read Data setup to $\overline{RDY}$	t13	$1.5t_c$	
Memory Read Data hold from $\overline{MIORD}$	t14	20	
Memory Write Data setup to $\overline{RDY}$	t15	$6t_c$	
Memory Write Data hold from $\overline{RDY}$	t16	$-1.5t_c$	
VALRAD delay from Address	t17		60
CDSEL0,1 delay from $\overline{MIOWR}$	t18		200
$\overline{RDY}$ width	t21	$6t_c$	$42t_c$

DRAM Timings High CPU Bandwidth Mode

Parameter	Symbol	Min.(ns)	Max.(ns)
Read/Write Cycle time (read)	t_{rc}	$5t_c$	
$\overline{RAS}$ Pulse Width (read)	t_{ras}	$3t_c$ -8	
Read/Write Cycle time (write)	t_{rc}	$6t_c$	
$\overline{RAS}$ Pulse Width (write)	t_{ras}	$4t_c$ -8	
Column Address Hold from $\overline{RAS}$	t_{ar}	$1.5t_c$ +10	
$\overline{RAS}$ precharge	t_{rp}	$2t_c$ -8	
$\overline{CAS}$ to $\overline{RAS}$ precharge	t_{crp}	t_c +3	
$\overline{CAS}$ hold from $\overline{RAS}$	t_{csh}	$4t_c$ -3	
$\overline{RAS}$ to $\overline{CAS}$ delay	t_{rcd}	$0.5t_c$ +4	
$\overline{RAS}$ hold from $\overline{CAS}$	t_{rsh}	$2.5t_c$ -28	
$\overline{CAS}$ Precharge	t_{cpn}	$1.5t_c$ +7	
$\overline{CAS}$ Pulse Width	t_{cas}	$3.5t_c$ -23	
Row Address Setup to $\overline{RAS}$	t_{asr}	$0.5t_c$ -5	
Column Address setup to $\overline{CAS}$	t_{asc}	1	
Row Address hold from $\overline{RAS}$	t_{rah}	$0.5t_c$	
Column Address hold from $\overline{CAS}$	t_{cah}	t_c	

DRAM Timings High CPU Bandwidth Mode (Continued)

Parameter	Symbol	Min.(ns)	Max.(ns)
Data Access time from $\overline{OE}$	t_{oea}		t_c -10
Data Access time from $\overline{CAS}$	t_{cac}		$2t_c$ -26
Data Access time from $\overline{RAS}$	t_{rac}		$2.5t_c$ -3
$\overline{WE}$ Pulse Width	t_{wp}	t_c -7	
Write Data Setup to $\overline{WE}$	t_{ds}	0	
Write Data Hold from $\overline{WE}$	t_{dh}	t_c -5	
Write Data Hold from $\overline{RAS}$	t_{dhr}	$2.5t_c$ -10	
$\overline{WE}$ hold from $\overline{CAS}$	t_{wch}	$2t_c$ -7	
$\overline{WE}$ hold from $\overline{RAS}$	t_{wcr}	$2.5t_c$ +2	
$\overline{WE}$ lead to $\overline{RAS}$	t_{rwl}	t_c -11	
$\overline{WE}$ lead to $\overline{CAS}$	t_{cwl}	t_c -6	

DRAM Timings Low CPU Bandwidth Mode

Parameter	Symbol	Min.(ns)	Max.(ns)
Read/Write Cycle time (read)	t_{rc}	$6t_c$	
$\overline{RAS}$ Pulse Width (read)	t_{ras}	$3.5t_c$ -1	
Read/Write Cycle time (write)	t_{rc}	$8t_c$	
$\overline{RAS}$ Pulse Width (write)	t_{ras}	$5.5t_c$ -1	
Column Address Hold from $\overline{RAS}$	t_{ar}	$2.5t_c$ +8	
$\overline{RAS}$ precharge	t_{rp}	$2.5t_c$ -2	
$\overline{CAS}$ to $\overline{RAS}$ precharge	t_{crp}	t_c +3	
$\overline{CAS}$ hold from $\overline{RAS}$	t_{csh}	$5t_c$ -3	
$\overline{RAS}$ to $\overline{CAS}$ delay	t_{rcd}	$0.5t_c$ +5	
$\overline{RAS}$ hold from $\overline{CAS}$	t_{rsh}	$3t_c$ -8	
$\overline{CAS}$ Precharge	t_{cpn}	$1.5t_c$ +6	
$\overline{CAS}$ Pulse Width	t_{cas}	$4.5t_c$ -13	
Row Address Setup to $\overline{RAS}$	t_{asr}	$0.5t_c$ -5	
Column Address setup to $\overline{CAS}$	t_{asc}	1	
Row Address hold from $\overline{RAS}$	t_{rah}	$0.5t_c$	
Column Address hold from $\overline{CAS}$	t_{cah}	$2t_c$	
Data Access time from $\overline{OE}$	t_{oea}		t_c -10

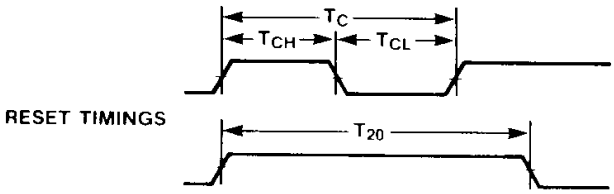
DRAM Timings Low CPU Bandwidth Mode (Continued)

Parameter	Symbol	Min.(ns)	Max.(ns)
Data Access time from $\overline{CAS}$	t_{cac}		$2t_c$ -16
Data Access time from $\overline{RAS}$	t_{rac}		$3.5t_c$ -6
$\overline{WE}$ Pulse Width	t_{wp}	$1.5t_c$ -23	
Write Data Setup to $\overline{WE}$	t_{ds}	0	
Write Data Hold from $\overline{WE}$	t_{dh}	t_c -5	
Write Data Hold from $\overline{RAS}$	t_{dhr}	$2.5t_c$ -10	
$\overline{WE}$ hold from $\overline{CAS}$	t_{wch}	$3.5t_c$ -14	
$\overline{WE}$ hold from $\overline{RAS}$	t_{wcr}	$4t_c$ -4	
$\overline{WE}$ lead to $\overline{RAS}$	t_{rwl}	$1.5t_c$ -3	
$\overline{WE}$ lead to $\overline{CAS}$	t_{cwl}	$2.5t_c$ -8	

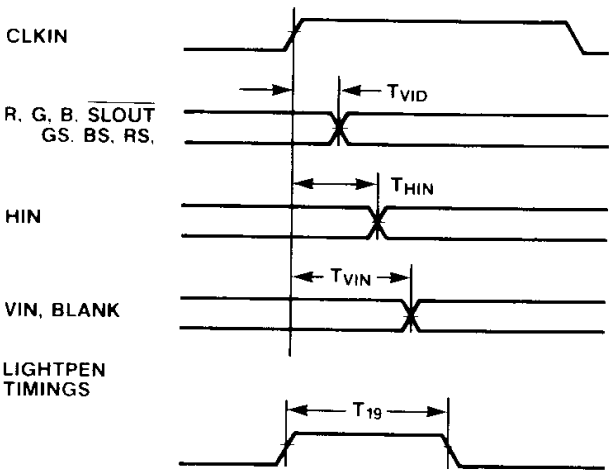
Compatibility with DRAMs

RAS access time	Maximum CLKIN frequency for	
	High CPU Bandwidth Mode	Low CPU Bandwidth Mode
150ns	16.5MHz	20MHz
120ns	20MHz	25MHz
100ns	20MHz	25MHz

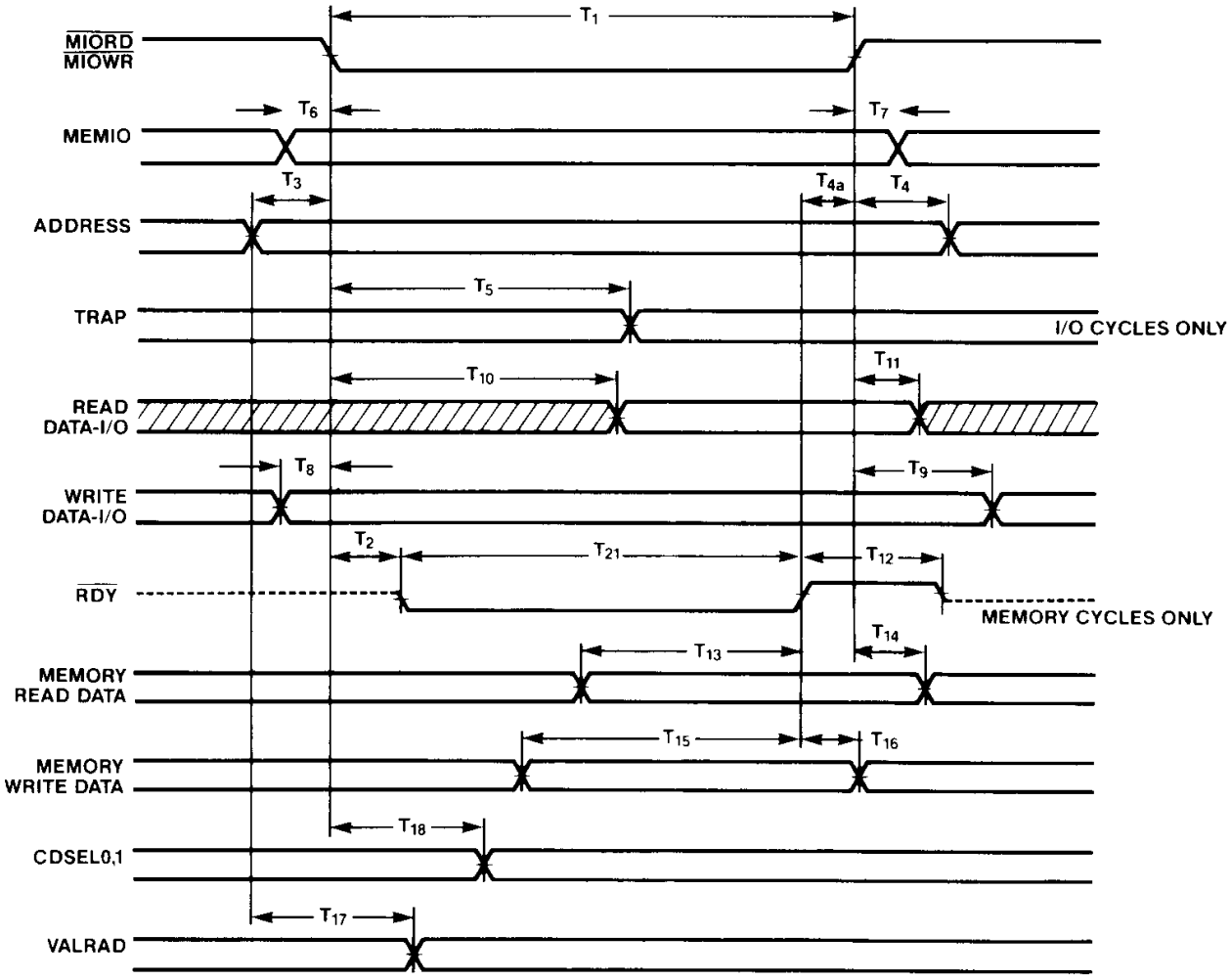
CLKIN TIMINGS



VIDEO TIMINGS

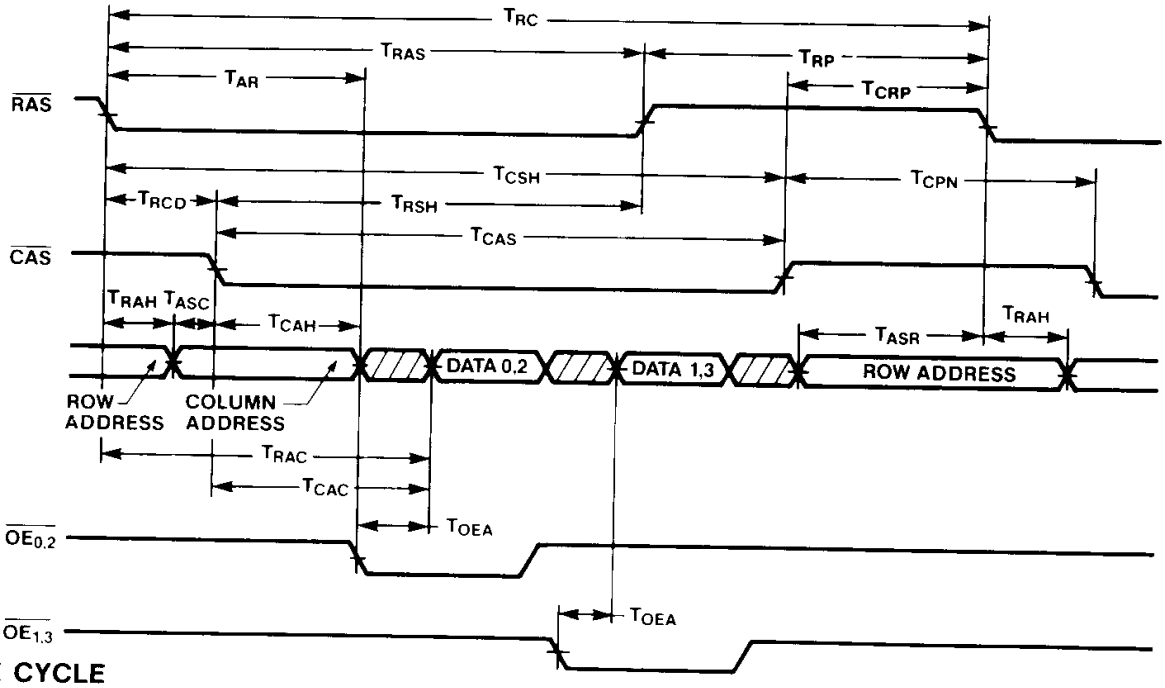


I/O BUS TIMINGS

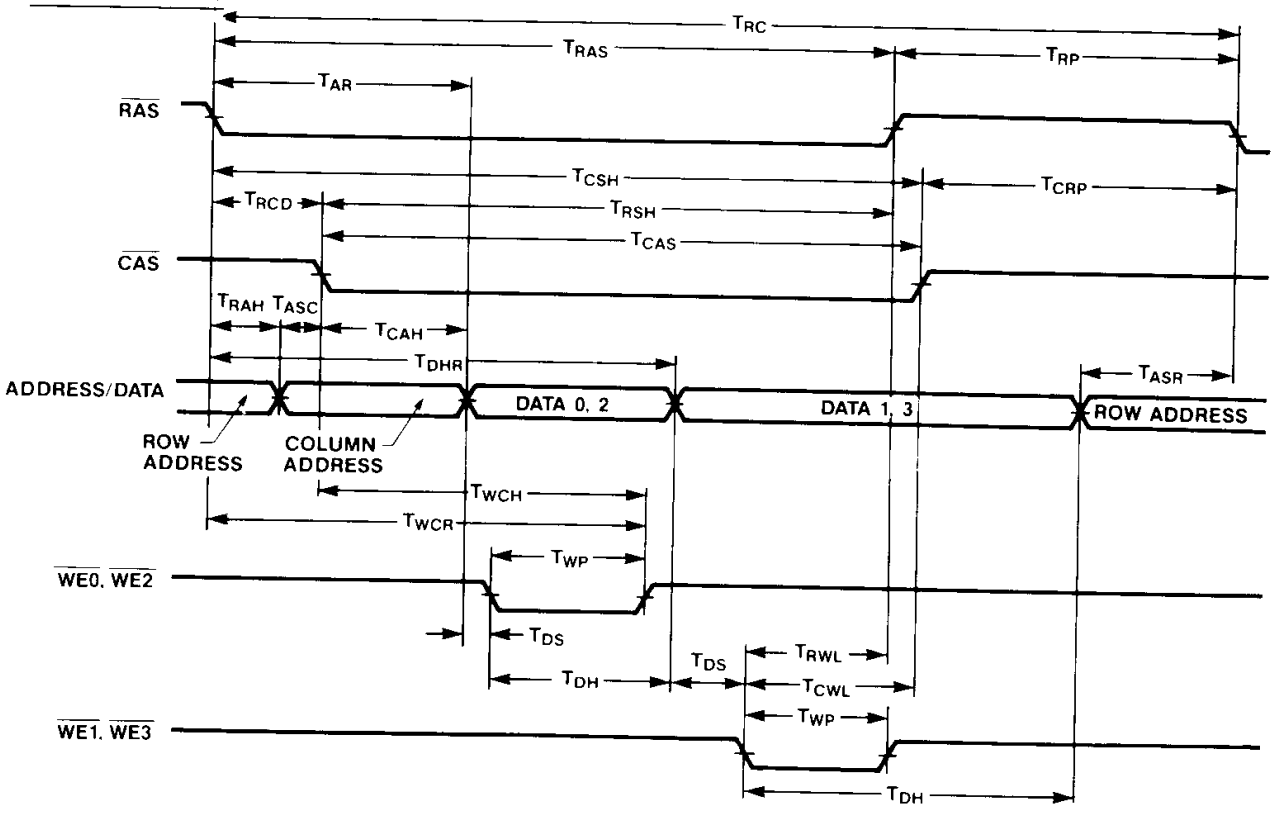


READ CYCLE

DRAM TIMINGS

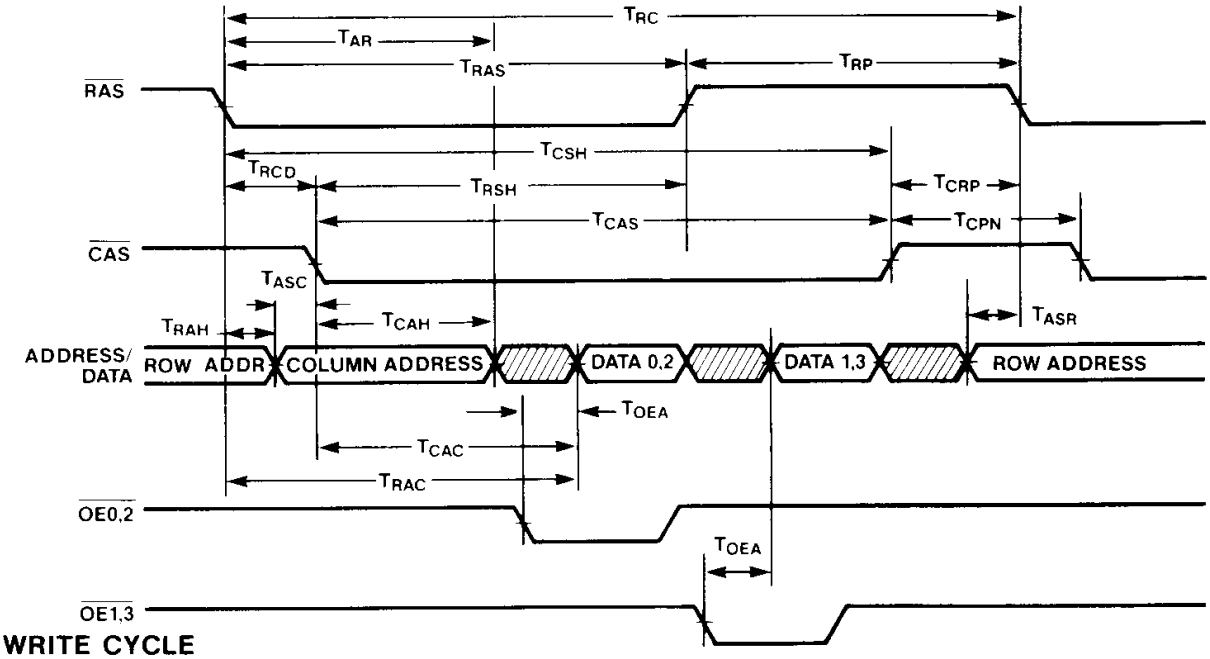


WRITE CYCLE

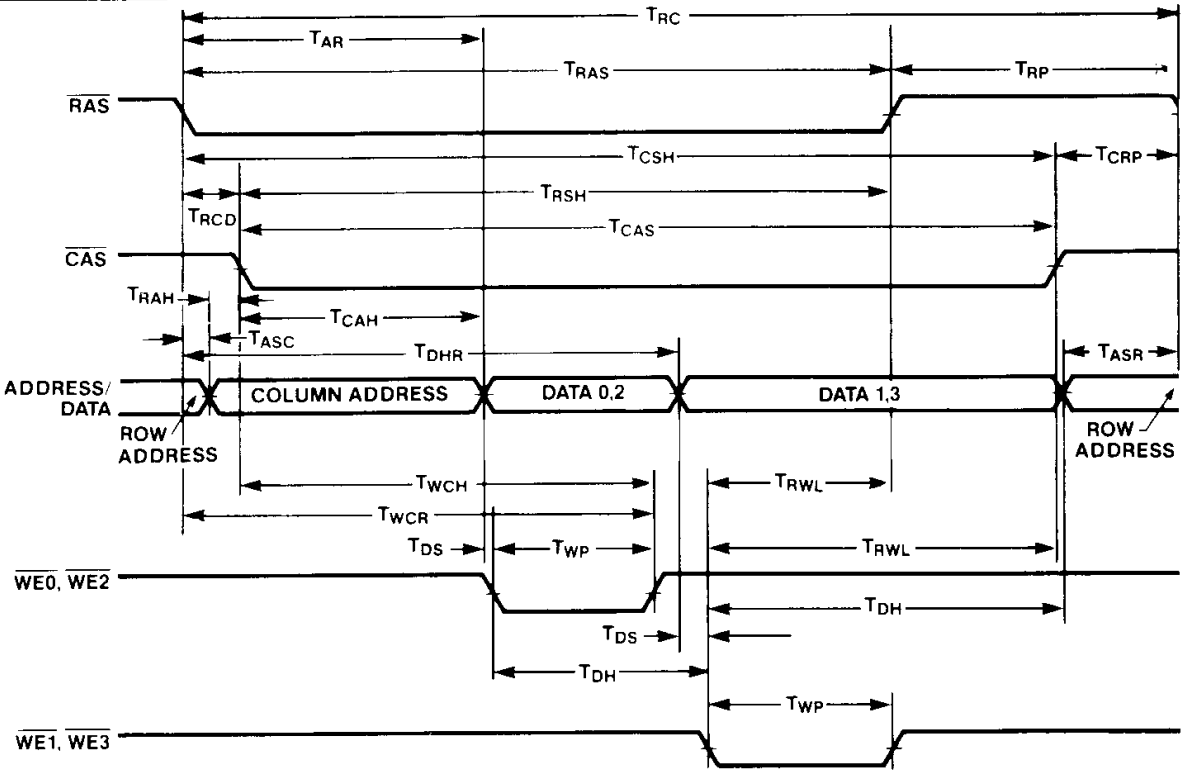


READ CYCLE

DRAM TIMINGS



WRITE CYCLE



82C435—38MHz AC Timing Characteristics

(T_A = 0°C–70°C, V_{DD} = 5V ±5%)

CLKIN Timings

Parameter	Symbol	Min.(ns)
CLKIN Period	t_C	26
CLKIN High time	t_{ch}	t_c/2-5%
CLKIN Low time	t_{cl}	t_c/2-5%

Video Timings

Parameter	Symbol	Min.(ns)	Max.(ns)
VIN, BLANK delay from CLKIN	t_{vin}		150
HIN delay from CLKIN	t_{hin}		150
R,G,B,RS,GS,BS delay from CLKIN	t_{vid}	5	30
SLOUT delay from CLKIN	t_{vid}	5	66

Other Timings

Parameter	Symbol	Min.(ns)	Max.(ns)
LPENSTB Pulse Width	t19	100	
RESET Pulse Width	t20	64t_c*	

* In CLKIN/2 mode, t20 must be 128 t_c minimum.

I/O Bus Timings

Parameter	Symbol	Min.(ns)	Max.(ns)
$\overline{\text{MIORD}}$, $\overline{\text{MIOWR}}$ Pulse Width	t1	200	
$\overline{\text{MIORD}}$, $\overline{\text{MIOWR}}$ to $\overline{\text{RDY}}$ Low delay	t2		50
Address setup to $\overline{\text{MIOWR}}$ (I/O Write)	t3	80	
Address hold from $\overline{\text{MIOWR}}$ (I/O Write)	t4	80	
Address setup to $\overline{\text{MIORD}}$ (I/O Read)	t3	20	
Address hold from $\overline{\text{MIORD}}$ (I/O Read)	t4	20	
Memory Address setup to $\overline{\text{MIORD}}$, $\overline{\text{MIOWR}}$	t3	20	
$\overline{\text{MIORD}}$,$\overline{\text{MIOWR}}$ hold from $\overline{\text{RDY}}$ (Memory)	t4a	0	
Trap delay from $\overline{\text{MIORD}}$,$\overline{\text{MIOWR}}$	t5		150

I/O Bus Timings (Continued)

Parameter	Symbol	Min.(ns)	Max.(ns)
MEMIO setup to $\overline{\text{MIORD}}$,$\overline{\text{MIOWR}}$	t6	20	
MEMIO hold from $\overline{\text{MIORD}}$,$\overline{\text{MIOWR}}$	t7	5	
I/O Write Data setup to $\overline{\text{MIOWR}}$	t8	45	
I/O Write Data hold from $\overline{\text{MIOWR}}$	t9	60	
I/O Read Data delay from $\overline{\text{MIORD}}$	t10		150
I/O Write Data hold from $\overline{\text{MIORD}}$	t11	5	100
$\overline{\text{RDY}}$ high time	t12	$0.5t_c$	
Memory Read Data setup to $\overline{\text{RDY}}$	t13	$1.5t_c$	
Memory Read Data hold from $\overline{\text{RDY}}$	t14	20	
Memory Write Data setup to $\overline{\text{RDY}}$	t15	$6t_c$	
Memory Write Data hold from $\overline{\text{RDY}}$	t16	$-1.5t_c$	
VALRAD delay from Address	t17		60
$\overline{\text{RDY}}$ width	t21	$6t_c$	$42t_c$

DRAM Timings High CPU Bandwidth Mode

Parameter	Symbol	Min.(ns)	Max.(ns)	Min.(ns)	Max.(ns)
		8 dot mode		9 dot mode	
Read/Write Cycle time (read)	t_{rc}	$5t_c$		$5t_c$	
$\overline{\text{RAS}}$ Pulse Width (read)	t_{ras}	$3t_c$ -8		$3t_c$	
Read/Write Cycle time (write)	t_{rc}	$6t_c$		$8t_c$	—
$\overline{\text{RAS}}$ Pulse Width (write)	t_{ras}	$4t_c$ -8		$4t_c$	
Column Address Hold from $\overline{\text{RAS}}$	t_{ar}	$1.5t_c$ +10		$1.5t_c$ +10	
$\overline{\text{RAS}}$ precharge	t_{rp}	$2t_c$ -2		$2t_c$ -2	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge	t_{crp}	t_c +1		t_c +1	
$\overline{\text{CAS}}$ hold from $\overline{\text{RAS}}$	t_{csh}	$4t_c$ -5		$4t_c$ -5	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay	t_{rcd}	$0.5t_c$ +4		$0.5t_c$ +4	
$\overline{\text{RAS}}$ hold from $\overline{\text{CAS}}$	t_{rsh}	$2.5t_c$ -28		$2.5t_c$ -28	
$\overline{\text{CAS}}$ Precharge	t_{cpn}	$1.5t_c$ +7		$1.5t_c$ +7	
$\overline{\text{CAS}}$ Pulse Width	t_{cas}	$3.5t_c$ -23		$3.5t_c$ -23	
Row Address Setup to $\overline{\text{RAS}}$	t_{asr}	$0.5t_c$ -11		$0.5t_c$ -11	
Column Address setup to $\overline{\text{CAS}}$	t_{asc}	1		1	
Row Address hold from $\overline{\text{RAS}}$	t_{rah}	$0.5t_c$		$0.5t_c$	

DRAM Timings High CPU Bandwidth Mode (Continued)

Parameter	Symbol	Min.(ns)	Max.(ns)	Min.(ns)	Max.(ns)
		8 dot mode		9 dot mode	
Column Address hold from $\overline{CAS}$	t_{cah}	t_c		t_c	
Data Access time from $\overline{OE}$	t_{oea}		t_c -10		t_c -10
Data Access time from $\overline{CAS}$	t_{cac}		$2t_c$ -26		$2t_c$ -26
Data Access time from $\overline{RAS}$	t_{rac}		$2.5t_c$ -3		$2.5t_c$ -3
$\overline{WE}$ Pulse Width	t_{wp}	t_c -7		t_c -7	
Write Data Setup to $\overline{WE}$	t_{ds}	0		0	
Write Data Hold from $\overline{WE}$	t_{dh}	t_c -5		t_c -5	
Write Data Hold from $\overline{RAS}$	t_{dhr}	$2.5t_c$ -10		$2.5t_c$ -10	
$\overline{WE}$ hold from $\overline{CAS}$	t_{wch}	$2t_c$ -7		$2t_c$ -7	
$\overline{WE}$ hold from $\overline{RAS}$	t_{wcr}	$2.5t_c$ +2		$2.5t_c$ +2	

DRAM Timings Low CPU Bandwidth Mode

Parameter	Symbol	Min.(ns)	Max.(ns)	Min.(ns)	Max.(ns)
		8 dot mode		9 dot mode	
Read/Write Cycle time (read)	t_{rc}	$6t_c$		$7t_c$	
$\overline{RAS}$ Pulse Width (read)	t_{ras}	$3.5t_c$ -1		$4.5t_c$ -1	
Read/Write Cycle time (write)	t_{rc}	$8t_c$		$8t_c$	
$\overline{RAS}$ Pulse Width (write)	t_{ras}	$5.5t_c$ -1		$5.5t_c$ -1	
Column Address Hold from $\overline{RAS}$	t_{ar}	$2.5t_c$ +8		$2.5t_c$ +8	
$\overline{RAS}$ precharge	t_{rp}	$2.5t_c$ -2		$2.5t_c$ -2	
$\overline{CAS}$ to $\overline{RAS}$ precharge	t_{crp}	t_c +1		t_c +1	
$\overline{CAS}$ hold from $\overline{RAS}$	t_{csh}	$5t_c$ -5		$5t_c$ -5	
$\overline{RAS}$ to $\overline{CAS}$ delay	t_{rcd}	$0.5t_c$ +7		$0.5t_c$ +7	
$\overline{RAS}$ hold from $\overline{CAS}$	t_{rsh}	$3t_c$ -8		$3t_c$ -8	
$\overline{CAS}$ Precharge	t_{cpn}	$1.5t_c$ +6		$1.5t_c$ +6	
$\overline{CAS}$ Pulse Width	t_{cas}	$4.5t_c$ -13		$4.5t_c$ -13	
Row Address Setup to $\overline{RAS}$	t_{asr}	$0.5t_c$ -11			$0.5t_c$ -11
Column Address setup to $\overline{CAS}$	t_{asc}	1		1	
Row Address hold from $\overline{RAS}$	t_{rah}	$0.5t_c$		$0.5t_c$	
Column Address hold from $\overline{CAS}$	t_{cah}	$2t_c$		$2t_c$	
Data Access time from $\overline{OE}$	t_{oea}		t_c -6		t_c -6

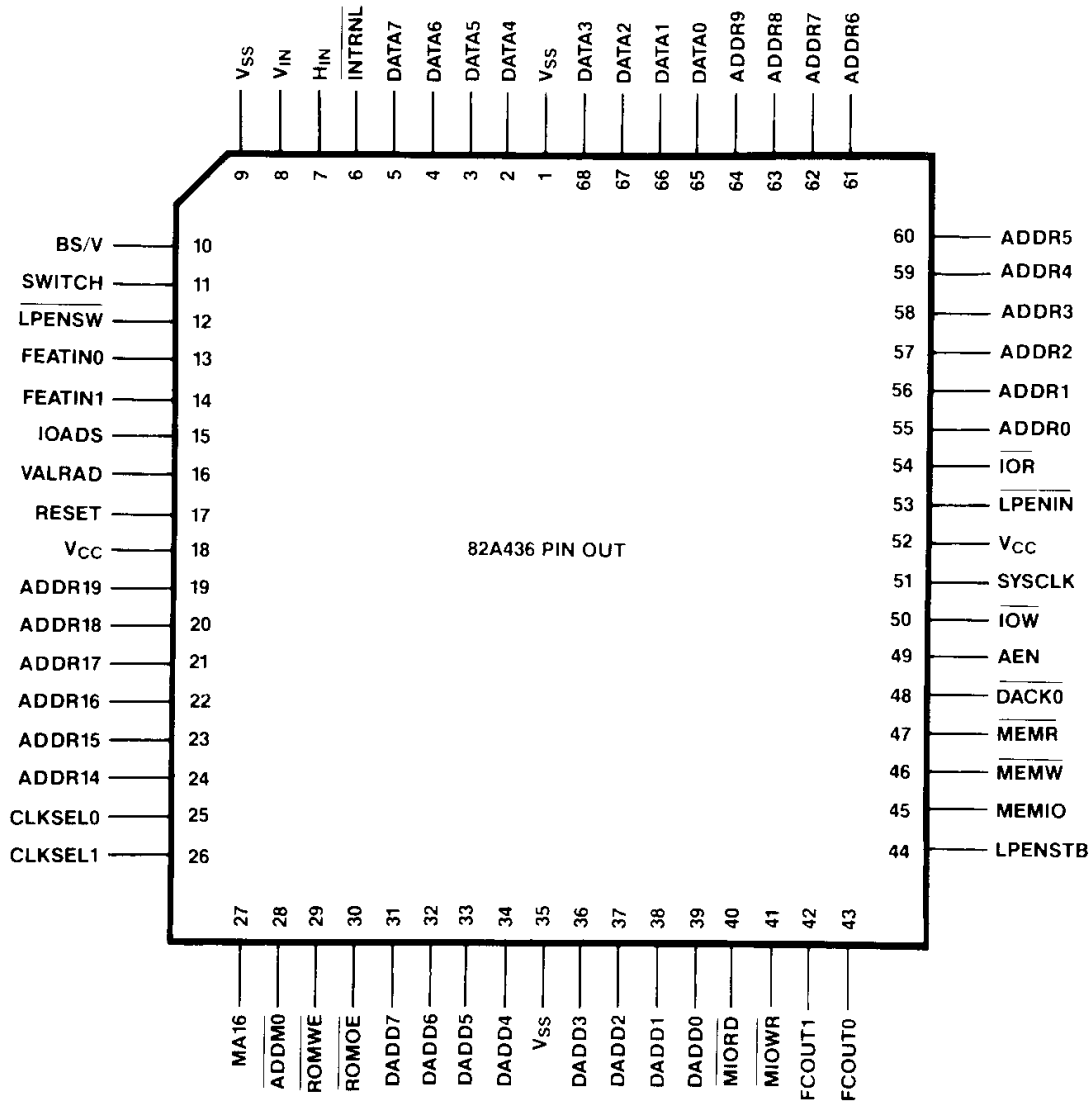
DRAM Timings Low CPU Bandwidth Mode (Continued)

Parameter	Symbol	Min.(ns)	Max.(ns)	Min.(ns)	Max.(ns)
		8 dot mode		9 dot mode	
Data Access time from $\overline{CAS}$	t_{cac}		$2t_c$ -10		$2t_c$ -10
Data Access time from $\overline{RAS}$	t_{rac}		$3.5t_c$ -6		$3.5t_c$ -6
$\overline{WE}$ Pulse Width	t_{wp}	$1.5t_c$ -15		$1.5t_c$ -15	
Write Data Setup to $\overline{WE}$	t_{ds}	0		0	
Write Data Hold from $\overline{WE}$	t_{dh}	t_c -2		t_c -2	
Write Data Hold from $\overline{RAS}$	t_{dhr}	$2.5t_c$ +3		$2.5t_c$ +3	
$\overline{WE}$ hold from $\overline{CAS}$	t_{wch}	$3.5t_c$ -14		$3.5t_c$ -14	
$\overline{WE}$ hold from $\overline{RAS}$	t_{wcr}	$4t_c$ -4		$4t_c$ -4	

Compatibility with DRAMs

RAS access time	Maximum CLKIN frequency for	
	High CPU Bandwidth Mode	Low CPU Bandwidth Mode
150ns	16.5MHz	20MHz
120ns	20MHz	27MHz
100ns	21.5MHz	30MHz

DRAM Refresh Interval (ms) = $43000/(V_r * V_1)$
V_r = Vertical Refresh Rate
V_1 = Total Number of lines/frame (including retrace)



82A436 Pin Description

Pin No.	Pin Type	Symbol	Description
55	I	ADDR0	SYSTEM ADDRESS bits 0-9 and 14-19. These bits are used for addressing the display memory and I/O operations. ADDR0-ADDR9 are I/O and memory addresses. ADDR14-ADDR19 are memory addresses only.
56	I	ADDR1	
57	I	ADDR2	
58	I	ADDR3	
59	I	ADDR4	
60	I	ADDR5	
61	I	ADDR6	
62	I	ADDR7	
63	I	ADDR8	
64	I	ADDR9	
24	I	ADDR14	
23	I	ADDR15	
22	I	ADDR16	
21	I	ADDR17	
20	I	ADDR18	
19	I	ADDR19	
65	I/O	DATA0	SYSTEM DATA BUS bits 0-7. These bits are used to transfer data to and from the CPU data bus.
66	I/O	DATA1	
67	I/O	DATA2	
68	I/O	DATA3	
2	I/O	DATA4	
3	I/O	DATA5	
4	I/O	DATA6	
5	I/O	DATA7	
47	I	$\overline{\text{MEMR}}$	MEMORY READ. $\overline{\text{MEMR}}$ is an active low input from the system bus. It is used by the CPU to read display memory and the EGA BIOS ROM in conjunction with the 82C435.
46	I	$\overline{\text{MEMW}}$	MEMORY WRITE. $\overline{\text{MEMW}}$ is an active low input from the system bus. It isused to write into the display memory and the EGA BIOS ROM in conjunction with the 82C435.
54	I	$\overline{\text{IOR}}$	I/O READ. $\overline{\text{IOR}}$ is an active low signal from the system bus. It is used to read the 82C435 and 82A436 registers.
50	I	$\overline{\text{IOW}}$	I/O WRITE. $\overline{\text{IOW}}$ is an active low signal from the system bus. It is used to write to the 82C435 and 82A436 registers.
48	I	$\overline{\text{DACK0}}$	DMA ACKNOWLEDGE. $\overline{\text{DACK0}}$ is an active low input from the system bus used to acknowledge DMA requests. It disables all memory read and memory write operations ($\overline{\text{MEMR}}$ and $\overline{\text{MEMW}}$) to the 82C435 and 82A436.

82A436 Pin Description (Continued)

Pin No.	Pin Type	Symbol	Description
49	I	AEN	ADDRESS ENABLE. AEN is an input from the system bus used to disable devices from the I/O channel to allow DMA transfers to take place.
17	I	RESET	RESET is an active high input, from the system bus used to reset the Miscellaneous Output Register (I/O address 3C2h), the Feature Control Register (I/O address 3BAh/3DAh) and the Emulation Mode Register (I/O address 3B5h/3D5h).
51	I	SYSCLK	SYSTEM CLOCK. SYSCLK is the I/O bus clock and is used to synchronize $\overline{IOW}$.
53	I	$\overline{LPENIN}$	LIGHT PEN INPUT. $\overline{LPENIN}$ is a negative edge triggered input which sets bit 1 (LIGHT PEN STROBE) in the Input Status Register 1 (I/O address 3BAh/3DAh). 0 = light pen trigger has not been set 1 = light pen trigger has been set A low level on $\overline{LPENIN}$ also generates a high level on output pin LPENSTB to inform the 82C435 of a valid light pen trigger.
12	I	$\overline{LPENSW}$	LIGHT PEN SWITCH. $\overline{LPENSW}$ goes to bit 2 of the Input Status Register 1 0 = light pen switch closed 1 = light pen switch open
44	O	LPENSTB	LIGHT PEN STROBE. LPENSTB goes active high on the falling edge of $\overline{LPENIN}$. It is used by the 82C435 to load the Light Pen High (CR10) and Light Pen Low (CR11) registers in the CRT Controller.
13 14	I I	FEATIN0 FEATIN1	FEATURE CODE 0 and FEATURE CODE 1 are inputs from the feature connector (pins 19 and 17, respectively) and can be read in the EGA mode as bits 5 and 6 in the Input Status Register 0 (I/O address 3C2h).
43 42	O O	FCOUT0 FCOUT1	FEATURE CONTROL 0, FEATURE CONTROL 1. FCOUT0 and FCOUT1 are bits 0 and 1 of the Feature Control Register (I/O address 3BAh/3DAh). FCOUT0 and FCOUT1 go to pins 20 and 21 of the Feature Connector.

82A436 Pin Description (Continued)

Pin No.	Pin Type	Symbol	Description
11	I	SWITCH	SWITCH is a multiplexed input from a 4-position external configuration DIP-switch. In the EGA mode, the state of this input can be read as the switch sense bit (bit 4 of the Input Status Register 0 - I/O address 3C2h). CLKSEL0 and CLKSEL1 pins (bits 2 and 3 of the Miscellaneous Output Register - I/O address 3C2h) determines which switch is read.
7	I	HIN	HORIZONTAL RETRACE INPUT. HIN is a an input from the 82C435. This input is used in Hercules mode to generate bit 0 of the Hercules Status Register (I/O address 3BAh).
8	I	VIN	VERTICAL RETRACE INPUT. VIN is an input from the 82C435. This input is used in CGA mode to generate bit 3 of the CGA Status Register (I/O address 3DAh). In Hercules mode, this input generates bit 7 of the Hercules Status Register (I/O address 3BAh).
10	I	BS/V	SECONDARY BLUE/MONOCHROME VIDEO. BS/V input on the 82A436 is normally the BS/V output from the 82C435. This input is used to generate bit 3 of the CRT Status Register in Hercules mode (I/O address 3BAh).
39 38 37 36 34 33 32 31	I/O I/O I/O I/O I/O I/O I/O I/O	DADD0 DADD1 DADD2 DADD3 DADD4 DADD5 DADD6 DADD7	Local data bus for memory or I/O data between the 82C435, 82A436 and the BIOS ROM.
29	O	$\overline{\text{ROMWE}}$	BIOS ROM WRITE ENABLE. $\overline{\text{ROMWE}}$ is active low for memory writes at address C0000h-C3FFFh. This output can be used to select the active page in Page Select ROMs (27513).
30	O	$\overline{\text{ROMOE}}$	BIOS ROM OUTPUT ENABLE. $\overline{\text{ROMOE}}$ is active low for memory reads at address C0000h-C3FFFh.
27	O	MA16	Buffered system address bus bit A16.
28	O	$\overline{\text{ADDM0}}$	Address Decode. Decoded output for three upper system address bus bits to address the display memory at locations AXXXX and BXXXX. This output is low when A19-A17 =101.

82A436 Pin Description (Continued)

Pin No.	Pin Type	Symbol	Description
40	O	$\overline{\text{MIORD}}$	MEMORY-I/O READ. $\overline{\text{MIORD}}$ is active low for memory or I/O read operations. $\overline{\text{MIORD}}$ is active whenever $\overline{\text{MEMR}}$ or $\overline{\text{IOR}}$ is active.
41	O	$\overline{\text{MIOWR}}$	MEMORY-I/O WRITE. $\overline{\text{MIOWR}}$ is active low for all memory or I/O write operations. $\overline{\text{MIOWR}}$ is active whenever $\overline{\text{MEMW}}$ or $\overline{\text{IOW}}$ is active.
45	O	MEMIO	MEMORY-I/O. MEMIO is a control signal, low for memory ($\overline{\text{MEMR}}$ or $\overline{\text{MEMW}}$), high for I/O ($\overline{\text{IOR}}$ or $\overline{\text{IOW}}$).
25 26	O O	CLKSEL0 CLKSEL1	CLOCK SELECT 0 AND 1. CLKSEL0 and CLKSEL1 are bits 2 and 3 of the Miscellaneous Output Register (I/O address 3C2h). These bits are used as select inputs into an external multiplexer to select the configuration switch bits and the clock source.
15	I	IOADS	I/O ADDRESS. IOADS selects the I/O address to the CRT Controller. 0 = 2XXh, 1 = 3XXh.
16	I	VALRAD	VALID READ ADDRESS. VALRAD, generated by the 82C435, allows the 82A436 to drive the system data bus during a memory read cycle ($\overline{\text{MEMR}}$).
6	O	$\overline{\text{INTERNL}}$	INTERNAL SELECT. $\overline{\text{INTERNL}}$ is bit 4 of the Miscellaneous Output Register (I/O address 3C2h). It is an active low signal which enables the 82C435 outputs (R, G, B, RS, GS/I, BS/V, HIN, VIN) through an external buffer to the monitor. It is also an output to the feature connector (pin 27).

82A436 Functional Description

The 82A436 integrates the bus drivers, decode logic and other external logic that is required to implement a complete EGA/CGA/Hercules compatible display subsystem around the 82C435.

The functionality of the 82A436 can be classified as follows:

a) Decodes memory addresses and control signals.
b) Serves as a data transceiver between the I/O bus and the 82C435, display memory and EGA BIOS.
c) Provides temporary storage locations.
d) Light Pen logic.
e) Feature Connector interface logic.
f) Includes parts of some registers on the EGA/CGA/Hercules display subsystems.

Memory Address and Control Decode

The 82A436 generates a memory address select signal (ADDM0) for the 82C435. This signal is active low for all memory accesses in the address space A0000h-BFFFFh. The 82A436 also generates Output Enable and Write Enable signals for the BIOS ROM in the address range C0000h-C3FFFh. The ROMOE signal is low for all read accesses to this address space. The ROMWE signal is low for all write accesses to this address space. The ROMWE signal allows the use of page select ROMs like 27513 on the EGA board.

The 82C435 uses the same control pins (MIORD & MIOWR) for memory and I/O accesses. The 82A436 generates MIORD, MIOWR and MEMIO signals from the I/O bus control signals.

Data Transceiver Function

The 82A436 also serves as a bidirectional transceiver for data transfer between the CPU (I/O bus) and the display memory, BIOS ROM and 82C435. When the CPU needs to write to the display subsystem, the 82A436 passes the data through to the local data bus in the display subsystem. When the CPU reads from the display subsystem, the 82A436 handles the data transfer in two ways:

a) If the data is to come from a register (or register bit) that exists in the 82A436, the 82A436 drives those specific bits onto the I/O bus data bus.
b) For all other read cycles (memory, other register and register bits), the 82A436 transfers the data from the local data bus through to the I/O bus. In this case, the local data bus is driven by the BIOS ROM or the 82C435.

Temporary Storage Registers

There are five byte wide temporary storage read-write registers in the 82A436. These registers are located at offset 0FAh-0FEh in the CRT Controller data register space. These registers can be accessed by first writing 0FAh/0FBh/0FCh/0FDh/0FEh in the CRTC Address Register (I/O address 3B4h/3D4h) and then accessing the CRTC Data Register (I/O address 3B5h/3D5h). These registers can be used as working registers.

Light Pen Logic

The Light Pen logic consists of the Light Pen Latch and Light Pen Switch. The Light Pen Latch is set by software through an internal register or by hardware when there is a valid negative pulse on the LPENIN input. The latch can only be cleared by software. The Light Pen Latch and Switch status can be read by software through the Input Status Register I at I/O address 3C2h (described later).

SET LIGHT PEN LATCH

Write Only Register
I/O Address: 3DCh/3B9h

The Set Light Pen Register is used to trigger the Light Pen from software. In the EGA mode, this is done by an I/O Write to address 3DCh. In CGA mode, the Light Pen is triggered by an I/O Read or I/O Write to address 3DCh. In Hercules mode, this is done by an I/O Write to address 3B9h.

CLEAR LIGHT PEN LATCH

Write Only Register
I/O Address: 3DBh/3BBh

The Clear Light Pen Register is used to clear the Light Pen Latch. In the EGA mode, this is done by an I/O Write to address 3DBh. In CGA mode, the Light Pen is triggered by an I/O Read or I/O Write to address 3DBh. In Hercules mode, this is done by an I/O Write to address 3BBh.

Feature Connector Interface Logic

The EGA has the facility to interface to an external video system. This interface is through the Feature Connector. The external video system, can take the Sync signals and video data stream from the 82C435. It can also accept a composite signal through an external port. This external video system, can then either drive a composite video signal or also drive a standard RGB monitor through the EGA. The Feature Connector interface logic consists of the Feature Control outputs, Feature Code inputs and a control signal to select between internal and external video source.

The CPU can pass control and status information to the external video system through the Feature Control Register. Feature Control Bits 0 and 1 from this register are output on 82A436 output pins FCOUT0 and FCOUT1 respectively. These pins are usually connected to the Feature Connector.

The Feature Connector can also pass information to the CPU. This is done though two pins FEATIN0 and FEATIN1 on the 82A436. The CPU can read the state of these two pins through Input Status Register 0 at I/O address 3C2h.

Select Video Source

The Video and Sync outputs to the monitor can come from two sources. The 82C435 could drive the monitor or the Feature Connector could drive the monitor. The internal video stream or the Feature Connector video stream is selected through the Disable Internal Video bit in the EGA Miscellaneous Register at I/O address 3C2h. This bit controls the state of the $\overline{\text{INTERNL}}$ output pin on the 82A436. The $\overline{\text{INTERNL}}$ output is typically used to enable a tri-state buffer that isolates the monitor from the 82C435. If the feature connector is to drive the monitor, then the Disable Internal Video bit must be programmed to 1.

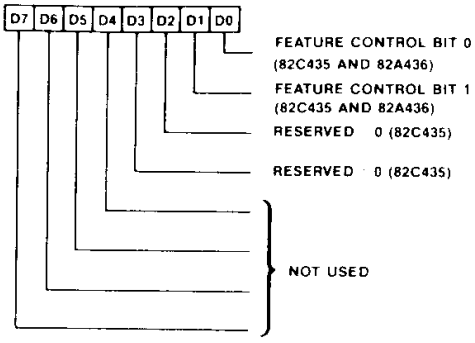
82A436 Registers

There are several registers (or parts of registers) in the 82A436. These are:

Register	Address
Bits D0, D1 of EGA Feature Control Register	3BAh/3DAh
Bits D0, D1, D2 of Emulation Mode Register (Pointer = FFh)	3B5h/3D5h
Bits D0, D2, D3, D4 of EGA Miscellaneous Output Register	3C2h
Bits D4, D5, D6 of EGA Input Status Register 0	3C2h
Bits D1, D2 of EGA Input Status Register I	3BAh/3DAh
Bits D1, D2, D3 of CGA Status Register	3DAh
Bits D0, D3, D7 of Hercules Status Register	3BAh
EGA/CGA Set Light Pen Register	3DCh
Hercules Set Light Pen Register	3B9h
EGA/CGA Clear Light Pen Register	3DBh
Hercules Clear Light Pen Register	3BBh
Temporary Storage Registers 0-4 (Pointer = FAh-FEh)	3B5h/3D5h

FEATURE CONTROL REGISTER

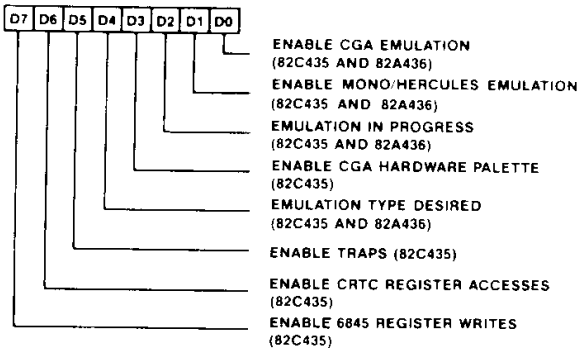
Write Only Register
I/O Address: 3BAh/3DAh



The Feature Control Register exists in both the 82C435 and the 82A436. In the 82A436 this is a write only register and only bits 0 and 1 are implemented. These bits are also present in the 82C435. When this register is read, the 82C435 drives the local data bus and the 82A436 transfers the contents of the local data bus to the CPU. Feature Control Bits 0 and 1 from this register are output on output pins FCOUT0 and FCOUT1 respectively. These bits can be used to transfer status information to the Feature Connector. On reset, bits D0 and D1 of this register default to 0.

EMULATION MODE REGISTER (CRFF)

Write Only Register
I/O Address: 3B5h/3D5h;
Address Pointer: FFh



The Emulation Mode Register exists in both the 82C435 and the 82A436. This register is located at offset 0FFh in the CRT Controller register space. In the 82A436 this is a write only register and only bits 0, 1 and 2 are implemented. These bits are also present in the 82C435. When this register is read, the 82C435 drives the local data bus and the 82A436 transfers the contents of the local data bus to the CPU.

D0 Enable CGA Emulation: This bit determines if CGA Emulation is to be enabled (=1) or disabled (=0). On reset, this bit defaults to 0.

D1 Enable Mono/Hercules Emulation: This bit determines if Monochrome/ Hercules Emulation is to be enabled (=1) or disabled (=0). On reset, this bit defaults to 0.

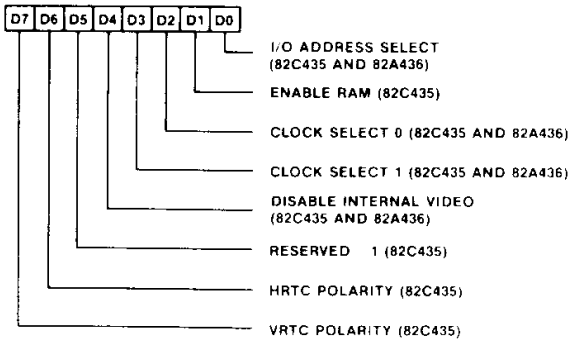
D2 Emulation in Progress: This bit determines if the 82C435/82A436 is currently in the CGA or Hercules emulation mode (=1) or in the normal EGA mode (=0). This bit must be set while CGA/MDA/ Hercules emulation is in progress. On reset, this bit defaults to 0.

D4 Emulation Type: This bit is set when software desires an automatic emulation mode switch. D4 = 0 and CGA emulation enabled means that the software desires CGA emulation. D4 = 1 and Hercules emulation enabled means that the software desires Hercules emulation. On reset, this bit is undefined.

The 82A436 determines the address for the Light Pen Set and Clear registers depending on the contents of these bits. The format for the Input Status Register 1 (CGA/Hercules Status Register) is also determined according to these bits.

EGA
MISCELLANEOUS OUTPUT REGISTER

Write Only Register
I/O Address: 3C2h



The EGA Miscellaneous Register exists in both the 82C435 and the 82A436. This register is located at I/O address 3C2h. In the 82A436, this is a write only register and only bits 0, 2, 3, and 4 are implemented. These bits are also present in the 82C435. When this register is read, the 82C435 drives the local data bus and the 82A436 transfers the contents of the local data bus to the CPU.

D0 I/O Address Select. This bit maps the CRT Controller address and data registers into the 3Bxh/3Dxh address space. This bit defaults to 0 on reset and is present in both the 82C435 and 82A436. Setting this bit to 0 or 1 maps the registers as follows:

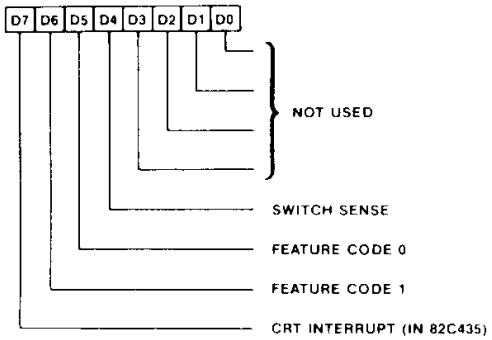
Register Name	I/O Address for D0 = 0	D0 = 1
CRTC Address Register	3B4h	3D4h
CRTC Data Register	3B5h	3D5h
Feature Control Register	3BAh	3DAh
Input Status Register I	3BAh	3DAh

D2-D3 D2-D3 bits are output on the CLKSEL0 and CLKSEL1 pins on the 82A436. Typically these are used to externally select the clock source for the 82C435. On reset, these bits default to 0.

D4 Disable Internal Video. This bit is output on the INTERNL pin on the 82A436. The INTERNL output is used to select the 82C435 video data stream or an external video data stream to the monitor. On reset, this bit defaults to 0.

INPUT STATUS REGISTER 0

Read Only Register
I/O Address: 3C2h



The EGA Input Status Register 0 exists in both the 82C435 and the 82A436. This register is located at I/O address 3C2h. In the 82A436, this is a read-only register and only bits 4, 5, and 7 are implemented. When this register is read in the EGA mode, the 82C435 drives the local data bus bit 7 and the 82A436 drives the other bits. In the CGA and Hercules modes, this register returns undefined values when read.

Switch Sense (D4)

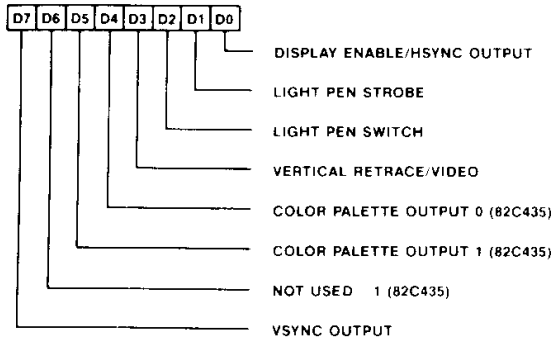
This bit returns the current status of the 82A436 input pin 'SWITCH' to the CPU. The CPU scans the state of the DIP switches on the EGA board through this bit.

Feature Code 0 and 1 (D5-D6)

These two bits return the current status of the 82A436 input pins FEATIN0 and FEATIN1 respectively. These bits are used to read the status information from the EGA Board Feature Connector.

INPUT STATUS REGISTER I (CGA/HERCULES STATUS REGISTER)

Read Only Register
I/O Address: 3BAh/3DAh



The Input Status Register I exists in both the 82C435 and the 82A436. This register changes address and format in the EGA, CGA and Hercules modes. In EGA mode this register is located at I/O address 3BAh/3DAh. In CGA mode this register is located at I/O address 3DAh. In Hercules mode this register is located at I/O address 3BAh. When this register is read, the 82C435 and 82A436 drive different bits in the three modes as follows:

EGA mode	82C435 drives bits 0, 3, 4, 5 82A436 drives bits 1 and 2 bits 6 and 7 are high
CGA mode	82C435 drives bit 0 82A436 drives bits 1, 2 and 3 bits 4, 5, 6 and 7 are high
Hercules mode	82A436 drives bits 0, 3 and 7 bits 1, 2, 4, 5 and 6 are high

Display Enable/HSYNC Output (D0)

In EGA and CGA modes, D0 is an active low Display Enable signal generated by the 82C435. A logical 0 indicates the active display interval. This bit is returned high during the horizontal and vertical retrace interval. In Hercules emulation mode this bit is driven by the 82A436 and it indicates the current level of the 82A436 HIN input.

Light Pen Strobe (D1)

D1 is driven by the 82A436 and indicates the state of the Light Pen Latch. This latch is set whenever a valid Light Pen pulse is generated.

Light Pen Switch (D2)

D2 is driven by the 82A436 and indicates the state of the Light Pen Switch (on the Light Pen Connector).

Vertical Retrace/Video (D3)

In EGA mode, D3 is an active high vertical retrace signal, which is functionally the same as the active high Vertical Sync output from the 82C435 (the polarity of this bit is always positive). In CGA emulation mode, D3 is driven by the 82A436 and is the complement of the VIN input on the 82A436. In Hercules emulation mode D3 is driven by the 82A436 and it indicates the current state of the BS/V input on the 82A436.

Vertical Sync Output (D7)

D7 is high during the Vertical Sync interval.

82A436 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{DD}	—	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{OP}	-25	85	C
Storage Temperature	T_{STG}	-40	125	C

82A436 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	°C

82A436 DC Characteristics

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL1} = 10mA[1] I_{OL2} = 24mA[2]	V_{OL}		0.5	V
Output High Voltage I_{OH} = 3.3mA	V_{OH}	2.4		V
Input Leakage Current	I_{IL}	-200	+200	μA
Power Supply Current	I_{CC}		250	mA
Output High Impedence Leakage $0.45 < V_{PIN} < V_{CC}$	I_{OZ}	-300	+120	μA

NOTES:
1. I_{OL} = 10mA on all pins except DATAA0-7
2. I_{OL} = 24mA on DATA0-7

82A436 AC Characteristics

(T_A = 0°C-70°C, V_{CC} = 5V ±5%)

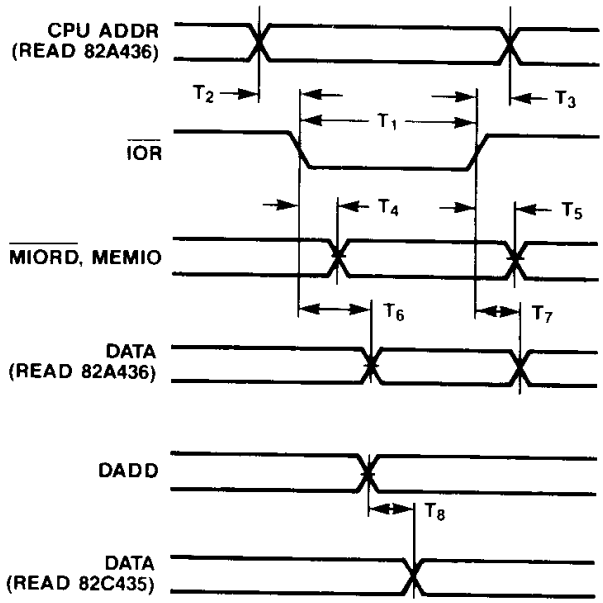
Timings

Parameter	Symbol	Min.(ns)	Max.(ns)
System Clock Period	T_C	80	
$\overline{IOR}$ Pulse Width	T_1	T_C	
Address Setup (82A436 Register Access)	T_2	20	
Address Hold (82A436 Register Access)	T_3	0	
Control Active Delay	T_4		25
Control Inactive Delay	T_5		23
I/O Read Data Delay (82A436 Register)	T_6		45
I/O Read Data Hold (82A436 Register)	T_7	10	30
Propagation Delay (DATA-DADD, DADD-DATA)	T_8		25
$\overline{IOW}$ Setup to System Clock	T_9*	10	
$\overline{IOW}$ Pulse Width (Short Write)	T_{10}		$2T_C$
$\overline{IOW}$Pulse Width (Long Write)	T_{10}	$2T_C$	
$\overline{MIOWR}$ Active Delay (I/O Write)	T_{11}*		31
$\overline{MIOWR}$ Inactive Delay (Short I/O Write)	T_{12}		28
$\overline{MIOWR}$ Inactive Delay (Long I/O Write)	T_{12}*		34
I/O Write Data Setup (82A436 Register)	T_{13}	10	
I/O Write Data Hold (82A436 Register)	T_{14}	20	
LPENSTB Delay (Software Strobe)	T_{15}		45
Register Output Delay (Long Write)	T_{16}		45
Register Output Delay (Short Write)	T_{16}		40
VALRAD Setup (Display Memory Access)	T_{20}	5	
Address Setup (ROM Access)	T_{20}	20	
VALRAD Hold (Display Memory Access)	T_{21}	0	
Address Hold (ROM Access)	T_{21}	0	
Control Active Delay (Memory Access)	T_{22}		26
Control Inactive Delay (Memory Access)	T_{23}		20
$\overline{ADDM0}$ Delay	T_{24}		26
MA16 Delay	T_{24}		20
LPENSTB Delay (Hardware Strobe)	T_{25}		40

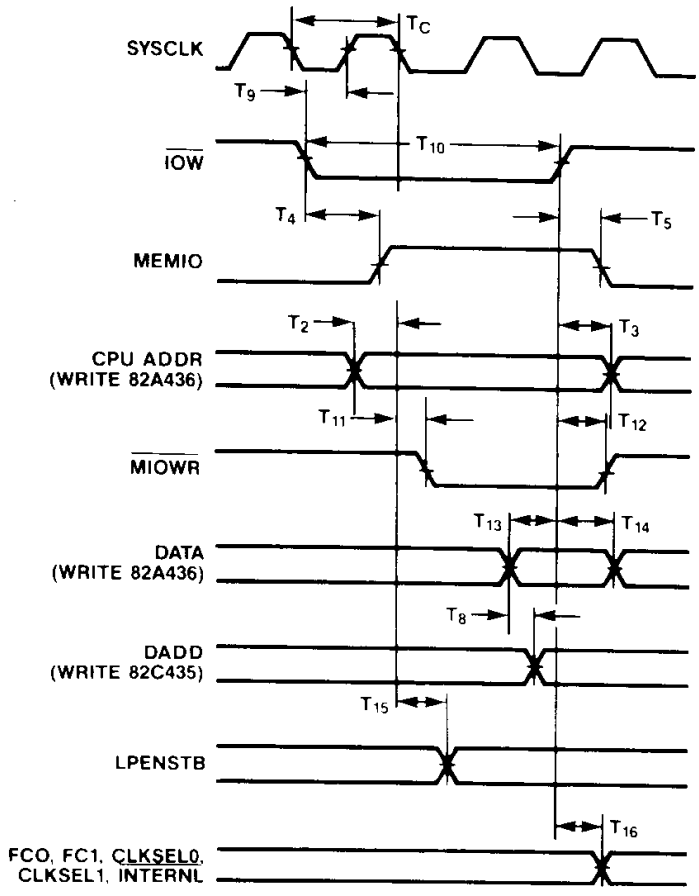
NOTE:

* T_9, T_{11} and T_{12} (long write) are specified on both rising and falling edges of SYSCLK. $\overline{MIOWR}$ stays active for a maximum of 1½ SYSCLKs starting at any of the edges of SYSCLK.

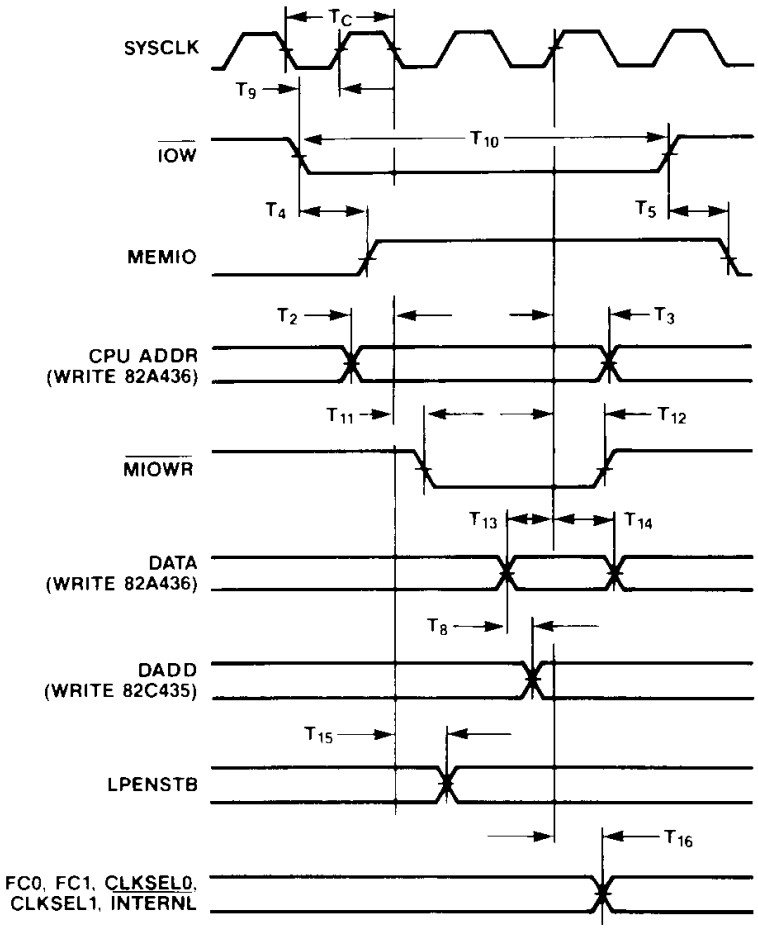
CPU—IO READ ACCESS



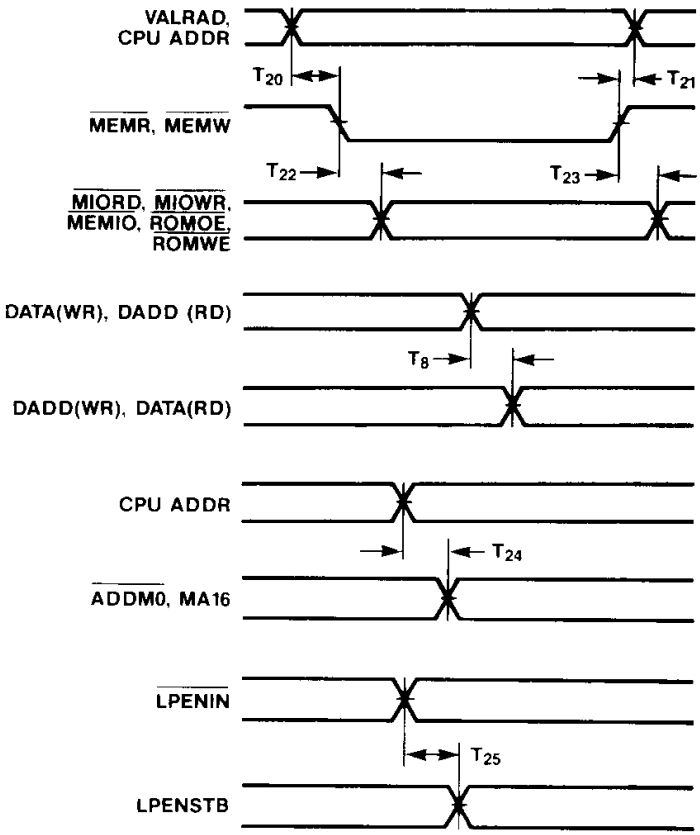
CPU—IO WRITE ACCESS (SHORT WRITE)



CPU—IO WRITE ACCESS (LONG WRITE)



CPU—MEMORY ACCESS



Load Circuit Measurement Conditions

Parameter	Output Type	Symbol	C_L(pF)	R_1 (s)	R_L (s)	SW_1	SW_2
Propagation Delay Time	Totem pole 3-state Bidirectional	t_{PLH} t_{PHL}	50	—	1.0KL	OFF	ON
Propagation Delay Time	Open drain or Open Collector	t_{PLH} t_{PHL}	50	0.5K	—	ON	OFF
Disable Time	3-state Bidirectional	t_{PLZ} t_{PHZ}	5	0.5K	1.0K	ON OFF	ON
Enable Time	3-state Bidirectional	t_{PZL} t_{PZH}	50	0.5K	1.0K	ON OFF	ON ON

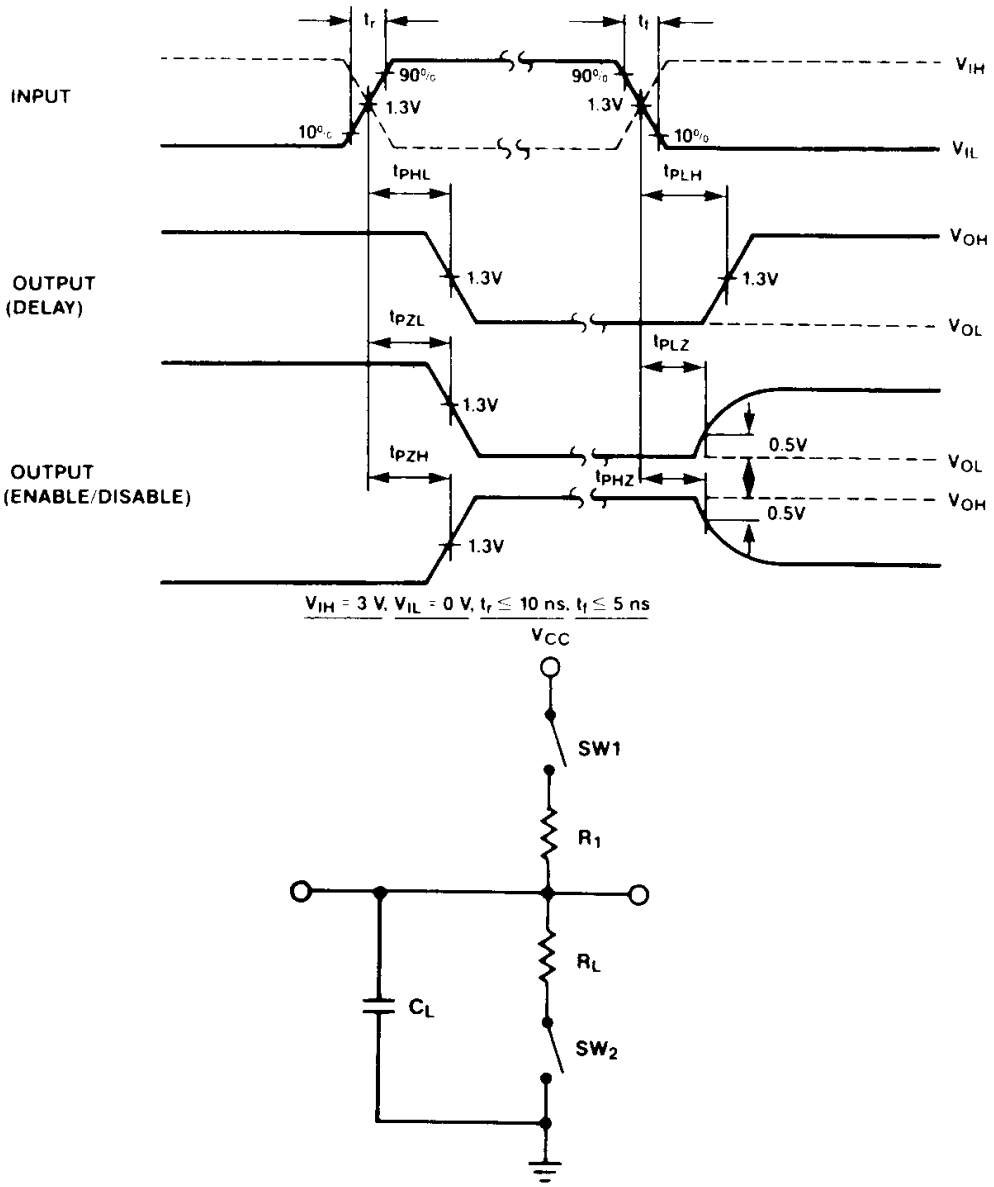
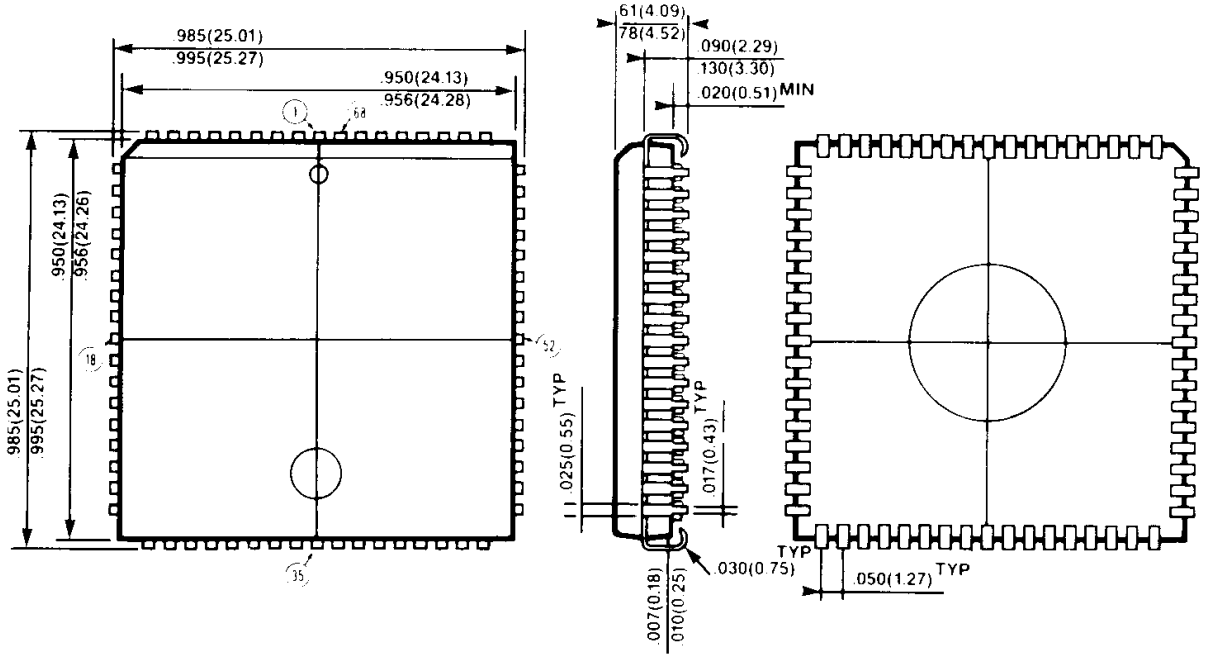
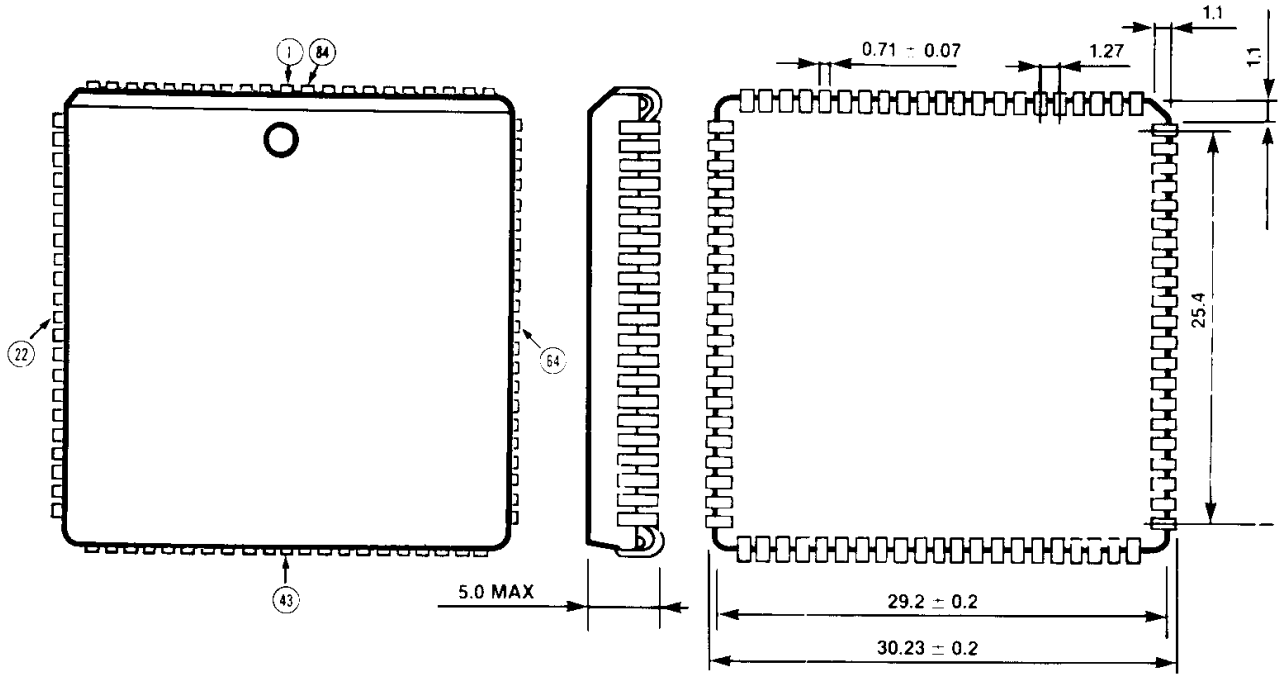


Figure 10. Load Circuit and AC Characteristics Measurement Waveform

68-PIN PLASTIC LEADED CHIP CARRIER



84-PIN PLASTIC LEADED CHIP CARRIER

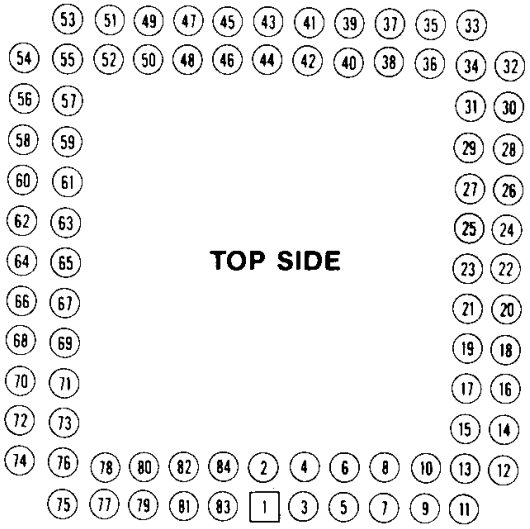


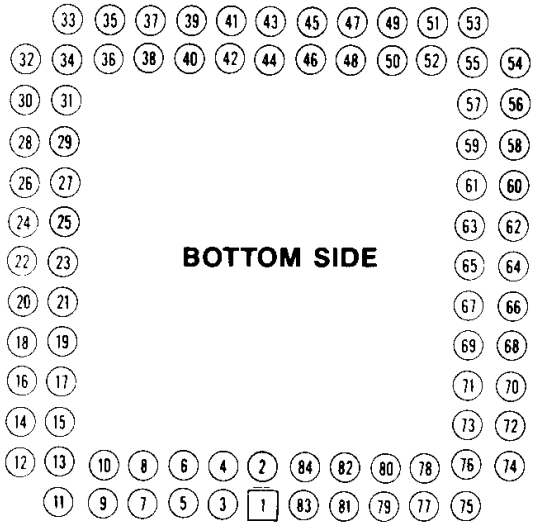
Ordering Information

Order Number	Package Type
P82C435	PLCC-84 pins
P82A436	PLCC-68 pins

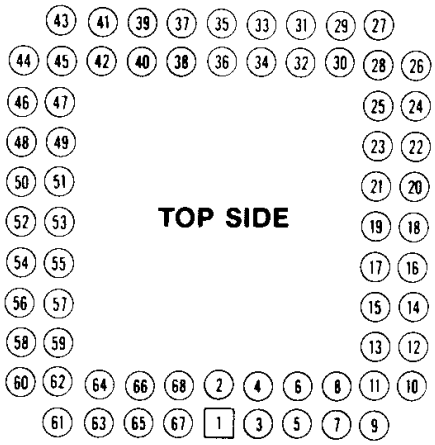
Note:
1. PLCC = Plastic Leaded Chip Carrier
   PFP = Plastic Flat Pack

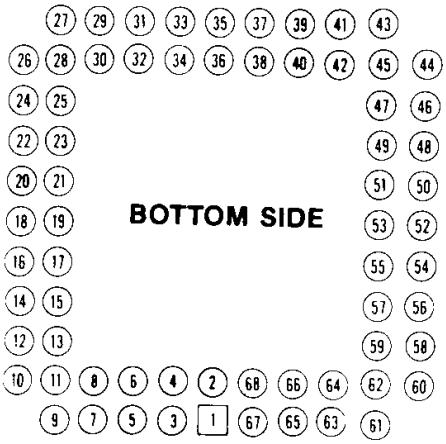
84-PIN PLCC SOCKET





68-PIN PLCC SOCKET





CHIPS

Chips and Technologies, Incorporated
3050 Zanker Road, San Jose, CA 95134 408-434-0600 Telex 272929 CHIP UR