FINAL

Am79C100

Twisted-Pair Ethernet Transceiver Plus (TPEX Plus)

DISTINCTIVE CHARACTERISTICS

- CMOS device provides IEEE 802.3-compliant operation and low operating current from a single +5 V supply
- Power Down mode for reduced power consumption in battery-powered applications
- Automatic twisted-pair link integrity
- Pin-selectable twisted-pair receive polarity detection and automatic inversion of the receive signal. Polarity indication output pin can directly drive an LED.
- Pin-selectable twisted-pair link integrity test capability conforming to the IEEE 802.3 standard. Link status pin can directly drive an LED.

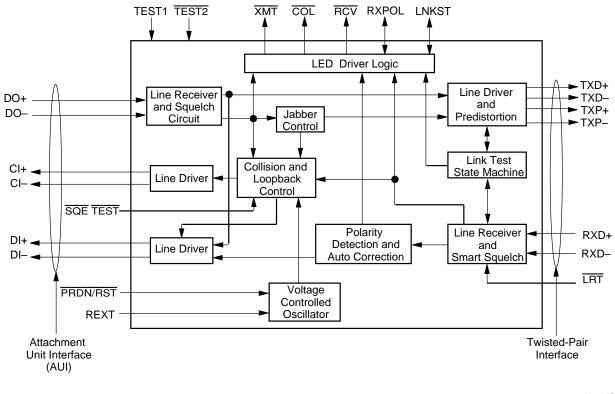
- Transmit, receive, and collision status indications available on separate, dedicated pins
- Outputs can directly drive LEDs with pulses stretched to ensure LED visibility
- Internal twisted-pair transmitter digital predistortion circuit to reduce medium-induced jitter
- Pin-selectable SQE Test (heartbeat) enable
- AUI loopback, Jabber Control, and SQE Test functions comply with the 10BASE-T standard
- User-selectable loopback operations
- Pin-selectable twisted-pair receive threshold programming for extended distance line lengths

GENERAL DESCRIPTION

The Am79C100 Twisted-Pair Ethernet Transceiver Plus (TPEX Plus) is an integrated circuit that implements the medium attachment unit (MAU) functions for the twisted-pair medium, as specified by the supplement to the IEEE 802.3 standard (Type 10BASE-T). This device provides the necessary electrical and functional interface between the IEEE 802.3 standard attachment unit interface (AUI) and the twisted-pair cable.

A network based on the 10BASE-T standard can use unshielded twisted-pair cables, providing an economical solution to networking by allowing the use of existing telephone wiring. The Am79C100 provides a minimal component count and a cost-effective solution to the design and implementation of 10BASE-T standard networks. TPEX Plus provides twisted-pair driver and receiver circuits, including on-board transmit digital predistortion, receiver squelch, and an AUI port with pin-selectable SQE Test enable. The device provides a number of additional features, including Link Status indication with automatic twisted-pair receive polarity detection/ correction and indication; pin-selectable receive threshold programming for extended distance line lengths; and Receive Carrier Sense, Transmit Active and Collision Present indications. The device provides separate twisted-pair Link Status, Polarity Status, Receive, Transmit, and Collision outputs to drive LEDs directly.

BLOCK DIAGRAM

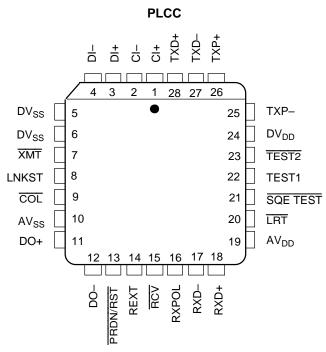


¹⁶⁵¹¹B-1

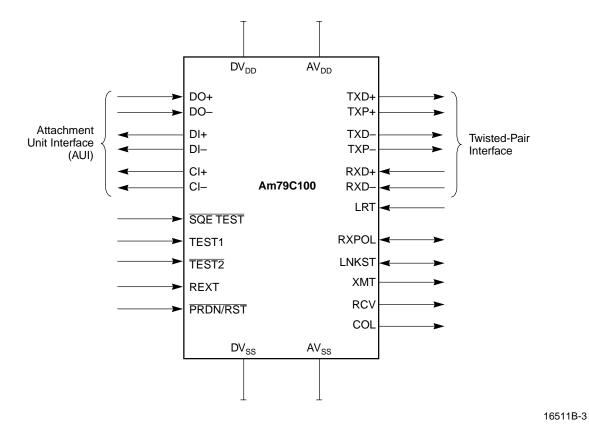
RELATED AMD PRODUCTS

| Part No. | Description |
|----------|--|
| Am7996 | IEEE-802.3/Ethernet/Cheapernet Tap Transceiver |
| Am79C90 | CMOS Local Area Network Controller for Ethernet [™] (C-LANCE) |
| Am79C900 | Integrated Local Area Communications Controller [™] (ILACC [™]) |
| Am79C940 | Media Access Controller for Ethernet (MACE™) |
| Am79C960 | PCnet-ISA Single-Chip Ethernet Controller (for ISA bus) |
| Am79C961 | PCnet-ISA Single-Chip Ethernet Controller (with Microsoft® Plug n' Play support) |
| Am79C965 | PCnet-32 Single-Chip Ethernet Controller (for 386DX, 486 and VL buses) |
| Am79C970 | PCnet-PCI Single-Chip Ethernet Controller (for PCI bus) |
| Am79C974 | PCnet-SCSI Combination Ethernet and SCSI Controller for PCI Systems |
| Am79C98 | Twisted-Pair Ethernet Transceiver (TPEX) |
| Am79C981 | Integrated Multiport Repeater Plus [™] (IMR+ [™]) |
| Am79C987 | Hardware Implemented Management Information Base™ (HIMIB™) |

CONNECTION DIAGRAM



16511B-2



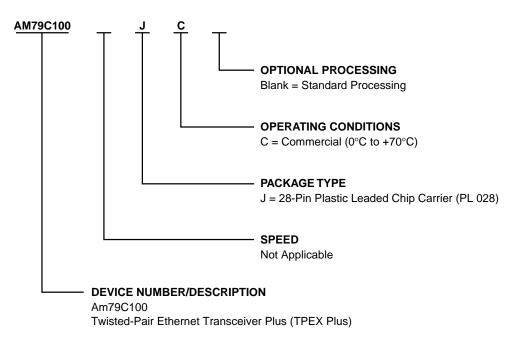
LOGIC SYMBOL

Am79C100

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (valid combination) is formed by a combination of the elements below.



| Valid Combinations | | | |
|--------------------|----|--|--|
| AM79C100 | JC | | |

Valid Combinations

Valid combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

PIN DESCRIPTION

AV_{DD}

Analog Power

This pin supplies +5 V to analog portions of the TPEX Plus circuitry.

$\mathrm{AV}_{\mathrm{SS}}$

Analog Ground

This pin is the ground reference for analog portions of TPEX Plus circuitry.

CI+, CI-

Control In Output

AUI port differential driver.

COL

Collision Output, Open Drain

This pin is driven LOW while the TPEX Plus is simultaneously receiving data on the AUI DO pins and the twisted-pair RXD pins, indicating that a collision condition exists. It is also driven if TPEX Plus enters the jabber condition due to excessive length of activity on the DO pair. In this case TPEX Plus will wait for a period of inactivity on DO for the "unjab" time of 250 to 750 ms, before the 10 MHz pattern on the CI pair is removed and COL returns inactive. COL will not be driven during SQE Test activity on the AUI CI pair. In the LOW output state, the pin is capable of sinking a maximum of 12 mA and can be used to drive an LED. The COL output is pulse stretched for 20 to 62 ms after the end of collision, to ensure LED visibility.

DI+, DI-

Data In Output

AUI port differential driver.

DO+, DO-

Data Out Input AUI port differential receiver.

$\mathbf{DV}_{\mathbf{DD}}$

Digital Power

This pin supplies +5 V to digital portions of the TPEX Plus circuitry, including all transmit drivers.

\mathbf{DV}_{SS}

Digital Ground

Two pins provide the ground reference for digital portions of TPEX Plus circuitry, including all transmit drivers and the status indication LED drivers.

LNKST

Link Status Input/Output, Open Drain

When this pin is tied LOW, the internal Link Test Receive function is disabled, and the Transmit and Receive functions will remain active regardless of arriving idle link pulses and data. TPEX Plus continues to generate idle link pulses irrespective of the status of this pin.

As an output, this pin is driven LOW if the link is identified as functional. However, if the link is determined to be nonfunctional due to missing idle link pulses or data packets, then this pin is not driven (internally pulled HIGH). In the LOW output state, the pin is capable of sinking a maximum of 12 mA and can be used to drive an LED.

In the absence of an external drive, the pin is internally pulled HIGH when inactive.

LRT

Low Receive Threshold Input, Active LOW

When this pin is tied LOW, the internal twisted-pair receive thresholds are reduced by 4.5 dB from their original values (approximately 3/5 of the normal 10BASE-T value). With \overline{LRT} in the HIGH state, the unsquelch threshold for the RXD± circuit will be 300 mV to 520 mV peak. With \overline{LRT} in the LOW state, the unsquelch threshold for the RXD± circuit will be 180 mV to 312 mV peak. In either case, the RXD± circuit post unsquelch threshold will be approximately one-half of the initial unsquelch threshold.

PRDN/RST

Power Down/Reset Input, Active LOW

Driving this input LOW resets the internal logic of TPEX Plus and places the device in a special Power Down mode. In the Power Down/Reset mode, all output drivers are placed in their inactive state.

REXT

External Resistor Input

An external precision resistor is connected between this pin and AV_{DD} in order to provide a current reference for the internal voltage-controlled oscillator (VCO).

RCV

Receive

Output, Open Drain

This pin is driven LOW while TPEX Plus is receiving data on the twisted-pair RXD pins and is transferring the received signal onto the AUI DI pair. The output is LOW during collision simultaneously with the $\overline{\text{COL}}$ pin.

In the LOW output state, the pin is capable of sinking a maximum of 12 mA and can be used to drive an LED. The $\overline{\text{RCV}}$ output is pulse stretched for 20 ms to 62 ms after the end of reception, to ensure LED visibility.

RXD+, RXD-

Receive Data Input

10BASE-T port differential receiver.

RXPOL

Receive Polarity Input/Output, Open Drain

The twisted-pair receiver is capable of detecting a receive signal with reversed polarity (wiring error). The RXPOL pin is normally in the LOW state, indicating correct polarity of the received signal. If the receiver detects a received packet with reversed polarity, then this pin is not driven (goes HIGH) and the polarity of subsequent packets is inverted. In the LOW output state, this pin can sink up to a maximum of 12 mA and is therefore capable of driving an LED.

This feature can be disabled by strapping this pin LOW. In this case, the Receive Polarity correction circuit is disabled and the internal Receive Signal remains noninverted, irrespective of the received signal.

In the absence of an external drive, the pin is internally pulled HIGH when inactive.

SQE TEST

Signal Quality Test (Heartbeat) Enable Input, Active LOW

The SQE Test function is enabled by tying this input LOW. When enabled, TPEX Plus will send a 10 MHz burst (heartbeat) on the Cl \pm lines after DO \pm has become inactive, indicating integrity of the collision detection and AUI circuitry. SQE TEST should be disabled for repeater applications.

In the absence of an external drive, the pin is internally pulled HIGH when inactive.

TEST1

Test

Input, Active HIGH

This pin should be tied LOW for normal operation. TEST1 permits system-level diagnostics to be performed. If TEST1 is driven HIGH (while TEST2 is maintained HIGH), TPEX Plus will enter the Loopback Test mode. The type of loopback is determined by the state of the SQE TEST pin. If SQE TEST is in the LOW state

(Station MAU), TPEX Plus transfers data independently from DO to the TXD/TXP circuits and from RXD to the DI circuit. If the $\overline{SQE TEST}$ is in the HIGH state (Repeater MAU), then data on the RXD circuit is transmitted back onto the TXD/TXP circuits and data on the DO circuit is transmitted onto the DI pair.

During either test mode, the Collision Detection and SQE Test functions are disabled, and Cl \pm will remain idle. Link beat pulses will continue to be generated normally in the absence of TXD/TXP output activity, and the Link Test Receive State Machine will be forced into the Link Pass state. The COL pin will be driven LOW whenever a link beat pulse or transmit data activity commences, and remain low during the output activity. The receive squelch will continue to operate on both the RXD \pm and DO \pm input circuits.

In the absence of an external drive, the pin is internally pulled LOW.

TEST2

Test

Input, Active LOW

This pin should be tied HIGH for normal operation. TEST2 is reserved for factory testing, and should be permanently tied HIGH.

In the absence of an external drive, the pin is internally pulled HIGH.

TXD+, TXD-

Transmit Data Output

10BASE-T port differential drivers.

TXP+, TXP-

Transmit Predistortion Output

Transmit waveform differential driver for predistortion.

ХМТ

Transmit Output, Open Drain

This pin is driven LOW while TPEX Plus is receiving data on the AUI DO pair and is transmitting data on the TXD/TXP pins. The output is LOW during collision simultaneously with the \overline{COL} pin. In the LOW output state, the pin is capable of sinking a maximum of 12 mA and can be used to drive an LED. The \overline{XMT} output is pulse stretched for 20 to 62 ms after the end of transmission, to ensure LED visibility.

FUNCTIONAL DESCRIPTION

The Twisted-Pair Ethernet Transceiver Plus (TPEX Plus) complies with the requirements specified by the IEEE 802.3 standard for the attachment unit interface (AUI) and the 10BASE-T standard for a twisted-pair medium attachment unit (MAU). TPEX Plus also implements a number of features in addition to the IEEE 802.3 standard. An outline of the functions of the Am79C100 is given below.

Attachment Unit Interface (DO±, DI±, CI±)

The AUI electrical and functional characteristics comply with those specified within the IEEE 802.3 documents, Sections 7 and 14. The AUI pins can be wired to an isolation transformer, for a remote MAU application, or directly to another device (e.g., Am7992B serial interface adapter), in the case of a local DTE application. The end-of-packet SQE Test function (heartbeat) can be disabled to allow the device to be employed in a repeater application.

Twisted-Pair Transmit Function

Data transmission to the 10BASE-T medium occurs when valid AUI signals appear on the DO± differential pair. This data stream is routed to the differential driver circuitry in the TXD± and TXP± pins. The driver circuitry provides the necessary electrical driving capability and the predistortion control for transmitting signals over maximum length twisted-pair cable, as specified by the IEEE 802.3 10BASE-T standard. During transmission, data is looped back to the DI± differential circuit, indicating normal operation. The transmit function for data output and loopback operations meets the propagation delays and jitter specified by the standard. During normal transmission, and providing that TPEX Plus is not in a Link Fail or Jabber state, the XMT pin will be driven LOW, and can be used to drive a status LED directly.

Twisted-Pair Receive Function

The receiver complies with the receiver specifications of the IEEE 802.3 10BASE-T standard, including noise immunity and received signal rejection criteria ("Smart Squelch"). Signals meeting these criteria appearing at the RXD \pm differential input pair are routed to the DI \pm outputs. The receiver function meets the propagation delays and jitter requirements specified by the standard. The receiver squelch level drops to approximately half its threshold value after unsquelch to allow reception of minimum amplitude signals and to mitigate carrier fade in the event of worst-case signal attenuation and crosstalk noise conditions. During receive, the RCV pin is driven LOW and can be used to drive a status LED directly.

Note that the 10BASE-T standard defines the receive input amplitude at the external media-dependent interface (MDI). Filter and transformer loss are not specified. The TPEX Plus receiver squelch levels are defined to account for a 1 dB insertion loss at 10 MHz, which is typical for the type of receive filters/transformers recommended (see also Table 1).

Normal 10BASE-T-compatible receive thresholds are employed when the LRT pin is inactive (HIGH). When the LRT pin is externally pulled LOW, the Low Receive Threshold option is invoked, and the sensitivity of the TPEX Plus receiver is increased. This allows longer line lengths to be employed, exceeding the 100 m target distance of normal 10BASE-T (assuming typical 24 AWG cable). The additional cable distance contributes directly to increased signal attenuation and reduced signal amplitude at the TPEX Plus receiver. However, from a system perspective, making the receiver more sensitive means that it is also more susceptible to extraneous noise, primarily caused by coupling from co-resident services (crosstalk). For this reason, it is recommended that when using the Low Receive Threshold option, the service should be installed on 4-pair cable only. Multipair cables within the same outer sheath have lower crosstalk attenuation, may allow noise emitted from adjacent pairs to couple into the receive pair, and be of sufficient amplitude to falsely unsquelch the TPEX Plus.

Link Test Function

The Link Test function is implemented as specified by the 10BASE-T standard. During periods of transmit pair inactivity, "link beat" pulses will be sent periodically over the twisted-pair medium to allow constant monitoring of medium integrity.

When the Link Test function is enabled, the absence of link beat pulses and receive data on the RXD± pair will cause the TPEX Plus to go into a Link Fail state. In the Link Fail state, data transmission, data reception, data loopback, and collision detection functions are disabled and remain disabled until valid data or >5 consecutive link pulses appear on the RXD± pair. During Link Fail, the LNKST pin is internally pulled HIGH. When the link is identified as functional, the LNKST pin is driven LOW, and is capable of directly driving a "Link OK" LED. In order to interoperate with systems that do not implement Link Test, this function can be disabled by grounding the LNKST pin. With Link Test disabled, the data driver, receiver, and loopback functions, as well as collision detection, remain enabled irrespective of the presence or absence of data or link pulses on the RXD± pair.

Polarity Detection and Reversal

The TPEX Plus receive function includes the ability to invert the polarity of the signals appearing at the RXD \pm pair if the polarity of the received signal is reversed (such as in the case of a wiring error). This feature allows data packets received from a reverse-wired RXD \pm input pair to be corrected in the TPEX Plus prior to transfer to the DTE via the AUI interface (DI \pm). The

polarity detection function is activated following reset or Link Fail, and will reverse the receive polarity based on both the polarity of any previous link beat pulses and the polarity of subsequent packets with a valid end transmit delimiter (ETD).

When in the Link Fail state, TPEX Plus will recognize link beat pulses of either positive or negative polarity. Exit from the Link Fail state is caused by the reception of 5 to 6 consecutive link beat pulses of identical polarity. On entry to the Link Pass state, the polarity of the last 5 link beat pulses is used to determine the initial receive polarity configuration and the receiver is reconfigured to subsequently recognize only link beat pulses of the previously recognized polarity. This link pulse algorithm is employed only until SFD polarity determination is made, as described later in this section.

Positive link beat pulses are defined as received signal with a positive amplitude greater than 520 mV (\overline{LRT} = HIGH) with a pulse width of 60 ns to 200 ns. This positive excursion may be followed by a negative excursion. This definition is consistent with the expected received signal at a correctly wired receiver, when a link beat pulse that fits the template of Figure 14-12 in the 10BASE-T standard is generated at a transmitter and passed through 100 m of twisted-pair cable.

Negative link beat pulses are defined as received signals with a negative amplitude greater than 520 mV (\overline{LRT} = HIGH) with a pulse width of 60 ns to 200 ns. This negative excursion may be followed by a positive excursion. This definition is consistent with the expected received signal at a reverse-wired receiver, when a link beat pulse that fits the template of Figure 14-12 in the 10BASE-T standard is generated at a transmitter and passed through 100 m of twisted-pair cable.

The polarity detection/correction algorithm will remain "armed" until two consecutive packets with valid ETD of identical polarity are detected. When "armed," the receiver is capable of changing the initial or previous polarity configuration based on the most recent ETD polarity.

On receipt of the first packet with valid ETD following reset or Link Fail, TPEX Plus will utilize the inferred polarity information to configure its RXD \pm input, regardless of its previous state. On receipt of a second packet with a valid ETD with correct polarity, the detection/correction algorithm will "lock in" the received polarity. If the second (or subsequent) packet is not detected as confirming the previous polarity decision, the most recently detected ETD polarity will be used as the default. Note that packets with invalid ETD have no effect on updating the previous polarity decision. Once two consecutive packets with valid ETD have been received, TPEX Plus will disable the detection/correction

algorithm until either a Link Fail condition occurs or PRDN/RST is asserted.

During polarity reversal, the RXPOL pin is internally pulled HIGH. During normal polarity conditions, the RXPOL pin is driven LOW, and is capable of directly driving a "Polarity OK" LED using an integrated 12 mA driver. If desired, the Polarity Reversal function can be disabled by grounding the RXPOL pin.

Twisted-Pair Interface Status

Three outputs (\overline{XMT} , \overline{RCV} , and \overline{COL}) indicate whether the TPEX Plus is transmitting (AUI to twisted-pair), receiving (twisted-pair to AUI), or in a collision state with both functions active simultaneously.

The TPEX Plus will power up in the Link Fail state. The normal algorithm will apply to allow it to enter the Link Pass state. On power up, the \overline{XMT} , \overline{RCV} , and \overline{COL} LED drivers activate for 20 ms to 62 ms as a lamp test feature, and will then go to their inactive state until TPEX Plus enters the Link Pass state.

In the Link Pass state, transmit or receive activity that passes the pulse-width/amplitude requirements of the DO \pm or RXD \pm inputs will be indicated by the XMT or RCV pin, respectively, going active. XMT, RCV, and COL are all asserted during a collision.

In the Link Fail state, \overline{XMT} , \overline{RCV} , and \overline{COL} are disabled.

In Jabber Detect mode, TPEX Plus will activate the COL driver, disable the XMT driver (regardless of DO \pm activity), and allow the RCV driver to indicate the current state of the RXD \pm pair. If there is no receive activity on RXD \pm , only COL will be active during Jabber Detect. If there is RXD \pm activity, both COL and RCV will be active.

All three outputs are active LOW and incorporate 12 mA drive capability with 20 ms to 62 ms pulse stretch circuitry, to extend the event to ensure LED visibility.

Collision Detect Function

Simultaneous Carrier Sense (presence of valid data signals) by both the AUI DO± pins and the twisted-pair RXD± pins constitutes a collision, thereby causing a 10 MHz signal to be asserted on the CI± output pair, and the COL output to be activated. The CI± output meets the drive requirements for the AUI interface. This 10 MHz signal will remain on the CI± pair until one of the two colliding states changes from active to idle. During the collision condition, data presented on the DI± pair will be sourced from the RXD± input. At the end of collision, the data presented on the DI± pair will be sourced from the last remaining active input, either RXD± or DO±. The CI± output pair stays HIGH for 2 bit times at the end of a collision, decreasing to the idle level within 80 bit times after the last transition. The XMT, RCV, and COL pins are driven LOW during collision.

Signal Quality Error (SQE) Test (Heartbeat) Function

When the SQE TEST pin is driven LOW, TPEX Plus will routinely exercise the collision detection circuitry by generating an SQE Test message at the end of every transmission. This signal is a self-test indication to the DTE that the MAU collision circuitry is functional and the AUI cable/connection is intact. An SQE Test message consists of a 10 MHz signal on the Cl± pair with a duration of 5 to 15 bit times (500 ns to 1500 ns). When enabled, an SQE Test will occur at the end of every transmission, starting 6 to 16 bit times (600 ns to 1600 ns) after the last transition of the transmitted signal. For repeater applications, the SQE Test function can be disabled by tying the <u>SQE TEST</u> pin HIGH or by leaving it disconnected. The <u>COL</u> output will remain inactive during the SQE Test message on Cl±.

Jabber Function

The Jabber function inhibits the twisted-pair transmit function of TPEX Plus if the DO± circuit is active for an excessive period (20 ms to 150 ms). This prevents any one node from disrupting the network due to a "stuck on" or faulty transmitter. If this maximum transmit time is exceeded, the TPEX Plus transmitter circuitry is disabled and a 10 MHz signal is driven onto the Cl± pair. Once the transmit data stream is removed from the DO± input pair, an "unjab" time of 250 ms to 750 ms will elapse before the TPEX Plus removes the 10 MHz signal from the Cl± pair and re-enables the transmit circuitry.

When jabber is detected, TPEX Plus will activate the \overline{COL} driver, disable the \overline{XMT} driver (regardless of DO± activity), and allow the RCV driver to indicate the current state of the RXD± pair. If there is no receive activity on RXD±, only COL will be active during Jabber Detect. If there is RXD± activity, both COL and RCV will be active.

Power Down

In addition to on-board power-on-reset circuitry, the PRDN/RST pin is used as the master reset for TPEX Plus. PRDN/RST must be driven LOW for a minimum of 2 μ s for reset to occur. The PRDN/RST pin can also be used to put the TPEX Plus into an inactive or "sleep" state, causing the device to consume less power. This feature is useful in battery-powered or low-duty-cycle systems. Driving PRDN/RST LOW resets the internal logic of TPEX Plus and places the device into idle mode. In this mode, the twisted-pair driver pins (TXD±, TXP±) are driven LOW, the AUI pins (Cl±, Dl±) are pulled to AV_{DD}, the LNKST and RXPOL pins are in the inactive state, and the XMT, RCV, and COL pins are in the high-impedance state. TPEX Plus will remain in idle mode as long as PRDN/RST is asserted. Following the rising edge of the signal on PRDN/RST, TPEX Plus will remain in the reset state for up to 10 μ s. Immediately after the reset condition is removed, TPEX Plus will drive the XMT, RCV, and COL outputs LOW for 20 ms to 62 ms as a lamp test feature, and will be forced into the Link Fail state. TPEX Plus will move to the Link Pass state only after 5 to 6 link beat pulses and/or a single received message is detected on the RXD± pair.

Test Modes

TPEX Plus implements two types of loopback test modes suitable for Station (DTE) or Repeater applications. The test mode is entered by driving the TEST1 pin HIGH. The TEST2 pin is intended for factory test only and should be tied HIGH for test mode or normal operation. The two available test modes are:

- Station (DTE): SQE TEST pin LOW. Data received on the DO± input pair is transmitted onto the TXD± and TXP± output pairs, and data received on the RXD± input pair is transmitted onto the DI± output pair.
- Repeater: SQE TEST pin HIGH. Data received on the DO± input pair is looped back onto the DI± output pair, and data received on the RXD± pair is looped back and retransmitted on the twisted-pair drivers (TXD± and TXP± pairs).

In both modes, TPEX Plus will be forced into the Link Pass state and will not enter the Link Fail state, regardless of RXD± inactivity. The following functions are disabled: jabber circuit, collision detection, and collision oscillator. The functions that remain enabled are: the DO± and RXD± squelch circuits, XMT and RCV outputs, link beat pulse generation, and polarity detection/ correction. In addition, in both modes, the COL pin (not used to indicate collision during test modes) will go active for the duration of any transmit activity on the TXD±/TXP± pairs, providing a leading high-to-low edge indicating the start of packet transmission or link beat pulse generation.

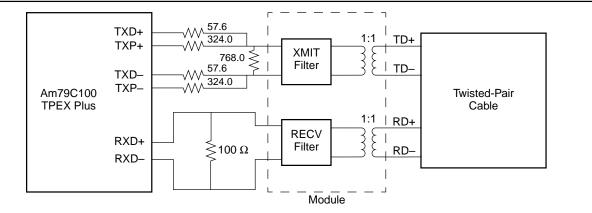
Upon exiting either of the test modes, the Link Test State Machine will be forced into the Link Fail state.

RXPOL may be pulled LOW and receive polarity correction will be disabled.

TPEX Plus External Components

Figure 1 shows a typical twisted-pair port external components schematic. The resistors used should have a \pm 1% tolerance to ensure interoperability with 10BASE-T-compliant networks. The filters and pulse transformers are necessary devices that have a major influence on the performance and compliance of a TPEX Plus-based MAU. Specifically, the transmitted waveforms are heavily influenced by filter characteristics and the twisted-pair receivers employ several

criteria to continuously monitor the incoming signal's amplitude and timing characteristics to determine when and if to assert the internal carrier sense. For these reasons, it is crucial that the values and tolerances of the external components be as specified. Several manufacturers produce a module that combines the functions of the transmit and receive filters and the pulse transformers into one package.



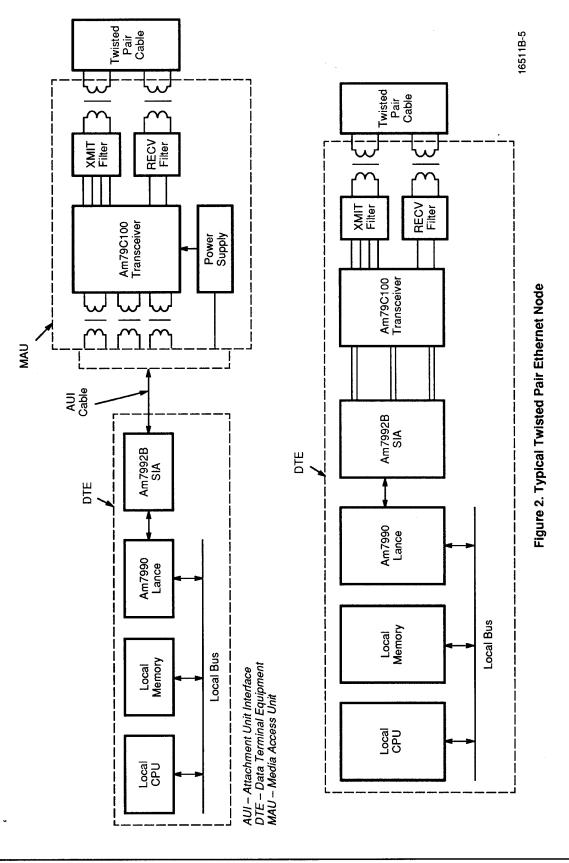
16511B-4

Note:

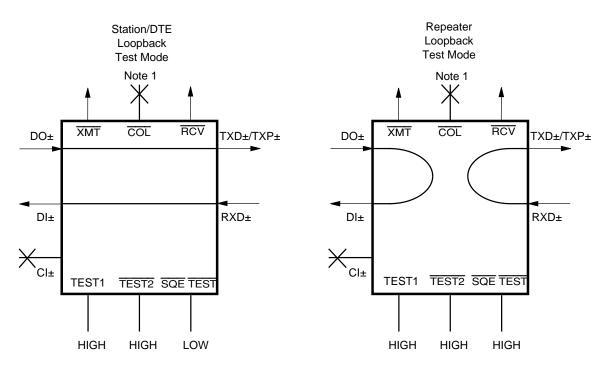
The filter/transformer module shown is available from the following manufacturers: Belfuse, TDK, Pulse Engineering, PCA, Valor Electronics, and Nano Pulse.

Figure 1. Typical Twisted-Pair Port External Components

TYPICAL APPLICATIONS



Am79C100



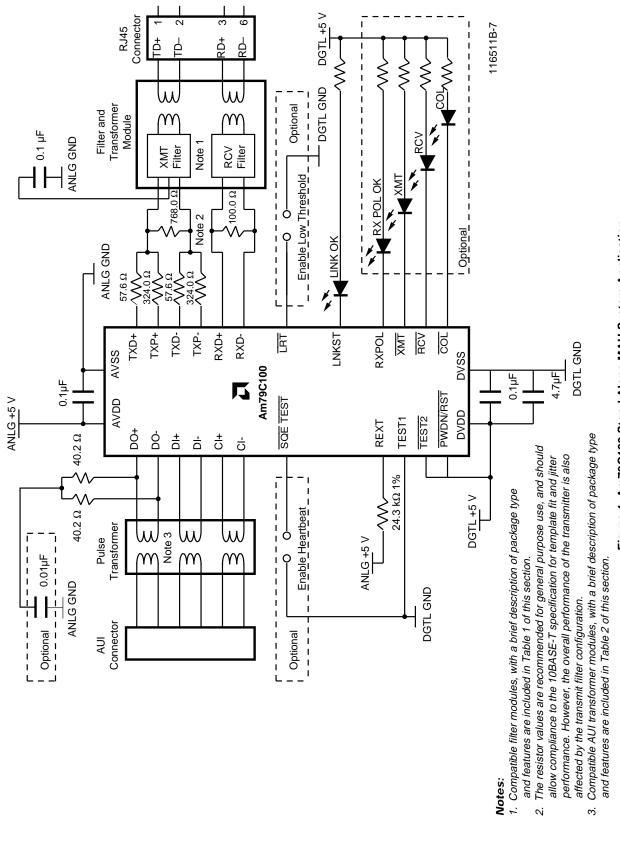
Note:

16511B-6

 During Loopback, the COL pin does not indicate collision, but instead provides indication of TXD±/TXP± activity. For details, refer to the section titled "Test Modes."

Figure 3. Am79C100 TPEX Plus Loopback Operation

SYSTEM APPLICATIONS



Am79C100

| Manufacturer | Part # | Package | Description |
|-------------------|--------------|-----------------|---|
| Bel Fuse | A556-2006-DE | 16-pin 0.3" DIL | Transmit and receive filters and transformers |
| Bel Fuse | 0556-2006-00 | 14-pin SIP | Transmit and receive filters and transformers |
| Bel Fuse | 0556-2006-01 | 14-pin SIP | Transmit and receive filters, transformers and common mode chokes |
| Valor Electronics | PT3877 | 16-pin 0.3" DIL | Transmit and receive filters and transformers |
| Valor Electronics | PT3983 | 8-pin 0.3" DIL | Transmit and receive common mode chokes |
| Valor Electronics | FL1012 | 16-pin 0.3" DIL | Transmit and receive filters and transformers, transmit common mode choke |
| Nano pulse | NP6612 | 16-pin 0.3" DIL | Transmit and receive filters, transformers and common mode chokes |
| Nano pulse | NP6581 | 8-pin 0.3" DIL | Transmit and receive common mode chokes |
| Nano pulse | NP6696 | 24-pin 0.6" DIL | Transmit and receive filters, transformers and common mode chokes |
| TDK | TLA 470 | 14-pin SIP | Transmit and receive filters and transformers |
| TDK | HIM3000 | 24-pin 0.6" DIL | Transmit and receive filters, transformers and common mode chokes |
| Pulse Engineering | PE65421 | 16-pin 0.3" DIL | Transmit and receive filters and transformers |
| Pulse Engineering | SUPRA 1.1 | 16-pin 0.5" DIL | Transmit and receive filters and transformers, transmit common mode choke |
| Bel Fuse | 0556-6392-00 | 16-pin 0.5" DIL | Transmit and receive filters, transformers, and common mode chokes |

Table 2. Am79C100 TPEX Plus Compatible AUI Transformers

| Manufacturer | Part # | Package | Description |
|-------------------|--------------|-----------------|-------------|
| Bel Fuse | A553-0506-AB | 16-pin 0.3" DIL | 50 μΗ |
| Valor Electronics | LT6031 | 16-pin 0.3" DIL | 50 μΗ |
| TDK | TLA 100-3E | 16-pin 0.3" DIL | 100 μH |
| Pulse Engineering | PE64106 | 16-pin 0.3" DIL | 50 μΗ |

ABSOLUTE MAXIMUM RATINGS

Storage Temperature: -65°C to +150°C Ambient Temperature Under Bias: 0°C to +70°C Supply Voltage to AV_{SS} or DV_{SS} (AV_{DD}, DV_{DD}): -0.3 V to +6 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

| Temperature (T _A): $0^{\circ}C$ to +70°C |
|--|
| Supply Voltages (AV _{DD} , DV _{DD}):+5 V \pm 5% |
| All inputs within the range: |
| AVss–0.5 V \leq Vin \leq AVdd + 0.5 V, or |
| DV_{SS} –0.5 V \leq VIN \leq DV_{DD} +0.5 V |
| |

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating range unless otherwise specified

| Parameter Symbol | Parameter Description | Test Conditions | Min | Max | Unit |
|---------------------|--|-----------------------------------|-----------------------|-----------------------|------|
| Digital Input | Voltage | | | | |
| VIL | Input LOW Voltage | | | 0.8 | V |
| Viн | Input HIGH Voltage | | 2.0 | | V |
| Digital Outpu | t Voltage | · | | • | |
| Vol | Output LOW Voltage (XMT, RCV, COL, LNKST and RXPOL) | IoL = 12 mA (Open Drain) | | 0.4 | V |
| Digital Input | Leakage Current | | | | |
| l _{ILL} | Input Leakage Current (PRDN/RST) | $DV_{SS} < V_{IN} < DV_{DD}$ | | 10 | μA |
| lild | Input Leakage Current (LNKST/RXPOL, output inactive) | DVss < Vin < DVdd | | 500 | μA |
| Digital Outpu | t Leakage Current | | | | |
| Iold | Output Leakage Current (XMT, RCV, COL) | DVss < Vin < DVdd | | 10 | μA |
| AUI | | • | | | |
| I _{IAXD} | Input Current at DO+, DO- | $AV_{SS} < Vin < AV_{DD}$ | -500 | 500 | μA |
| VAICM | DO± Open Circuit Input Common Mode Voltage (Bias) | lin = 0 V | AV _{DD} -3.0 | AV _{DD} -1.0 | V |
| VAIDV | Differential Mode Input Voltage Range (DO±) | Avdd = +5 V | -2.5 | +2.5 | V |
| Vasq | DO± Squelch Threshold | | -160 | -275 | mV |
| Vath | DO± Switching Threshold | (Note 1) | -35 | +35 | mV |
| Vaod | Differential Output Voltage (DI+)–(DI–) OR (CI+)–(CI–) | RL = 78 Ω | 620 | 1100 | mV |
| Vaodi | DI± & CI± Differential Output Voltage Imbalance | R _L = 78 Ω (Note 1) | -25 | +25 | mV |
| VAODOFF | DI± & CI± Differential Idle Output Voltage | RL = 78 Ω | -40 | +40 | mV |
| IAODOFF | DI± & CI± Differential Idle Output Current | R _L = 78 Ω (Note 1) | -1 | 1 | mA |
| VAOCM | DI± & CI± Common Mode Output Voltage | RL = 78 Ω | 2.5 | AV _{DD} | V |

DC CHARACTERISTICS (continued)

| Parameter Symbol | Parameter Description | Test Conditions | Min | Max | Uni |
|---------------------|--|---|-----------|------------|-----|
| Twisted Pair | Interface | • | • | • | |
| I _{IRXD} | Input Current at RXD± | AVss < VIN < AVDD | -500 | 500 | uA |
| R _{RXD} | RXD± Differential Input Resistance | (Note 1) | 10 | | KΩ |
| VTIVB | RXD+, RXD– Open Circuit Input Voltage (Bias) | lın = 0 mA | Avdd -3.0 | Avdd -1.5 | V |
| Vtidv | Differential Mode Input Voltage Range (RXD±) | AV _{DD} = +5 V | -3.1 | 3.1 | V |
| VTSQ+ | RXD Positive Squelch Threshold (Peak) | Sinusoid 5 MHz < f < 10 MHz | 300 | 520 | m\ |
| Vtsq- | RXD Negative Squelch Threshold (Peak) | Sinusoid 5 MHz < f < 10 MHz | -520 | -300 | m۱ |
| V _{THS+} | RXD Post-Squelch Positive Threshold (Peak) | Sinusoid 5 MHz < f < 10 MHz | 150 | 293 | ۳۱ |
| VTHS- | RXD Post-Squelch Negative Threshold (Peak) | Sinusoid 5 MHz < f < 10 MHz | -293 | -150 | ۳۱ |
| Vltsq+ | RXD Positive Squelch Threshold (Peak) | LRT = LOW | 180 | 312 | ۳۱ |
| Vltsq- | RXD Negative Squelch Threshold (Peak) | LRT = LOW | -312 | -180 | mʻ |
| V _{LTHS+} | RXD Post-Squelch Positive Threshold (Peak) | LRT = LOW | 90 | 175 | mʻ |
| VLTHS- | RXD Post-Squelch Negative Threshold (Peak) | LRT = LOW | -175 | -90 | mʻ |
| Vrxdth | RXD Switching Threshold | (Note 1) | -60 | 60 | m |
| Vtxh | TXD± and TXP± Output HIGH Voltage | DVss = 0 V (Note 2) | DVDD -0.6 | DVdd | V |
| Vtxl | TXD± and TXP± Output LOW Voltage | DVss = +5 V (Note 2) | DVss | DVss + 0.6 | V |
| V _{TXI} | TXD± and TXP± Differential Output Voltage Imbalance | | -40 | 40 | mʻ |
| Vtxoff | TXD± and TXP± Idle Output Voltage | DV _{DD} = +5 V | -40 | 40 | m |
| Rtx | TXD± and TXP± Differential Driver Output Impedance | (Note 1) | | 40 | Ω |
| IIREXT | Input Current at REXT Pin | Rext = 24.3 kΩ ±1% AV _{DD} = +5 V | | 120 | μA |
| Power Supply | y Current | | | | |
| IDD | Power Supply Current (Idle) | $\overline{PRDN/RST} = HIGH$ $DV_{DD} = AV_{DD} = +5 V$ | | 40 | m/ |
| | Power Supply Current (Transmitting—No TP load) | PRDN/RST = LOW | | 95 | m |
| | Power Supply Current (Transmitting—with TP load) | PRDN/RST = HIGH DVdd = AVdd = +5 V | | 150 | m/ |
| Iddprdn | Power Supply Current in Power Down Mode | PRDN/RST = LOW | | 4 | m/ |

Notes:

1. Parameter not tested.

2. Uses switching test load.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges

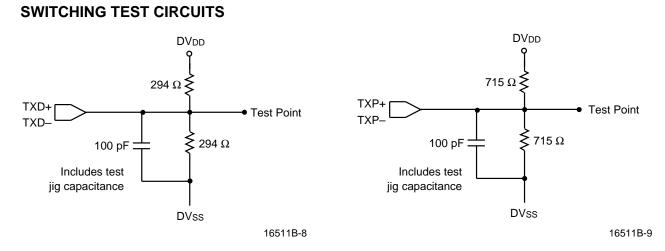
| Parameter Symbol | Parameter Description | Test Conditions | Min | Max | Unit |
|---------------------|---|--|-----------------------|-----------------------|----------|
| Transmit Tin | ning | • | • | • | <u>.</u> |
| t PWODO | DO Pulse Width Accept/ Reject Threshold | VDO > VASQ max (Note 3) | 15 | 35 | ns |
| t PWKDO | DO Pulse Width Maintain/ Turn-Off Threshold | V _{DO} > V _{ASQ} max (Note 4) | 105 | 200 | ns |
| t ton | Transmit Start Up Delay | | | 300 | ns |
| t tsd | Transmit Static Propagation Delay (DO± to TXD±) | | | 120 | ns |
| t tetd | Transmit End Transmit Delimiter | | 250 | 450 | ns |
| t TR | Transmitter Rise Time (10% to 90%) | | | 10 | ns |
| tτϝ | Transmitter Fall Time (90% to 10%) | | | 10 | ns |
| tтм | Transmitter Rise and Fall Time Mismatch | | | 4 | ns |
| tтнр | DO ↑ to TXD+ ↑ and TXD– ↓ Delay | Steady State (Note 1) | ttsd – 1.0 | ttsd + 1.0 | ns |
| tτld | DO \downarrow to TXD+ \downarrow and TXD– \uparrow Delay | Steady State (Note 1) | ttsd – 1.0 | ttsd + 1.0 | ns |
| t thdp | DO \uparrow to TXP+ \downarrow and TXP- \uparrow Delay | Steady State (Note 1) | ttsd + 40 | ttsd + 60 | ns |
| t _{TLDP} | DO \downarrow to TXP+ \uparrow and TXP- \downarrow Delay | Steady State (Note 1) | t _{TSD} + 40 | t _{TSD} + 60 | ns |
| t XMTON | XMT Asserted Delay | | | 100 | ns |
| t XMTOFF | XMT De-asserted Delay | | 20 | 62 | ms |
| t PERLP | Idle Signal Period | | 8 | 24 | ms |
| t PWLP | Link Beat Pulse Width | (Note 1) | 75 | 120 | ns |
| t PWPLP | Predistortion Idle Link Beat Width | (Note 1) | 40 | 60 | ns |
| tJA | Transmit Jabber Activation Time | | 20 | 150 | ms |
| t _{JR} | Transmit Jabber Reset Time | | 250 | 750 | ms |
| tjrec - | Transmit Jabber Recovery Time (Minimum time gap between transmitted packets to prevent jabber activation) | (Note 1) | 1.0 | - | μs |
| t DODION | DO to DI Startup Delay | | | 300 | ns |
| tDODISD | DO to DI Static Propagation Delay | | | 100 | ns |

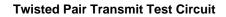
SWITCHING CHARACTERISTICS (Continued)

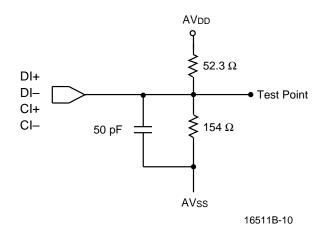
| Parameter Symbol | Parameter Description | Test Conditions | Min | Max | Unit |
|---------------------|--|-------------------------------|------------|------------|------|
| Receive Tim | ing | • | • | • | 1 |
| t PWKRD | RXD Pulse Width Maintain/ Turn-Off Threshold | VIN >VTHS min (Note 5) | 136 | 200 | ns |
| tron | Receiver Start Up Delay (RXD to Dl±) | Tested with 5 MHz Sinusoid | 200 | 400 | ns |
| trvв | First Validly Timed Bit on DI± | | | tron+100 | ns |
| tRSD | Receiver Static Propagation Delay (RXD± to DI±) | | | 70 | ns |
| t RETD | DI End of Transmission | | 200 | | ns |
| tRHD | RXD \pm 1 to DI+ 1 and DI- \downarrow Delay | (Note 1) | trsd – 2.5 | tRSD + 2.5 | ns |
| trld | RXD $\pm \downarrow$ to DI+ \downarrow and DI- \uparrow Delay | (Note 1) | trsd – 2.5 | tRSD + 2.5 | ns |
| tRR | DI+, DI–, CI+, CI– Rise Time (10% to 90%) | | | 5 | ns |
| t _{RF} | DI+, DI–, CI+, CI– Fall Time (10% to 90%) | | | 5 | ns |
| trм | DI± and CI± Rise and Fall Time Mismatch (trR – trF) | | | 2 | ns |
| t RCVON | RCV Asserted Delay | | tron – 50 | tron + 100 | ns |
| trcvoff | RCV De-asserted Delay | | 20 | 62 | ms |
| Collision Det | tection and SQE Test | · | - | - | - |
| tCON | Collision Turn-On Delay (Cl±) | | | 500 | ns |
| tCOFF | Collision Turn-Off Delay (Cl±) | | | 500 | ns |
| t PER | Collision Period (CI±) | | 87 | 117 | ns |
| tCPW | Collision Output Pulse Width (CI±) | | 40 | 60 | ns |
| tsqed | SQE Test Delay Time | | 600 | 1600 | ns |
| t SQEL | SQE Test Length | | 500 | 1500 | ns |
| tCOLON | COL Asserted Delay | | tcon – 50 | tcon + 100 | ns |
| tCOLOFF | COL De-asserted Delay | | 20 | 62 | ms |

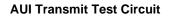
Notes:

- 1. Parameter not tested.
- 2. Uses switching test load.
- 3. DO pulses narrower than tpwodo (min) will be rejected; pulses wider than tpwodo (max) will turn internal DO carrier sense on.
- 4. DO pulses narrower than tPWKDO (min) will maintain internal DO carrier sense on; pulses wider than tPWKDO (max) will turn internal DO carrier sense off.
- 5. RXD pulses narrower than tPWKRD (min) will maintain internal RXD carrier sense on; pulses wider than tPWKRD (max) will turn internal RXD carrier sense off.

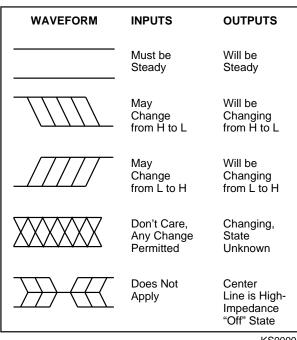






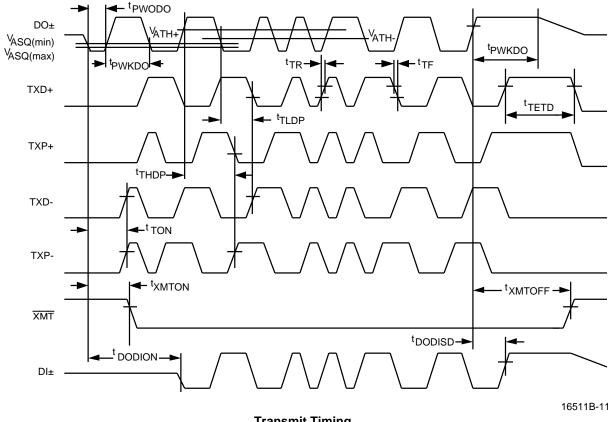


KEY TO SWITCHING WAVEFORMS

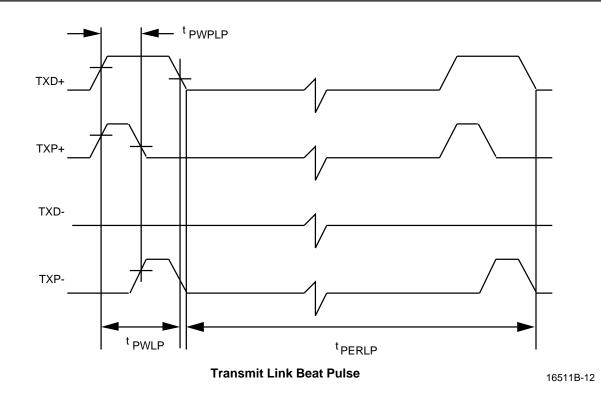


KS000010

SWITCHING WAVEFORMS

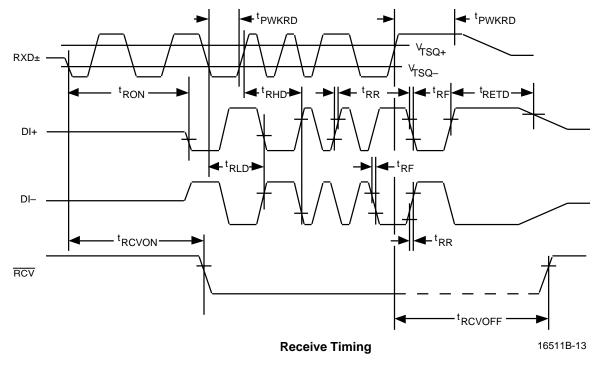


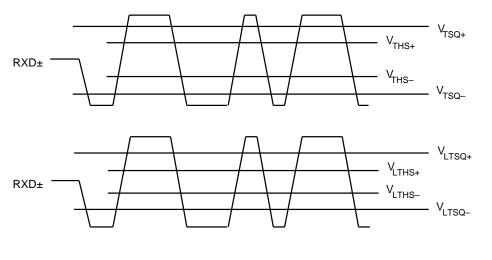
Transmit Timing



Am79C100

SWITCHING WAVEFORMS

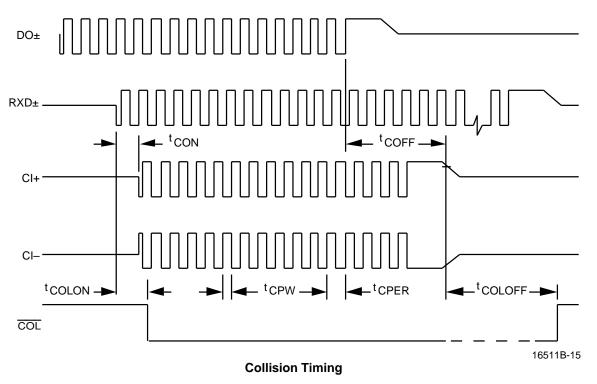


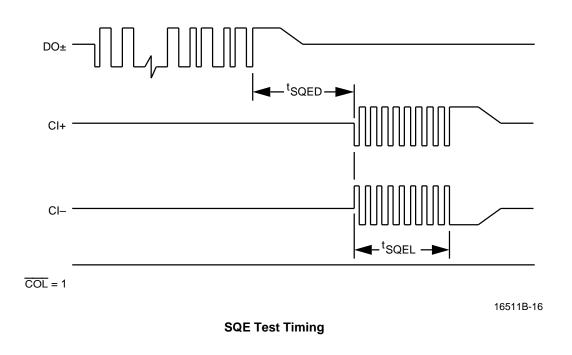


16511B-14

Receive Thresholds

SWITCHING WAVEFORMS





Trademarks

Copyright © 1998 Advanced Micro Devices, Inc. All rights reserved.

AMD, the AMD logo, and combinations thereof are trademarks of Advanced Micro Devices, Inc.

Am186, Am386, Am486, Am29000, *b*IMR, eIMR, eIMR+, GigaPHY, HIMIB, ILACC, IMR, IMR+, IMR2, ISA-HUB, MACE, Magic Packet, PCnet, PCnet-*FAST*, PCnet-*FAST*+, PCnet-Mobile, QFEX, QFEXr, QuASI, QuEST, QuIET, TAXIchip, TPEX, and TPEX Plus are trademarks of Advanced Micro Devices, Inc.

Microsoft is a registered trademark of Microsoft Corporation.

Product names used in this publication are for identification purposes only and may be trademarks of their respective companies.