

LB11999,11999H

Three-Phase Brushless Motor Drivers for CD-ROM Spindle Motor Driver (supports 44×, 48×, 50×)

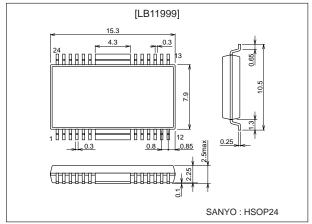
Features

- · Current linear drive
- Control V type amplifier
- Separate power supply for output upper side bias circuit allows low output saturation by boosting this power supply only (useful for 5V power supply types).
- Upper side current detection technique loses loss voltage of current detection resistor. Voltage drop caused by this resistor reduces internal power dissipation of IC.
- Built-in short braking circuit
- · Built-in reverse blocking circuit
- · Hall FG output
- Built-in S/S function
- Built-in current limiter circuit (selectable, 2 steps)
- Built-in Hall power supply
- · Built-in thermal shutdown circuit
- Supports 3.3V DSP

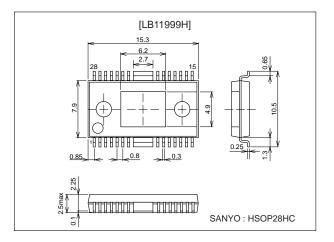
Package Dimensions

unit: mm

3227-HSOP24



3234-HSOP28HC



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Specifications

Absolute Maximum Ratings at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum power supply voltage 1	VCC1max		7.0	V
Maximum power supply voltage 2	VCC2max		14.4	V
Maximum power supply voltage 3	VCC3max		14.4	V
Maximum applied output voltage	Vomax		14.4	V
Maximum applied intput voltage	Vimax		VCC1	V
Maximum output current	Iomax		1.3	Α
Allowable power dissipation	Pdmax	*With specified substrate	0.8 (*1.9)	W
Operating temperature	Topr		-20 to +75	℃
Storage temperature	Tstr		-55 to +150	°C

Allowable Operating Ranges at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage 1	VCC1		4 to 6	V
Power supply voltage 2	VCC2	≥VCC1	4 to 13.6	V
Power supply voltage 3	VCC3		4 to 13.6	V

Application Example at $Ta = 25^{\circ}C$

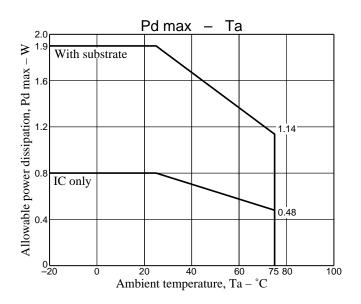
(1) 12V type

Power supply pin	Conditions	Ratings	Unit
VCC1	Regulated voltage	4 to 6	V
VCC2 = VCC3	Unregulated voltage	4 to 13.6	V

(2) 5V type

Power supply pin	Conditions	Ratings	Unit
VCC1 = VCC3	Regulated voltage	4 to 6	V
VCC2	Boost-up voltage or regulated voltage (Note)	4 to 13.6	V

Note: When boost-up voltage is used at VCC2, output can be set to low-saturation.



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Electrical Characteristics at $Ta = 25^{\circ}C$, Vcc1 = 5V, Vcc2 = Vcc3 = 12V (unless otherwise specified)

Power supply current	Daramatas	Cumbal	Conditions	Ratings			Unit	
Power supply current 1	Parameter	Symbol	Joi Conditions		typ	max	Offic	
Power supply current 2	[Power supply current]							
Power supply current 3	Power supply current 1	ICC1	VC = VCREF		8		mA	1
Output ide current 1 ICC1OQ VS/S = 0V 200 μA 4 Output ide current 2 ICC2OQ VS/S = 0V 30 μA 5 Output ide current 3 ICC2OQ VS/S = 0V 30 μA 5 Output ide current 3 ICC2OQ VS/S = 0V 30 μA 5 Output ide current 3 ICC2OQ VS/S = 0V 30 μA 5 Output ide current 3 ICC2OQ VS/S = 0V 30 μA 5 Saturation voltage, upper side 1 VOD1 IO = 0.5A, VCC1 = 5V, VCC2 = VCC3 = 12V 0.3 V 8 Saturation voltage, lower side 2 VOD12 IO = 0.5A, VCC1 = VCC3 = 5V, VCC2 = 12V 0.3 V 10 Current limiter setting voltage VCL1 RRF = 0.33Ω, LMC: OPEN 0.24 V 11 Iput bias current VHIB 1.2 VCC1-1.0 V 12 Imput bias current VHIB 1 1 μA 13 Imput bias current VHIB 2.0 VCC1	Power supply current 2	ICC2	VC = VCREF		0		mA	2
Output idle current 2 ICCZOQ VS/S = 0V 30 μA 5 Output idle current 3 ICC3OQ VS/S = 0V 30 μA 6 Output idle current 3 ICC3OQ VS/S = 0V 30 μA 6 Gutput idle current 3 ICC3OQ VS/S = 0V 30 μA 6 Saturation voltage, upper side 1 VOU1 IO = -0.5A, VCC1 = 5V, VCC2 = VCC3 = 12V 0.3 V 8 Saturation voltage, upper side 2 VOU2 IO = -0.5A, VCC1 = VCC3 = 5V, VCC2 = 12V 0.3 V 9 Saturation voltage, lower side 2 VOD2 IO = -0.5A, VCC1 = VCC3 = 5V, VCC2 = 12V 0.3 V 10 Current limiter setting voltage VCL1 RRF = 0.3302, LMC: OPEN 0.24 V 11 VCL1 RRF = 0.3302, LMC: OPEN 0.24 V 11 Iput Limiter setting voltage range VHCOM 1.2 VCC1-1.0 V 12 Imput Limiter setting voltage range VHCOM 1.2 VCC1-1.0 V 12 Imput bias current	Power supply current 3	ICC3	VC = VCREF		150	250	μΑ	3
Output idle current 3 ICC3OQ VS/S = 0V 30 μA 6 [Output] Saturation voltage, upper side 1 VOU1 IO = -0.5A, VCC1 = 5V, VCC2 = VCC3 = 12V 1.0 V 7 Saturation voltage, lower side 1 VOD1 IO = 0.5A, VCC1 = 5V, VCC2 = VCC3 = 12V 0.3 V 8 Saturation voltage, lower side 2 VOD2 IO = -0.5A, VCC1 = VCC3 = 5V, VCC2 = 12V 0.3 V 10 Current limiter setting voltage VCL1 RRF = 0.330, LMC: OPEN 0.24 V 11 Current limiter setting voltage VCL1 RRF = 0.330, LMC: GND 0.37 V 11 [Hall amplifier] Common mode input voltage range VHCOM 1.2 VCC1-1.0 V 12 Input bias current VHIB 1.2 VCC1-1.0 V 12 Input bias current VHIB 1.2 VCC1-1.0 V 12 Input bias current VHIB 0.7 V 12 Input bias current VHIB 0.7 V 12	Output idle current 1	ICC10Q	VS/S = 0V			200	μΑ	4
Output Saturation voltage, upper side 1	Output idle current 2	ICC2OQ	VS/S = 0V			30	μΑ	5
Saturation voltage, upper side 1	Output idle current 3	ICC3OQ	VS/S = 0V			30	μΑ	6
Saturation voltage, lower side 1 VOD1 IO = 0.5A, VCC1 = 5V, VCC2 = VCC3 = 12V 0.3 V 8 Saturation voltage, lower side 2 VOU2 IO = -0.5A, VCC1 = VCC3 = 5V, VCC2 = 12V 0.3 V 9 Saturation voltage, lower side 2 VOD2 IO = 0.5A, VCC1 = VCC3 = 5V, VCC2 = 12V 0.3 V 10 Current limiter setting voltage VCL1 RRF = 0.33Q, LMC: OPEN 0.24 V 11 Hall amplifier] VHCOM 1.2 VCC1-1.0 V 12 Input bias current VHIB 1 1 µA 13 Minimum Hall input level VHIN 60 mVp-p 14 IS/S pin VS/SH 2.0 VCC1 V 15 Low level voltage VS/SL VS/SL 0 0 µA 17 Leak current IS/SL VS/S=5V 0 0 µA 18 Low level voltage VS/SL VS/S=6V 0 0 µA 18 Low leve	[Output]							
Saturation voltage, upper side 2 VOU2 IO = -0.5A, VCC1 = VCC3 = 5V, VCC2 = 12V 0.3 V 9	Saturation voltage, upper side 1	VOU1	IO = -0.5A, VCC1 = 5V, VCC2 = VCC3 = 12V		1.0		V	7
Saturation voltage, lower side 2 VOD2 IO = 0.5A, VCC1 = VCC3 = 5V, VCC2 = 12V O.3 V 10	Saturation voltage, lower side 1	VOD1	IO = 0.5A, VCC1 = 5V, VCC2 = VCC3 = 12V		0.3		V	8
Current limiter setting voltage VCL1 RRF = 0.33Ω, LMC: OPEN 0.24 V 11 VCL2 RRF = 0.33Ω, LMC: GND 0.37 V 11 Iplat amplifier] Common mode input voltage range VHCOM 1.2 VCC1-1.0 V 12 Input bias current VHIB 1 µA 13 Minimum Hall input level VHIN 60 mVP-p 14 [SS pin] WCCI VI 15 Low level voltage VS/SH 2.0 VCCI V 15 Low level voltage VS/SL 0.7 V 16 Input current IS/SI VS/S = 5V 200 µA 17 Leak current IS/SI VS/S = 0V -30 µA 18 [Control] VC pin input current IVC VC = VCREF = 1.65V 1 µA 19 VC pin input current IVCREF VC = VCREF = 1.65V 0.35 times 21 Startup voltage gain GVCO ΔVRE/AVC 0.3	Saturation voltage, upper side 2	VOU2	IO = -0.5A, VCC1 = VCC3 = 5V, VCC2 = 12V		0.3		V	9
VCL2 RRF = 0.33Ω, LMC: GND 0.37 V 11 Hall amplifier] Common mode input voltage range VHCOM 1.2 VCC1-1.0 V 12 Input bias current VHIB 1 μA 13 Minimum Hall input level VHIN 60 mVP-p 14 IS/S pin]	Saturation voltage, lower side 2	VOD2	IO = 0.5A, VCC1 = VCC3 = 5V, VCC2 = 12V		0.3		V	10
Hall amplifier] Common mode input voltage range VHCOM 1.2 VCC1-1.0 V 12 Input bias current VHIB	Current limiter setting voltage	VCL1	RRF = 0.33Ω , LMC: OPEN		0.24		V	11
Common mode input voltage range VHCOM 1.2 VCC1-1.0 V 12 Input bias current VHIB 1 μA 13 Minimum Hall input level VHIN 60 mVp-p 14 [S/S pin] High level voltage VS/SH 2.0 VCC1 V 15 Low level voltage VS/SL 2.0 VCC1 V 15 Low level voltage VS/SL 2.0 VCC1 V 15 Low level voltage VS/SL VS/SL 0.7 V 16 Input current IS/SL VS/S = 5V 200 μA 17 Leak current IS/SL VS/S = 0V -30 μA 18 [Control] VC pin input current IVC VC = VCREF = 1.65V 1 1 μA 19 VCREF pin input current IVCREF VC = VCREF = 1.65V 1 1 μA 20 Voltage gain GVCO ΔVRE/ΔVC 0.35 1 1 μA		VCL2	RRF = 0.33Ω , LMC: GND		0.37		V	11
Input bias current VHIB	[Hall amplifier]	•						
Minimum Hall input level VHIN 60 mVp-p 14 S/S pin High level voltage VS/SH 2.0 VCC V 15 Low level voltage VS/SL 0.7 V 16 Input current IS/SI VS/S = 5V 200 μA 17 Leak current IS/SI VS/S = 0V -30 μA 18 IControl VC pin input current IVC VC = VCREF = 1.65V 1 μA 19 VCREF pin input current IVCREF VC = VCREF = 1.65V 1 μA 20 Voltage gain GVCO ΔVRE/ΔVC 0.35 times 21 Startup voltage VCTH VCREF = 1.65V 1.5 1.8 V 22 Startup voltage width ΔVCTH VCREF = 1.65V 50 150 mV 23 Hall power supply voltage VH IH = 5 mA 0.8 V 24 Allowable current ITSD 150 180 210 °C Target Hysteresis ΔTTSD 15 °C Target Starke pin at High level VBRH 4 5 V 26 Starke pin at High level VBRH 4 5 V 26 Starke pin at High level VBRH 4 5 V 26 Allowable pin at High level VBRH 4 5 V 26 Control 2.0 2.0 2.0 Control 2.0 2.0 2.0 Control 2.0 2.0 Control 2.0 2.0 Control 2.0 Control	Common mode input voltage range	VHCOM		1.2		VCC1-1.0	V	12
S/S pin High level voltage	Input bias current	VHIB			1		μΑ	13
High level voltage	Minimum Hall input level	VHIN		60			mVp-p	14
Low level voltage VS/SL 0.7 V 16 Input current IS/SI VS/S = 5V 200 μA 17 Leak current IS/SL VS/S = 0V -30 μA 18 [Control] VC pin input current IVC VC = VCREF = 1.65V 1 μA 19 VCREF pin input current IVCREF VC = VCREF = 1.65V 1 μA 20 Voltage gain GVCO ΔVE/ΔVC 0.35 times 21 Startup voltage VCTH VCREF = 1.65V 1.5 1.8 V 22 Startup voltage width ΔVCTH VCREF = 1.65V 50 150 mV 23 [Hall power supply] Hall power supply voltage VH IH = 5 mA 0.8 V 24 Allowable current IH 20 mA 25 [Thermal shutdown] Operating temperature TTSD 150 180 210 °C Target Hysteresis ΔTTSD 15 °C Target Brake pin at High level V	[S/S pin]							
Input current	High level voltage	VS/SH		2.0		VCC1	V	15
Leak current IS/SL VS/S = 0V -30 μA 18	Low level voltage	VS/SL				0.7	V	16
Control VC pin input current	Input current	IS/SI	VS/S = 5V			200	μΑ	17
VC pin input current IVC VC = VCREF = 1.65V 1	Leak current	IS/SL	VS/S = 0V	-30			μΑ	18
VCREF pin input current IVCREF VC = VCREF = 1.65V 1 μA 20 Voltage gain GVCO ΔVRΕ/ΔVC 0.35 times 21 Startup voltage VCTH VCREF = 1.65V 1.5 1.8 V 22 Startup voltage width ΔVCTH VCREF = 1.65V 50 150 mV 23 [Hall power supply] Hall power supply voltage VH IH = 5 mA 0.8 V 24 Allowable current IH 20 mA 25 [Thermal shutdown] Operating temperature TTSD 150 180 210 °C Target Hysteresis ΔTTSD 15 °C Target [Short braking] Brake pin at High level VBRH 4 5 V 26	[Control]	•						
Voltage gain GVCO ΔVRE/ΔVC 0.35 times 21 Startup voltage VCTH VCREF = 1.65V 1.5 1.8 V 22 Startup voltage width ΔVCTH VCREF = 1.65V 50 150 mV 23 [Hall power supply] Hall power supply voltage VH IH = 5 mA 0.8 V 24 Allowable current IH 20 mA 25 [Thermal shutdown] Operating temperature TTSD 150 180 210 °C Target Hysteresis ΔTTSD 15 °C Target [Short braking] Brake pin at High level VBRH 4 5 V 26	VC pin input current	IVC	VC = VCREF = 1.65V			1	μΑ	19
Startup voltage VCTH VCREF = 1.65V 1.5 1.8 V 22	VCREF pin input current	IVCREF	VC = VCREF = 1.65V			1	μΑ	20
Startup voltage width ΔVCTH VCREF = 1.65V 50 150 mV 23 [Hall power supply] Hall power supply voltage VH IH = 5 mA 0.8 V 24 Allowable current IH 20 mA 25 [Thermal shutdown] Operating temperature TTSD 150 180 210 °C Target Hysteresis ΔTTSD 15 °C Target [Short braking] Brake pin at High level VBRH 4 5 V 26	Voltage gain	GVCO	ΔVRE/ΔVC		0.35		times	21
[Hall power supply] Hall power supply voltage	Startup voltage	VCTH	VCREF = 1.65V	1.5		1.8	V	22
Hall power supply voltage	Startup voltage width	ΔVCTH	VCREF = 1.65V	50		150	mV	23
Allowable current IH 20 mA 25 [Thermal shutdown]	[Hall power supply]	•						
Thermal shutdown Operating temperature	Hall power supply voltage	VH	IH = 5 mA		0.8		V	24
Operating temperature TTSD 150 180 210 °C Target Hysteresis ΔTTSD 15 °C Target [Short braking] Brake pin at High level VBRH 4 5 V 26	Allowable current	IH		20			mA	25
Hysteresis ΔTTSD 15 °C Target [Short braking] Brake pin at High level VBRH 4 5 V 26	[Thermal shutdown]	[Thermal shutdown]						
[Short braking] Brake pin at High level	Operating temperature	TTSD		150	180	210	℃	Target
Brake pin at High level VBRH 4 5 V 26	Hysteresis	ΔTTSD			15		°C	Target
VEINT 1	[Short braking]	•		•				•
	Brake pin at High level	VBRH		4		5	V	26
	Brake pin at Low level	VBRL					V	26

Note:

- During S/S OFF (standby), the Hall comparator is at High.
- Items shown to be "Target" are not measured.

Truth Table

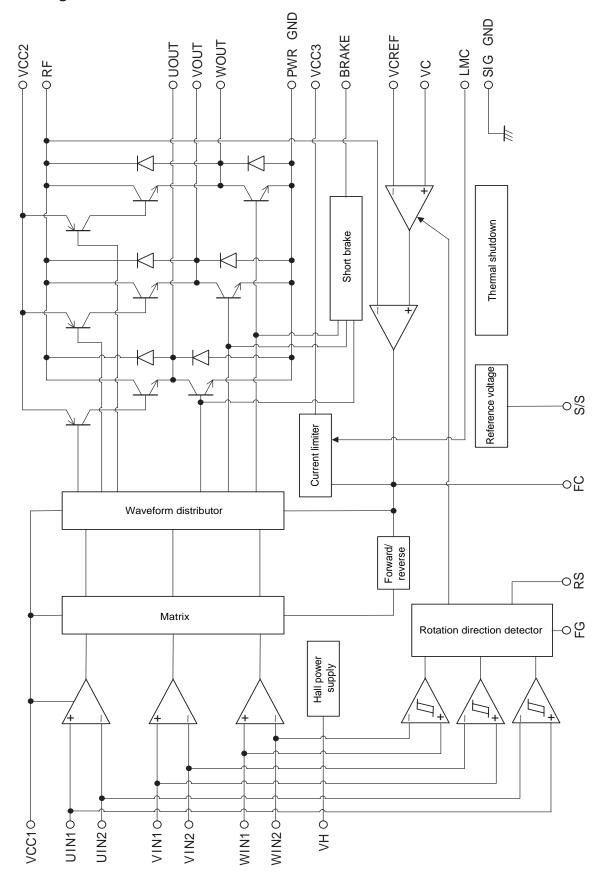
	Source		Input	Control		
	Sink	U	V	W	VC	
1	Phase W -> Phase V	Н	Н	-	Н	
ı.	Phase V -> Phase W	''	'''	_	L	
2	Phase W -> Phase U	Н	L	L	Н	
2	Phase U -> Phase W	''	L	L	L	
3	Phase V -> Phase W	L		L	Н	Н
3	Phase W -> Phase V			''	L	
4	Phase U -> Phase V	_	Н	1	Н	
4	Phase V -> Phase U	_	''	L	L	
5	Phase V -> Phase U	Н	L	Н	Н	
3	Phase U -> Phase V	''	L.	П	L	
6	Phase U -> Phase W		Н	Н	Н	
	Phase W -> Phase U	1 -	11	11	L	

Input:

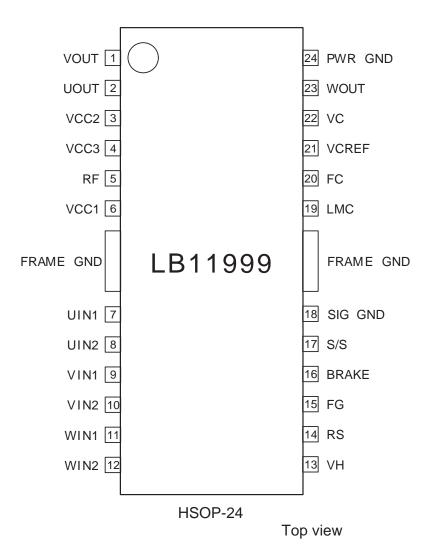
H: Input 1 is higher in potential than input 2 by at least 0.2V.

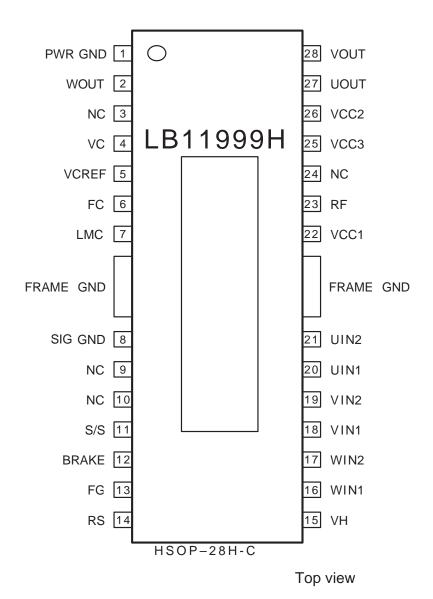
L: Input 1 is lower in potential than input 2 by at least 0.2V.

Block Diagram

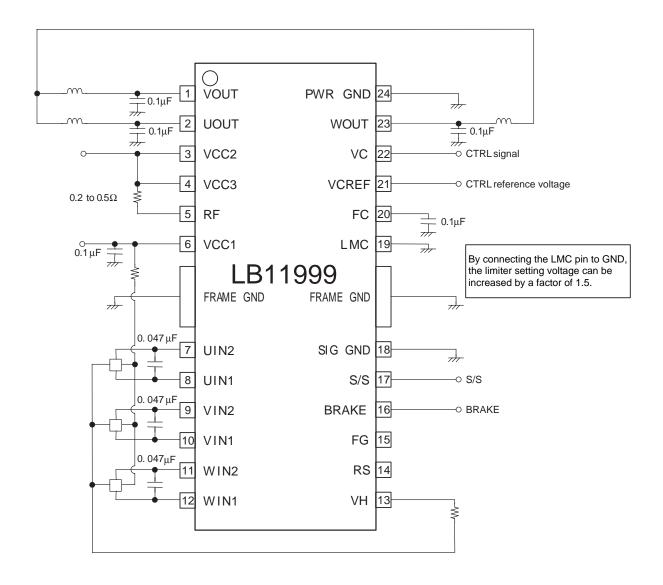


Pin Assignment

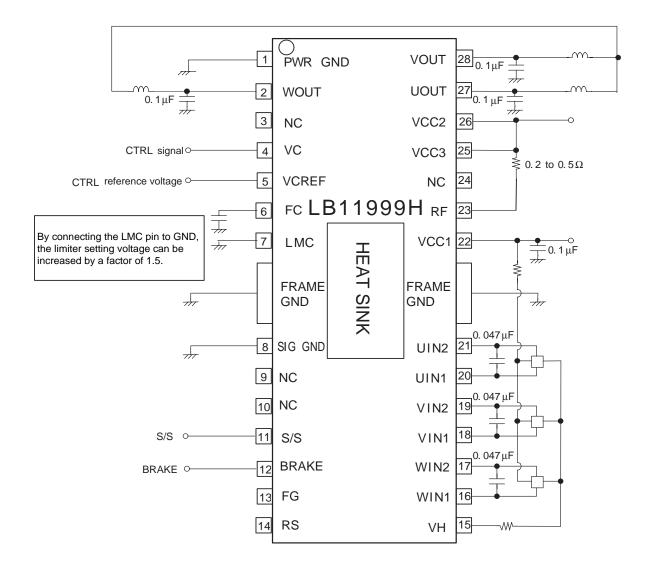




Sample Application Circuit (LB11999)



Sample Application Circuit (LB11999H)



Pin	Descr	intion	*(): LB11999H
	D C301	IDUOII	(). LD 1100011

	p	` '		• • •
Pin number	Pin name	Pin voltage	Equivalent circuit	Pin function
3 (26)	VCC2	4V to 13.6V		Source side predrive voltage supply pin.
4 (25)	VCC3	4V to 13.6V		Constant current control amplifier voltage supply pin.
6 (22)	VCC1	4V to 6V		Power supply pin for all voltage except output transistors, source predrive, and low current control amplifier.
14 (14)	RS		100μ VCC1 1100μ Δ 114 (15)	Reverse detector pin Forward rotation: High Reverse rotation: Low
15 (13)	FG		(13)	1 Hall element waveform Schmitt comparator composite output
8 (20)	UIN1			U phase Hall element input and reverse detector U phase Schmitt
7 (21)	UIN2		8 7 7	comparator input pin. Logic High indicates UIN1 > UIN2.
10 (18)	VIN1	1.2V to VCC1–1V	10 200 (1)	V phase Hall element input and reverse detector V phase Schmitt
9 (19)	VIN2	VOCITIV	20 25µA D 25µA 21	comparator input pin. Logic High indicates VIN1 > VIN2.
12 (16)	WIN1		18	W phase Hall element input and reverse detector W phase Schmitt
11 (17)	WIN2		16 17	comparator input pin. Logic High indicates WIN1 > WIN2.
13 (15)	VH		VCC1 75μA (13) (15)	Hall element lower side bias voltag supply pin.
17 (11)	S/S	0V to VCC1	VCC1 75k 50k 177 177 177 177 177 177 177 1	When this pin is at 0.7V or lower, o when it is open, all circuits are inactive. When driving motor, set this pin to 2V or higher.

Continued on next page

Unit (Resistance: Ω , capacitance: F)

Continued from preceding page

Unit (Resistance: Ω , capacitance: F)

Pin number	Pin name	Pin voltage	Equivalent circuit	Pin function
18 (8)	SIG GND			GND pin for all circuits except output.
20 (6)	FC		VCC1 20 (6) 20k 5k 77	Control loop frequency compensator pin. Connecting a capacitor between this pin and GND prevents closed loop oscillation in current limiting circuitry.
21 (5)	VCREF	1.3V to 2V	15µ V 25µ V 25µ V 15µ	Control reference voltage applied pin. Determines control start voltage.
22 (4)	VC	0V to VCC1	200 (22)-w-(21) (4) (5)	Speed control voltage applied pin. V type control technique VC > VCREF: Forward VC < VCREF: Slowdown (Reverse-blocking circuit prevents reverse rotation.)
23 (2)	WOUT		—— VCC2	W-phase output.
24 (1)	PWR GND		5 (23)	Output transistor GND.
1 (28)	VOUT		3.9	V-phase output.
2 (27)	UOUT		23(1)(2)	U-phase output.
5 (23)	RF		3.9 (2, 28, 27) (24) (1)	Upper side output NPN transistor collector pin (common for all 3 phases). For current detection, connect resistor between VCC3 pin and RF pin. Constant current control and current limiter works by detecting this voltage.
19 (7)	LMC		VCC1 RF RF (7)	
16 (12)	BRAKE		75k	Short brake pin. BRAKE: High -> Brake Low/Open -> Drive

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