Ordering number: EN 5132

Monolithic Digital IC

No. 5132

LB1952/LB1952M

3-phase Brushless Motor Driver for VTR Capstans

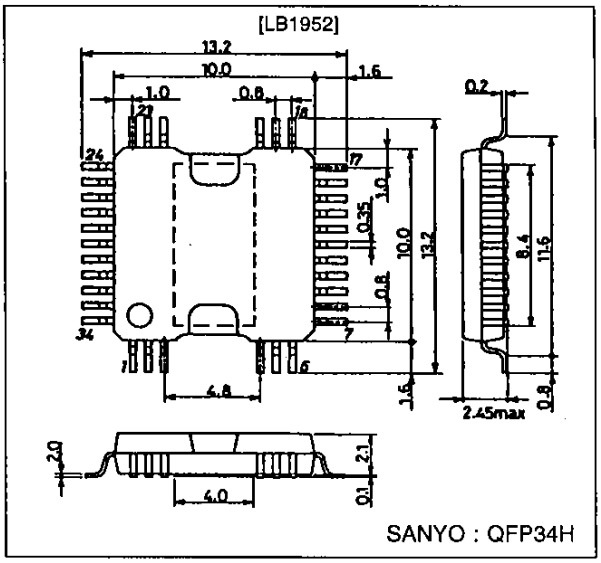
Functions

- 3-phase full-wave current linear drive system
- Torque ripple correction circuit built in (variable correction factor)
- Current limiting circuit built in
- Output stage upper/lower oversaturation prevention circuit built in (no external capacitor required)
- FG amplifier built in
- Thermal shutdown circuit built in

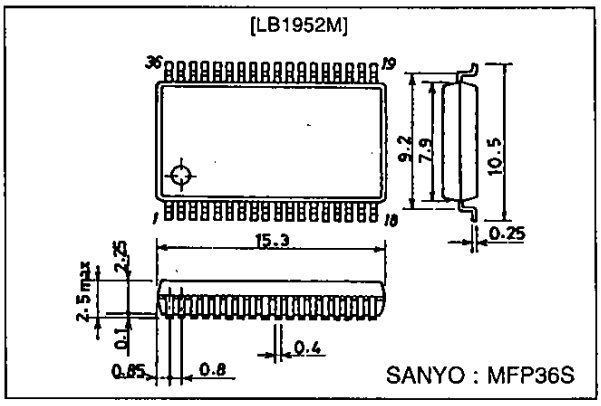
Package Dimensions

unit : mm

3206-QFP34H



3129-MFP36S



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Specifications

Absolute Maximum Ratings at Ta = 25 °C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		7	V
	V_S max		24	V
Maximum output current	I_O max		1.3	A
Allowable power dissipation	Pd max	Arbitrarily large heat sink LB1952	12.5	W
		Independent IC LB1952	0.77	W
		Independent IC LB1952M	0.95	W
Operating temperature	Topr		−20 to +75	°C
Storage temperature	Tstg		−55 to +150	°C

Allowable Operating Ranges at Ta = 25 °C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_S		5 to 22	V
	V_{CC}		4.5 to 5.5	V
Hall input amplitude	V_{HALL}	Between Hall inputs	±30 to ±80	mV_{0-P}
GSENSE input range	V_{GSENSE}	Relative to control system GND	−0.20 to +0.20	V

Electrical Characteristics at Ta = 25 °C, V_{CC} = 5 V, V_S = 15 V

Parameter	Symbol	Conditions	min	typ	max	Unit
V_{CC} supply current	I_{CC}	R_L = ∞ (when stopped), V_{CTL} = 0 V, V_{LIM} = 0 V		12	18	mA
[Output]						
Output saturation voltage	$V_{Osat}1$	I_O = 500 mA, Rf = 0.5 Ω, Sink + Source V_{CTL} = V_{LIM} = 5 V (with saturation prevention)		2.1	2.6	V
	$V_{Osat}2$	I_O = 1.0 A, Rf = 0.5 Ω, Sink + Source V_{CTL} = V_{LIM} = 5 V (with saturation prevention)		2.6	3.5	V
Output leakage current	Ioleak				1.0	mA
[FR]						
FR pin input threshold voltage	V_{FSR}		2.25	2.50	2.75	V
FR pin input bias current	Ib (FSR)		−5.0			µA
[Control]						
CTLREF pin voltage	V_{CREF}		2.05	2.15	2.25	V
CTLREF pin input range	V_{CREF}IN		1.50		3.50	V
CTL pin input bias current	Ib (CTL)	With V_{CTL} = 5 V, CTLREF : Open			4.0	µA
CTL pin control start voltage	V_{CTL} (ST)	With Rf = 0.5 Ω, V_{LIM} = 5 V, I_O ≧ 10 mA, Hall input logic fixed, (u, v, w = H, H, L)	2.00	2.15	2.30	V
CTL pin control Gm	Gm (CTL)	With Rf = 0.5 Ω, ΔI_O = 200 mA, Hall input logic fixed, (u, v, w = H, H, L)	0.46	0.58	0.70	A/V
[Current Limit]						
LIM current limit offset voltage	Voff (LIM)	With Rf = 0.5 Ω, V_{CTL} = 5 V, I_O ≧ 10 mA, Hall input logic fixed, (u, v, w = H, H, L)	140	200	260	mV
LIM pin input bias current	Ib (LIM)	With V_{CTL} = 5 V, CTLREF : Open, V_{LIM} = 0 V	−2.5			µA
LIM pin current limit level	I lim	With Rf = 0.5 Ω, V_{CTL} = 5 V, V_{LIM} = 2.06 V, Hall input logic fixed, (u, v, w = H, H, L)	830	900	970	mA
[Hall Amplifier]						
Hall amplifier input offset voltage	Voff (HALL)		−6		+6	mV
Hall amplifier input bias current	Ib (HALL)			1.0	3.0	µA
Hall amplifier common-mode input voltage	Vcm (HALL)		1.3		3.3	V
[TRC]						
Torque ripple correction factor	T_{RC}	At bottom and peak in Rf waveform at I_O = 200 mA (RF=0.5 Ω, ADJ-OPEN) Note 2		9		%
ADJ pin voltage	Vadj		2.37	2.50	2.63	V

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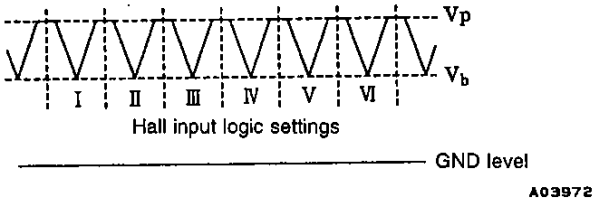
Parameter	Symbol	Conditions	min	typ	max	Unit
[FG Amplifier]						
FG amplifier input offset voltage	Voff (FG)		–8		+8	mV
FG amplifier input bias current	Ib (FG)		–100			nA
FG amplifier output saturation voltage	V_{Osat} (FG)	At internal pull-up resistor load on sink side			0.5	V
FG amplifier common-mode input voltage	V_{CM} (FG)		0.5		4.0	V
[Saturation]						
Saturation prevention circuit lower set voltage	V_{Osat} (DET)	Voltage between each Out and Rf at I_O = 10 mA, Rf = 0.5 Ω, V_{CTL} = V_{LIM} = 5 V	0.175	0.25	0.325	V
[TSD]						
TSD operation temperature	T-TSD	(Design target) Note 1		180		°C
TSD temperature hysteresis width	ΔTSD	(Design target) Note 1		20		°C

Note 1: No measurements are performed for any values listed in the condition column as design targets.
Note 2: The torque ripple correction factor is calculated using the Rf voltage waveform as follows.



$$\text{Correction factor} = \frac{2 \times (Vp - Vb)}{Vp + Vb} \times 100\ (\%)$$

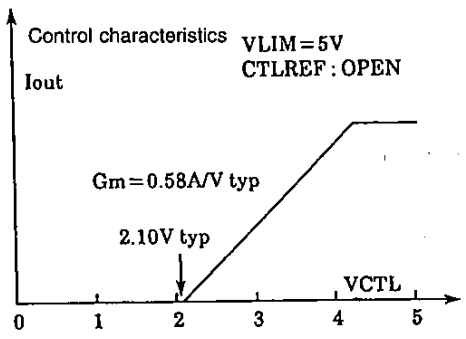
Truth Table & Control Function

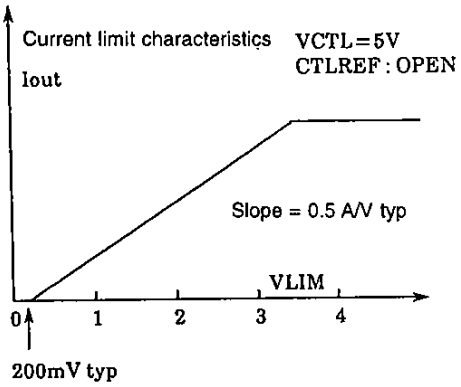
	Source → Sink	Hall input U	Hall input V	Hall input W	FR
1	V → W	H	H	L	H
	W → V				L
2	U → W	H	L	L	H
	W → U				L
3	U → V	H	L	H	H
	V → U				L
4	W → V	L	L	H	H
	V → W				L
5	W → U	L	H	H	H
	U → W				L
6	V → U	L	H	L	H
	U → V				L

Note: "H" in the FR column represents a voltage of 2.75V or more; "L" represents a voltage of 2.25V or less. (At V_{CC} = 5 V)
Note: "H" in the hall input columns represents a state in which "+" has a potential which is higher by 0.01 V or more than that of the "–" phase inputs. Conversely, "L" represents a state in which "+" has a potential which is lower by 0.01V or more than that of the "–" phase input.

Note: Since 180° conduction is used as the drive system, other phases than the sink and source phases are turned off.

Control Function & Current Limit Function





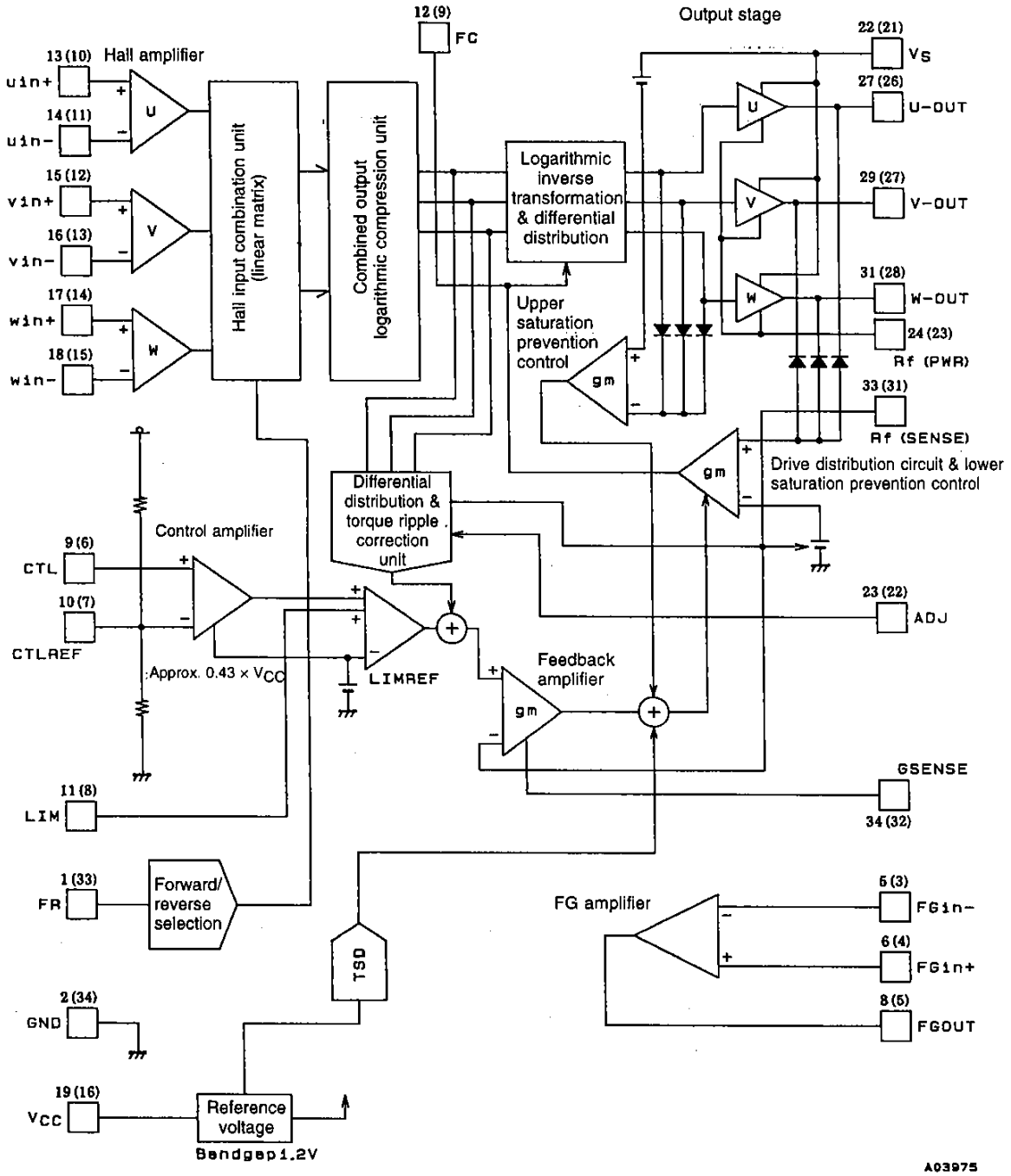
Pin Functions

The pin numbers in ( ) are for MFP.

Pin name	Pin No.	Function
FR	1 (33)	Forward/reverse select pin. The pin voltage selects forward/reverse. (Vth = 2.5 V typ at V_{CC} = 5 V)
GND	2 (34)	GND for other than output transistor. Minimum potential of output transistor is at Rf pin.
FGin (–)	5 (3)	Input pin when FG amplifier is used with inverted input. Feedback resistor is connected between this pin and FG-OUT.
FGin (+)	6 (4)	Noninverting input pin when FG amplifier is used with differential input. Internal bias is not applied.
FG-OUT	8 (5)	FG amplifier output pin. Resistive load provided internally.
CTL	9 (6)	Speed control pin. Control is exercised by constant-current drive with current feedback applied from Rf. Gm = 0.58 A/V typ at Rf=0.5 Ω
CTLREF	10 (7)	Control reference voltage pin. The voltage is set internally to approx. 0.43 x V_{CC} but this can be varied by applying voltage through a low impedance (input impedance = approx. 4.3 kΩ).
LIM	11 (8)	Current limiting function control pin. The output current is varied linearly by this pin voltage; slope = 0.5 A/V typ at Rf = 0.5 Ω.
FC	12 (9)	Speed control loop frequency characteristic correction pin
Uin^+, Uin^- Vin^+, Vin^- Win^+, Win^-	13, 14 (10, 11) 15, 16 (12, 13) 17, 18 (14, 15)	U-phase Hall device input pin; logic "H" represent IN+ > IN–. V-phase Hall device input pin; logic "H" represent IN+ > IN–. W-phase Hall device input pin; logic "H" represent IN+ > IN–.
V_{CC}	19 (16)	Power supply pin for supplying power to all circuits except output section in IC; this voltage must be stabilized so as to eliminate ripple and noise.
V_S	22 (21)	Output section power supply pin
ADJ	23 (22)	Pin for external adjustment of torque ripple correction factor. When this factor is to be adjusted, a voltage is externally applied to the ADJ pin through a low impedance. If the voltage applied is increased, the factor drops; conversely, if it is reduced, the factor rises. The factor varies between 0 and 2 times that of the open state. (The voltage is set to approx. $V_{CC}/2$ internally, and the input impedance is approx. 5 kΩ.)
Rf (PWR) Rf (SNS)	24 (23) 33 (31)	Output current detection pin. Current feedback is applied to the control section by connecting Rf between this pin and GND. The lower oversaturation prevention circuit and torque ripple correction circuit are activated in accordance with this pin voltage. Since the oversaturation prevention level is set with this voltage, the lower oversaturation prevention effect may deteriorate in the high current range if the Rf value is reduced to an extremely low level. The PWR and SENSE pins must always be connected.
Uout Vout Wout	27 (26) 29 (27) 31 (28)	U-phase output pin V-phase output pin (Built-in spark killer diode) W-phase output pin
GSENSE	34 (32)	GND sensing pin. By connecting this pin to the neighboring GND on the Rf resistor side of the motor GND wire which contains Rf, the effect that GND common impedance exerts on Rf can be eliminated. (This pin must not be left open.)

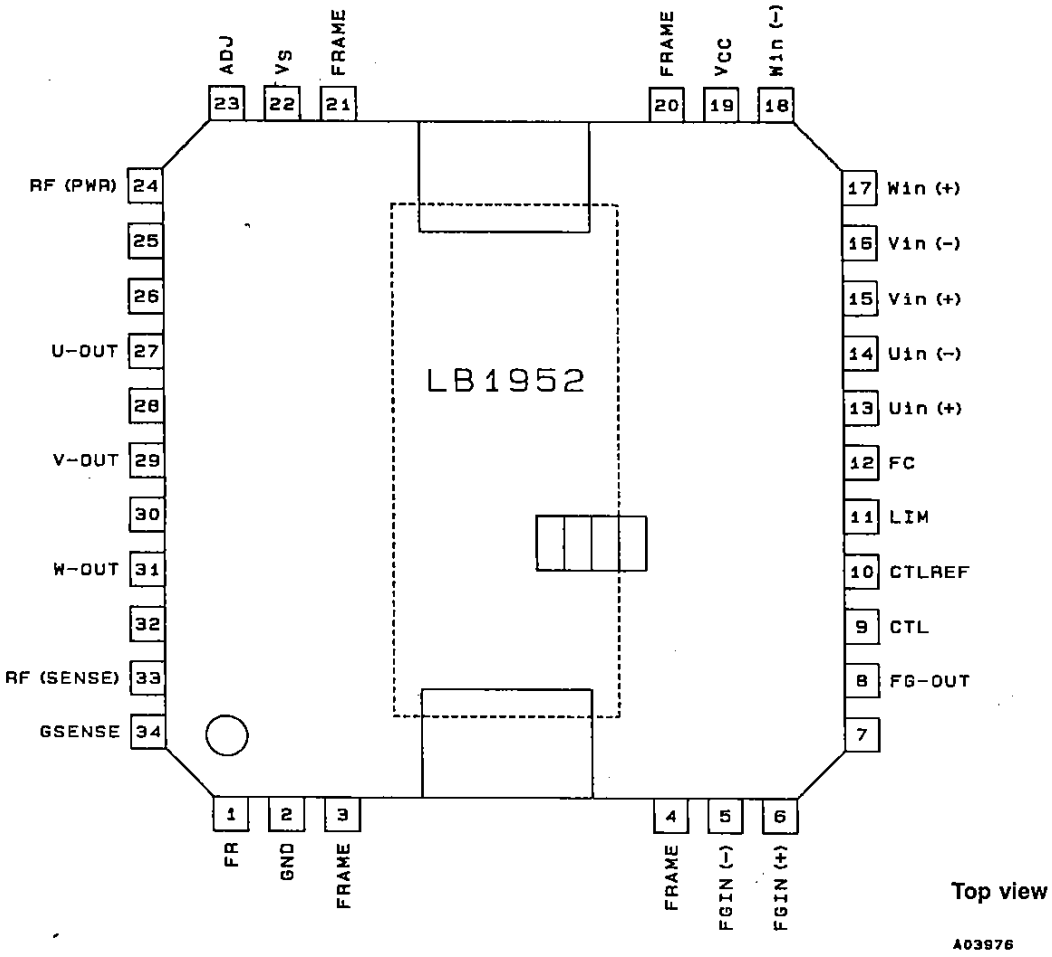
Block Diagram

Pin number inside ( ): for MFP

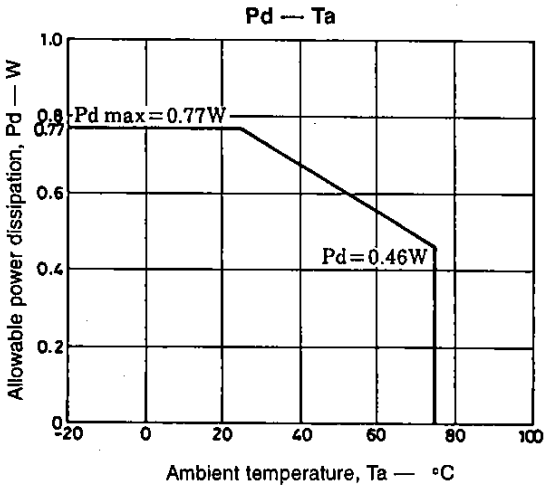


Pin Assignment [LB1952]

(PACKAGE: QFP-34H-A)

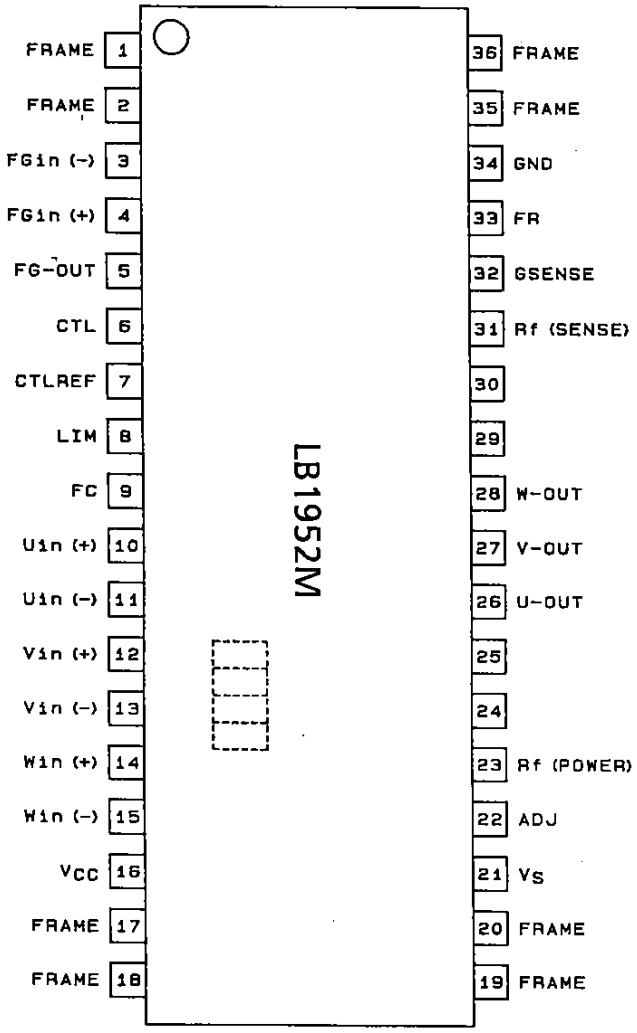


Note: FRAME must be connected to GND for GND potential stabilization.



Pin Assignment [LB1952M]

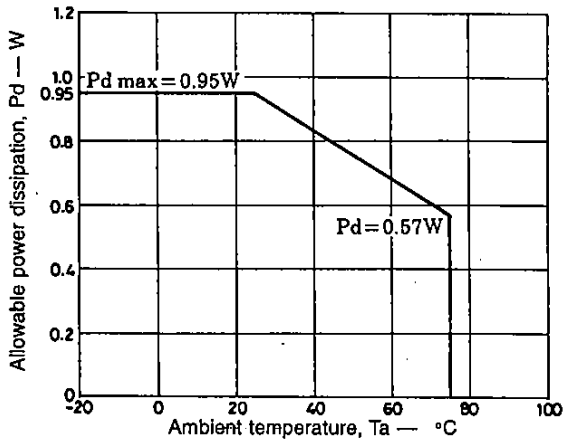
(PACKAGE: MFP-36S-LF)



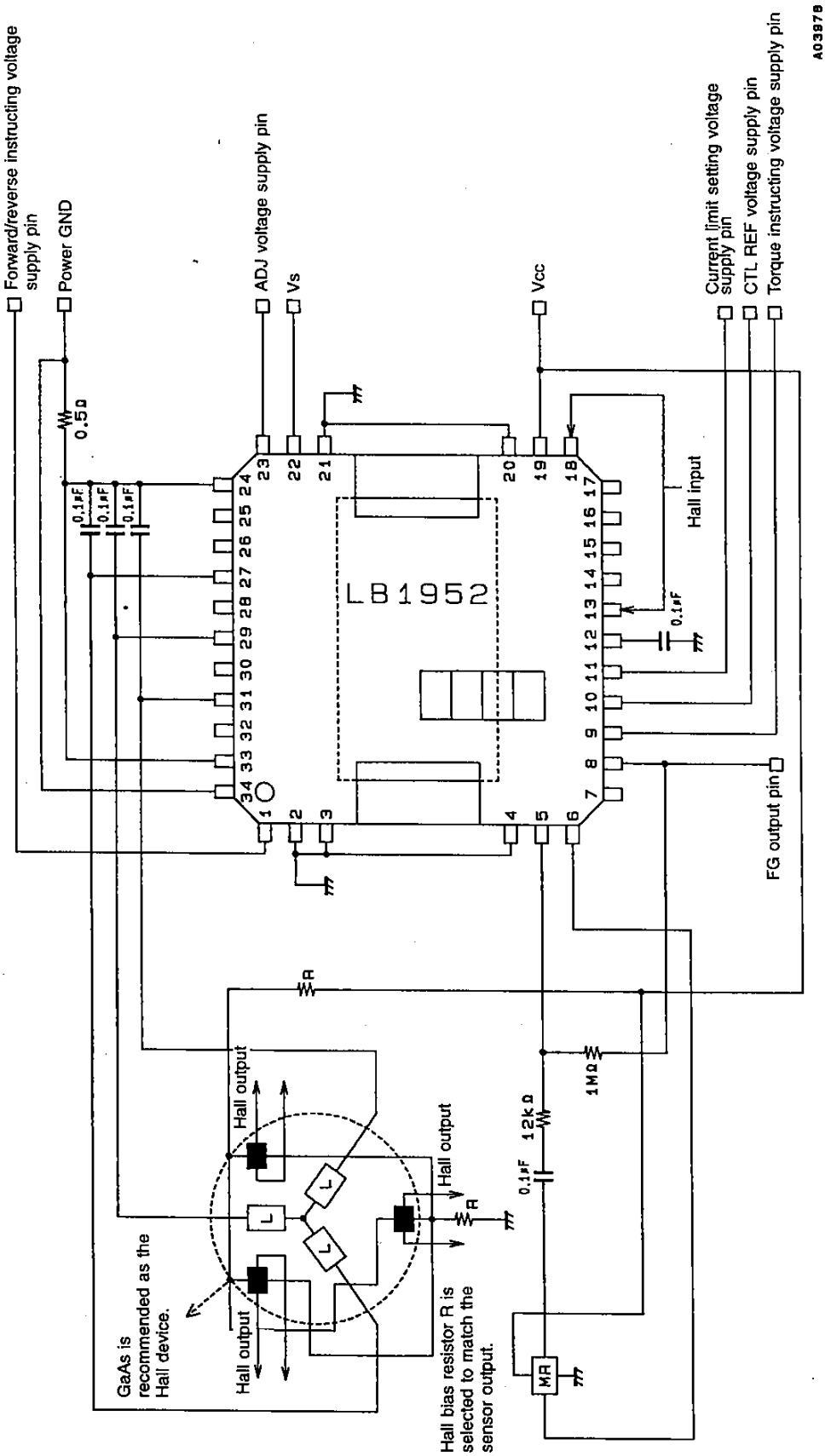
A03977 **Top view**

Note: Although there is no internal connections between the FRAME pin and GND, FRAME must be connected to GND externally for GND potential stabilization.

Pd — Ta

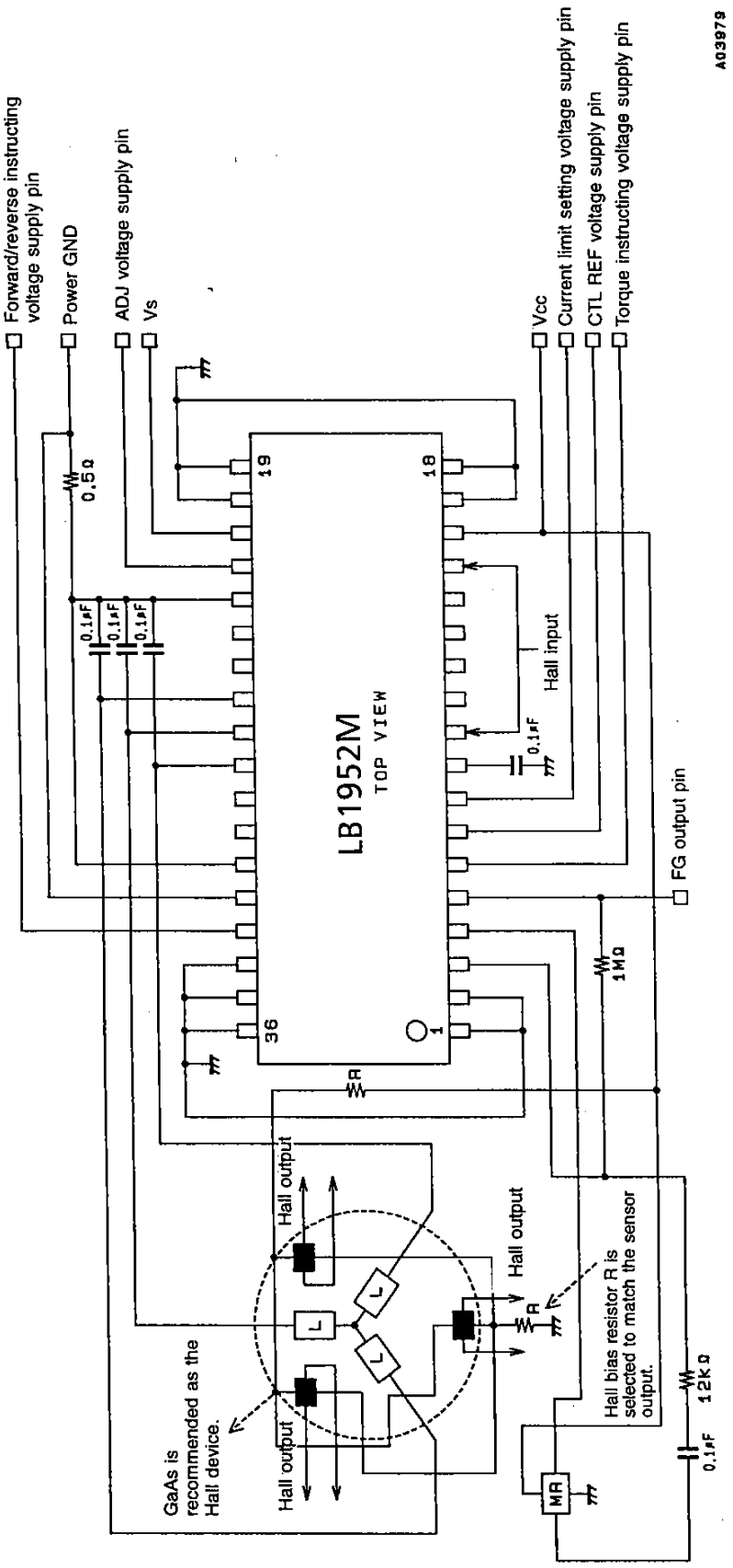


Sample Application Circuit [LB1952]



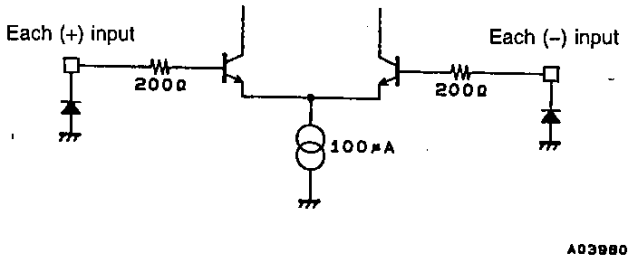
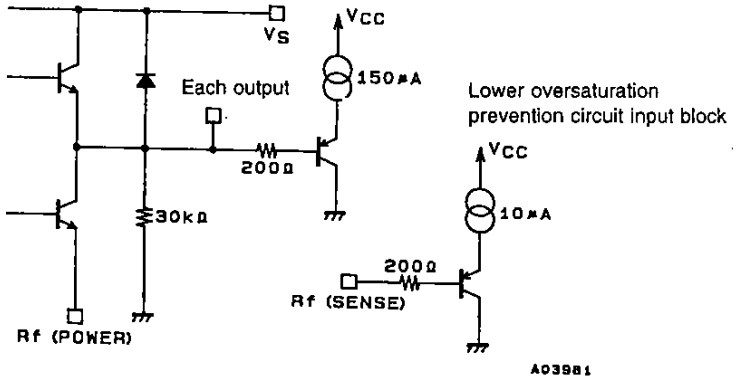
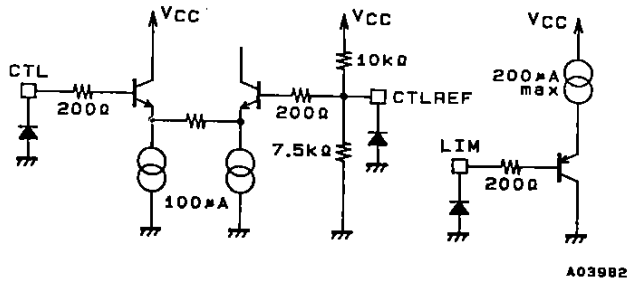
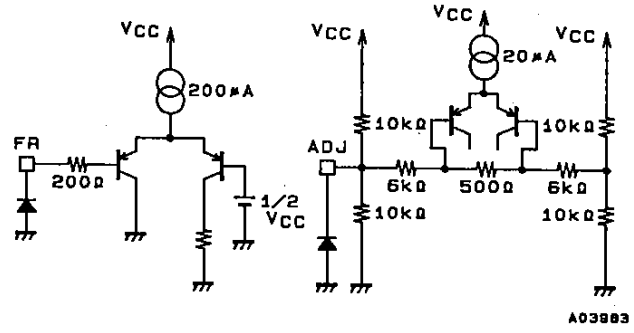
Note: The constants provided in this sample application circuit are provided by way of example and are not intended to guarantee the characteristics.

Sample Application Circuit [LB1952M]



Note: The constants provided in this sample application circuit are provided by way of example and are not intended to guarantee the characteristics.

Pin Input/Output Equivalent Circuit

Pin name	Input/Output Equivalent Circuit
Uin (+) Uin (–) Vin (+) Vin (–) Win (+) Win (–)	
U-OUT V-OUT W-OUT V_S Rf (POWER) Rf (SENSE)	
CTL LIM CTLREF	
FR ADJ	

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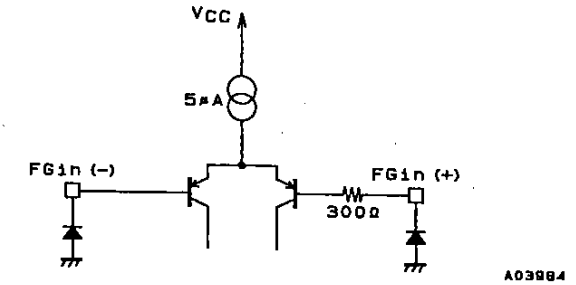
Pin name	Input/Output Equivalent Circuit
FGin (–) FGin (+)	
FGOUT FC