STR-A6300 Series

Application Notes(Ver. 1.2)

May 15th, 2002

System Engineering Dept.
Semiconductor Operations
Sanken Electric Co., Ltd.

CONTENTS

***Specifications and information herein are subject to change without notice.**

1 INTRODUCTION

STR-A6300 series is a hybrid IC with a built-in power MOSFET and a controller IC, designed for fly-back converter type SMPS(Switching Mode Power Supply) applications, packaged into DIP8, applicable for PRC operation only for small power SMPS.

This IC realizes downsizing and standardizing of a power supply system that reduces external components count and simplifies circuit designs.

(Note) PRC is abbreviation of “Pulse Ratio Control”(On-width control with fixed OFF-time).

2 FEATURES

- Small sized 8-pin DIP type full molded package, optimum IC for low-height SMPS
- Oscillator is incorporated in the monolithic control IC with adopting On-Chip-Trimming technology.
- Small temperature characteristics variation by adopting a comparator compensated for temperature in the control part
- Low start-up circuit current(50uA max)
- Built-in Active Low-Pass Filter for stabilizing the operation at light load
- Avalanche energy guaranteed MOSFET with high VDSS
  - The built-in power MOSFET simplifies the surge absorption circuit since the MOSFET guarantees the avalanche energy.
  - No VDSS de-rating is required.
- Built-in constant voltage drive circuit
- Various kinds of protection functions
  - Pulse-by-pulse Overcurrent Protection(OCP)
  - Overvoltage Protection with latch mode (OVP)
  - Thermal Shutdown with latch mode (TSD)

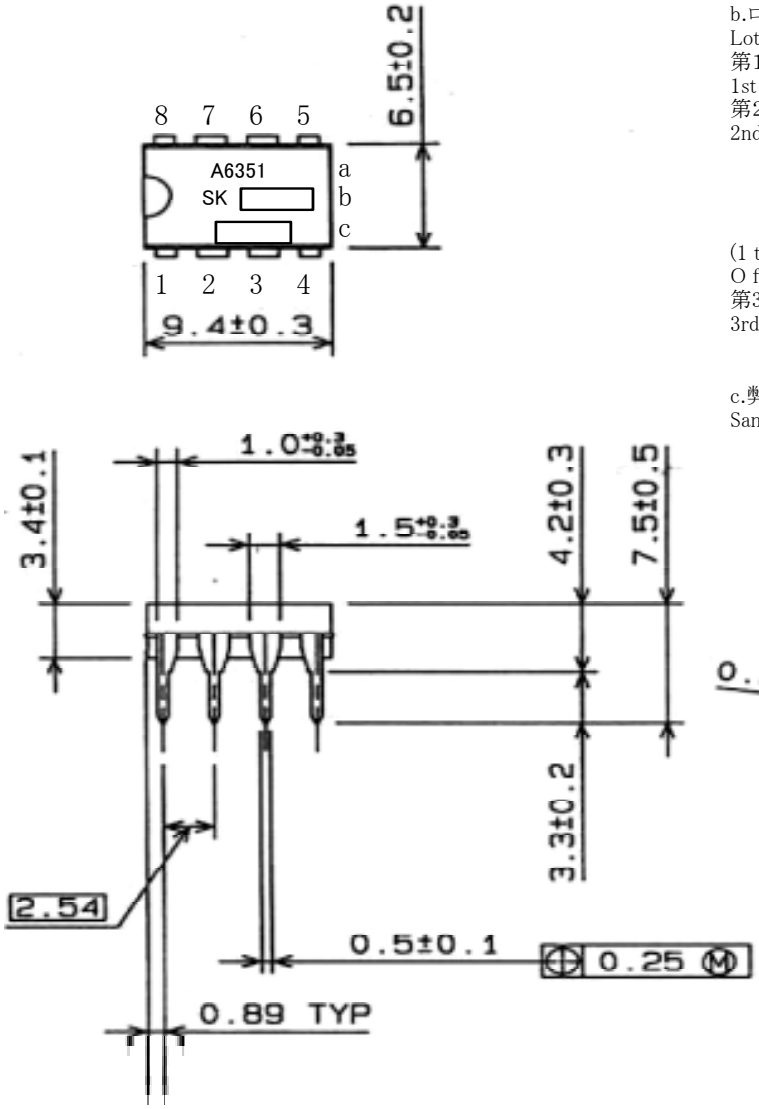
3 LINE-UP OF STR-A6300 SERIES

Type Number	MOSFET V_{DSS}[V]	$r_{DS(ON)}$ MAX.	V_{IN}[V]	Pout [W] Note 1	Production status
STR-A6351	650	3.95 ohm	220	10	In MP
			WIDE	8	
STR-A6331	500	3.95 ohm	100/120	10	In MP
			WIDE	-	
STR-A6359	650	6.0 ohm	100/120	5	In MP
			WIDE	5	

Note 1. The Pout(W) represents the thermal ratings at PRC operation, and the peak power output is obtainable by approx. 120%~140% of the above listed. When the output voltage is low and ON-duty is narrow, the Pout(W) shall become lower than that of above.

4 OUTLINE DRAWINGS&PIN ARRANGEMENT

Note: Below are reference drawings. For details, please see each data sheet.



a.品名標示
Type Number
b.ロット番号
Lot Number
第1文字 西暦年号下一桁
1st letter The last digit of year
第2文字 月
2nd letter Month
1～9月 :アラビア数字
10月 :O
11月 :N
12月 :D
(1 to 9 for Jan. to Sept.,
O for Oct. N for Nov. D for Dec.)
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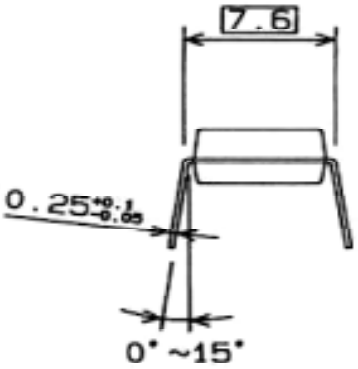
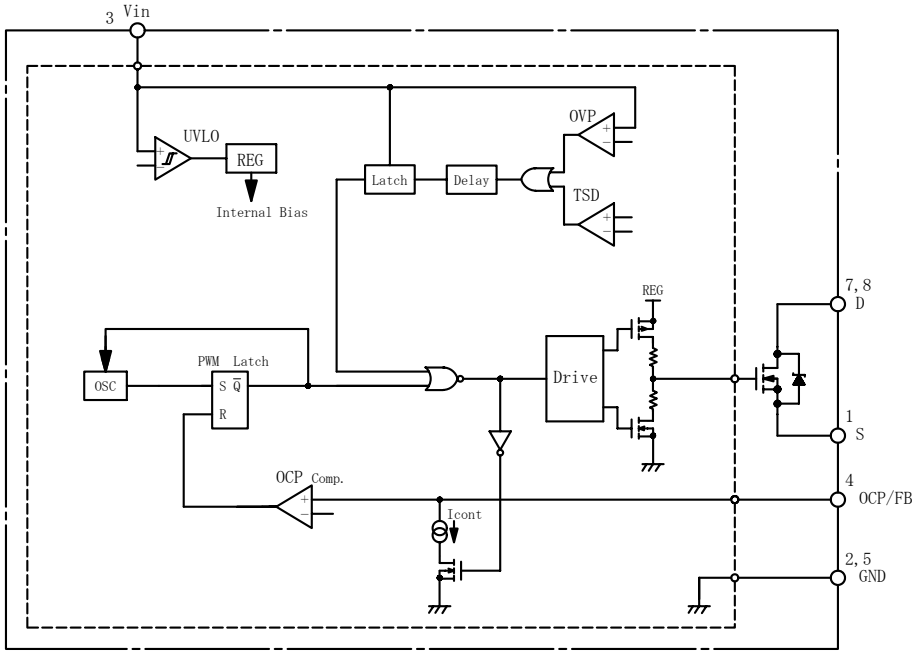
3rd letter Week
1～3 アラビア数字
Arabic numerals
c.弊社管理番号
Sanken Registration Number



端子材質:Cu
Material of terminal: Cu
端子の処理:半田メッキ
Treatment of terminal:solder plating
製品重量:約0.51g
Weight: Approx. 0.51g

5 STR-A6300 BLOCK DIAGRAM



PIN FUNCTIONS

Pin #	Symbol	Description	Functions
1	S	Source terminal	MOSFET Source
2	GND	Ground terminal	Ground
3	Vin	Input voltage terminal	Power supply for Control circuit
4	OCP/FB	Overcurrent/Feedback	Overcurrent detection/Constant Voltage Control Signals input
5	GND	Ground terminal	Ground
6	N.C.	-	Non-connection
7	D	Drain terminal	MOSFET Drain
8	D	Drain terminal	MOSFET Drain

Other functions

Symbol	Functions
O. V. P.	Built-in Overvoltage Protection circuit
T. S. D.	Built-in Themal Protection circuit

6 ELECTRICAL CHARACTERISTICS: STR-A6351(Example)

6.1 Absolute Maximum Ratings(Ta=25 °C)

Parameter	Pin	Symbol	Ratings	Units	Remarks
Drain Current	8-1	Idpeak*	2.36	A	Single pulse
Maximum Switching Current	8-1	IDMAX*	2.36	A	ΔV1-2=0.82V Ta=-20~+125 °C
Avalanche Energy Capacity	8-1	EAS*	56	mJ	Single pulse ILpeak=2.36A
Voltage supply to Control Part	3-2	VIN	35	V	
OCP/FB Terminal Voltage	4-2	Vth	6	V	
Power Dissipation at MOSFET	8-1	PD1*	1.35	W	*
Power Dissipation at Control part(MIC)	3-2	PD2*	0.14	W	Specified by VIN x IIN
Internal Frame Temp. in operation	-	TF	-20~+125	°C	Measured at the end of pin 5
Operating ambient temp.	-	Top	-20~+125	°C	
Storage temp.	-	Tstg	-40~+125	°C	
Channel temp.	-	Tch	+150	°C	

*Refer to each data sheet since the values vary in each device.

6.2 ELECTRICAL CHARACTERISTICS OF CONTROL UNIT

VIN＝20V(Ta＝25 °C), unless otherwise specified

Parameter	Pin	Symbol	Ratings			Unit	Conditions
			MIN	TYP	MAX		
Operation Start Voltage	3-2	VIN(ON)	15.8	17.6	19.4	V	See each data sheet
Operation Stop Voltage	3-2	VIN(OFF)	9.1	10.1	11.1	V	
Circuit Current at operation	3-2	IIN(ON)	-	-	5	mA	
Circuit Current at non-operation	3-2	IIN(OFF)	-	-	50	uA	
Maximum OFF time	-	TOFF(MAX)	12	15	18	usec	
OCP/FB/Tri terminal threshold voltage1	4-2	Vth(1)	0.70	0.76	0.82	V	
OCP/FB terminal discharging voltage	4-2	IOCP/FB	0.7	0.8	0.9	mA	
OVP operating voltage	3-2	VIN(OVP)	23.2	25.5	27.8	V	See each data sheet
Latch circuit holding current	3-2	IIN(H)	-	-	70	uA	
Latch circuit releasing current	3-2	VIN(La.OFF)	7.9	-	10.5	V	
Thermal shutdown operating temp.	-	Tj(TSD)	135	-	-	°C	

6.3 ELECTRICAL CHARACTERISTICS OF MOSFET(STR-A6351)

Parameter	Pin	Symbol	Ratings			Unit	Conditions
			MIN	TYP	MAX		
Drain to source breakdown voltage	8-1	V_{DSS}	650*	-	-	V	See each data sheet.
Drain leakage current	8-1	I_{DSS}	-	-	300	uA	
ON-Resistance	8-1	$rDS_{(ON)}$	-	-	3.95*	Ohm	
Switching time	8-1	tf	-	-	250	nsec	
Thermal resistance	-	Θ_{ch-F}	-	-	52*	°C /W	Channel to internal frame

*Please refer to each data sheet for details.

7 FUNCTIONS OF EACH TERMINAL AND OPERATION

7.1 Vin Terminal(Pin 3)/Start-up Circuit

The start-up circuit detects the voltage at the VIN terminal (Pin 3), and the circuit starts and stops the operation of the control IC. The power supply circuit (VIN terminal input) of the control IC employs a circuit as shown on Fig.1.

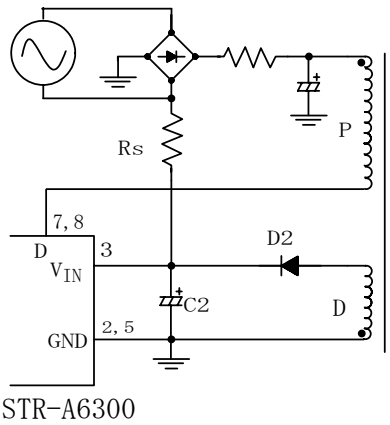


Fig.1. Start-up Circuit

At start-up of the power supply, C2 is charged through the start-up resistor Rs. The Rs value, due to the slight increase of the latch circuit holding current (70uA MAX) at low temperature, should be determined in order for **100uA** or higher current to flow at the minimum AC input voltage.

However, where the Rs value is too high, the current charging C2 after AC input shall be reduced, as a result, longer time is required to reach the operation start voltage. Consequently, Rs value as well as C2 value that will be mentioned later should be monitored.

Vin terminal voltage falls immediately after the control circuit starts its operation, but the drop ratio of the voltage shall reduce by increasing the C2 capacitance. Consequently, even though the start-up of the drive winding voltage is delayed, the Vin terminal voltage would not reach the operation stop voltage to maintain the start-up operation.

However, the time of AC input to operation start becomes longer since it takes much time to charge the C2, if the C2 capacitance is too large. In general, a power supply shall operate at the value of C2(=4.7~10uF approx.) and of Rs (=470kohm~1Mohm) for a wide input start-up.

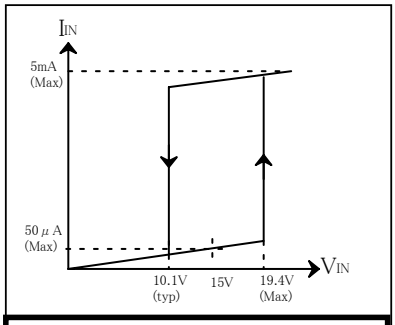


Fig.2. Vin-IIN(Circuit current)

As shown on Fig.2, circuit current is kept below **50uA max**. (Vin=15.0V, Ta=25℃) until the control circuit starts its operation, and a higher value of Rs is applicable to the circuit.

The control circuit starts its operation by **start-up circuit** as soon as the Vin terminal voltage reaches **17.6V(TYP.),** and the current

consumption shall be increased.

When the Vin terminal voltage drops lower than 10.1V(TYP.), the control operation stops by a Under Voltage Lock Out(UVLO) function and returns to the start-up mode. After the control circuit starts its operation, a power supply is earned by rectifying and smoothing the voltage of drive winding D.

Fig.3 shows the start-up voltage waveform at the Vin terminal. The drive winding voltage does not rise up to a set voltage immediately after the control circuit starts falling, thanks to the operation stop voltage set as low as 11.1V(MAX), the drive winding voltage reaching stabilized voltage before falling to the operation stop voltage, the control circuit continuing its operation.

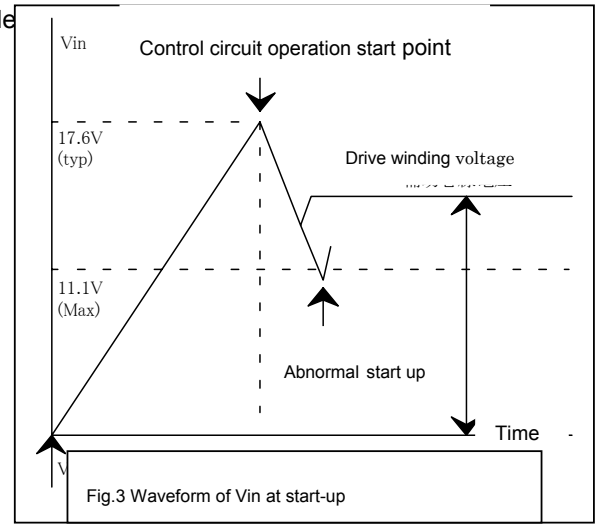


Fig.3 Waveform of Vin at start-up

The number of windings is to be set at a normal power supply operation so that both of the end volts of C2 may be higher than the operation stop voltage [Vin(OFF) 11.1V(MAX)] and lower than the OVP operating voltage[Vin(OVP) 23.2V(MIN)].

The preferable drive winding D voltage for stabilization is 18V approx.. However, in an actual power supply circuit there is a case that the Vin terminal voltage varies due to the secondary output current as shown on Fig.4.

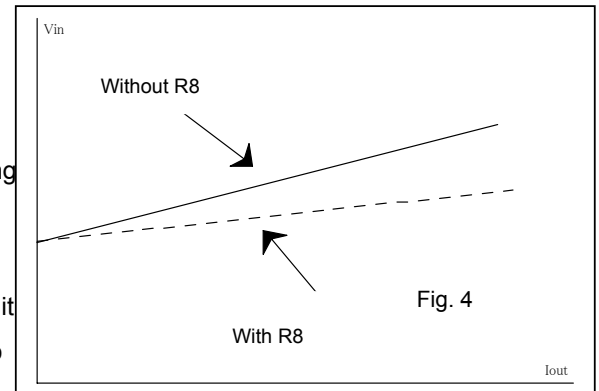


Fig. 4

This is because the circuit current of STR-A6300 series is small, the C2 being charged up to the peak value by the surge voltage generated instantly after the MOSFET is turned OFF. In order to prevent this, it is effective to add a resistor having several to several tens of ohms(R8) in series with the rectifier diode as shown on Fig.5.

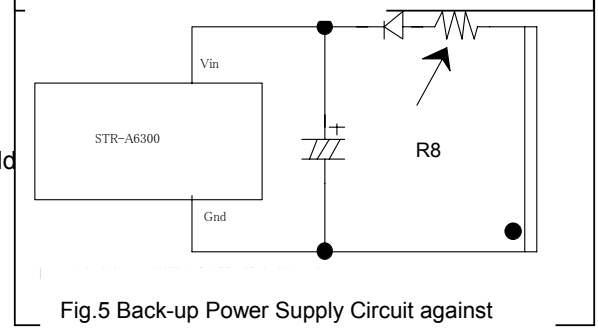


Fig.5 Back-up Power Supply Circuit against Output current(Io)

The optimum resistance value of the R8 should be determined in accordance with the specs of a transformer since the Vin terminal voltage varies by the structural differences of the transformer.

Furthermore, the variation ratio of the Vin terminal voltage becomes worse due to an inaccurate coupling between the primary and the secondary winding of the transformer(the coupling between the drive winding D and the stabilized output winding for the constant voltage control circuitry). Thus, in designing the transformer, the winding position of the drive winding D should also be studied carefully.

7.2 OCP/FB Terminal (Pin 4), Oscillator and Constant Voltage Control Circuit

The oscillator, making use of charging and discharging of the capacitor incorporated in the IC, generates pulse signals to determine OFF-time of the MOSFET. The control operation is made by the PRC (Pulse Ratio Control) operation fixing OFF-time (≒15usec) and varying ON-time of the MOSFET.

Fig.6 shows how the oscillator works when the IC operates without the constant voltage control.
The built-in capacitor is discharged and the value becomes around 0V when the MOSFET is ON. Besides, the voltage drop (VR5) occurs at the OCP/FB terminal (Pin 4) by the drain current ID flowing to R5. The voltage has a saw-tooth waveform as that of the ID, and almost the same voltage as VR5 is imposed on the No.4 terminal. When the No. 4 terminal voltage reaches the threshold voltage Vth(1)≒0.76V, OCP Comp. starts its operation, and the MOSFET shall be turned OFF by reversing the comparator of the internal oscillator.

The capacitor starts charging when the MOSFET is turned OFF, and the capacitor starts charging through the constant current charging circuit, and both-ends-of-the capacitor voltage starts rising in accordance with the gradient determined by the capacitor and the constant current charging circuit.
When both-ends-of-the capacitor voltage rises up to around 5V, the oscillator output is reversed again and the MOSFET is turned ON, and the capacitor is discharged to around 0V rapidly.
The MOSFET continues the oscillation by repeating this cycle.
The time determined by the gradient of VR5 (ID) becomes ON-time of the MOSFET. Furthermore, the fixed time determined by the capacitor and the constant current charging circuit is OFF-time of the MOSFET.
This fixed time is adjusted at approximately 15usec by the constant current charging circuit

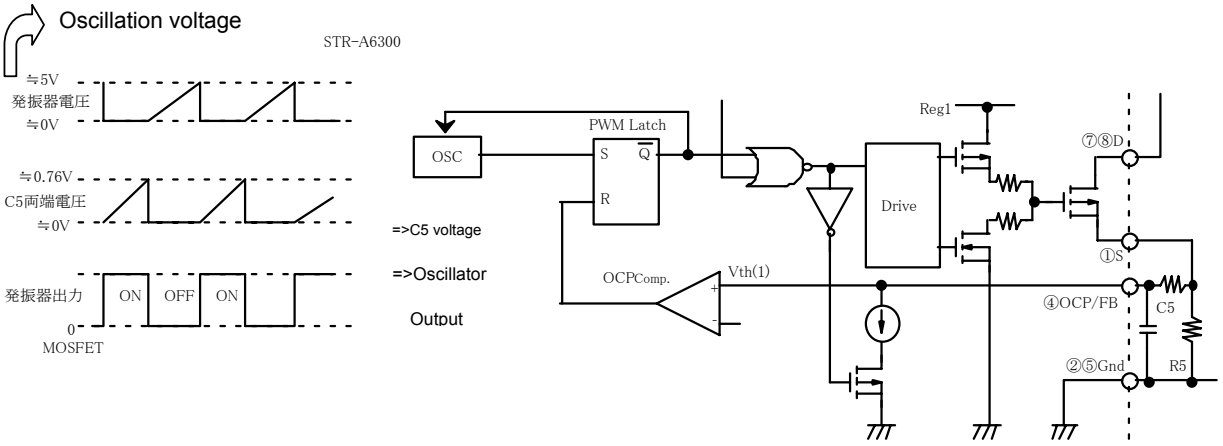


Fig.6 Oscillation Operation of Switch-Mode Power Supply

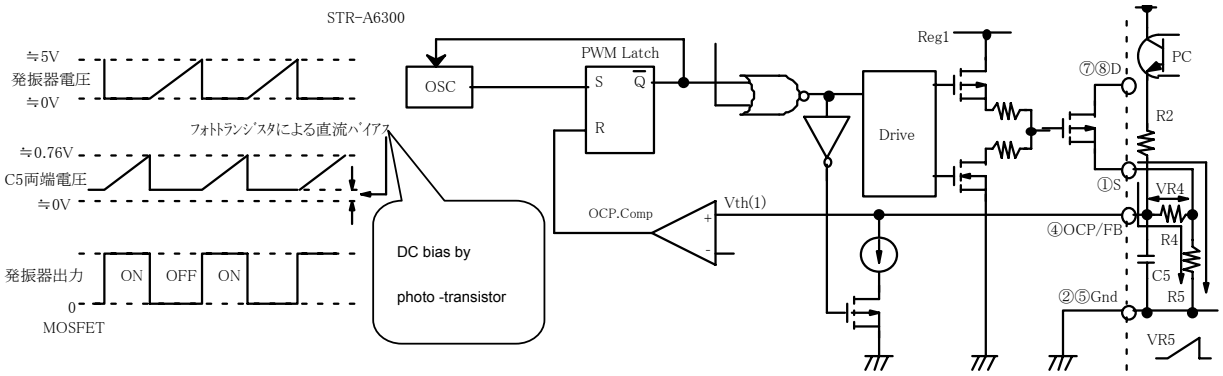


Fig.7 Oscillating Operation at constant voltage control

Feedback current (FB current) through a photo-coupler flows to R4, and the voltage drop VR4 is added to VR5. That is, the VR4 (FB current) controls the VR5 voltage (peak ID) which requires to reverse the OCP Comp., and the output is controlled in the current mode.

Generally, in the current mode control, the bias from VR4 increases at light mode, and the OCP Comp. shall be functioned faultily by the noise caused from the surge current at the MOSFET turn-ON. In order to avoid this problem, the impedance between the OCP/FB (No.5) and the GND terminal is reduced by an **Active-Low-Pass Filter Circuit** while the MOSFET is turned OFF.

The Active-Low-Pass Filter circuit is composed of the 0.8mA constant current by-pass circuit between the OCP/FB (No.5) and the GND terminal, and it reduces the bias by 50% until the MOSFET is turned ON.

This function enables C5 to absorb surge noise when the MOSFET is turned ON and achieves a stable control at light load.

7.3 OCP/FB Terminal(Pin 4)/OCP Circuit

This is a pulse-by-pulse overcurrent protection circuit that detects peak value of drain current of the MOSFET in every pulse and reverses the oscillator output. OCP(Overcurrent Protection) circuit is shown on Fig. 9.

MOSFET drain current is detected by puttig the voltage drop of R5 into OCP/FB terminal. <R5 is connected between Source terminal(Pin 1) and GND terminal(Pin 2 and 5)>

Threshold voltage, Vth(1) of the OCP terminal is set at around 0.76V against GND terminal. External components, R4 and C5, function as a filter circuit to prevent malfunction caused by surge current when the MOSFET is turned ON.

Output characteristics of the secondary side at the time the OCP circuit operates, due to the overload of the secondary side output, is shown on Fig. 8. Where the output voltage drops with the overload, drive winding voltage of the primary side also falls proportionally, and the Vin terminal voltage falls below shutdown voltage to stop the operation. In this case, as circuit current also decreases simultaneously, the Vin terminal voltage rises again by the charged current through Rs, and the circuit itself re-operates intermittently at the operation start voltage. However, when a transformer has many output windings and coupling is not sufficient, primary side winding voltage would not drop, and operation may not become intermittent accordingly, even though the secondary side output voltage drops in overload status.

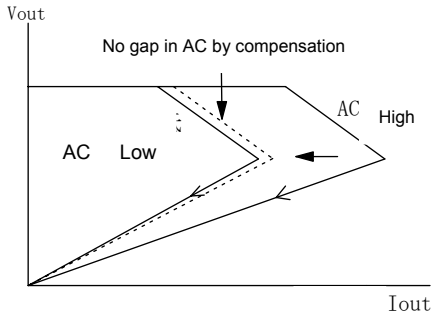


Fig.8 Power supply output overload characteristics

As the OCP circuit is operated by detecting drain current of the MOSFET, output power becomes high when the protection circuit operates with high input voltage as shown on Fig. 8. In order to prevent this, it is effective to add a bias circuit(using two resistors and a Zener diode) which should be in proportional to the input voltage as displayed on Fig.9.

There are two merits in adding the bias circuit;

(1) When input voltage is high, the drain current of the MOSFET is kept at low level; thus, the voltage stresses to the MOSFET both at start up and at light load are also reduced by lowering the surge voltage generated by the transformer.

(2) Current stresses to the diodes at the secondary side are reduced by the constant control of the output power.

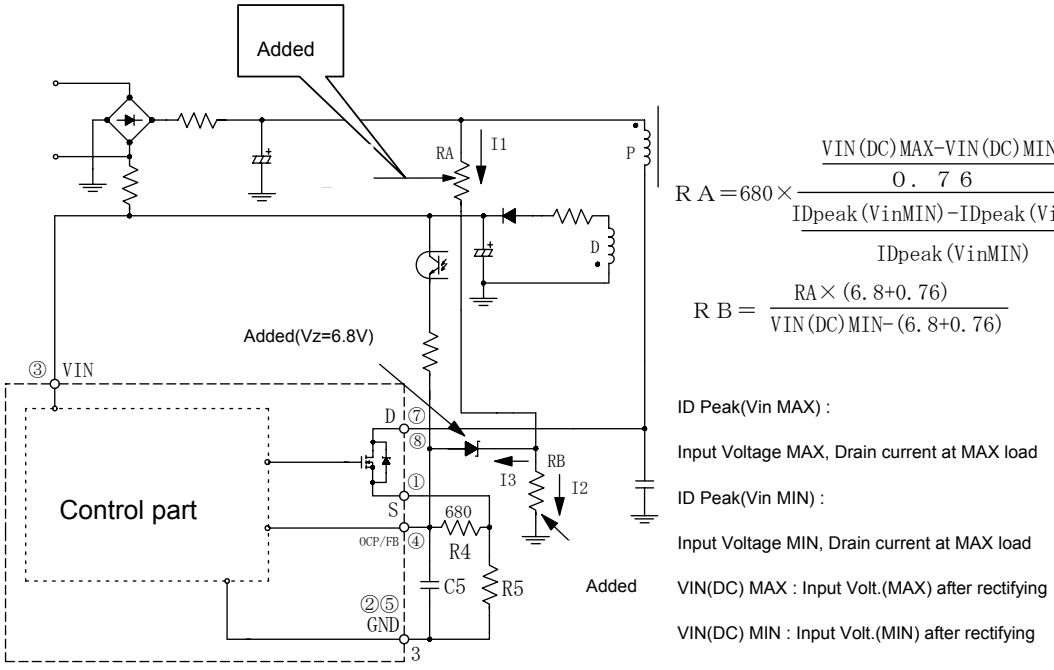


Fig.9 OCP compensation circuit with input voltage

7.4 Latch Circuit

Latch circuit keeps the oscillator output low and stops the power supply circuit operation when either the Overvoltage Protection(OVP) or Thermal Shutdown(TSD) circuit operates.

The holding current of the latch circuit is 70uA MAX(Ta=25^{o}C) when the Vin is 20V. However, considering slight voltage increase at low temperature, it is required to flow 100uA or higher to the Vin terminal from the start-up resistor in order to maintain the latch circuit operation.

In order to prevent malfunction caused by noises, etc., the delay time is set by a timer circuit incorporated in the IC, and thereafter, the latch circuit starts its operation when either the OVP or TSD circuit operates for 8usec or longer.

The Vin terminal voltage, however, will drop even after the latch circuit starts its operation because the constant voltage power supply(Reg.) circuit in the control circuitry continues its operation and maintains higher circuit current.

When the Vin terminal voltage falls to the shutdown voltage(7.9V MIN) or lower, the circuit current becomes below 70uA(Ta=25 ^{o}C), and the Vin terminal voltage starts rising again.

When the Vin terminal voltage reaches the operation start voltage(17.6V TYP), it falls as the circuit current increases again. Consequently, the latch circuit operation prevents the Vin terminal voltage from rising abnormally by managing the voltage between 10.1V(TYP) and 17.6V(TYP). The Fig.10 shows the voltage waveform when the latch circuit is in

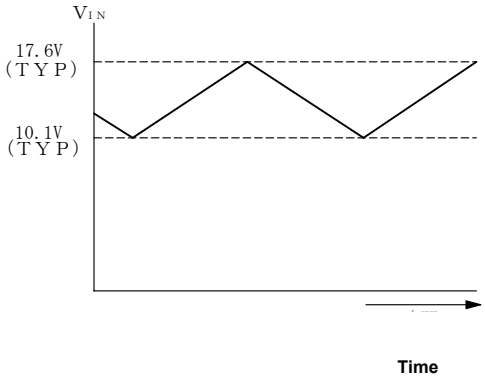


Fig.10 Example of Vin waveform at Latch Circuit ON

operation. The cancellation of the latch circuit is made by reducing the Vin terminal voltage below 7.9V, and generally, it is restarted by AC input switch-off of the power supply.

7.5 Thermal Shutdown(TSD) Circuit

TSD circuit makes the latch circuit operate when the frame temperature of the IC is above **135 °C(MIN)**. Temperature detection is actually made by the control IC.

7.6 Overvoltage Protection(OVP) Circuit

OVP circuit makes the latch circuit operate when the Vin terminal voltage exceeds 25.5V(TYP), and it functions as a protection against the overvoltage at the Vin terminal of the control circuit.

In general, the Vin terminal voltage is provided from the drive winding of the transformer and it is proportional to the output voltage. Therefore, the circuit operates even in the overvoltage output of the secondary side, for instance, when the voltage detection circuit is open. In this case, the secondary output voltage when the OVP circuit operates is obtained from;

$$V_{OUT}\,(OVP) \fallingdotseq \frac{V_{OUT}\text{ at Normal Operation}}{V_{IN}\text{ Terminal Voltage at Normal Operation}} \times 22.5V\ (TYP)$$

8 CALCULATION OF PRIMARY INDUCTANCE

Design of the transformer is basically same as that of RCC type power supplies. Assuming D as ON-Duty decided from the ratio between P winding(Np) and S winding(Ns), the Lp is obtained from the formula below. Also, due to the fixed OFF-time of the PRC operation, the transformer should be designed in order the drain current to be un-continuous at the MIN input and MAX load.

$$LP = \frac{(VIN \cdot D)^2}{2 \times fo \times Po} \times \eta \qquad (\mathrm{H})$$

Po: Maximum Output Power

fo: Minimum Oscillating Frequency

η : : Power supply efficiency=approx. 0.9(In case of CTV), 0.75~0.85(Low Output Voltage)

D: ON-Duty at Vin(AC)

VIN: C1 voltage at Minimum VIN(AC)

9 DESIGN GUIDELINES

9.1 External components

Care needs to be taken in the capacitance, inductance, and allowable dissipation of external components. For the loss of input/output capacitors to the ripple current and voltage, and for the loss of transformer for copper and iron, the sufficient margin is to be considered in a power supply. Especially for the OCP resistor, R5, where high frequency elements flow, a resistor having high internal inductance is likely to cause malfunctions. Thus a resistor having low internal inductance and high surge energy should be selected. As switching current contains high frequency elements, the influence of the surface effect is not to be neglected. Therefore, it is recommended to enlarge the surface area of the transformer winding by using

either a wire with small diameter or a Litz wire. Resonant capacitors and electrolytic capacitors for high ripple applications, or for low impedance for the power supply should be selected.

9.2 Switching speed control

The source terminal is isolated, and switching noise can be reduced by adding a ferrite bead(FB) to the source terminal, which enables to control switching speed. However, with the ferrite bead only, switching speed is decreased not only at turn-ON but also at turn-OFF, resulting in the increase of switching loss.

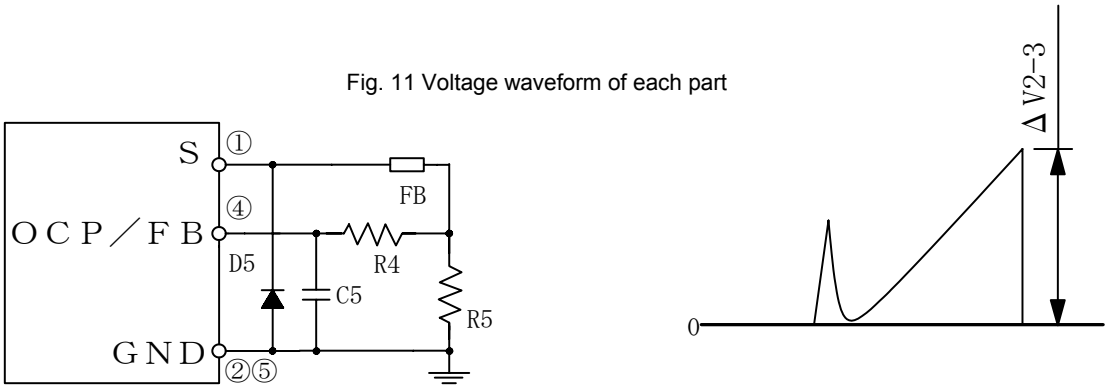
In order to prevent this, adding a diode between pin 1 and pin 2,5(GND) is recommended as displayed on Fig. 11. The small signal switching diode having high speed and small junction capacitance, or a Schottky Barrier diode(such as AK 03 manufactured by Sanken) is recommended.

9.3 Maximum switching current

The voltage between the source and GND terminal shall be dropped by inserting a current detecting resistor and a ferrite bead. Due to the voltage drop, gate drive voltage of the MOSFET falls, and maximum switching current for MOSFET operation decreases, accordingly. Therefore, as shown on Fig. 11, the maximum switching current needs to be de-rated in accordance with the de-rating curve listed In each data sheet, measuring the voltage drop between the source and the GND terminal.

Make sure the voltage drop and the maximum switching current measured at both the normal operation and the overcurrent protection operation are within the de-rating curve.

Fig. 11 Voltage waveform of each part



9.4 Phase compensation

Current mode control circuit is applied in the STR-A6300 Series; therefore, it requires no special phase compensation, and gain adjustments by a secondary side error-amplifier shall be enough.

Furthermore, in case a Sanken's error-amplifier is applied, thanks to its excellent response and low gain, phase compensation might not be required at all.

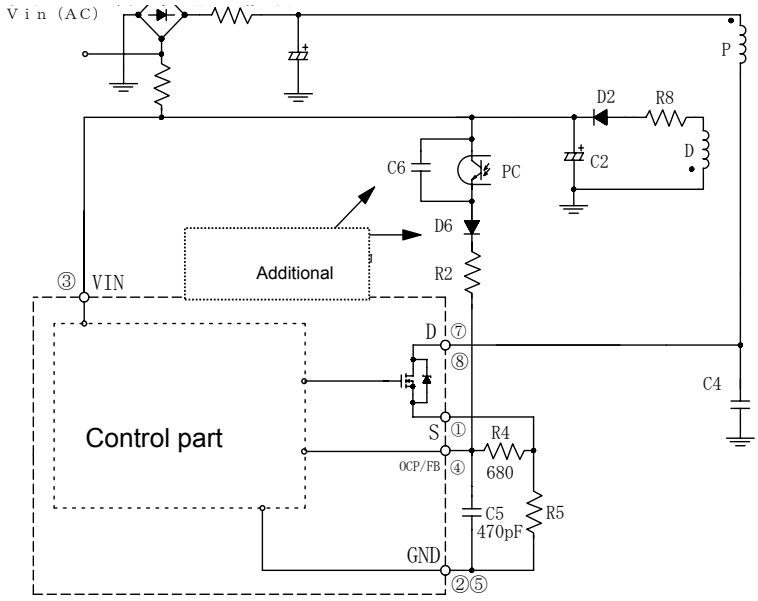


Fig. 12 Phase compensation circuit

However, when the phase compensation by the secondary side error-amplifier is not sufficient, due to the quite large ripple of a smoothing capacitor or unique loads specifications, it is effective to insert the capacitor, C6, in the range of 0.01~0.1uF at both ends of the primary side photo-transistor as displayed on Fig. 12.
In this case, it is necessary to connect a diode, D6, which is for preventing reverse current, to the photo-transistor in series.

In case of a wide input, the variation of intermittent oscillating frequency is quite large because of unstable AC input voltage. Converting the start-up resistor area to a constant current circuit can reduce rattling noise produced at low AC input voltage.

9.5 Notes for PCB layouts for Switching Power Supply with PRC operation in using STR-A6300 Series

As shown on Fig. 13, the connection from pin 2 to R5(GND side) should be as short and wide as possible. Nearest to the R5, the pattern to pin 5 should be isolated from that of both the electrolyte input capacitor and the voltage resonance capacitor. In addition, pin 2(GND) and pin 5(GND) should be connected through external pattern as short as possible. The pattern width is 1A/1mm or wider, and C2(C2'), C3, C5, and R3 should be connected on this pattern. In case the pattern from the IC to the C2 is far, the capacitor, C2, in the range of 0.01~0.1uF approx. should be connected near the IC.

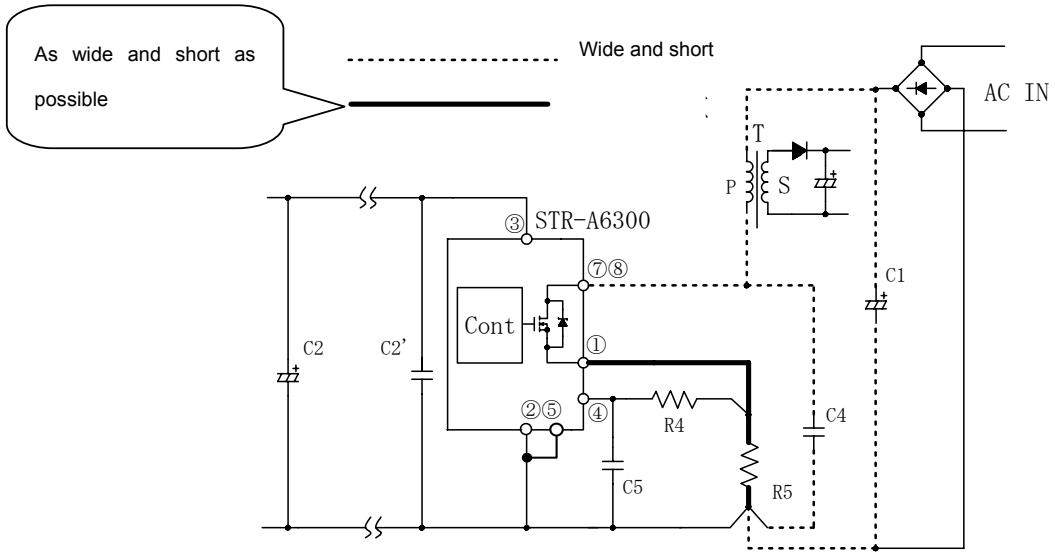


Fig.13 Example of Ancillary Circuit Connection

9.6 Notes for Mounting Design

Where PCB pattern and mounting conditions are applied improperly, malfunction, noise, and loss might occur. Based on the principle of "wider and shorter", line impedance can be lowered by making thicker pattern where a high frequency current flows, and by making shorter wiring between components. As shown on Fig. 14, where high frequency current makes a loop, the pattern should be designed in order the area inside the loop(the shaded area) to keep minimized. Especially, the ground and the earth line described by slashed lines in Fig.14, which considerably affect radiant noise, should be as short and wide as possible. In the switching power supply, as there are current circuits where

high frequency and high voltage flows, the layout of components and the pattern clearance are required for safety standards and regulation.

In addition, care also needs to be taken in the heat radiation design due to positive temperature coefficient of MOSFET rDS.

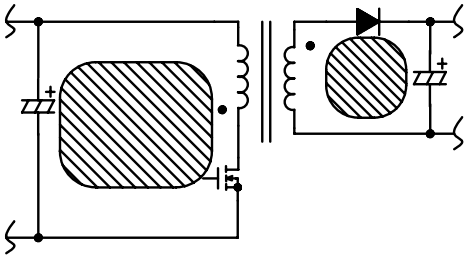


図14　高周波電流ループ

Fig.14 High Frequency Current Loop