Am29705A/707

16-Word by 4-Bit 2-Port RAM

DISTINCTIVE CHARACTERISTICS

- 16-word by 4-bit, 2-port RAM
- Two output ports, each with separate output control
- Separate four-bit latches on each output port (Am29707 has separate output control)
- Data output is noninverting with respect to data input
- Chip select and write enable inputs for ease in cascading
- Am29707 offers 20% improved cycle time over Am29705A when used with Am29203 in three address architecture
- Am29705A is a pin-for-pin replacement for the Am29705 but is significantly faster on critical paths

GENERAL DESCRIPTION

The Am29705A is a 16-word by 4-bit, two-port RAM. This RAM features two separate output ports such that any two 4-bit words can be read from these outputs simultaneously. Each output port has a four-bit Latch but a common Latch Enable (LE) input is used to control all eight latches. The device has two Write Enable ($\overline{WE}$) inputs and is designed such that the Write Enable 1 ($\overline{WE_1}$) and Latch Enable (LE) inputs can be wired together to make the operation of the RAM appear edge triggered.

The device has a fully decoded four-bit A-address field to address any of the 16 memory words for the A-output port. Likewise, a four-bit B-address input is used to simultaneously select any of the 16 words for presentation at the B-output port. New incoming data is written into the four-bit RAM word selected by the B-address. The D inputs are used to load new data into the device.

The Am29705A features three-state outputs and several devices can be cascaded to increase the total number of memory words in the system. The A-output port is in the high-impedance state when the $\overline{OE}$-A input is HIGH. Likewise, the B-output port is in the high-impedance state when the $\overline{OE}$-B input is HIGH. Four devices can be paralleled using only one Am25LS139 decoder for output control.

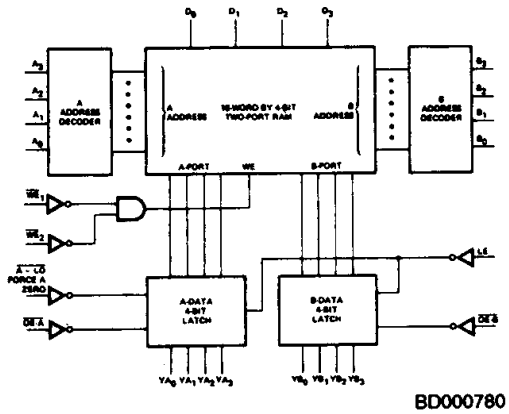
The Write Enable inputs control the writing of new data into the RAM. When both Write Enable inputs are LOW, new data is written into the word selected by the B-address field. When either Write Enable input is HIGH, no data is written into the RAM.

The Am29707 is an identical circuit to the Am29705A, except each output port has a separate Latch Enable (LE) input. An extra write enable input ($\overline{WE_2}$) may be connected directly to the IEN of the Am29203 for improved cycle times over the Am29705A. The $\overline{WE}$/BLE input can then be connected directly to system clock.

The Am29705A is a plug-in replacement for the Am29705, but is significantly faster. The Am29705A and Am29707 feature AMD's advanced ion-implanted micro-oxide (IMOX™) processing.

BLOCK DIAGRAMS

Am29705A



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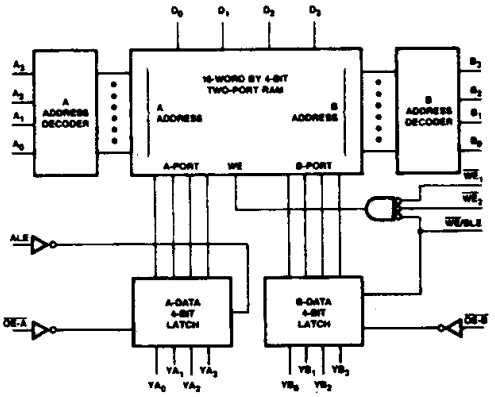
Am29707



BD000790

RELATED PRODUCTS

Am29751A	Bipolar PROM
Am2921	One-of-Eight Decoder
Am25LS138	One-of-Four Decoder
Am25LS139	Dual One-of-Four Decoder
Am25LS157	Quad 2-by-1 MUX
Am29203	Four Bit Bipolar Microprocessor Slice
Am2902A	Carry Look Ahead Generator
Am2904	Status and Shift Control Unit
Am2910A	Microprogram Controller
Am2914	Vectored Priority Interrupt Controller
Am2940	DMA Address Generator
Am2950-54	8 Bit Bidirectional I/O Port
Am29118	8 Bit Bidirectional I/O Port with ACC

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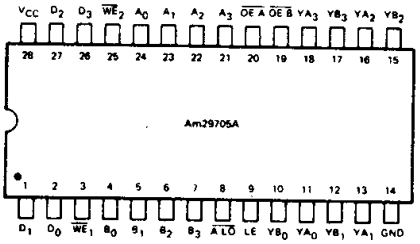
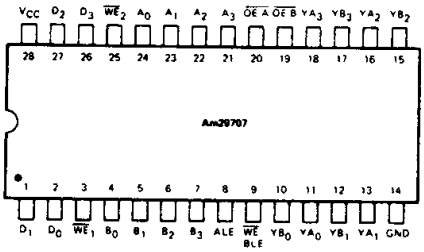
CONNECTION DIAGRAMS – TOP VIEWS

D-28-1*
P-28-1*



CD001060

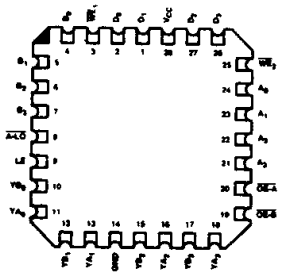
D-28-1*
P-28-1*



CD001050

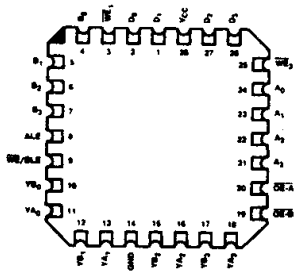
*Devices are also offered in a 28 pin flatpak.
Connections are the same as DIPs.

L-28-1



CD001080

L-28-1

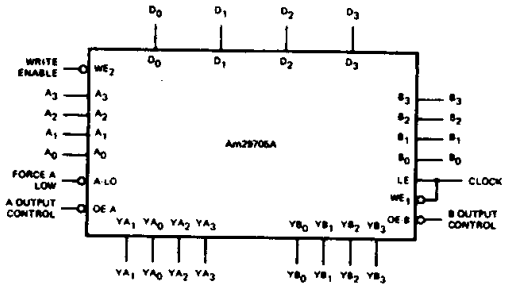


CD001070

Note: Pin 1 is marked for orientation

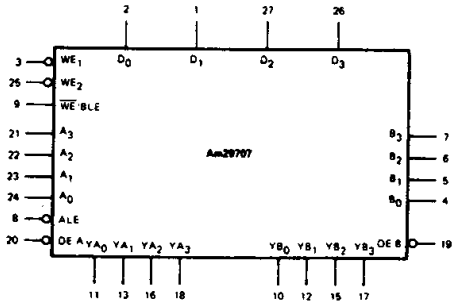
LOGIC SYMBOLS

Am29705A



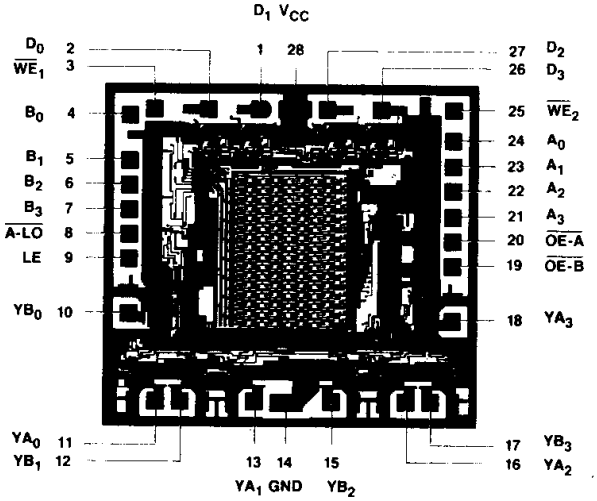
LS000340

Am29707



LS000330

METALLIZATION AND PAD LAYOUT



DIE SIZE: .104 x .96

ORDERING INFORMATION

Am29707 A D C B

- B — Burn-In Option: B = 96 hour burn-in
- C — Temperature Range: C = 0 to +70°C; M = −55 to +125°C
- D — Package: D = 28 pin ceramic SLIMDIP; F = 28 pin Flat Pak; L = 28 pin Chip Pak; P = 28 pin Molded Dip; X = 28 Dice
- A — Speed: See Product Select Guide
- Am29707 — Part Number

Valid Combinations	
Am29707	DC, DCB, DMB, FMB, LC, LMB, PC, XC, XM
Am29707	DC, DCB, DMB, FMB, LC, LMB, PC, XC, XM

PIN DESCRIPTION

$D_0 - D_3$ **Data Inputs**
New data is written into the RAM through these inputs.

$A_0 - A_3$ **The A-Address Inputs**
The four-bit field presented at the A inputs selects one of the 16 memory words for presentation to the A-Data Latch.

$B_0 - B_3$ **The B-Address Inputs**
The four bit field presented at the B inputs selects one of the 16 memory words for presentation to the B-Data Latch. The B address field also selects the word into which new data is written.

$YA_0 - YA_3$ **The Four A-Data Latch Outputs**

$YB_0 - YB_3$ **The Four B-Data Latch Outputs**

$\overline{WE}_1$, $\overline{WE}_2$ **Write Enables**
When both Write Enables are LOW, new data is written into the word selected by the B-address field. If either Write Enable input is HIGH, no new data can be written into the memory.

$\overline{OE}$-A **A-Port Output Enable**
When $\overline{OE}$-A is LOW, data in the A-Data Latch is present at the YA_i outputs. If $\overline{OE}$-A is HIGH the YB_i outputs are in the high-impedance (off) state.

$\overline{OE}$-B **B-Port Output Enable**
When $\overline{OE}$-B is LOW, data in the B-Data Latch is present at the YB_i outputs. When $\overline{OE}$-B is HIGH the YB_i outputs are in the high-impedance (off) state.

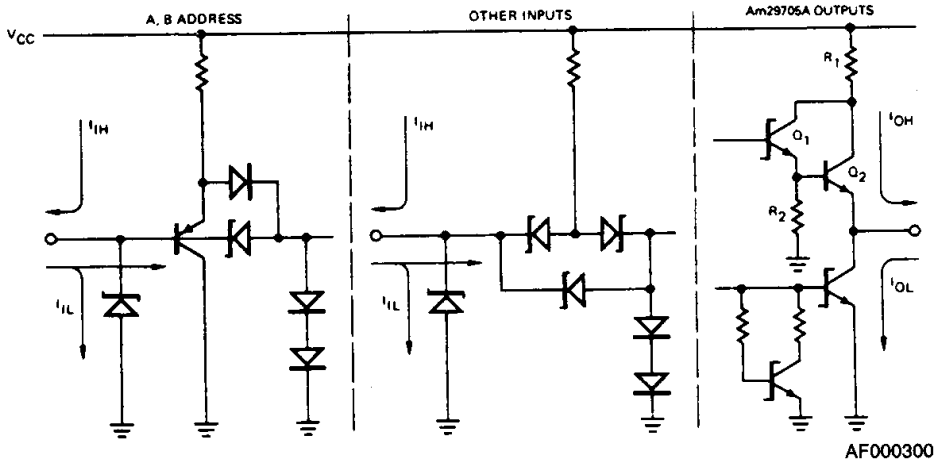
LE **Latch Enable**
The LE input controls the latches for both the RAM A-output port and RAM B-output port. When the LE input is HIGH, the latches are open (transparent) and data from the RAM, as selected by the A and B address fields, is present at the outputs. When LE is LOW, the latches are closed and they retain the last data read from the RAM independent of the current A and B address field inputs. (Am29705A only.)

$\overline{A\text{-}LO}$ **Force A Zero**
This input is used to force the outputs of the A-port latches LOW independent of the Latch Enable input or A-address field select inputs. Thus, the A-output bus can be forced LOW using this control signal. When the $\overline{A\text{-}LO}$ input is HIGH, the A latches operate in their normal fashion. Once the A latches are forced LOW, they remain LOW independent of the $\overline{A\text{-}LO}$ input if the latches are closed. (Am29705A only.)

ALE **A-Output Port Latch Enable**
When ALE is HIGH, the A latch is open (transparent) and data from the RAM, as selected by the A address field, is present at the A output. When ALE is LOW, the A latch is closed and retains the last data read from the RAM independent of the current A address field input. (Am29707 only.)

$\overline{WE}$/BLE **Write Enable/B-Output Port Latch Enable**
When $\overline{WE}$/BLE is LOW together with $\overline{WE}_1$ and $\overline{WE}_2$, new data is written into the word selected by the B address field. When $\overline{WE}$/BLE or any Write Enable input is HIGH, no data is written into the RAM.
$\overline{WE}$/BLE also controls the B output port. When $\overline{WE}$/BLE is HIGH, the B latch is open (transparent), and when this input is LOW, the B latch is closed (Am29707 only).

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

FUNCTION TABLES

Am29705A

WRITE CONTROL

$\overline{WE_1}$	$\overline{WE_2}$	Function	RAM Outputs at Latch Inputs	
			A-Port	B-Port
L	L	Write D into B	A data (A ≠ B)	Input Data
L	L	Write D into B	(A = B) Input Data	Input Data
X	H	No Write	A Data	B Data
H	X	No Write	A Data	B Data

H = HIGH L = LOW X = Don't Care

YA READ

Inputs			YA Output	Function
$\overline{OE\text{-}A}$	$\overline{A\text{-}LO}$	LE		
H	X	X	Z	High Impedance
L	L	X	L	Force YA LOW
L	H	H	A-Port RAM Data	Latches Transparent
L	H	L	NC	Latches Retain Data

H = HIGH X = Don't Care NC = No Change
L = LOW Z = High Impedance

YB READ

Inputs		YB Output	Function
$\overline{OE\text{-}B}$	LE		
H	X	Z	High Impedance
L	H	B-Port RAM Data	Latches Transparent
L	L	NC	Latches Retain Data

H = HIGH X = Don't Care NC = No change
L = LOW Z = High Impedance

Am29707

WRITE CONTROL

$\overline{WE_1}$	$\overline{WE_2}$	$\overline{WE}$/BLE	Function	RAM Outputs at Latch Inputs	
				A-Port	B-Port
L	L	L	Write D into B	A Data (A = B)	Input Data
X	X	H	No Write	A Data	B Data
X	H	X	No Write	A Data	B Data
H	X	X	No Write	A Data	B Data

H = HIGH L = LOW X = Don't Care

YA READ

Inputs		YA Output	Function
$\overline{OE\text{-}A}$	ALE		
H	X	Z	High Impedance
L	H	A-Port RAM Data	Latches Transparent
L	L	NC	Latches Retain Data

H = HIGH D = Don't Care NC = No Change
L = LOW Z = High Impedance

YB READ

Inputs		YB Output	Function
$\overline{OE\text{-}B}$	$\overline{WE}$/BLE		
H	X	Z	High Impedance
L	H	B-Port RAM Data	Latches Transparent
L	L	NC	Latches Retain Data

H = HIGH D = Don't Care NC = No Change
L = LOW Z = High Impedance

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
D_1	1	1	–	–
D_0	2	1	–	–
$\overline{WE_1}$	3	1	–	–
B_0	4	0.55	–	–
B_1	5	0.55	–	–
B_2	6	0.55	–	–
B_3	7	0.55	–	–
$\overline{A\text{-}LO}$ (29705A Only)	8	1	–	–
LE (29705A Only)	9	1	–	–
ALE (29707 Only	8	1	–	–
$\overline{WE}$/BLE (29707 Only)	9	1	–	–
YB_0	10	–	100/200	33
YA_0	11	–	100/200	33
YB_1	12	–	100/200	33
YA_1	13	–	100/200	33
GND	14	–	–	–
YB_2	15	–	100/200	33
YA_2	16	–	100/200	33
YB_3	17	–	100/200	33
YA_3	18	–	100/200	33
$\overline{OE\text{-}B}$	19	1	–	–
$\overline{OE\text{-}A}$	20	1	–	–
A_3	21	0.55	–	–
A_2	22	0.55	–	–
A_1	23	0.55	–	–
A_0	24	0.55	–	–
$\overline{WE_2}$	25	1	–	–
D_3	26	1	–	–
D_2	27	1	–	–
V_{CC}	28	–	–	–

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage to Ground
Potential Continuous ..... −0.5V to +7.0V
DC Voltage Applied to OUtput
for HIGH Output State ..... −0.5V to +V_{CC}max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into
Output 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Symbol	Parameter	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −2.0mA	2.4			Volts
			COM'L, I_{OH} = −4.0mA	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA (MIL)			0.5	Volts
			I_{OL} = 20mA (COM)			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V	All			−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 55V				0.1	mA
I_O	Off State (High Impedance) Output Current	V_{CC} = MAX. V_{IN} = V_{IH} or V_{IL}	V_O = 2.4V			20	μA
			V_O = 0.5V			−20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−30		−85	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Worst case I_{CC} is at minimum temperature) (Note 4)					mA
			T_A = 0°C to +70°C			210	
			T_A = 70°C			170	
			T_C = −55°C to +125°C			210	
			T_C = 125°C			150	

Notes:

1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All inputs grounded except $\overline{OE}$-A and $\overline{OE}$-B = 2.4V.

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SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Parameters	From	To	Test Conditions	COM'L	MIL
Access Time	A Address Stable or B Address Stable	YA Stable or YB Stable	LE = HIGH	25	30
Turn-On Time	$\overline{OE}$-A or $\overline{OE}$-B LOW	YA or YB Stable		20	20
Turn-Off Time	$\overline{OE}$-A or $\overline{OE}$-B HIGH	YA or YB Off	C_L = 5pF Note 1	20	20
Reset Time	$\overline{A\text{-}LO}$ LOW	YA LOW		20	20
Latch Enable Time	LE HIGH	YA and YB Stable		20	22
Transparency	$\overline{WE_1}$ and $\overline{WE_2}$ LOW	YA or YB	LE = HIGH	30	35
	D	YA or YB	LE = HIGH	30	35

Note 1. Measured from 1.5V at the input to 0.5V change in the output level.

MINIMUM SETUP AND HOLD TIME (in ns)

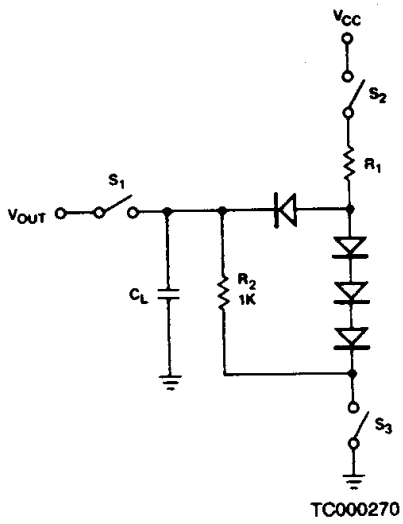
Parameters	From	To	Test Conditions	COM'L	MIL
Data Setup Time	D Stable	Either $\overline{WE}$ HIGH		12	15
Data Hold Time	Either $\overline{WE}$	D Changing		0	0
Address Setup Time	B Stable	Both $\overline{WE}$ LOW		6	8
Address Hold Time	Either $\overline{WE}$ HIGH	B Changing		0	0
Latch Close Before Write Begins	LE LOW	$\overline{WE_1}$ LOW	$\overline{WE_2}$ LOW	0	0
	LE LOW	$\overline{WE_2}$ LOW	$\overline{WE_1}$ LOW	0	0
Address Setup Before Latch Closes	A or B Stable	LE LOW		12	15

MINIMUM PULSE WIDTHS

Parameters	Input	Pulse	Test Conditions	COM'L	MIL
Write Pulse Width	$\overline{WE_1}$	HIGH-LOW-HIGH	$\overline{WE_2}$ LOW	15	15
	$\overline{WE_2}$	HIGH-LOW-HIGH	$\overline{WE_1}$ LOW	15	15
A Latch Reset Pulse	$\overline{A\text{-}LO}$	HIGH-LOW-HIGH		15	15
Latch Data Capture	LE	LOW-HIGH-LOW		15	18

Note: The Am29705A meets or exceeds all of the specifications of the Am29705.

A. THREE-STATE OUTPUTS



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$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

Notes:

1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all A.C. tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open to t_{PZH} test. S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5pF for output disable tests.

TEST OUTPUT LOADS FOR Am29705A

Pin # (DIP)	Pin Label	Test Circuit	R_1	R_2
–	$YA_0 - YA_3$, $YB_0 - YB_3$	A	230	1k

Notes on Testing

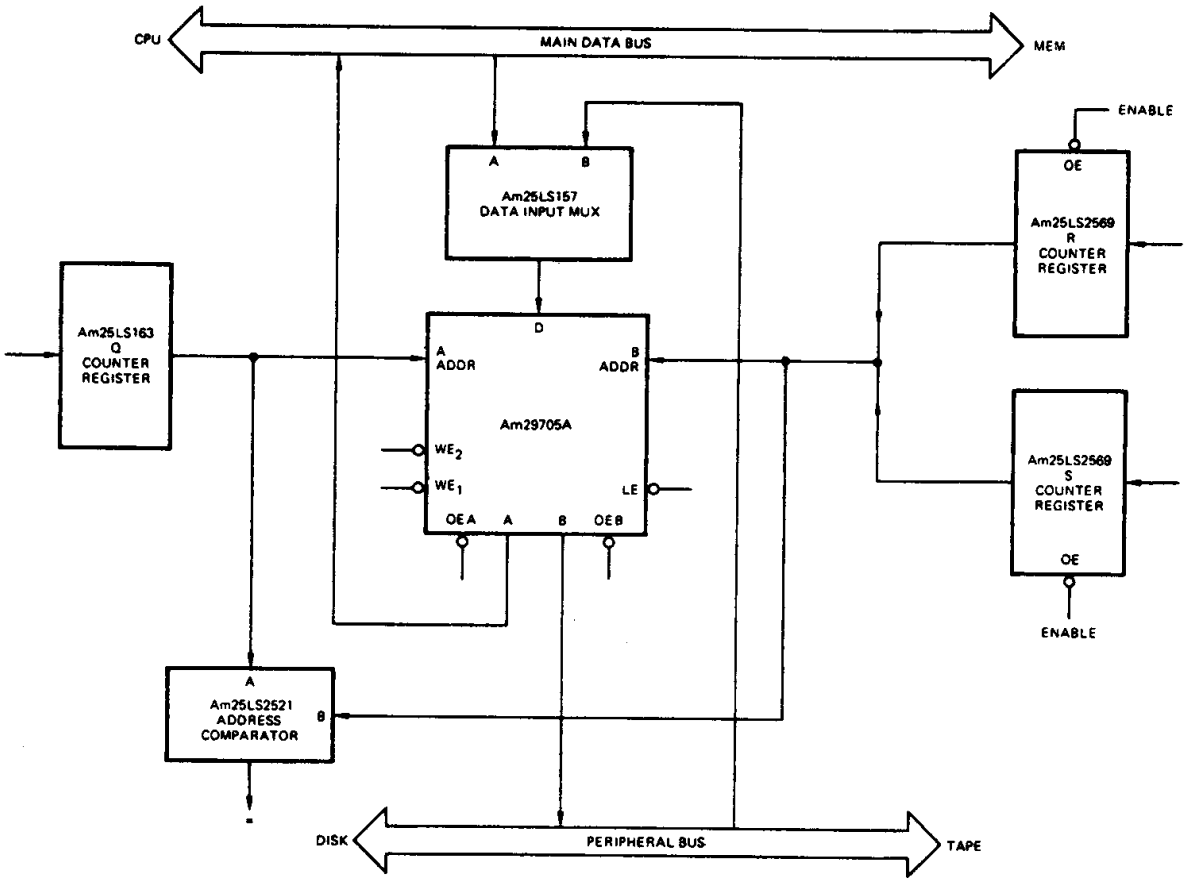
Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful:

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5–8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100s of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leqslant$ OV and $V_{IH} \geqslant$ 3V for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

USING THE Am29705A AND Am29707

The Am2903 and Am29203 each contain only 16 scratch-pad registers plus the Q register. For applications which require more than 17 registers, the register set of the Am2903 and Am29203 can be easily expanded.
- Use the Am29705A with the Am2903A
- Use the Am29707 with the Am29203

For further applications information on using the Am29705A with the Am2903A, see Chapter III of *Bit Slice Microprocessor Design*, Mick and Brick, McGraw-Hill Publications.



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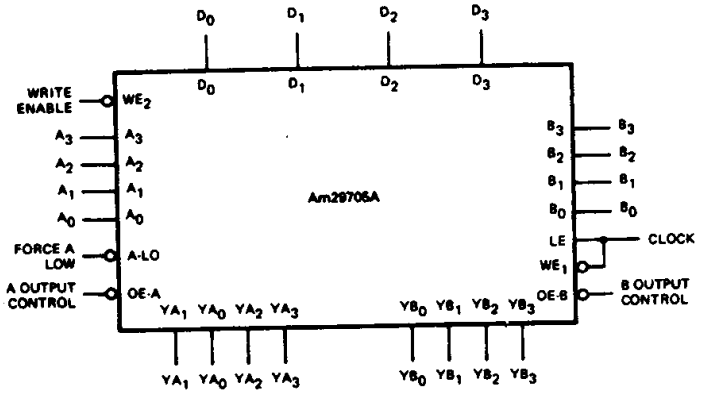
The Am29705A as a two-way interface buffer. Data may be passed between the main data bus and the peripheral data bus under I/O control. The two-port RAM allows data to be written into buffer storage from a peripheral device, using the B address port and the S counter register, while it is being read into main memory, using the A address port and the Q counter register. This simultaneous read/write capability facilitates DMA transfers because the CPU can ignore write requests from the peripheral device. Data output from CPU to the peripheral device is handled by sequential write and read operations. Data is written into buffer storage from the CPU, using the B address port and the R counter register. It is read onto the peripheral device using the B address port and either the R register, for single word transfers, or the S register, for block transfers.

APPLICATIONS (Cont.)



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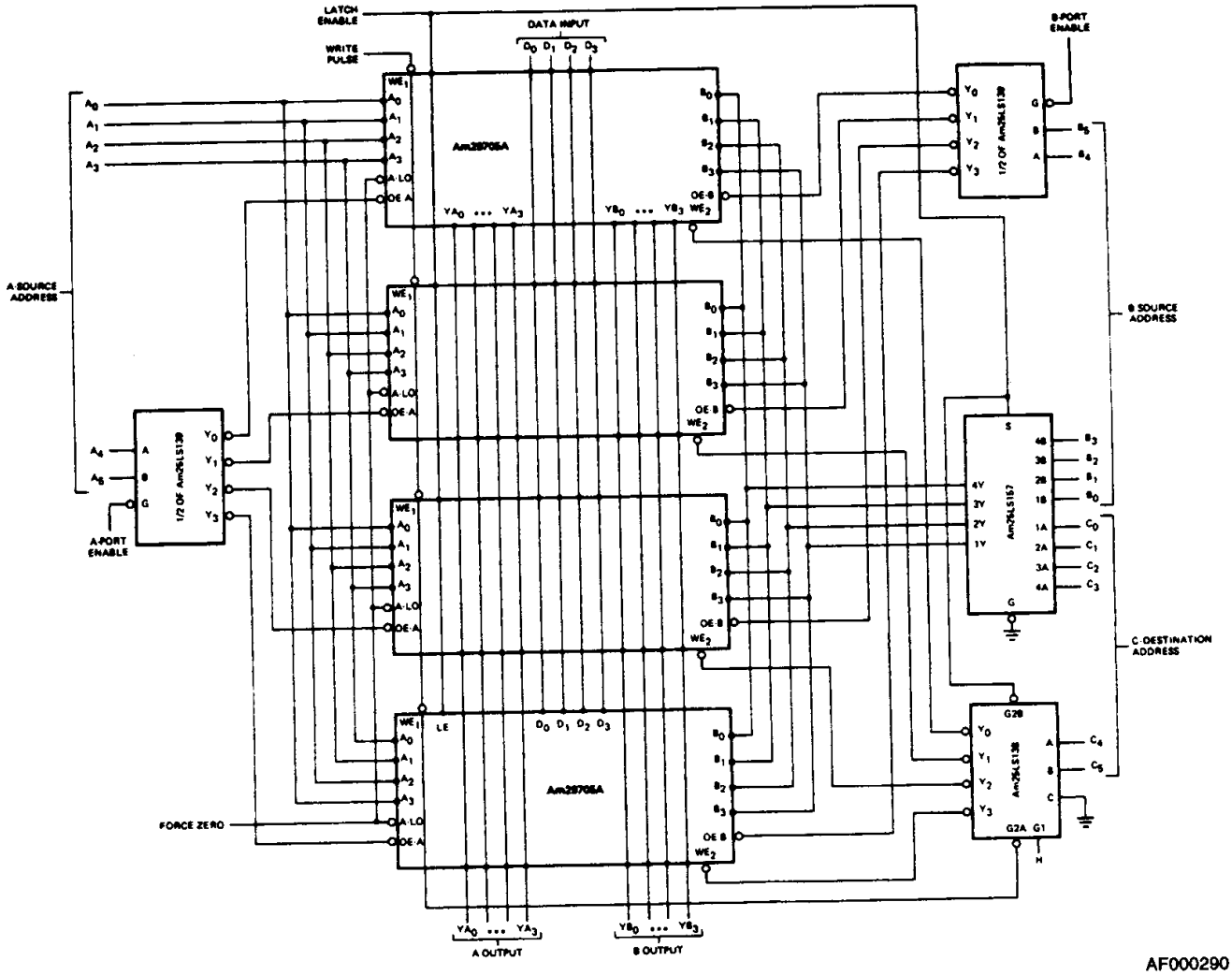
A 16-word by 4-bit two-port RAM with LE and WE_1 connected to make the device appear edge triggered. WE_1 and WE_2 are logically identical but are electrically slightly different. For synchronous operation without possibility of race, WE_1 should be connected to LE.



AF000290

A 64-word by 4-bit three address memory. Data is read from the A address to the YA outputs and from the B address to the YB outputs while the latch enable is HIGH. When the latch enable goes LOW, the YA and YB data is held in the internal latches, and the RAM B address is switched to the C-destination address lines. A write pulse will then deposit the input data into the location selected by the C address.

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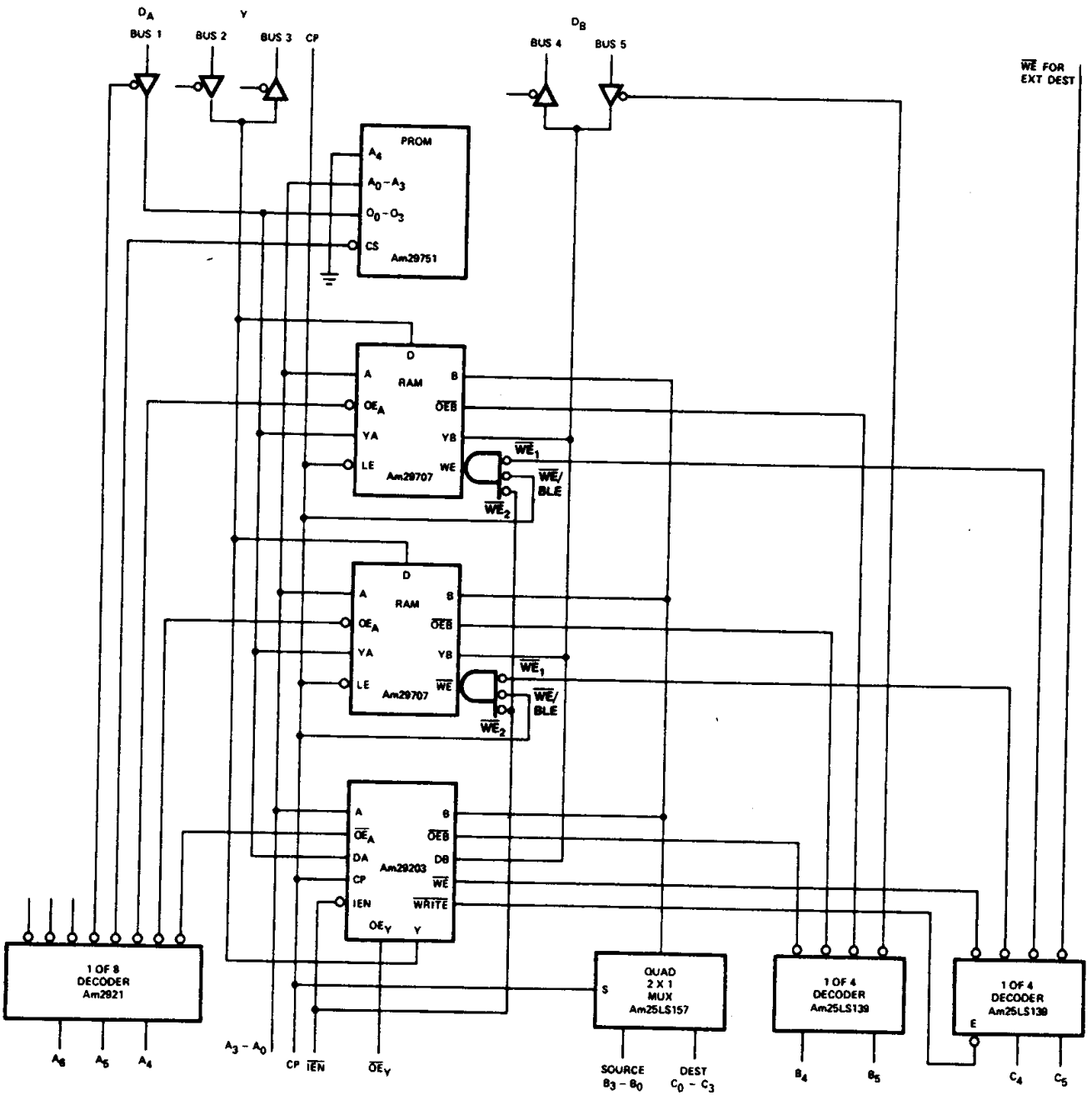
APPLICATIONS (Cont.)



AF000310

Am29203 EXPANDED MEMORY

A 48-word by 4-bit expanded memory for the Am29203 using the Am29707. The Am29751 PROM serves as a constant store.