

# Am2946/Am2947

Octal Three-State Bidirectional Bus Transceivers

## DISTINCTIVE CHARACTERISTICS

- 8-bit bidirectional data flow reduces system package count
- 3-state inputs/outputs for interfacing with bus-oriented systems; PNP inputs reduce input loading
- $V_{CC} - 1.15V_{OH}$  interfaces with TTL, MOS and CMOS
- 48mA, 300pF bus drive capability; Low power – 8mA per bidirectional bit
- Am2946 inverting transceivers; Am2947 noninverting transceivers; Transmit/Receive and Chip Disable simplify control logic
- Bus port stays in hi-impedance state during power up/down

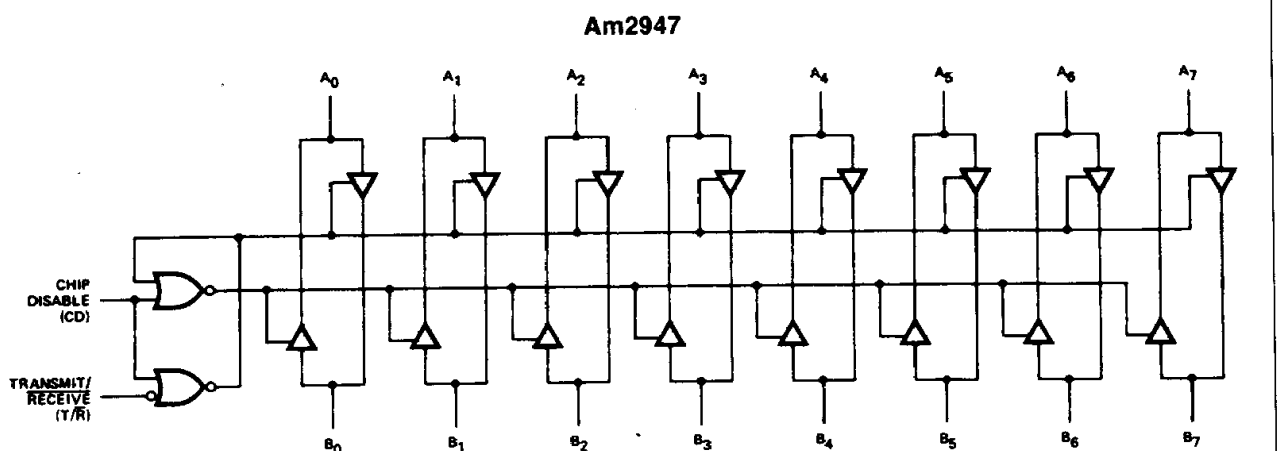
## GENERAL DESCRIPTION

The Am2946 and Am2947 are 8-bit state Schottky transceivers. They provide bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 24mA drive capability on the A ports and 48mA bus drive capability on the B ports. PNP inputs are incorporated to reduce input loading.

One input, Transmit/Receive, determines the direction of logic signals through the bidirectional transceiver. The Chip Disable input disables both A and B ports by placing them in a 3-state condition. Chip Disable is functionally the same as an active LOW chip select.

The output high voltage ( $V_{OH}$ ) is specified at  $V_{CC} - 1.15V$  minimum to allow interfacing with MOS, CMOS, TTL, ROM, RAM, or microprocessors.

## BLOCK DIAGRAM



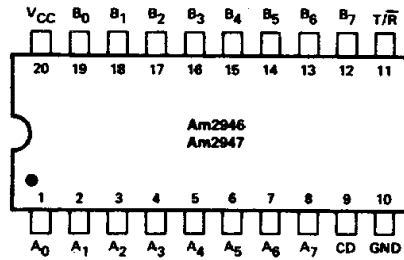
BD002530

Am2946 has inverting transceivers.

[www.DataSheet.in](http://www.DataSheet.in)

**CONNECTION DIAGRAM  
Top View**

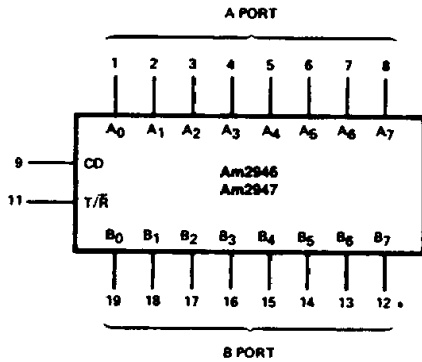
D-20-1



CD004760

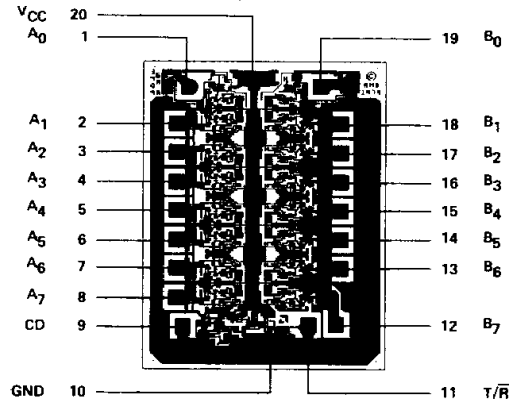
Note: Pin 1 is marked for orientation

**LOGIC SYMBOL**



LS001060

**METALLIZATION AND PAD LAYOUT  
Am2947**

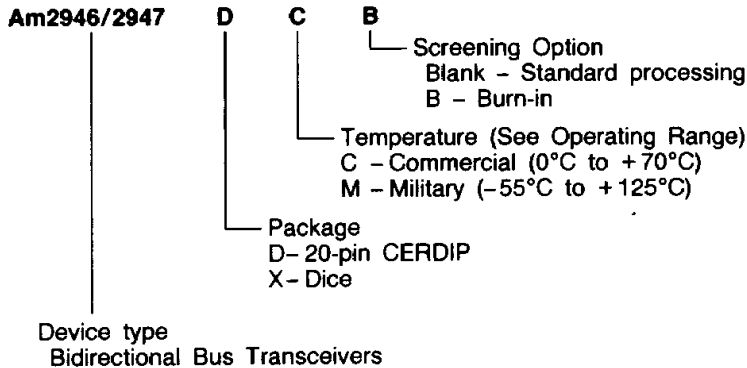


DIE SIZE .069" x .089"

Note: The Am2946 has inverting transceivers

**ORDERING INFORMATION**

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).



Valid Combinations	
Am2946	PC
Am2947	DC, DCB, DM, DMB XC

**Valid Combinations**

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

[www.DataSheet.in](http://www.DataSheet.in)

## PIN DESCRIPTION

Pin No.	Name	I/O	Description
	A <sub>0</sub> -A <sub>7</sub>	I/O	A port inputs/outputs are receiver output drivers when T/ $\bar{R}$ is LOW and are transmit inputs when T/ $\bar{R}$ is HIGH.
	B <sub>0</sub> -B <sub>7</sub>	I/O	B port inputs/outputs are transmit output drivers when T/ $\bar{R}$ is HIGH and receiver inputs when T/ $\bar{R}$ is LOW.
9	CD	I	Chip Disable forces all output drivers into 3-state when HIGH (same function as active LOW chip select, $\overline{CS}$ ).
11	T/ $\bar{R}$	I	Transmit/ $\bar{R}$ eceive direction control determines whether A port or B port drivers are in 3-state. With T/ $\bar{R}$ HIGH A port is the input and B port is the output. With T/ $\bar{R}$ LOW A port is the output and B port is the input.

## FUNCTION TABLE

Inputs	Conditions		
	L	L	H
Chip Disable	L	L	H
Transmit/ $\bar{R}$ eceive	L	H	X
A Port	Out	In	HI-Z
B Port	In	Out	HI-Z

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature .....	-65°C to +150°C
Supply Voltage .....	7.0V
Input Voltage .....	5.5V
Output Voltage .....	5.5V
Lead Temperature (Solder, 10 seconds) .....	300°C

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## OPERATING RANGES

Commercial (C) Devices	Temperature .....	0°C to +70°C
	Supply Voltage .....	+4.75V to +5.25V

Military (M) Devices	Temperature .....	-55°C to +125°C
	Supply Voltage .....	+4.5V to +5.5V

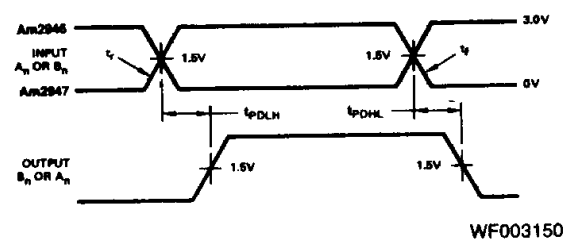
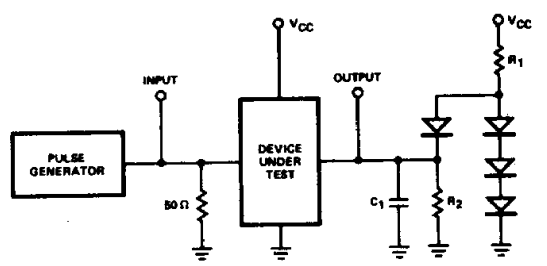
Operating ranges define those limits over which the functionality of the device is guaranteed.

## DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions	Min	Typ (Note 1)	Max	Units	
<b>A PORT (A<sub>0</sub>-A<sub>7</sub>)</b>							
V <sub>IH</sub>	Logical "1" Input Voltage	CD = V <sub>IL</sub> MAX, T/ $\bar{R}$ = 2.0V	2.0			Volts	
V <sub>IL</sub>	Logical "0" Input Voltage	CD = V <sub>IL</sub> MAX T/ $\bar{R}$ = 2.0V	COM'L		0.8	Volts	
			MIL		0.7		
V <sub>OH</sub>	Logical "1" Output Voltage	CD = V <sub>IL</sub> MAX, T/ $\bar{R}$ = 0.8V	I <sub>OH</sub> = -0.4mA	V <sub>CC</sub> - 1.15	V <sub>CC</sub> - 0.7	Volts	
			I <sub>OH</sub> = -3.0mA	2.7	3.95		
V <sub>OL</sub>	Logical "0" Output Voltage	CD = V <sub>IL</sub> MAX, T/ $\bar{R}$ = 0.8V	I <sub>OL</sub> = 12mA		0.3	0.4	Volts
			COM'L I <sub>OL</sub> = 24mA		0.35	0.50	
I <sub>OS</sub>	Output Short Circuit Current	CD = V <sub>IL</sub> MAX, T/ $\bar{R}$ = 0.8V, V <sub>O</sub> = 0V, V <sub>CC</sub> = MAX, Note 2	-10	-38	-75	mA	
I <sub>IH</sub>	Logical "1" Input Current	CD = V <sub>IL</sub> MAX, T/ $\bar{R}$ = 2.0V, V <sub>I</sub> = 2.7V		0.1	80	$\mu$ A	
I <sub>I</sub>	Input Current at Maximum Input Voltage	CD = 2.0V, V <sub>CC</sub> MAX, V <sub>I</sub> = V <sub>CC</sub> MAX			1	mA	
I <sub>IL</sub>	Logical "0" Input Current	CD = V <sub>IL</sub> MAX, T/ $\bar{R}$ = 2.0V, V <sub>I</sub> = 0.4V		-70	-200	$\mu$ A	
V <sub>C</sub>	Input Clamp Voltage	CD = 2.0V, I <sub>IN</sub> = -12mA		-0.7	-1.5	Volts	
I <sub>OD</sub>	Output/Input 3-State Current	CD = 2.0V	V <sub>O</sub> = 0.4V		-200	$\mu$ A	
			V <sub>O</sub> = 4.0V		80		
<b>B PORT (B<sub>0</sub>-B<sub>7</sub>)</b>							
V <sub>IH</sub>	Logical "1" Input Voltage	CD = V <sub>IL</sub> MAX, T/ $\bar{R}$ = V <sub>IL</sub> MAX	2.0			Volts	
V <sub>IL</sub>	Logical "0" Input Voltage	CD = V <sub>IL</sub> MAX, T/ $\bar{R}$ = V <sub>IL</sub> MAX	COM'L		0.8	Volts	
			MIL		0.7		
V <sub>OH</sub>	Logical "1" Output Voltage	CD = V <sub>IL</sub> MAX, T/ $\bar{R}$ = 2.0V	I <sub>OH</sub> = -0.4mA	V <sub>CC</sub> - 1.15	V <sub>CC</sub> - 0.8	Volts	
			I <sub>OH</sub> = -5.0mA	2.7	3.9		
			I <sub>OH</sub> = -10mA	2.4	3.6		
V <sub>OL</sub>	Logical "0" Output Voltage	CD = V <sub>IL</sub> MAX, T/ $\bar{R}$ = 2.0V	I <sub>OL</sub> = 20mA		0.3	0.4	Volts
			I <sub>OL</sub> = 48mA		0.4	0.5	
I <sub>OS</sub>	Output Short Circuit Current	CD = V <sub>IL</sub> MAX, T/ $\bar{R}$ = 2.0V, V <sub>O</sub> = 0V V <sub>CC</sub> = MAX, Note 2	-25	-50	-150	mA	
I <sub>IH</sub>	Logical "1" Input Current	CD = V <sub>IL</sub> MAX, T/ $\bar{R}$ = V <sub>IL</sub> MAX, V <sub>I</sub> = 2.7V		0.1	80	$\mu$ A	
I <sub>I</sub>	Input Current at Minimum Input Voltage	CD = 2.0V, V <sub>CC</sub> = MAX, V <sub>I</sub> = V <sub>CC</sub> MAX			1	mA	
I <sub>IL</sub>	Logical "0" Input Current	CD = V <sub>IL</sub> MAX, T/ $\bar{R}$ = V <sub>IL</sub> MAX, V <sub>I</sub> = 0.4V		-70	-200	$\mu$ A	
V <sub>C</sub>	Input Clamp Voltage	CD = 2.0V, I <sub>IN</sub> = -12mA		-0.7	-1.5	Volts	
I <sub>CO</sub>	Output/Input 3-State Current	CD = 2.0V	V <sub>O</sub> = 0.4V		-200	$\mu$ A	
			V <sub>O</sub> = 4.0V		200		
<b>CONTROL INPUTS CD, T/<math>\bar{R}</math></b>							
V <sub>IH</sub>	Logical "1" Input Voltage		2.0			Volts	
V <sub>IL</sub>	Logical "0" Input Voltage		COM'L		0.8	Volts	
			MIL		0.7		
I <sub>IH</sub>	Logical "1" Input Current	V <sub>I</sub> = 2.7V		0.5	20	$\mu$ A	
I <sub>I</sub>	Input Current at Maximum Input Voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = V <sub>CC</sub> MAX			1.0	mA	
I <sub>IL</sub>	Logical "0" Input Current	V <sub>I</sub> = 0.4V	T/ $\bar{R}$		-0.1	-0.25	mA
			CD		-0.1	-0.25	
V <sub>C</sub>	Input Clamp Voltage	I <sub>IN</sub> = -12mA		-0.8	-1.5	Volts	
<b>POWER SUPPLY CURRENT</b>							
I <sub>CC</sub>	Power Supply Current	Am2946	CD = V <sub>I</sub> = 2.0V, V <sub>CC</sub> = MAX		70	100	mA
			CD = 0.4V, V <sub>INA</sub> = T/ $\bar{R}$ = 2.0V, V <sub>CC</sub> = MAX		100	150	
		Am2947B	CD = 2.0V, V <sub>I</sub> = 0.4V, V <sub>CC</sub> = MAX		70	100	
			CD = V <sub>INA</sub> = 0.4V, T/ $\bar{R}$ = 2.0V, V <sub>CC</sub> = MAX		90	140	

**SWITCHING TEST CIRCUIT**

**SWITCHING TIME WAVEFORM**



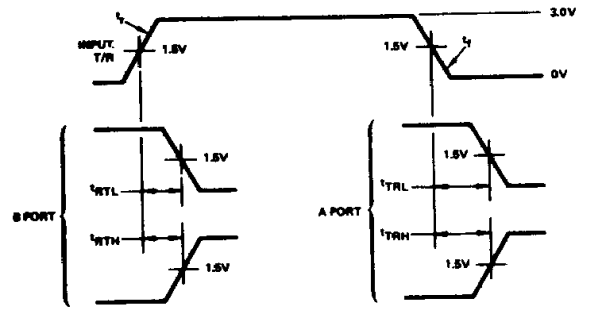
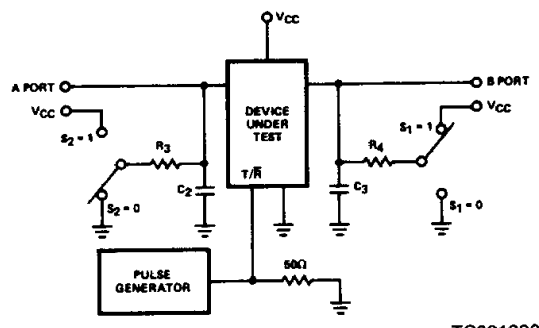
TC001480

WF003150

Note: C<sub>1</sub> includes test fixture capacitance.

$t_r = t_f < 10\text{ns } 10\% \text{ to } 90\%$

**Figure 1. Propagation Delay from A Port to B Port or from B Port to A Port.**



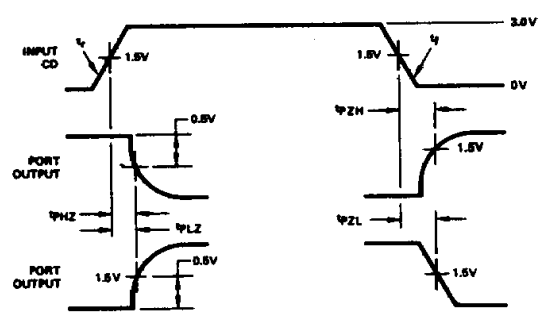
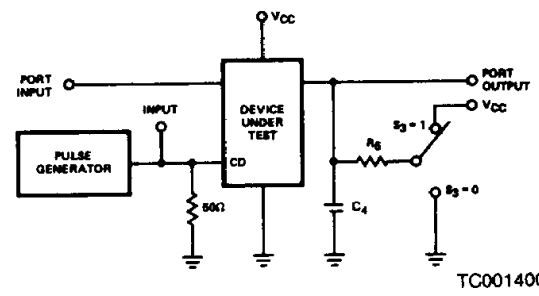
TC001390

WF003110

Note: C<sub>2</sub> and C<sub>3</sub> include test fixture capacitance.

$t_r = t_f < 10\text{ns } 10\% \text{ to } 90\%$

**Figure 2. Propagation Delay from T/R to A Port or B Port.**



TC001400

WF003011

Note: C<sub>4</sub> includes test fixture capacitance. Port input is in a fixed logical condition.

$t_r = t_f < 10\text{ns } 10\% \text{ to } 90\%$

**Figure 3. Propagation Delay from CD to A Port or B Port.**

**SWITCHING CHARACTERISTICS** ( $T_A = +25^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V}$ )  
**Am2946**

Parameter	Description	Test Conditions	Typ (Note 1)	Max	Units
<b>A PORT DATA/MODE SPECIFICATIONS</b>					
$t_{PDHLA}$	Propagation Delay to a Logical "0" from B Port to A Port	$CD = 0.4\text{V}$ , $T/\bar{R} = 0.4\text{V}$ (Figure 1) $R_1 = 1\text{k}$ , $R_2 = 5\text{k}$ , $C_1 = 30\text{pF}$	8	12	ns
$t_{PDLHA}$	Propagation Delay to a Logical "1" from B Port to A Port	$CD = 0.4\text{V}$ , $T/\bar{R} = 0.4\text{V}$ (Figure 1) $R_1 = 1\text{k}$ , $R_2 = 5\text{k}$ , $C_1 = 30\text{pF}$	11	16	ns
$t_{PLZA}$	Propagation Delay from a Logical "0" to 3-State from CD to A Port	$B_0$ to $B_7 = 2.4\text{V}$ , $T/\bar{R} = 0.4\text{V}$ (Figure 3) $S_3 = 1$ , $R_5 = 1\text{k}$ , $C_4 = 15\text{pF}$	10	15	ns
$t_{PHZA}$	Propagation Delay from a Logical "1" to 3-State from CD to A Port	$B_0$ to $B_7 = 0.4\text{V}$ , $T/\bar{R} = 0.4\text{V}$ (Figure 3) $S_3 = 0$ , $R_5 = 1\text{k}$ , $C_4 = 15\text{pF}$	8	15	ns
$t_{PZLA}$	Propagation Delay from 3-State to a Logical "0" from CD to A Port	$B_0$ to $B_7 = 2.4\text{V}$ , $T/\bar{R} = 0.4\text{V}$ (Figure 3) $S_3 = 1$ , $R_5 = 1\text{k}$ , $C_4 = 30\text{pF}$	19	25	ns
$t_{PZHA}$	Propagation Delay from 3-State to a Logical "1" from CD to A Port	$B_0$ to $B_7 = 0.4\text{V}$ , $T/\bar{R} = 0.4\text{V}$ (Figure 3) $S_3 = 0$ , $R_5 = 5\text{k}$ , $C_4 = 30\text{pF}$	19	25	ns
<b>B PORT DATA/MODE SPECIFICATIONS</b>					
$t_{PDHLB}$	Propagation Delay to a Logical "0" from A Port to B Port	$CD = 0.4\text{V}$ , $T/\bar{R} = 2.4\text{V}$ (Figure 1) $R_1 = 100\Omega$ , $R_2 = 1\text{k}$ , $C_1 = 300\text{pF}$	12	18	ns
		$R_1 = 667\Omega$ , $R_2 = 5\text{k}$ , $C_1 = 45\text{pF}$	7	12	ns
$t_{PDLHB}$	Propagation Delay to a Logical "1" from A Port to B Port	$CD = 0.4\text{V}$ , $T/\bar{R} = 2.4\text{V}$ (Figure 1) $R_1 = 100\Omega$ , $R_2 = 1\text{k}$ , $C_1 = 300\text{pF}$	15	20	ns
		$R_1 = 667\Omega$ , $R_2 = 5\text{k}$ , $C_1 = 45\text{pF}$	9	14	ns
$t_{PLZB}$	Propagation Delay from a Logical "0" to 3-State from CD to B Port	$A_0$ to $A_7 = 2.4\text{V}$ , $T/\bar{R} = 2.4\text{V}$ (Figure 3) $S_3 = 1$ , $R_5 = 1\text{k}$ , $C_4 = 15\text{pF}$	13	18	ns
$t_{PHZB}$	Propagation Delay from a Logical "1" to 3-State from CD to B Port	$A_0$ to $A_7 = 0.4\text{V}$ , $T/\bar{R} = 2.4\text{V}$ (Figure 3) $S_3 = 0$ , $R_5 = 1\text{k}$ , $C_4 = 15\text{pF}$	8	15	ns
$t_{PZLB}$	Propagation Delay from 3-State to a Logical "0" from CD to B Port	$A_0$ to $A_7 = 0.4\text{V}$ , $T/\bar{R} = 2.4\text{V}$ (Figure 3) $S_3 = 1$ , $R_5 = 100\Omega$ , $C_4 = 300\text{pF}$	25	35	ns
		$S_3 = 1$ , $R_5 = 667\Omega$ , $C_1 = 45\text{pF}$	16	22	ns
$t_{PZHB}$	Propagation Delay from 3-State to a Logical "1" from CD to B Port	$A_0$ to $A_7 = 0.4\text{V}$ , $T/\bar{R} = 2.4\text{V}$ (Figure 3) $S_3 = 0$ , $R_5 = 1\text{k}$ , $C_4 = 300\text{pF}$	22	35	ns
		$S_3 = 0$ , $R_5 = 5\text{k}$ , $C_1 = 45\text{pF}$	14	22	ns
<b>TRANSMIT RECEIVE MODE SPECIFICATIONS</b>					
$t_{RTL}$	Propagation Delay from Transmit Mode to Receive a Logical "0", $T/\bar{R}$ to A Port	$CD = 0.4\text{V}$ (Figure 2) $S_1 = 1$ , $R_4 = 100\Omega$ , $C_3 = 5\text{pF}$ $S_2 = 1$ , $R_3 = 1\text{k}$ , $C_2 = 30\text{pF}$	23	33	ns
$t_{TRH}$	Propagation Delay from Transmit Mode to Receive a Logical "1", $T/\bar{R}$ to A Port	$CD = 0.4\text{V}$ (Figure 2) $S_1 = 0$ , $R_4 = 100\Omega$ , $C_3 = 5\text{pF}$ $S_2 = 0$ , $R_3 = 5\text{k}$ , $C_2 = 30\text{pF}$	22	33	ns
$t_{RTL}$	Propagation Delay from Transmit Mode to Receive a Logical "0", $T/\bar{R}$ to B Port	$CD = 0.4\text{V}$ (Figure 2) $S_1 = 1$ , $R_4 = 100\Omega$ , $C_3 = 300\text{pF}$ $S_2 = 1$ , $R_3 = 300\Omega$ , $C_2 = 5\text{pF}$	26	35	ns
$t_{TRH}$	Propagation Delay from Transmit Mode to Receive a Logical "1", $T/\bar{R}$ to B Port	$CD = 0.4\text{V}$ (Figure 2) $S_1 = 0$ , $R_4 = 1\text{k}$ , $C_3 = 300\text{pF}$ $S_2 = 0$ , $R_3 = 300\Omega$ , $C_2 = 5\text{pF}$	27	35	ns

Note: 1. All typical values given are for  $V_{CC} = 5.0\text{V}$  and  $T_A = 25^\circ\text{C}$ .  
 2. Only one output at a time should be shorted.

**SWITCHING CHARACTERISTICS** over operating range unless otherwise specified  
Am2946

Parameter	Description	Test Conditions	COMMERCIAL	MILITARY	Units
			Am2946	Am2946	
			Max	Max	
<b>A PORT DATA/MODE SPECIFICATIONS</b>					
t <sub>PDHLA</sub>	Propagation Delay to a Logical "0" from E Port to A Port	CD = 0.4V, T/R = 0.4V (Figure 1) R <sub>1</sub> = 1k, R <sub>2</sub> = 5k, C <sub>1</sub> = 30pF	16	19	ns
t <sub>PDLHA</sub>	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, T/R = 0.4V (Figure 1) R <sub>1</sub> = 1k, R <sub>2</sub> = 5k, C <sub>1</sub> = 30pF	20	23	ns
t <sub>PLZA</sub>	Propagation Delay from a Logical "0" to 3-State from CD to A Port	B <sub>0</sub> to B <sub>7</sub> = 2.4V, T/R = 0.4V (Figure 3) S <sub>3</sub> = 1, R <sub>5</sub> = 1k, C <sub>4</sub> = 15pF	18	21	ns
t <sub>PHZA</sub>	Propagation Delay from a Logical "1" to 3-State from CD to A Port	B <sub>0</sub> to B <sub>7</sub> = 0.4V, T/R = 0.4V (Figure 3) S <sub>3</sub> = 0, R <sub>5</sub> = 1k, C <sub>4</sub> = 15pF	18	21	ns
t <sub>PZLA</sub>	Propagation Delay from 3-State to a Logical "0" from CD to A Port	B <sub>0</sub> to B <sub>7</sub> = 2.4V, T/R = 0.4V (Figure 3) S <sub>3</sub> = 1, R <sub>5</sub> = 1k, C <sub>4</sub> = 30pF	28	33	ns
t <sub>PZHA</sub>	Propagation Delay from 3-State to a Logical "1" from CD to A Port	B <sub>0</sub> to B <sub>7</sub> = 0.4V, T/R = 0.4V (Figure 3) S <sub>3</sub> = 0, R <sub>5</sub> = 5k, C <sub>4</sub> = 30pF	28	33	ns
<b>B PORT DATA/MODE SPECIFICATIONS</b>					
t <sub>PDHLB</sub>	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V, T/R = 2.4V (Figure 1) R <sub>1</sub> = 100Ω, R <sub>2</sub> = 1k, C <sub>1</sub> = 300pF	24	29	ns
		R <sub>1</sub> = 667Ω, R <sub>2</sub> = 5k, C <sub>1</sub> = 45pF	16	19	ns
t <sub>PDLHB</sub>	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4V, T/R = 2.4V (Figure 1) R <sub>1</sub> = 100Ω, R <sub>2</sub> = 1k, C <sub>1</sub> = 300pF	25	30	ns
		R <sub>1</sub> = 367Ω, R <sub>2</sub> = 5k, C <sub>1</sub> = 45pF	19	22	ns
t <sub>PLZB</sub>	Propagation Delay from a Logical "0" to 3-State from CD to B Port	A <sub>0</sub> to A <sub>7</sub> = 2.4V, T/R = 2.4V (Figure 3) S <sub>3</sub> = 1, R <sub>5</sub> = 1k, C <sub>4</sub> = 15pF	23	26	ns
t <sub>PHZB</sub>	Propagation Delay from a Logical "1" to 3-State from CD to B Port	A <sub>0</sub> to A <sub>7</sub> = 0.4V, T/R = 2.4V (Figure 3) S <sub>3</sub> = 0, R <sub>5</sub> = 1k, C <sub>4</sub> = 15pF	18	21	ns
t <sub>PZLB</sub>	Propagation Delay from 3-State to a Logical "0" from CD to B Port	A <sub>0</sub> to A <sub>7</sub> = 2.4V, T/R = 2.4V (Figure 3) S <sub>3</sub> = 1, R <sub>5</sub> = 100Ω, C <sub>4</sub> = 300pF	38	43	ns
		S <sub>3</sub> = 1, R <sub>5</sub> = 667Ω, C <sub>4</sub> = 45pF	26	30	ns
t <sub>PZHB</sub>	Propagation Delay from 3-State to a Logical "1" from CD to B Port	A <sub>0</sub> to A <sub>7</sub> = 0.4V, T/R = 2.4V (Figure 3) S <sub>3</sub> = 0, R <sub>5</sub> = 1k, C <sub>4</sub> = 300pF	38	43	ns
		S <sub>3</sub> = 0, R <sub>5</sub> = 5k, C <sub>4</sub> = 45pF	26	30	ns
<b>TRANSMIT RECEIVE MODE SPECIFICATIONS</b>					
t <sub>TRL</sub>	Propagation Delay from Transmit Mode to Receive a Logical "0", T/R to A Port	CD = 0.4V (Figure 2) S <sub>1</sub> = 1, R <sub>4</sub> = 100Ω, C <sub>3</sub> = 5pF S <sub>2</sub> = 1, R <sub>3</sub> = 1k, C <sub>2</sub> = 30pF	38	43	ns
t <sub>TRH</sub>	Propagation Delay from Transmit Mode to Receive a Logical "1", T/R to A Port	CD = 0.4V (Figure 2) S <sub>1</sub> = 0, R <sub>4</sub> = 100Ω, C <sub>3</sub> = 5pF S <sub>2</sub> = 0, R <sub>3</sub> = 5k, C <sub>2</sub> = 30pF	38	43	ns
t <sub>RTL</sub>	Propagation Delay from Receive Mode to Transmit a Logical "0", T/R to B Port	CD = 0.4V (Figure 2) S <sub>1</sub> = 1, R <sub>4</sub> = 100Ω, C <sub>3</sub> = 300pF S <sub>2</sub> = 1, R <sub>3</sub> = 300Ω, C <sub>2</sub> = 5pF	41	47	ns
t <sub>RTH</sub>	Propagation Delay from Receive Mode to Transmit a Logical "1", T/R to B Port	CD = 0.4V (Figure 2) S <sub>1</sub> = 0, R <sub>4</sub> = 1k, C <sub>3</sub> = 300pF S <sub>2</sub> = 0, R <sub>3</sub> = 300Ω, C <sub>2</sub> = 5pF	41	47	ns

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**SWITCHING CHARACTERISTICS** ( $T_A = +25^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V}$ )  
**Am2947**

Parameter	Description	Test Conditions	Typ (Note 1)	Max	Units
<b>A PORT DATA/MODE SPECIFICATIONS</b>					
$t_{PDHLA}$	Propagation Delay to a Logical "0" from B Port to A Port	$CD = 0.4\text{V}$ , $T/\bar{R} = 0.4\text{V}$ (Figure 1) $R_1 = 1\text{k}$ , $R_2 = 5\text{k}$ , $C_1 = 30\text{pF}$	14	18	ns
$t_{PDLHA}$	Propagation Delay to a Logical "1" from B Port to A Port	$CD = 0.4\text{V}$ , $T/\bar{R} = 0.4\text{V}$ (Figure 1) $R_1 = 1\text{k}$ , $R_2 = 5\text{k}$ , $C_1 = 30\text{pF}$	13	18	ns
$t_{PLZA}$	Propagation Delay from a Logical "0" to 3-State from CD to A Port	$B_0$ to $B_7 = 0.4\text{V}$ , $T/\bar{R} = 0.4\text{V}$ (Figure 3) $S_3 = 1$ , $R_5 = 1\text{k}$ , $C_4 = 15\text{pF}$	11	15	ns
$t_{PHZA}$	Propagation Delay from a Logical "1" to 3-State from CD to A Port	$B_0$ to $B_7 = 2.4\text{V}$ , $T/\bar{R} = 0.4\text{V}$ (Figure 3) $S_3 = 0$ , $R_5 = 1\text{k}$ , $C_4 = 15\text{pF}$	8	15	ns
$t_{PZLA}$	Propagation Delay from 3-State to a Logical "0" from CD to A Port	$B_0$ to $B_7 = 0.4\text{V}$ , $T/\bar{R} = 0.4\text{V}$ (Figure 3) $S_3 = 1$ , $R_5 = 1\text{k}$ , $C_4 = 30\text{pF}$	19	25	ns
$t_{PZHA}$	Propagation Delay from 3-State to a Logical "1" from CD to A Port	$B_0$ to $B_7 = 2.4\text{V}$ , $T/\bar{R} = 0.4\text{V}$ (Figure 3) $S_3 = 0$ , $R_5 = 5\text{k}$ , $C_4 = 30\text{pF}$	19	25	ns
<b>B PORT DATA/MODE SPECIFICATIONS</b>					
$t_{PDHLB}$	Propagation Delay to a Logical "0" from A Port to B Port	$CD = 0.4\text{V}$ , $T/\bar{R} = 2.4\text{V}$ (Figure 1) $R_1 = 100\Omega$ , $R_2 = 1\text{k}$ , $C_1 = 300\text{pF}$	18	23	ns
		$R_1 = 667\Omega$ , $R_2 = 5\text{k}$ , $C_1 = 45\text{pF}$	11	18	ns
$t_{PDLHB}$	Propagation Delay to a Logical "1" from A Port to B Port	$CD = 0.4\text{V}$ , $T/\bar{R} = 2.4\text{V}$ (Figure 1) $R_1 = 100\Omega$ , $R_2 = 1\text{k}$ , $C_1 = 300\text{pF}$	16	23	ns
		$R_1 = 667\Omega$ , $R_2 = 5\text{k}$ , $C_1 = 45\text{pF}$	11	18	ns
$t_{PLZB}$	Propagation Delay from a Logical "0" to 3-State from CD to B Port	$A_0$ to $A_7 = 0.4\text{V}$ , $T/\bar{R} = 2.4\text{V}$ (Figure 3) $S_3 = 1$ , $R_5 = 1\text{k}$ , $C_4 = 15\text{pF}$	13	18	ns
$t_{PHZB}$	Propagation Delay from a Logical "1" to 3-State from CD to B Port	$A_0$ to $A_7 = 2.4\text{V}$ , $T/\bar{R} = 2.4\text{V}$ (Figure 3) $S_3 = 0$ , $R_5 = 1\text{k}$ , $C_4 = 15\text{pF}$	8	15	ns
$t_{PZLB}$	Propagation Delay from 3-State to a Logical "0" from CD to B Port	$A_0$ to $A_7 = 0.4\text{V}$ , $T/\bar{R} = 2.4\text{V}$ (Figure 3) $S_3 = 1$ , $R_5 = 100\Omega$ , $C_4 = 300\text{pF}$	25	35	ns
		$R_3 = 1$ , $R_5 = 667\Omega$ , $C_1 = 45\text{pF}$	16	22	ns
$t_{PZHB}$	Propagation Delay from 3-State to a Logical "1" from CD to B Port	$A_0$ to $A_7 = 2.4\text{V}$ , $T/\bar{R} = 2.4\text{V}$ (Figure 3) $S_3 = 0$ , $R_5 = 1\text{k}$ , $C_4 = 300\text{pF}$	26	35	ns
		$S_3 = 0$ , $R_5 = 5\text{k}$ , $C_1 = 45\text{pF}$	14	22	ns
<b>TRANSMIT RECEIVE MODE SPECIFICATIONS</b>					
$t_{TRL}$	Propagation Delay from Transmit Mode to Receive a Logical "0", $T/\bar{R}$ to A Port	$CD = 0.4\text{V}$ (Figure 2) $S_1 = 1$ , $R_4 = 100\Omega$ , $C_3 = 5\text{pF}$ $S_2 = 1$ , $R_3 = 1\text{k}$ , $C_2 = 30\text{pF}$	28	38	ns
$t_{TRH}$	Propagation Delay from Transmit Mode to Receive a Logical "1", $T/\bar{R}$ to A Port	$CD = 0.4\text{V}$ (Figure 2) $S_1 = 1$ , $R_4 = 100\Omega$ , $C_3 = 5\text{pF}$ $S_2 = 0$ , $R_3 = 5\text{k}$ , $C_2 = 30\text{pF}$	28	38	ns
$t_{RTL}$	Propagation Delay from Transmit Mode to Receive a Logical "0", $T/\bar{R}$ to B Port	$CD = 0.4\text{V}$ (Figure 2) $S_1 = 1$ , $R_4 = 100\Omega$ , $C_3 = 300\text{pF}$ $S_2 = 0$ , $R_3 = 300\Omega$ , $C_2 = 5\text{pF}$	31	40	ns
$t_{RTH}$	Propagation Delay from Transmit Mode to Receive a Logical "1", $T/\bar{R}$ to B Port	$CD = 0.4\text{V}$ (Figure 2) $S_1 = 0$ , $R_4 = 1\text{k}$ , $C_3 = 300\text{pF}$ $S_2 = 1$ , $R_3 = 300\Omega$ , $C_2 = 5\text{pF}$	31	40	ns

Note: 1. All typical values given are for  $V_{CC} = 5.0\text{V}$  and  $T_A = 25^\circ\text{C}$ .  
 2. Only one output at a time should be shorted.



**SWITCHING CHARACTERISTICS** over operating range unless otherwise specified  
**Am2947**

Parameter	Description	Test Conditions	COMMERCIAL Am2947	MILITARY Am2947	Units
			Max	Max	
<b>A PORT DATA/MODE SPECIFICATIONS</b>					
t <sub>PDHLA</sub>	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, T/R = 0.4V (Figure 1) R <sub>1</sub> = 1k, R <sub>2</sub> = 5k, C <sub>1</sub> = 30pF	21	24	ns
t <sub>PDLHA</sub>	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, T/R = 0.4V (Figure 1) R <sub>1</sub> = 1k, R <sub>2</sub> = 5k, C <sub>1</sub> = 30pF	21	24	ns
t <sub>PLZA</sub>	Propagation Delay from a Logical "0" to 3-State from CD to A Port	B <sub>0</sub> to B <sub>7</sub> = 0.4V, T/R = 0.4V (Figure 3) S <sub>3</sub> = 1, R <sub>5</sub> = 1k, C <sub>4</sub> = 15pF	18	21	ns
t <sub>PHZA</sub>	Propagation Delay from a Logical "1" to 3-State from CD to A Port	B <sub>0</sub> to B <sub>7</sub> = 2.4V, T/R = 0.4V (Figure 3) S <sub>3</sub> = 0, R <sub>5</sub> = 1k, C <sub>4</sub> = 15pF	18	21	ns
t <sub>PZLA</sub>	Propagation Delay from 3-State to a Logical "0" from CD to A Port	B <sub>0</sub> to B <sub>7</sub> = 0.4V, T/R = 0.4V (Figure 3) S <sub>3</sub> = 1, R <sub>5</sub> = 1k, C <sub>4</sub> = 30pF	28	33	ns
t <sub>PZHA</sub>	Propagation Delay from 3-State to a Logical "1" from CD to A Port	B <sub>0</sub> to B <sub>7</sub> = 2.4V, T/R = 0.4V (Figure 3) S <sub>3</sub> = 0, R <sub>5</sub> = 5k, C <sub>4</sub> = 30pF	28	33	ns
<b>B PORT DATA/MODE SPECIFICATIONS</b>					
t <sub>PDHLB</sub>	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V, T/R = 2.4V (Figure 1)	28	34	ns
		R <sub>1</sub> = 100Ω, R <sub>2</sub> = 1k, C <sub>1</sub> = 300pF			
		R <sub>1</sub> = 667Ω, R <sub>2</sub> = 5k, C <sub>1</sub> = 45pF	22	25	ns
t <sub>PDLHB</sub>	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4V, T/R = 2.4V (Figure 1)	28	34	ns
		R <sub>1</sub> = 100Ω, R <sub>2</sub> = 1k, C <sub>1</sub> = 300pF			
		R <sub>1</sub> = 667Ω, R <sub>2</sub> = 5k, C <sub>1</sub> = 45pF	22	25	ns
t <sub>PLZB</sub>	Propagation Delay from a Logical "0" to 3-State from CD to B Port	A <sub>0</sub> to A <sub>7</sub> = 0.4V, T/R = 2.4V (Figure 3) S <sub>3</sub> = 1, R <sub>5</sub> = 1k, C <sub>4</sub> = 15pF	23	26	ns
t <sub>PHZB</sub>	Propagation Delay from a Logical "1" to 3-State from CD to B Port	A <sub>0</sub> to A <sub>7</sub> = 2.4V, T/R = 2.4V (Figure 3) S <sub>3</sub> = 0, R <sub>5</sub> = 1k, C <sub>4</sub> = 15pF	18	21	ns
t <sub>PZLB</sub>	Propagation Delay from 3-State to a Logical "0" from CD to B Port	A <sub>0</sub> to A <sub>7</sub> = 0.4V, T/R = 2.4V (Figure 3)	38	43	ns
		S <sub>3</sub> = 1, R <sub>5</sub> = 100Ω, C <sub>4</sub> = 300pF			
		S <sub>3</sub> = 1, R <sub>5</sub> = 667Ω, C <sub>4</sub> = 45pF	26	30	ns
t <sub>PZHB</sub>	Propagation Delay from 3-State to a Logical "1" from CD to B Port	A <sub>0</sub> to A <sub>7</sub> = 2.4V, T/R = 2.4V (Figure 3)	38	43	ns
		S <sub>3</sub> = 0, R <sub>5</sub> = 1k, C <sub>4</sub> = 300pF			
		S <sub>3</sub> = 0, R <sub>5</sub> = 5k, C <sub>4</sub> = 45pF	26	30	ns
<b>TRANSMIT RECEIVE MODE SPECIFICATIONS</b>					
t <sub>TRL</sub>	Propagation Delay from Transmit Mode to Receive a Logical "0", T/R to A Port	CD = 0.4V (Figure 2) S <sub>1</sub> = 0, R <sub>4</sub> = 100Ω, C <sub>3</sub> = 5pF S <sub>2</sub> = 1, R <sub>3</sub> = 1k, C <sub>2</sub> = 30pF	42	48	ns
t <sub>TRH</sub>	Propagation Delay from Transmit Mode to Receive a Logical "1", T/R to A Port	CD = 0.4V (Figure 2) S <sub>1</sub> = 1, R <sub>4</sub> = 100Ω, C <sub>3</sub> = 5pF S <sub>2</sub> = 0, R <sub>3</sub> = 5k, C <sub>2</sub> = 30pF	42	48	ns
t <sub>RTL</sub>	Propagation Delay from Receive Mode to Transmit a Logical "0", T/R to B Port	CD = 0.4V (Figure 2) S <sub>1</sub> = 1, R <sub>4</sub> = 100Ω, C <sub>3</sub> = 300pF S <sub>2</sub> = 1, R <sub>3</sub> = 300Ω, C <sub>2</sub> = 5pF	45	51	ns
t <sub>RTH</sub>	Propagation Delay from Receive Mode to Transmit a Logical "1", T/R to B Port	CD = 0.4V (Figure 2) S <sub>1</sub> = 0, R <sub>4</sub> = 1k, C <sub>3</sub> = 300pF S <sub>2</sub> = 1, R <sub>3</sub> = 300Ω, C <sub>2</sub> = 5pF	45	51	ns