Two-Phase DC/DC Controller for CPU Core Power Supply

General Description

The RT9241 is a two-phase buck DC/DC controller integrated with all control functions for high performance processor VRM. The RT9241 drives 2 buck switching stages operating in 180 degree phase shift. The two-phase architecture provides high output current while maintaining low power dissipation on power devices and low stress on input and output capacitors. The high equivalent operating frequency also reduces the component dimension and the output voltage ripple in load transient.

RT9241 regulates both easily set voltage and current loops. Precise current sharing for power stage is achieved by differential input current sense and processing circuit. The settings of current sense, droop tuning and over current protection are independent to compensation circuit of voltage loop. The feature greatly facilitates the flexibility of CPU power supply design and tuning.

The RT9241 uses a 5-bit DAC of 1.1V to 1.85V (25mV/step) output with load current droop compensation to meet the strict VRM transient requirement. The IC monitors the VCORE voltage for PGOOD and over voltage protection. Soft start, over current protection and programmable under voltage lockout are also provided to assure the safety of microprocessor and power system.

Ordering Information

RT9241□ □

- Package Type
  S : SOP-20
- Operating temperature range
  C: Commercial standard

Features

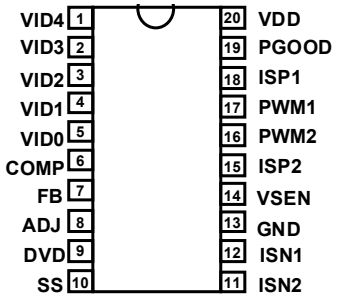
- **Two-Phase Power Conversion**
- **VRM 9.0 DAC Output with Active Droop Compensation for Fast Load Transient**
- **Precise Channel Current Sharing with Differential Sense Input**
- **Hiccup Mode Over Current Protection**
- **Programmable Under Voltage Lockout and Soft Start**
- **High Ripple Frequency, (Channel Frequency 200KHz) Times Channel Number**

Applications

- Power Supply for Server and Workstation
- Power Supply for High Current Microprocessor

Pin Configurations

Part Number	Pin Configurations
RT9241CS (Plastic SOP-20)	TOP VIEW



Absolute Maximum Ratings

- Supply Voltage 6V
- Input, Output or I/O Voltage ..... GND-0.3V ~ VDD+0.3V
- Ambient Temperature Range ..... 0°C ~ 70°C
- Operating Junction Temperature Range ..... 0°C ~ 125°C
- Storage Temperature Range ..... -65°C ~ 150°C
- Power Dissipation, P_D @ T_A = 25°C
  SOP-20 ..... 0.625W
- Package Thermal Resistance
  SOP-20, θ_{JA} ..... 60°C /W
- Lead Temperature (Soldering, 10 sec.) ..... 260°C

Electrical Characteristics

(V_{DD} = 5V, GND = 0V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
V_{DD} Supply Current						
Nominal Supply Current	I_{DD}	PWM 1,2 Open	--	6	--	mA
Power-On Reset						
V_{DD} Rising Threshold			4.2	4.35	4.5	V
V_{DD} Falling Threshold			3.7	3.85	4	V
VDVD Rising Trip Threshold			1.19	1.25	1.31	V
Oscillator						
Frequency		For each phase	170	200	230	kHz
Ramp Amplitude			--	1	--	V
Ramp Valley			1.0	1.3	--	V
Maximum On Time of Each Channel			--	75	--	%
Reference and DAC						
DACOUT Voltage Accuracy			-1.0	--	+1.0	%
DAC (VID0-VID4) Input Low Voltage			--	--	0.8	V
DAC (VID0-VID4) Input High Voltage			2.0	--	--	V
DAC (VID0-VID4) Bias Current			10	20	40	µA
PWM Controller Error Amplifier						
DC Gain			--	85	--	dB
Bandwidth			--	10	--	MHz
Slew Rate		C_L = 10pF	--	5	--	V/µS
Current Sense GM Amplifier						
ISP 1,2 Full Scale Source Current			--	50	--	µA
ISP 1,2 Current for OCP			--	75	--	µA

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Protection						
SS Current		V_{SS} = 1V	--	10	--	μA
Over-Voltage Trip (VSEN/DACOUT)			116	120	124	%
Power Good						
Upper Threshold (VSEN/DACOUT)		VSEN Rising	--	108	--	%
Lower Threshold (VSEN/DACOUT)		VSEN Rising	--	92	--	%

Function Block Diagram

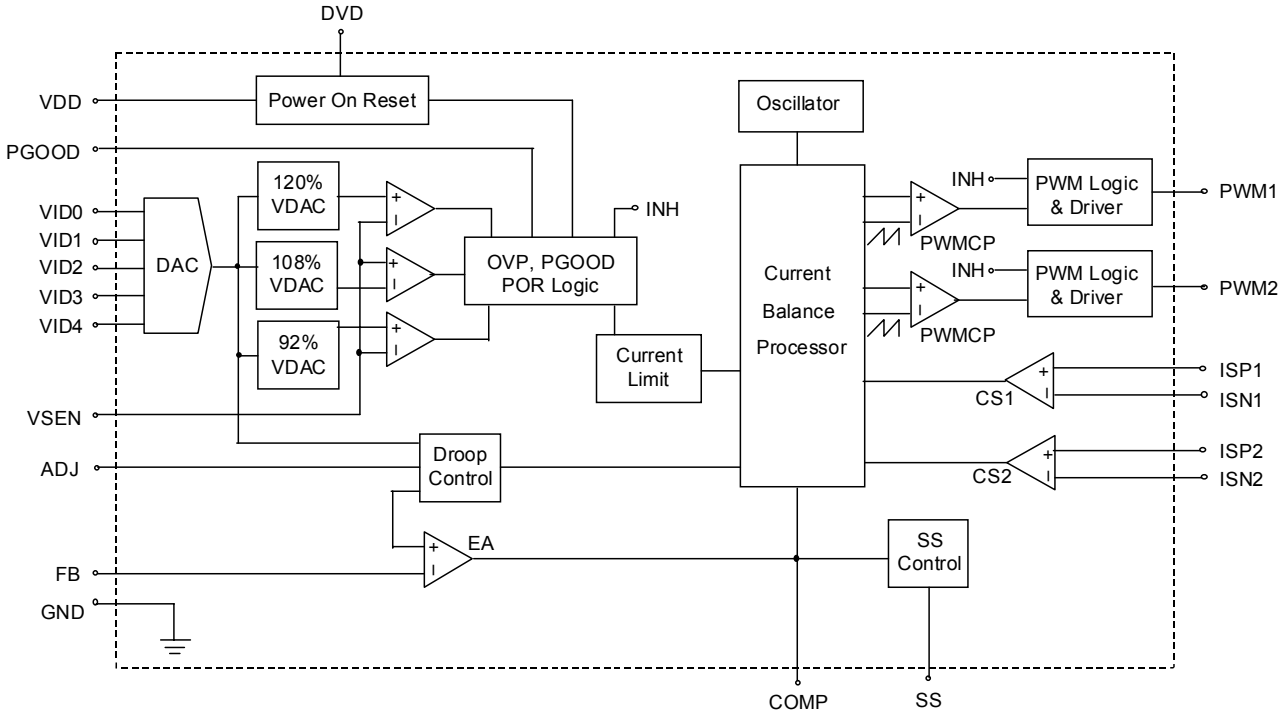
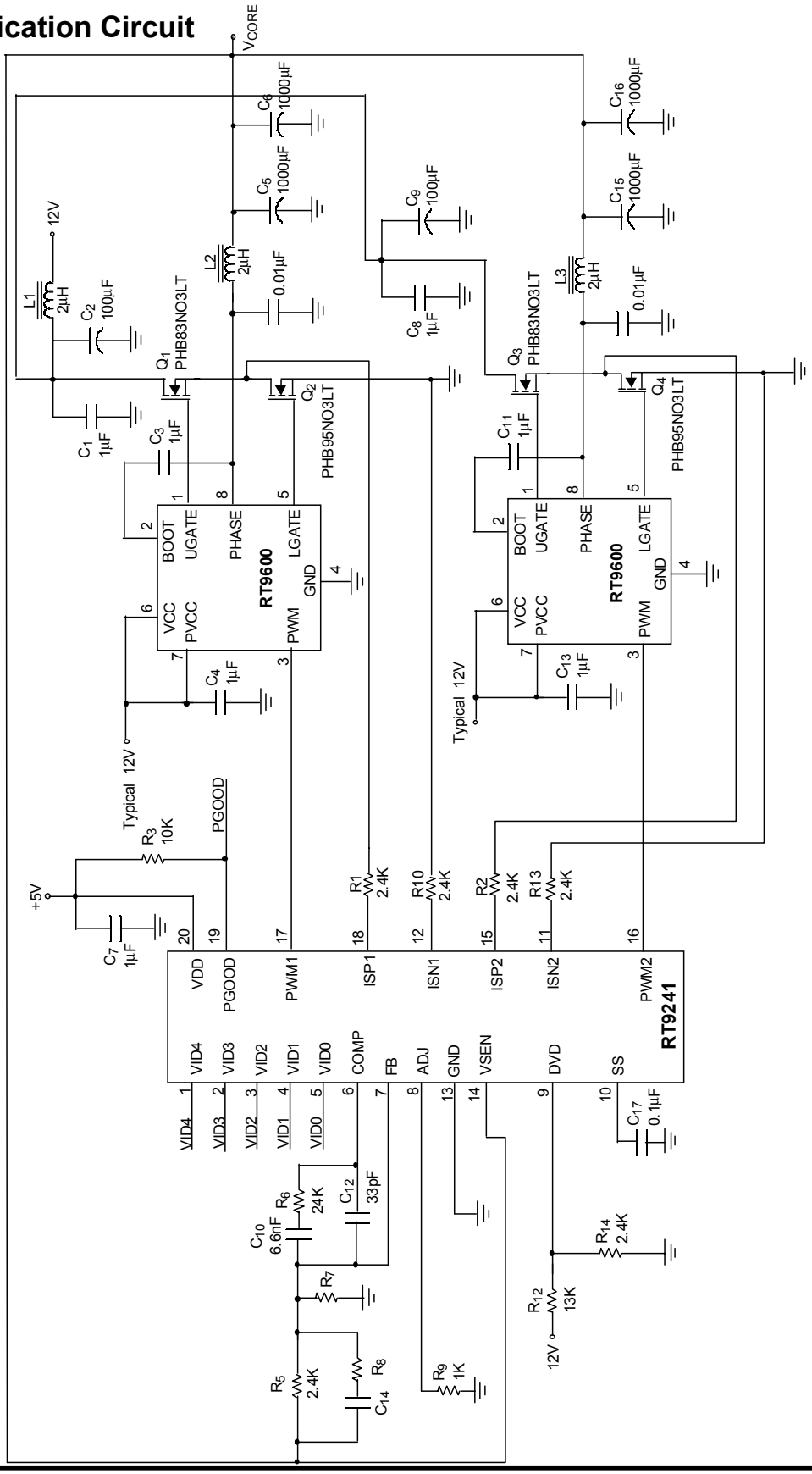


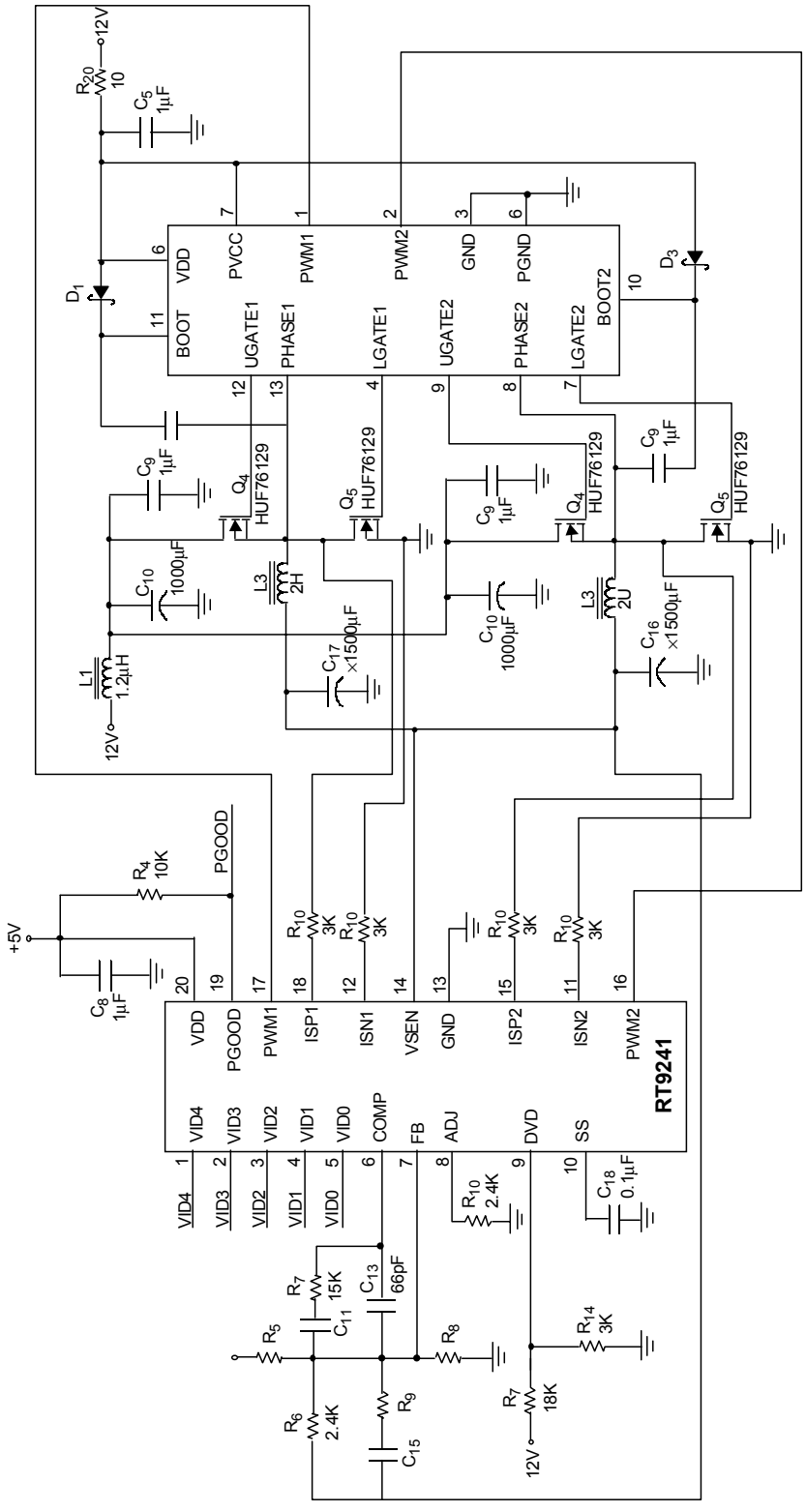
Table 1 Output Voltage Program

Pin Name					Nominal Output Voltage DACOUT
VID4	VID3	VID2	VID1	VID0	
1	1	1	1	1	Off
1	1	1	1	0	1.100V
1	1	1	0	1	1.125V
1	1	1	0	0	1.150V
1	1	0	1	1	1.175V
1	1	0	1	0	1.200V
1	1	0	0	1	1.225V
1	1	0	0	0	1.250V
1	0	1	1	1	1.275V
1	0	1	1	0	1.300V
1	0	1	0	1	1.325V
1	0	1	0	0	1.350V
1	0	0	1	1	1.375V
1	0	0	1	0	1.400V
1	0	0	0	1	1.425V
1	0	0	0	0	1.450V
0	1	1	1	1	1.475V
0	1	1	1	0	1.500V
0	1	1	0	1	1.525V
0	1	1	0	0	1.550V
0	1	0	1	1	1.575V
0	1	0	1	0	1.600V
0	1	0	0	1	1.625V
0	1	0	0	0	1.650V
0	0	1	1	1	1.675V
0	0	1	1	0	1.700V
0	0	1	0	1	1.725V
0	0	1	0	0	1.750V
0	0	0	1	1	1.775V
0	0	0	1	0	1.800V
0	0	0	0	1	1.825V
0	0	0	0	0	1.850V

Note: (1) 0:Connected to GND (2) 1:Open

Typical Application Circuit





Functional Pin Description

VID4, VID3, VID2, VID1 and VID0 (Pin1,2,3,4,5)

DAC voltage identification inputs for VRM9.0. These pins are TTL-compatible and internally pulled to VDD if left open.

COMP (Pin 6)

Output of the error amplifier and input of the PWM comparator.

FB (Pin 7)

Inverting input of the internal error amplifier.

ADJ (Pin 8)

Current sense output for active droop adjust. Connect a resistor from this pin to GND to set the amount of load droop.

DVD (Pin 9)

Programmable power UVLO detection input. Trip threshold = 1.25V at V(DVD) rising

SS (Pin 10)

Connect this SS pin to GND with a capacitor to set the start time interval. Pull this pin below 1V(ramp valley of saw-tooth wave in pulse width modulator) to shutdown the converter output.

ISEN1 (Pin 12), ISEN2 (Pin 11)

Current sense inputs from the individual converter channel's sense component GND nodes.

GND (Pin 13)

Ground for the IC.

VSEN (Pin 14)

Power good and over voltage monitor input. Connect to the microprocessor-CORE voltage.

ISP1 (Pin 18), ISEN2 (Pin 15)

Current sense inputs for individual converter channels. Tie this pin to the component sense node.

PWM1 (Pin 17), PWM2 (Pin 16)

PWM outputs for each driven channel. Connect these pins to the PWM input of the MOSFET driver.

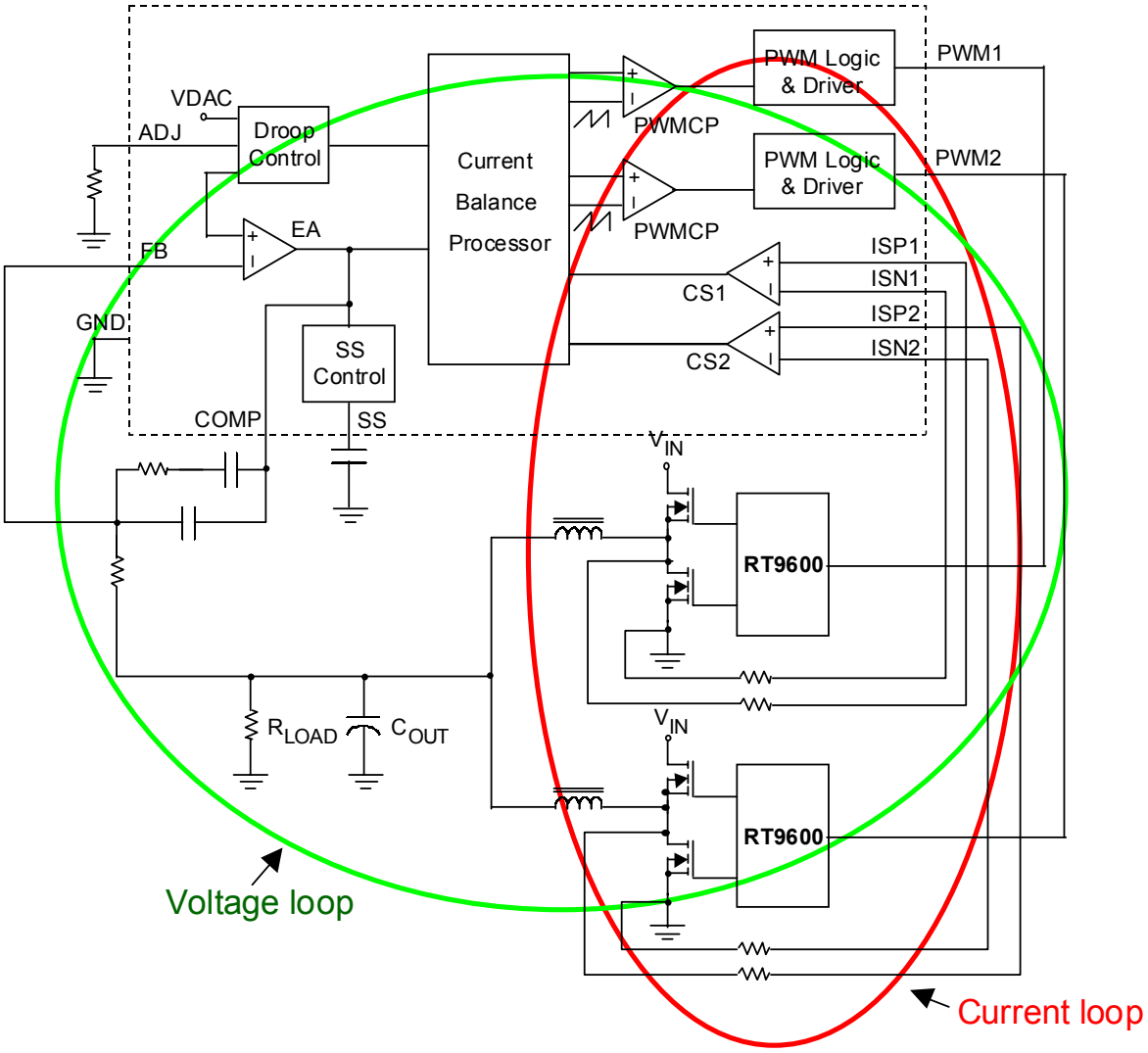
PGOOD (Pin 19)

Power good open-drain output.

VDD (Pin 20)

IC power supply. Connect this pin to a 5V supply.

Simplified Block Diagram Control Loops for a Two Phase Converter



Operation

RT9241 is a two-phase DC/DC controller that precisely regulates CPU core voltage and balances the current of different power channels. The converter consists of RT9241 and its companion MOSFET driver provide high quality CPU power and all protection function to meet the requirement of modern VRM.

Voltage control

The reference of V_{CORE} is provided by a 5-bit DAC of VRM9.0 specification. Control loop consists of error amplifier, two-phase pulse width modulator, driver and power components. Like conventional voltage mode PWM controller, the output voltage is locked at the VREF of error amplifier and the error signal is used as the control signal VC of pulse width modulator. The PWM signals of different channels are generated by comparison of EA output and spilt-phase saw-tooth wave. Power stage transforms V_{IN} to output by PWM signal on-time ratio.

Current balance

RT9241 senses the current of low side MOSFET in each synchronous rectifier when it is conducting for channel current balance and droop tuning. The differential sensing GM amplifier converts the voltage on the sense component (can be a sense resistor or the $R_{DS(ON)}$ of the low side MOSFET) to current signal into internal balance circuit. The current balance circuit sums and averages the current signals then produces the balancing signals injected to pulse width modulator. If the current of some power channel is greater than average, the balancing signal reduces the output pulse width to keep the balance.

Load Droop

The sensed power channel current signals regulate the reference of DAC to form a output voltage droop proportional to the load current. The droop or so call “active voltage positioning” can reduce the output voltage ripple at load transient and the LC filter size.

Fault detection

The chip detects V_{CORE} for over voltage and power good detection. The “hiccup mode” operation of over current protection is adopted to reduce the short circuit current. The in-rush current at the start up is suppressed by the soft start circuit through clamping the pulse width and output voltage.

Application Circuit setting

MOSFET driver detection and converter start up

RT9241 interface with companion MOSFET driver (like RT9600 or HIP660X series) for correct converter initialization. The tri-phase PWM output (high, low, high impedance) pins sense the interface voltage at IC POR acts (both VDD and DVD trip). The channel is enabled if the pin voltage is 1.2V less than VDD. Please tie the both PWM output to driver input for correct converter start-up.

Current sensing setting

RT9241 senses the current of low side MOSFET in each synchronous rectifier when it is conducting for channel current balance and droop tuning. The differential sensing GM amplifier converts the voltage on the sense component (can be a sense resistor or the $R_{DS(ON)}$ of the low side MOSFET) to current signal into internal circuit (see Fig.1).

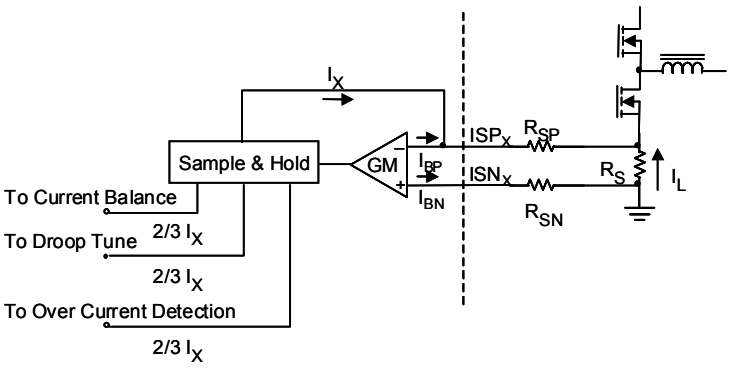


Fig.1 Current Sense Circuit

The sensing circuit gets $I_X = \frac{I_L \times R_S}{R_{SP}}$ by local feedback. $R_{SP} = R_{SN}$ to cancel the voltage drop caused by GM amplifier input bias current. I_X is sampled and held just before low side MOSFET turns off (See Fig.2). Therefore,

$$I_{X(S/H)} = \frac{I_{L(S/H)} \times R_S}{R_{SP}}, \quad I_{L(S/H)} = I_{L(AVG)} - \frac{V_O}{L} \times \frac{T_{OFF}}{2},$$

$$T_{OFF} = \left(\frac{V_{IN} - V_O}{V_{IN}}\right) \times 5\mu S, \text{ for operating frequency = 200kHz}$$

$$I_{X(S/H)} = \left[I_{L(AVG)} - \frac{V_O - \left(\frac{V_{IN} - V_O}{V_{IN}}\right) \times 5\mu S}{2L} \right] \times \frac{R_S}{R_{SP}}$$

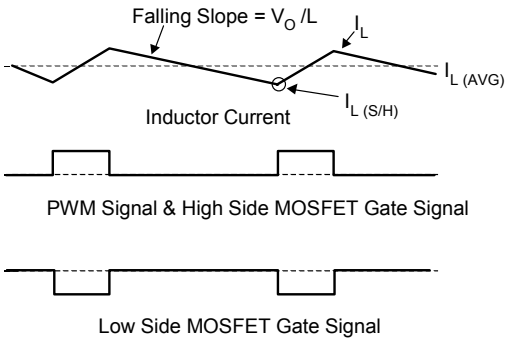


Fig. 2 Inductor Current and PWM Signal

Droop Tuning

The S/H current signals from power channels are injected to ADJ pin to create droop voltage.

$$V_{ADJ} = R_{ADJ} \times \frac{2}{3} \sum I_X$$

The DAC output voltage decreases by V_{ADJ} to form the VCORE load droop(see Fig.3).

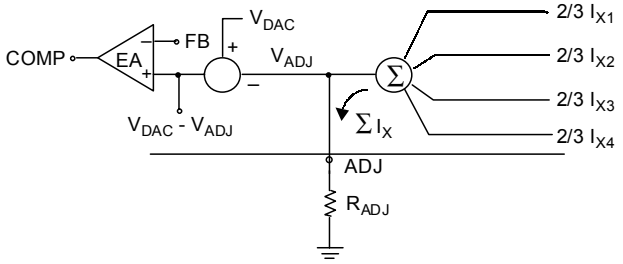


Fig. 3 Droop Tune Circuit

Protection and SS function

For OVP, the RT9241 detects the V_{CORE} by V_{SEN} pin. Eliminate the parasitic delay and noise influence on the PCB path for fast and accurate detection. The trip point of OVP is 120% of normal output level. The PWM outputs are pulled low to turn on the low side MOSFET and turn off the high side MOSFET of the synchronous rectifier at OVP. The OVP latch can only be reset by VDD or DVD restart power on reset sequence. The PGOOD detection trip point of V_{CORE} is ±8% out of the normal level. The PGOOD open drain output pulls low when V_{OCRE} exceeds the range.

Soft start circuit generates a ramp voltage by charging external capacitor with 10uA current after IC POR acts. The PWM pulse width and V_{CORE} are clamped by the rising ramp to reduce the in-rush current and protect the power devices.

Over current protection trip point is set by the resistor R_{IMAX} connected to IMAX pin. OCP is triggered if one channel S/H current signal $I_X > \frac{3}{2} \times \frac{0.6}{R_{IMAX}}$. Controller forces PWM output latched at high impedance to turn off both high and low side MOSFET in the power stage and initial the hiccup mode protection. The SS pin voltage is pulled low with a 10μA current after it is less than 90% VDD. The converter restarts after SS pin voltage < 0.2V. Three times of OCP disable the converter and only release the latch by POR acts (see Fig.4).

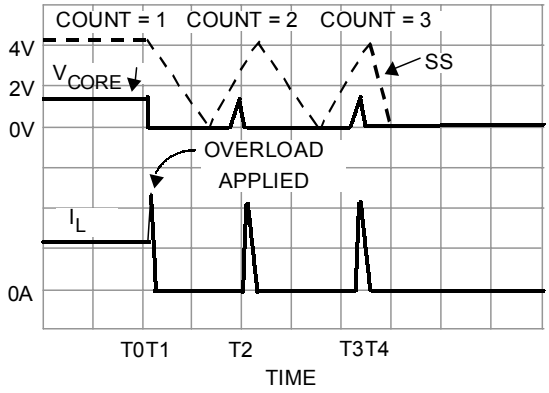
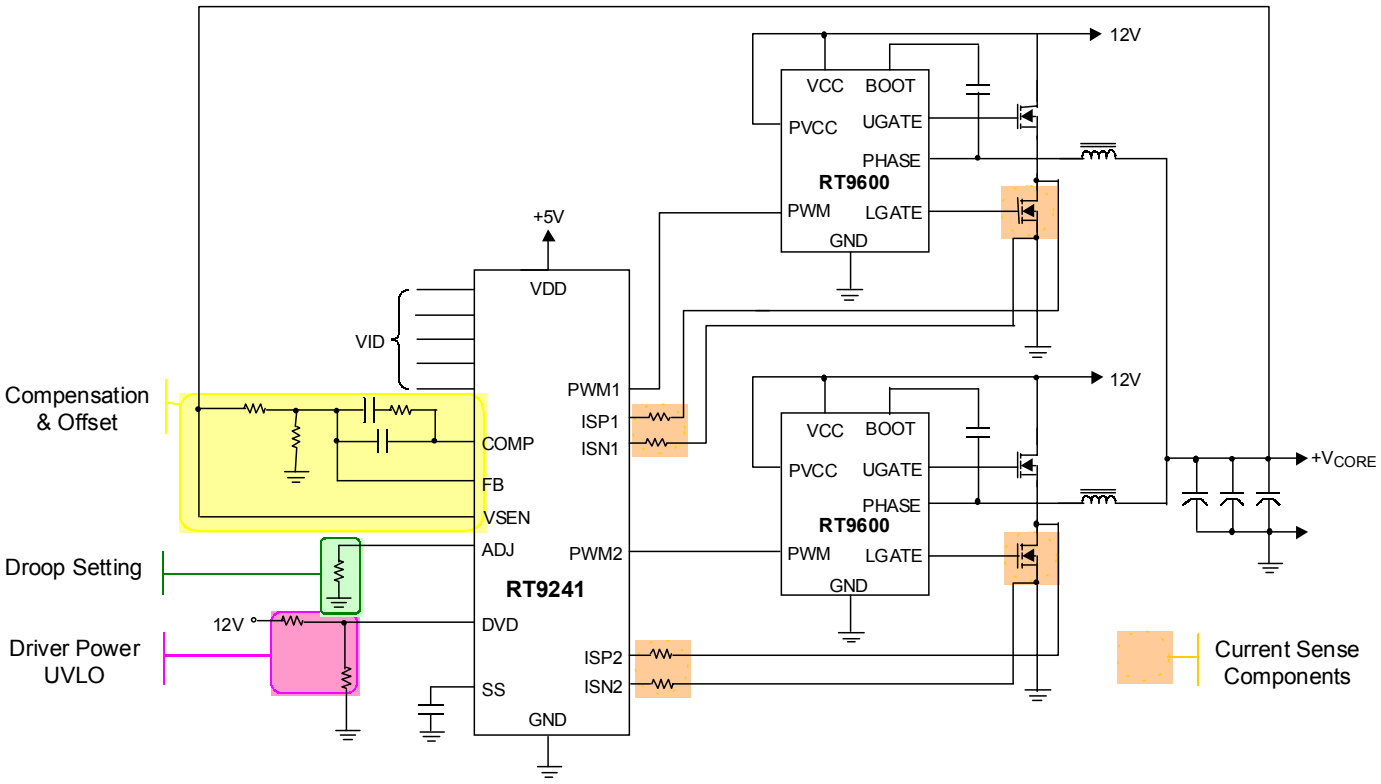
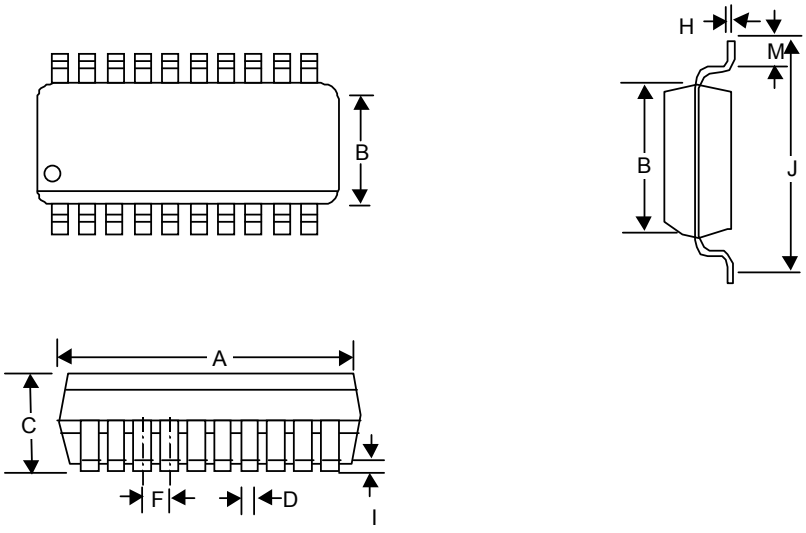


Fig. 4

Two-Phase Converter and Components Function Grouping



Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	12.598	13.005	0.496	0.512
B	7.391	7.595	0.291	0.299
C	2.362	2.642	0.093	0.104
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.229	0.330	0.009	0.013
I	0.102	0.305	0.004	0.012
J	10.008	10.643	0.394	0.419
M	0.381	1.270	0.015	0.050

20–Lead SOP Plastic Package

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