Monolithic Multiplier/Detector

GENERAL DESCRIPTION

The XR-2228 is a monolithic multiplier/detector circuit especially designed for interfacing with integrated phase-locked loop (PLL) circuits, to perform synchronous AM detection and triangle-to-sinewave conversion. It combines a four-quadrant analog multiplier (or modulator) and a high-gain operational amplifier in a single monolithic circuit.

As shown in the equivalent schematic diagram, the four-quadrant multiplier section is designed with fully differential X- and Y-inputs and differential outputs. For maximum versatility, the multiplier and the operational amplifier sections are not internally connected. The operational amplifier can also function as a pre-amplifier for low-level input signals, or as a post-detection amplifier for synchronous demodulation, phase-detection or for sine-shaper applications.

FEATURES

Independent Multiplier and Op Amp Sections
Differential X and Y Inputs
Interfaces with all PLL and VCO Circuits
Wide Common Mode Range
Wide Transconductance Bandwidth (100MHz, Typ.)
Wide Supply Voltage Range (±4.5V to ±16V)

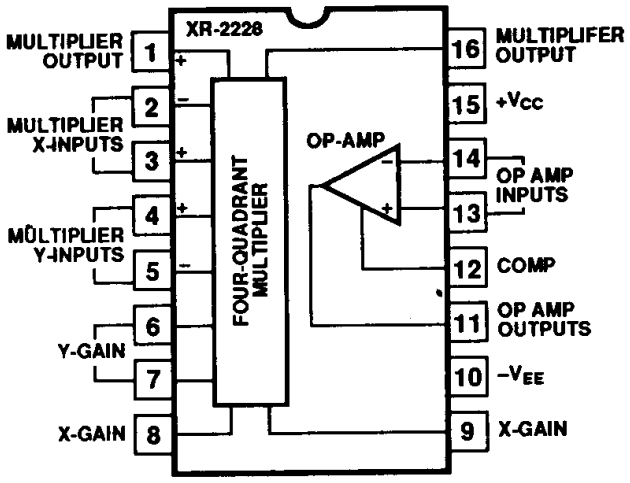
APPLICATIONS

Phase-Locked Loop Design
Phase Detection
Synchronous AM Detection
AM Generation
Triangle-to-Sinewave Conversion
Frequency Translation

ABSOLUTE MAXIMUM RATINGS

Power Supply	±18 Volts
Power Dissipation	
Ceramic Package	750mW
Derate above +25°C	6mW/°C
Plastic Package	625mW
Derate above +25°C	5mW/°C
Storage Temperature Range	–65°C to +150°C

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2228CN	Ceramic	0°C to + 70°C
XR-2228CP	Plastic	0°C to + 70°C

SYSTEM DESCRIPTION

The XR-2228 multiplier/detector contains a four quadrant multiplier and a fully independent operational amplifier. The four quadrant multiplier has fully differential X and Y inputs and outputs. Both inputs have 3MHz dynamic response and 100MHz transconductance band- width. The operational amplifier features high gain and a large common mode range. The device is powered by 4.5V to 16V split supplies.

For higher frequency applications, consider the XR- 2208.

ELECTRICAL CHARACTERISTICS

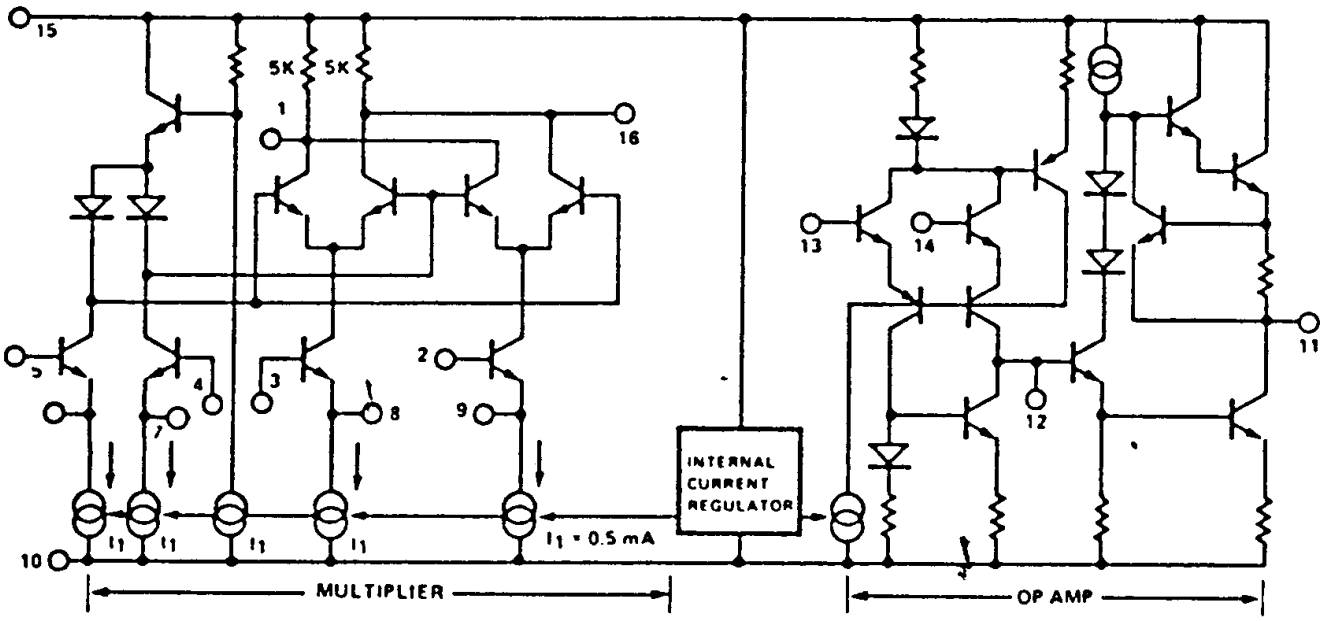
Test Conditions: Supply Voltage = ±15V. T_A = 25°C, unless otherwise specified.

PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	FIGURE	CONDITIONS
I. GENERAL						
Supply Voltage	±4.5		±16	V dc		See Figure 11
Supply Current		5	8	mA	1	Measured at Pin 15
II. MULTIPLIER/MODULATOR SECTION						
Non-linearity						No external offset trim
(Output Error in % of Full Scale)		0.5	1.0	%	2	V_y = ±10V, −10V < V_x < +10V
		0.5	1.0	%		Vx = ±10V, −10V < V_y < +10V
		0.8		%		$T_{LOW} \le T_A \le T_{HIGH}$ (Note 1)
						f = 50Hz
Feedthrough						
a. With Offset Adj.						
X-input		70	120	mVp-p	3	V_x = 20 Vp-p V_y = 0
Y-input		90	150	mVp-p		V_y = 20 Vp-p, V_x = 0
b. No Offset Adj.						
X-input		200		mVp-p		V_x = 20 Vp-p, V_x = 0
Y-input		200		mVp-p		V_y = 20 Vp-p, V_x = 0
Temperature Coefficient of Scale Factor		±0.07		%/°C		$T_{LOW} \le T_A \le T_{HIGH}$ (Note 1)
Input Bias Current						
X or Y inputs		3	8	µA	1	Measured at Pins 2, 3, 4 or 5.
Input Resistance		1.0		MΩ	2	Measured at Pins 2, 3, 4 or 5.
Output Offset Voltage		80	140	mV	2	Measured across Pins 1 and 16
Avg. Temp. Drift		0.5		mV/°C		$T_{LOW} \le T_A \le T_{HIGH}$
Dynamic Response					4	See definition section, and Note 1
3-dB Bandwidth						
X-input	1	3		MHz		
Y-input	1	3		MHz		
3° Phase-Shift Bandwidth		1		MHz		
1% Absolute Error Bandwidth		30		kHz		
Transconductance Bandwidth		100		MHz		
Output Impedance		5		kΩ		Measured looking into Pins 1or 16
III. OPERATIONAL AMPLIFIER SECTION						
Input Offset Voltage		2	6	mV	5	R_S < 50Ω
Temp. Coef. of Input Offset Voltage		9	30	µV/°C		$T_{LOW} \le T_A \le T_{HIGH}$ (Note 1)
Input Offset Current		10	100	nA	5	$I_{B1} - I_{B2}$
Input Bias Current		50	300	nA	5	$\frac{I_{B1} + I_{B2}}{2}$
Voltage Gain	70	75		dB	5	$R_L \ge 2K$, V_o = ±10V, f = 20Hz
Differential Input Resistance		3		MΩ	5	
Output Voltage Swing	±10	±12		V		$R_L \ge 2K$, $T_{LOW} \le T_A \le T_{HIGH}$
Input Common Mode	+12	+14				
Range	−10	−12		V	5	
Common Mode Rejection	70	90		dB	5	f = 20Hz
Output Resistance		2		kΩ	5	
Slew Rate		0.5		V/µs	5	Gain = 1, $R_L \ge 2K$, $C_L \le 100pF$, C_C = 20pF
Power Supply Sensitivity		30		µV/V	5	$R_S \le 10K$

Note 1: T_{LOW} = 0°C, T_{HIGH} = +70°C for XR-2228C; not tested in production

CAUTION: *When using only the op amp or only the multiplier section of the XR-2228, the input terminals to the unused section must be grounded. Thus, when using the multiplier section alone, ground pins 13 and 14; when using the op amp section alone, ground pins 2, 3, 4 and 5.*

EQUIVALENT SCHEMATIC DIAGRAM



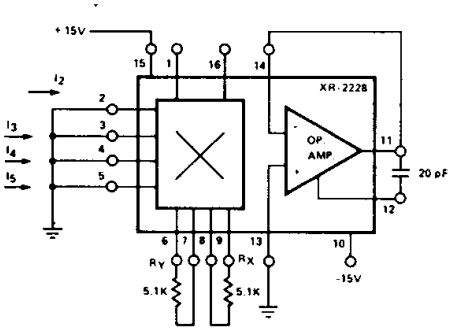


Figure 1. Test Circuit for Quiescent Supply Current, Multiplier Input Bias and Output Offset Voltage

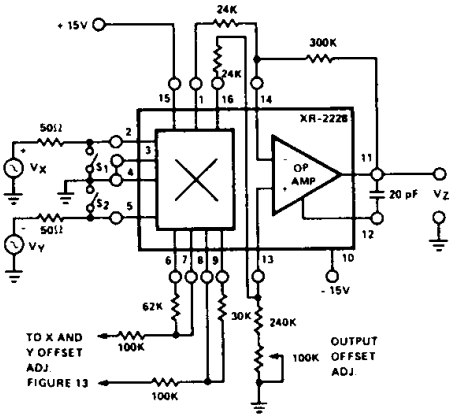


Figure 3. Test Circuit for Feedthrough Measurement. X-Input Feedthrough = V_Z with S_1, open S_2 closed. Y-Input Feedthrough = V_Z with S_1 closed, S_2 open.

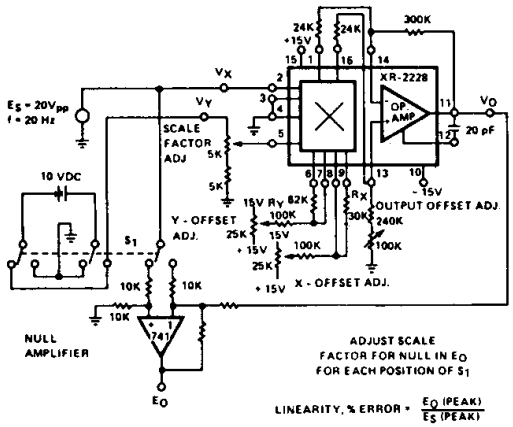


Figure 2. Linearity Test Circuit

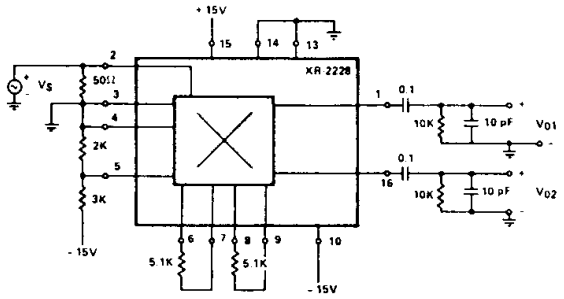


Figure 4. Test Circuit for Multiplier Small-Signal Bandwidth for X-Input (For Y-Input, reverse connections between Pins 2 and 5)

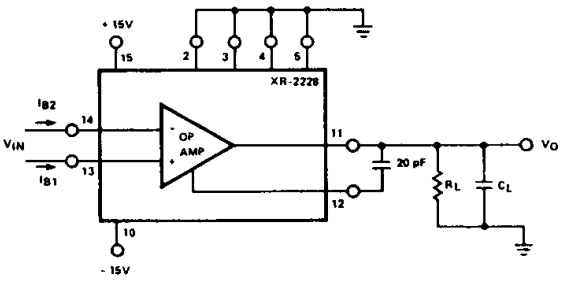


Figure 5. Test Circuit for Op Amp DC Parameters

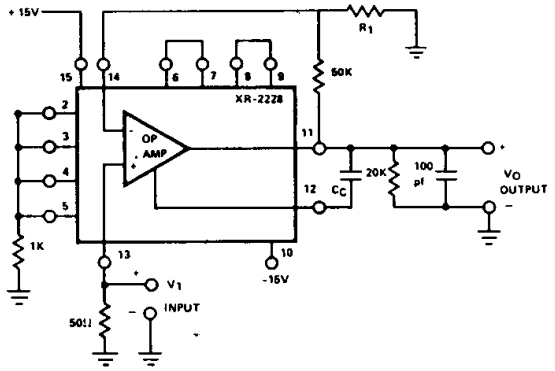


Figure 6. Op Amp AC Test Circuit

DEFINITION OF MULTIPLIER TERMS

NONLINEARITY: Nonlinearity is the maximum deviation of the output voltage from a straight-line transfer function. It is measured separately for the X and Y inputs and is specified as (%) of full scale output.

FEEDTHROUGH: The amount of peak-to-peak output voltage present with one input grounded and a specified peak-to-peak input applied to the other input. Feedthrough is a function of multiplier offsets and can be minimized by offset adjustment (see Figure 13).

OFFSET VOLTAGES: A four-quadrant analog multiplier has three separate offsets: the X and Y input offsets and the output offset. The transfer function of a practical multiplier with scale factor K can be written as:

$$V_Z = K[(V_x + \varnothing_x)(V_y + \varnothing_y)] + \varnothing_0$$

where $\varnothing_x$ and $\varnothing_y$ are the offset voltages associated with the respective inputs, $\varnothing_0$ is the offset voltage of the output. V_Z is the multiplier output, V_x and V_y are the multiplier inputs. As shown in Figures 13 and 14, each of these offset voltages can be nulled to zero by external adjustments.

SCALE FACTOR, K: The constant of proportionality that relates the multiplier output to the X and Y inputs. If the offset terms are neglected, the multiplier output, V_Z, is related to the X and Y inputs as $V_Z = K(V_x \cdot V_y)$. The scale factor K has the dimensions of $(volts)^{-1}$ and can be adjusted externally.

In most arithmetic applications the multiplier and op amp sections of the XR-2228 are interconnected as shown in Figure 14. In such applications, over-all scale factor K can be written as:

$$K = (K_m)(K_a) = \left(\frac{V_o}{V_x V_y}\right)\left(\frac{V_z}{V_o}\right)$$

where K_m is the gain constant of the multiplier section, and K_a is the gain of the op amp stage in Figure 14. V_o is the multiplier output across pins 1 and 16, and V_z is the op amp output at pin 11. With reference to Figure 14, the gain constants can be expressed as:

$$K_m \simeq \frac{25}{R_x R_y}\ (volts)^{-1}; \qquad K_a \simeq \frac{R_f}{6 + R_i}$$

where all resistors are in kilo-ohms.

Thus, overall scale factor K can be adjusted by varying R_x, R_y, R_f. For fine adjustment of the scale factor, K, an additional potentiometer can be included into the circuit, as shown in Figure 14.

INPUT DYNAMIC RANGE: The maximum peak signal which can be applied to the X or Y inputs for a given supply voltage without impairing linearity. (See Figure 10).

MULTIPLIER BANDWIDTH: Depending on the particular application, a different definition of "multiplier band-width" may be used. The most commonly accepted definitions are:

a) *3-dB Bandwidth:* Frequency where the multiplier output is 3-dB below its low frequency (f = 20Hz) level.

b) *3° Phase Shift Bandwidth:* Frequency where the net phase shift across the multiplier is equal to 3°.

c) *1% Absolute Error Bandwidth:* Frequency where the phase vector error between the actual and ideal output vectors is equal to 1%. This frequency is reached when the net phase shift across the multiplier is equal to 0.01 radian or 0.57°.

d) *Transconductance Bandwidth:* Frequency where the transconductance of the multiplier drops 3-dB below its low frequency value. This bandwidth defines the frequency range of operation for phase-detector and synchronous AM detector applications.

TYPICAL CHARACTERISTICS CURVES.

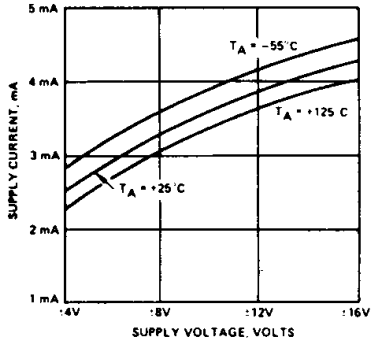


Figure 7. Supply Current vs Supply Voltage

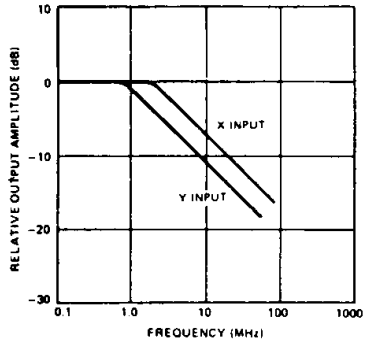


Figure 8. Small-Signal Frequency Response for the Multiplier Section. (Output Measured at Pin 16-See Fig. 4)

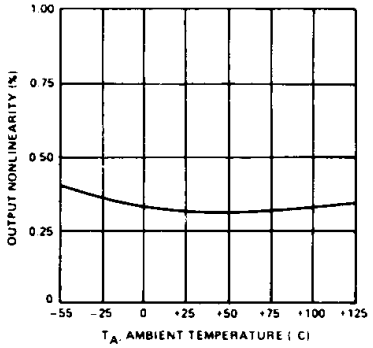


Figure 9. Temperature Dependence of Output Nonlinearity for X or Y Inputs (See Figure 2)

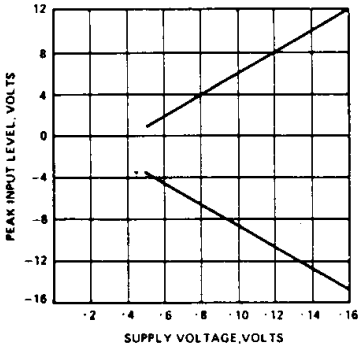


Figure 10. Multiplier Input Dynamic Range vs Power Supply

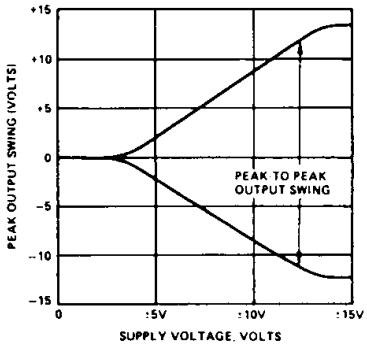


Figure 11. Op Amp output Swing vs Power Supply

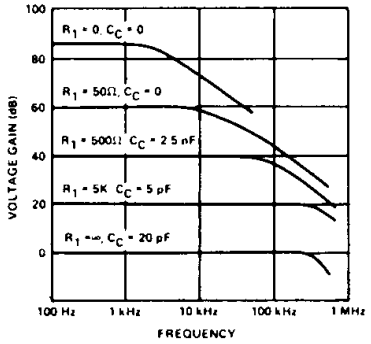


Figure 12. Op Amp Frequency Response

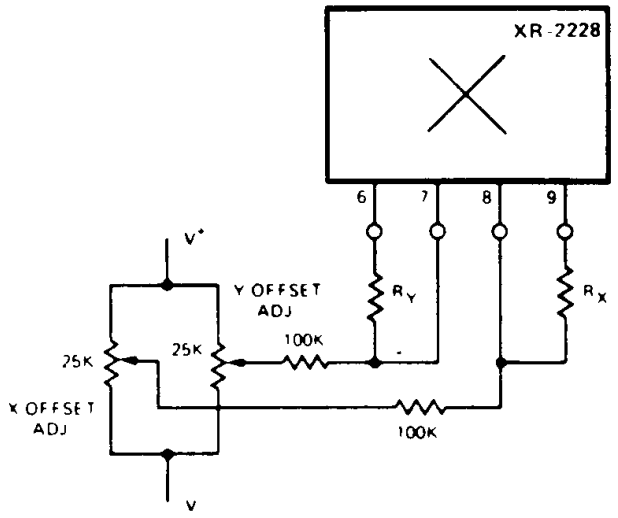


Figure 13. Offset Adjustment

DESCRIPTION OF CIRCUIT CONTROLS

MULTIPLIER INPUTS (Pins 2, 3, 4 and 5): These four terminals provide the differential inputs to the X- and Y-sections of the multiplier, respectively. The output will be a linear product of the two voltages, Vx and Vy, applied differentially across pins (2,3) and (4,5). Typical input bias current at the multiplier inputs is approximately 3μA, for each of the four inputs. In circuit applications requiring single-ended, rather than differential, input signals, pins 3 and 4 can be shorted together and connected to a common bias point.

MULTIPLIER OUTPUTS (Pins 1 and 16): The differential output voltage, V_o, across these terminals is proportional to the linear product of voltages V_x and V_y applied to the inputs. V_o can be expressed as:

$$V_o \approx \left(\frac{25}{R_x R_y}\right)\left(V_x V_y\right)$$

where all voltages are in volts and the resistors are in kΩ. R_x and R_y are the gain control resistors for X and Y sections of the multiplier.

The common-mode dc potential at the multiplier outputs is approximately 3 volts below the positive supply.

In most analog computation operations, such as multiplication, division, etc., pins 1 and 16 are dc coupled to the op amp inputs (pins 13 and 14). The final output, V_z, is then obtained from the op amp output at pin 11, as shown in Figures 14 and 15.

X AND Y GAIN ADJUST (Pins 6, 7, 8, 9): The gains of the X and Y sections of the multiplier are inversely proportional to resistors R_x and R_y connected across the respective gain terminals. The multiplier conversion gain, K_m, can be expressed as:

$$K_m \simeq \frac{25}{R_x R_y} (\text{volts})^{-1}$$

where R_x and R_y are in kΩ.

X AND Y OFFSET ADJUST (Pins 7 and 8): Two of the gain- control terminals, pins 7 and 8, are also used for adjusting X and Y offsets. Figure 13 shows the typical adjustment circuitry which can be connected to these pins to null-out input offsets.

OP AMP INPUTS (Pins 13 and 14): Pin 13 is the non-inverting and pin 14 the inverting inputs for the op amp section. In most multiplier applications, these terminals are connected to the multiplier outputs (pins 1 and 16). Note: When the op amp section is not used, these terminals should be grounded.

OP AMP COMPENSATION (Pin 12): The op amp section can be compensated for unconditional stability with a 20pF capacitor connected between pin 12 and pin 11. For op amp voltage gains greater than unity, this compensation capacitance can be reduced to improve slew rate and small signal bandwidth as shown in Figure 12.

OP AMP OUTPUT (Pin 11): This terminal serves as the output for the op amp section. It is internally protected against accidental short circuit conditions, and can sink or source 10mA of current into a resistive load. In most multiplier applications, pin 11 is the actual XR-2228 output, with the op amp inputs being connected to the multiplier outputs.

APPLICATIONS INFORMATION

PART 1: ARITHMETIC OPERATIONS

Multiplication

For most multiplication applications, the multiplier and op amp sections are interconnected as shown in Figure 14 to provide a single-ended analog output with a wide dynamic range. The circuit of Figure 14 provides a linear output swing of 10V for maximum input signals of 10V, with a scale factor K = 0.1. The trimming procedure for the circuit is as follows:

1. Apply 0V to both inputs and adjust the output offset to 0V using the output offset control.
2. Apply 20V p-p at 50Hz to the X-input and 0V to the Y-input. Trim the Y-offset adjust for minimum peak-to-peak output.
3. Apply 20V p-p to the Y-input and 0V to the X-input. Trim X-offset adjust for minimum peak-to-peak output.
4. Repeat step 1.
5. Apply +10V to both inputs and adjust scale factor for V_o = +10V. This step may be repeated with different amplitudes and polarities of input voltages to optimize accuracy over the entire range of input voltages, or over any specific portion of input voltage range.

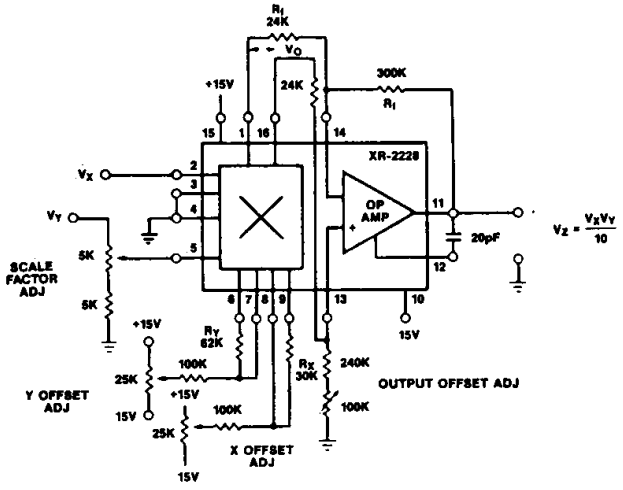


Figure 14. Multiplication Circuit

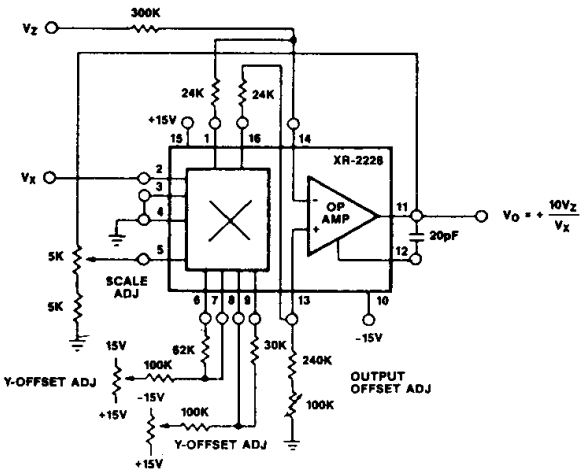


Figure 15. Dividing Circuit

Dividing Circuit

Recommended circuit connection for performing analog division is shown in Figure 15. This circuit uses the multiplier in the feedback path of the op amp. For the circuit shown, $V_o = +10\ V_Z/V_X$ where $V_X < 0$ and V_Z can have either sign. Positive values of V_X are not allowed, since this will reverse the polarity of the feed- back loop, causing positive feedback and latchup.

This latchup mode is nondestructive to the XR-2228, and is common to all analog division circuits. The divider circuit is trimmed as follows:

1. Apply $V_Z = 0$ and trim the output offset adjustment for constant output voltage as V_X is varied from –1V to –10V.

2. Keeping $V_Z = 0$, and applying $V_X = -10V$, trim the Y-offset adjust until $V_o = 0$.

3. Let $V_Z = V_X$ and/or $V_Z = -V_X$ and trim the X-offset adjustment for constant output voltage as V_X is varied from –1V to –10V.

4. If step 3 requires a large initial adjustment, repeat steps 1, 2 and 3.

5. Keeping $V_Z = V_X$, adjust the scale factor trim for V_o = –10V as V_X is varied from –1V to –10V.

PART II: ANALOG SIGNAL PROCESSING

Phase Detection

The multiplier section of the XR-2228 can be used as a linear phase-discriminator. A recommended circuit connection for this application is shown in Figure 16. In this case, the reference input (input 1) is applied to pin 2, and the input signal whose phase is to be detected (input 2) is applied to pin 5. For input signal amplitudes ≥ 50mV rms, the differential output voltage, V_o across pins 1 and 16 is directly proportional to the phase difference, ø, between the two input signals. It can be expressed as

$$V_o(\phi) = 5\left(\frac{2\phi}{\pi} - 1\right)$$

here ø is the phase difference expressed in radians. Even though the op amp is, in this application, not used, it is necessary to bias its inputs within their common mode range. This is easily accomplished in the phase detector circuit of pin 16 by tying pins 13 and 14 to pin 3 (which puts pins 13 and 14 at half supply).

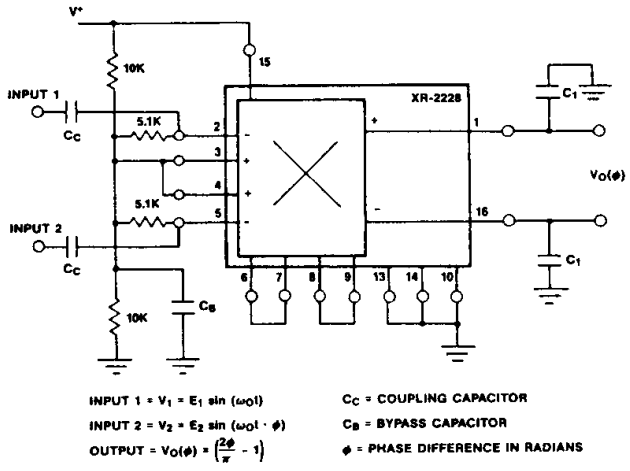


Figure 16. Phase-Detector Circuit

The capacitors C_1 at pins 1 and 16 provide a low-pass filter with a time constant $T_1 = R_1C_1$, where $R_1 = 5k\Omega$ is the international impedance level at these pins.

If needed, the phase conversion gain can be increased by using the op amp section of the XR-2228 to further amplify the output voltage, $V_o(\phi)$. The XR-2228 is suitable for phase detection of input frequencies up to 100MHz.

Synchronous AM Detection

Figure 17 is a typical circuit connection for synchronous AM detection for carrier frequencies up to 100MHz. The AM input signal is applied to the multiplier X- and Y-input terminals (pins 3 and 4) simultaneously.

The Y-gain terminals (pins 6 and 7) are shorted, and this section of the multiplier serves as a "limiter" for input signals ≥ 50mVrms; the X-section of the multiplier operates in its linear mode. The low-pass filter capacitors, C_1, and at pins 1 and 16 are used to filter the carrier feedthrough. If desired, the op amp section can be used as an audio preamplifier to increase the demodulated output amplitude.

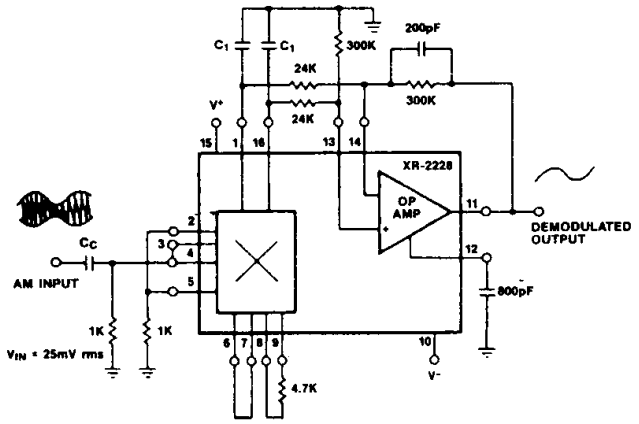


Figure 17. Synchronous AM Detector

Precision Phase-Locked Loop Design

A precision phase-locked loop may be constructed using an XR-2209 voltage controlled oscillator and the XR-2228. (See Figure 18.) Due to the excellent temperature stability and wide sweep range of the XR-2209 this PLL circuit exhibits especially good stability of center frequency and wide lock range. In this application the XR-2228 serves as a phase comparator and level shifter. Resistor R_L adjusts the loop gain of the PLL, thus varying the lock range. Tracking range may be varied from about 1.5:1 up to 12:1. For large values of R_L, temperature stability of center frequency is better than 30ppm/°C.

Triangle-to-Sinewave Conversion

A triangular input can be converted into a low distortion (THD < 1%) sinusoidal output with the XR-2228. A recommended connection for this application is shown in Figure 19. The triangle input signal is applied to the X-input (pin 2). The multiplier section rounds off the peaks of this input and converts it to a low distortion sine wave.

For the component values shown in Figure 19, the recommended input signal level at pin 2 is ≅ 300mV pp, in order to obtain a 2V pp signal at pins 1 or 16, with R_X set at approximately 100Ω. The dc level at pin 5 can be used for adjusting the output amplitude, or providing amplitude modulation. The sensitivity of the output amplitude to the dc voltage level at pin 5 is inversely proportional to the external resistor across pins 6 and 7.

If higher amplitude output signal is required, the op amp section of XR-2228 can be used to provide additional amplification. If the op amp is not used, its inputs must be biased within common mode range to ensure proper device operation.

Phase-Locked AM Detection

The XR-2228 can be used in conjunction with any one of the commercially available monolithic phase-locked loop (PLL) IC's to provide phase-locked AM detection. In this manner, frequency-selective detection capabilities of PLL circuits can be extended to AM signals.

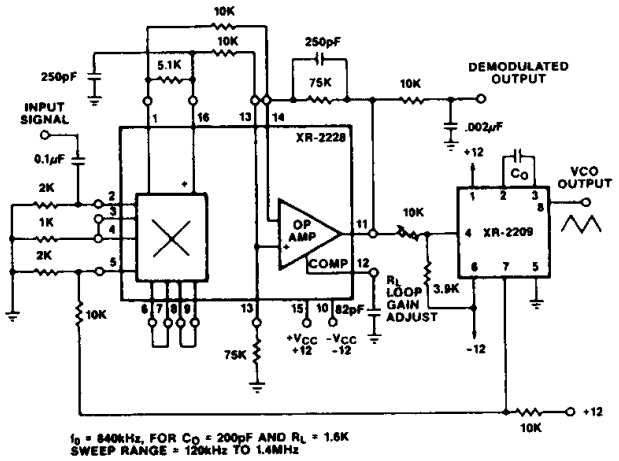


Figure 18. Precision PLL

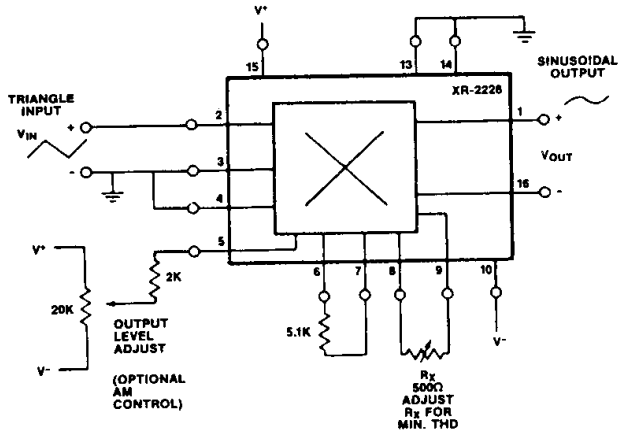


Figure 19. Triangle-to-Sinewave Converter

Figure 20 shows the circuit connection diagram for a two-chip AM and FM detection system, using the XR-215 high-frequency PLL in conjunction with the XR-2228 multiplier/detector. Because of the high-frequency capability of the XR-215, the circuit is useful as a phase-locked AM detector for carrier frequencies up to 20MHz, and operates over a supply voltage range of 10V to 20V.

The VCO section of XR-215 does not have a separate "quadrature" output. However, this problem can be overcome by driving the XR-2228 multiplier directly from the timing capacitor terminals (pins 13 and 14) of XR-215. The Y-input of the XR-2228 is operated with maximum gain, since the Y-gain control terminals (pins 6 and 7) are shorted together. This causes the triangular waveform across the timing capacitor, C_0, to be converted to an effective "quadrature" drive.

The modulated input signal is simultaneously applied to both circuits through coupling capacitors. The phase-detector inputs of the XR-215, as well as the multiplier X-inputs of the XR-2228, are biased at approximated one-half of V_{CC}, by means of an external resistive divider.

In Figure 20, C_0 sets the VCO frequency of the XR-215. In the case of FM demodulation, R_1 and C_1 serve as the post-detection filter for the detected FM signal and R_{F1} sets the gain of the FM post-detection amplifier,

The Y-input of the XR-2228 is operated in its switching mode, with the Y-gain terminals (pins 6 and 7) shorted together. The AM and/or FM signal is simultaneously applied to both circuits through coupling capacitors; the output of the multiplier, at pin 16, is AC coupled to the op amp section of the XR-2228, which serves as the post-detection amplifier for the demodulated AM signal. In the circuit, R_X sets the amplifier demodulation gain, C_3 serves as the low-pass post-detection filter.

A detailed description of the circuit operation, and the design equations for calculating the external component values are given in Exar's Application Note AN-13, entitled "Frequency Selective AM Detection using Monolithic Phase-Locked Loops."

Phase-Locked Loop Tone Detection

The XR-2228 multiplier/detector can be used in conjunction with the XR-210 or the XR-215 high-frequency PLL circuits, to provide high-frequency tone or carrier- detect systems. The generalized circuit connection for such an application is given in Figure 21. The circuit, as shown, can operate with a single power supply, from 10V, to 20V, or with split supplies in the range of ±5V to ±10V. In the case of split power supplies, the resistor string biasing the input terminals of the XR-2228 is not necessary and can be eliminated by connecting node A of Figure 21 to ground.

The input signal is AC coupled, with separate coupling capacitors, both to the input of the particular PLL circuit to be used and to the X-input terminal (pin 2) of the XR-2228.

The Y-inputs (pins 4 and 5) are driven differentially from the VCO timing capacitor signal (available at pins 13 and 14 of the PLL IC) which is AC coupled to pins 4 and 5 of the XR-2228 multiplier input. the differential DC voltage level at the multiplier output terminals (pins 1 and 16) is offset by means of an external resistor, R_A. This initial offset causes the op amp output of the XR- 2228 to settle to a known state when there is no carrier or tone signal to be detected. With the op amp input connections as shown in Figure 21, the op amp output (pin 11) would be at a "low" state when the PLL is not locked on a tone, and goes to a "high" state (i.e., near $+V_{CC}$) when the PLL circuit is "locked" on to an input tone. The output logic polarity can be reversed simply by reversing the op amp inputs.

The filter capacitor, C_A, connected across pins 1 and 16 of the multiplier outputs, serves as the post- detection low-pass filter. The value of C_A is chosen to provide a compromise between the response time and the spurious noise rejection characteristics of the circuit: increasing C_A improves the noise rejection characteristics of the circuit, but slows down the response time.

A detailed description of the principle of operation of the circuit of Figure 21 is given in Exar's Application Note AN-12 entitled: "Designing High Frequency Phase-Locked Loop Carrier-Detector Circuits".

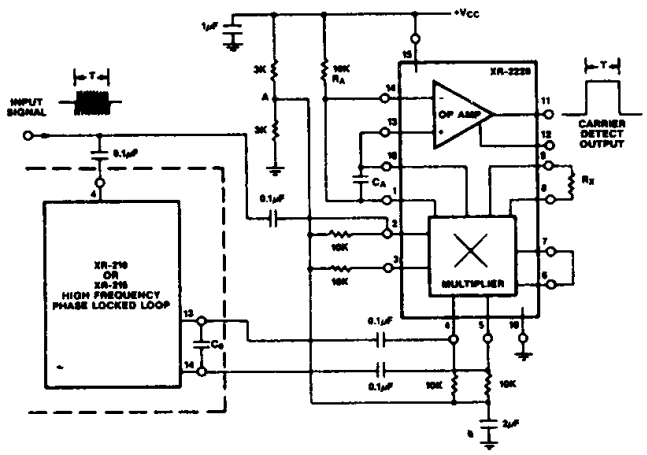


Figure 21. Recommended Circuit Connection of the XR-2228 with the XR-210 or the XR-215 High-Frequency Phase-Locked Loops for Tone or Carrier-Detector Application

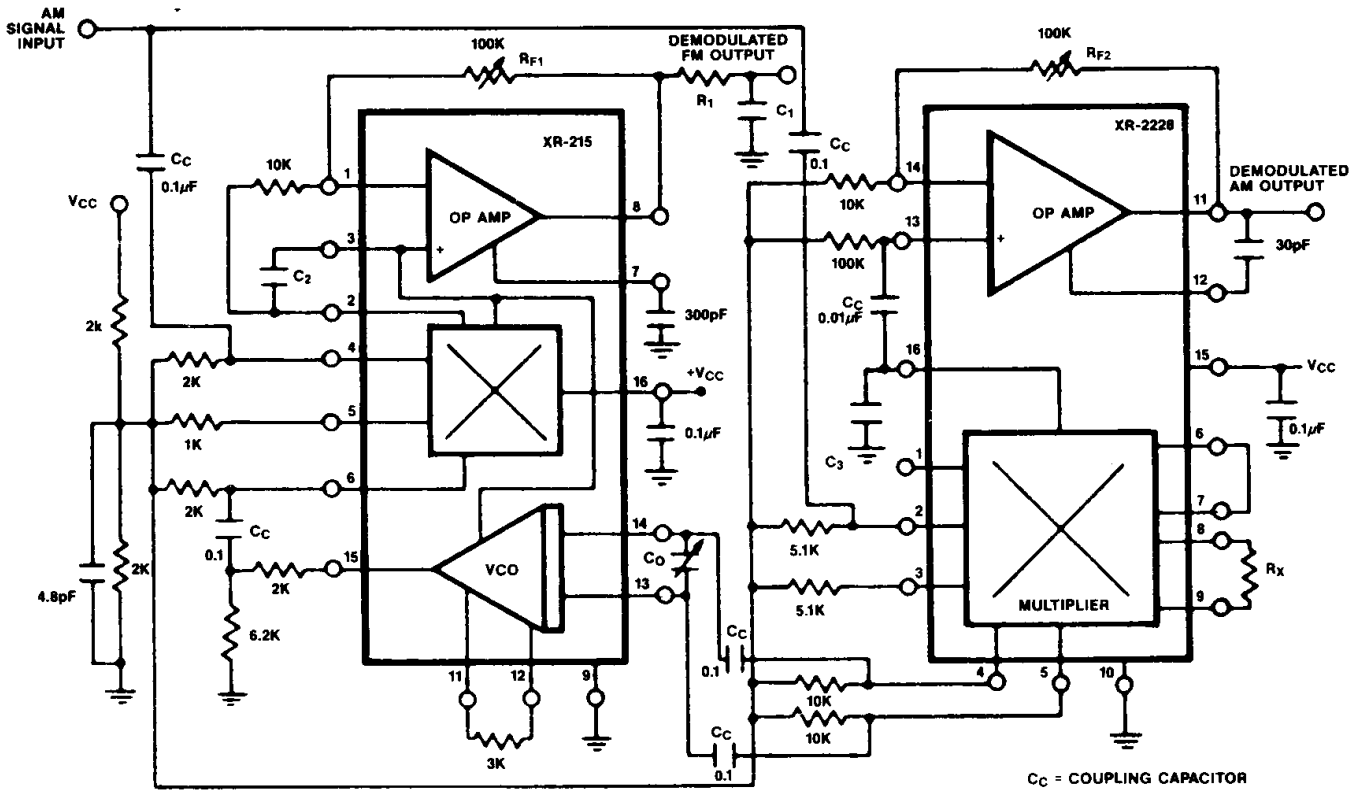


Figure 20. Phase-Locked AM Detection Using XR-215 Monolithic PLL and XR-2228 Multiplier/Detector