



## P-Channel Enhancement-Mode Vertical DMOS FETs

### Ordering Information

BV <sub>DSS</sub> / BV <sub>DGS</sub>	R <sub>DS(ON)</sub> (max)	V <sub>GS(th)</sub> (max)	I <sub>D(ON)</sub> (min)	Order Number / Package	
				TO-243AA*	Die**
-350V	15Ω	-2.4V	-800mA	TP2435N8	TP2435NW

\* Same as SOT-89. Product supplied on 2000 piece carrier tape reels.

\*\* Die in wafer form.

Product marking for TO-243AA:

TP4S\*

where \* = 2-week alpha date code

### Features

- Low threshold
- High input impedance
- Low input capacitance
- Fast switching speeds
- Free from secondary breakdown
- Low input and output leakage
- Complementary N- and P-channel devices

### Applications

- Logic level interfaces
- Solid state relays
- Linear Amplifiers
- Power Management
- Analog switches
- Telecom switches

### Absolute Maximum Ratings

Drain-to-Source Voltage	BV <sub>DSS</sub>
Drain-to-Gate Voltage	BV <sub>DGS</sub>
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

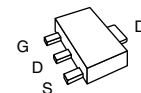
\* Distance of 1.6 mm from case for 10 seconds.

### Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

### Package Option



TO-243AA  
(SOT-89)

Note: See Package Outline section for dimensions.

11/12/01

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## Thermal Characteristics

Package	$I_D$ (continuous)*	$I_D$ (pulsed)	Power Dissipation @ $T_A = 25^\circ\text{C}$	$\theta_{jc}$ $^\circ\text{C/W}$	$\theta_{ja}$ $^\circ\text{C/W}$	$I_{DR}^*$	$I_{DRM}$
TO-243AA	-231mA	-1.1A	1.6W <sup>†</sup>	15	78 <sup>†</sup>	-231mA	-1.1A

\*  $I_D$  (continuous) is limited by max rated  $T_j$ .

<sup>†</sup> Mounted on FR5 board, 25mm x 25mm x 1.57mm. Significant  $P_D$  increase possible on ceramic substrate.

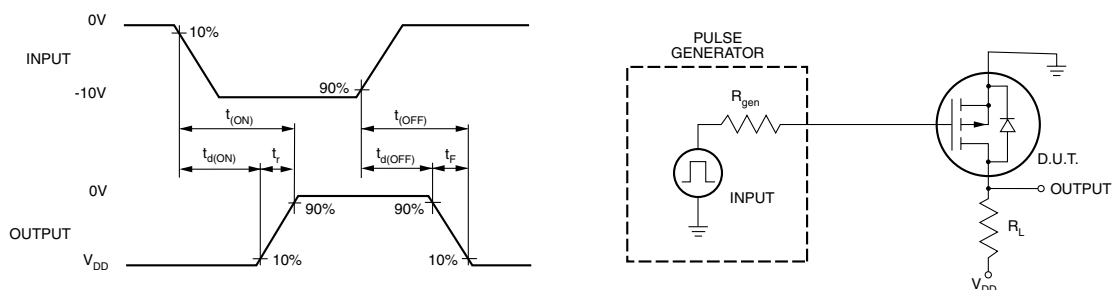
## Electrical Characteristics (@ $25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	-350			V	$V_{GS} = 0V, I_D = -250\mu\text{A}$
$V_{GS(th)}$	Gate Threshold Voltage	-1.0		-2.4	V	$V_{GS} = V_{DS}, I_D = -1.0\text{mA}$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			4.5	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = -1.0\text{mA}$
$I_{GSS}$	Gate Body Leakage			-100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
$I_{DSS}$	Zero Gate Voltage Drain Current			-10.0	$\mu\text{A}$	$V_{GS} = 0V, V_{DS} = \text{Max Rating}$
				-1.0	mA	$V_{GS} = 0V, V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ\text{C}$
$I_{D(ON)}$	ON-State Drain Current	-0.3			A	$V_{GS} = -4.5V, V_{DS} = -25V$
		-0.8				$V_{GS} = -10V, V_{DS} = -25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			15	$\Omega$	$V_{GS} = -3.0V, I_D = -20\text{mA}$
				15		$V_{GS} = -4.5V, I_D = -150\text{mA}$
				15		$V_{GS} = -10V, I_D = -500\text{mA}$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			1.7	%/ $^\circ\text{C}$	$V_{GS} = -10V, I_D = -150\text{mA}$
$G_{FS}$	Forward Transconductance	125			m $\Omega$	$V_{DS} = -25V, I_D = -350\text{mA}$
$C_{ISS}$	Input Capacitance			200	pF	$V_{GS} = 0V, V_{DS} = -25V$ $f = 1.0 \text{ MHz}$
$C_{OSS}$	Common Source Output Capacitance			70		
$C_{RSS}$	Reverse Transfer Capacitance			25		
$t_{d(ON)}$	Turn-ON Delay Time			15	ns	$V_{DD} = -25V,$ $I_D = -250\text{mA},$ $R_{GEN} = 25\Omega$
$t_r$	Rise Time			20		
$t_{d(OFF)}$	Turn-OFF Delay Time			25		
$t_f$	Fall Time			50		
$V_{SD}$	Diode Forward Voltage Drop			-1.5	V	$V_{GS} = 0V, I_{SD} = -750\text{mA}$
$t_{rr}$	Reverse Recovery Time		300		ns	$V_{GS} = 0V, I_{SD} = -750\text{mA}$

### Notes:

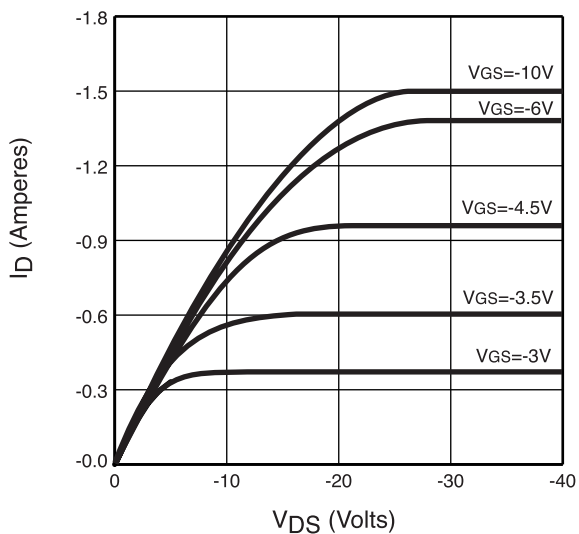
- All D.C. parameters 100% tested at  $25^\circ\text{C}$  unless otherwise stated. (Pulse test: 300 $\mu\text{s}$  pulse, 2% duty cycle.)
- All A.C. parameters sample tested.

## Switching Waveforms and Test Circuit

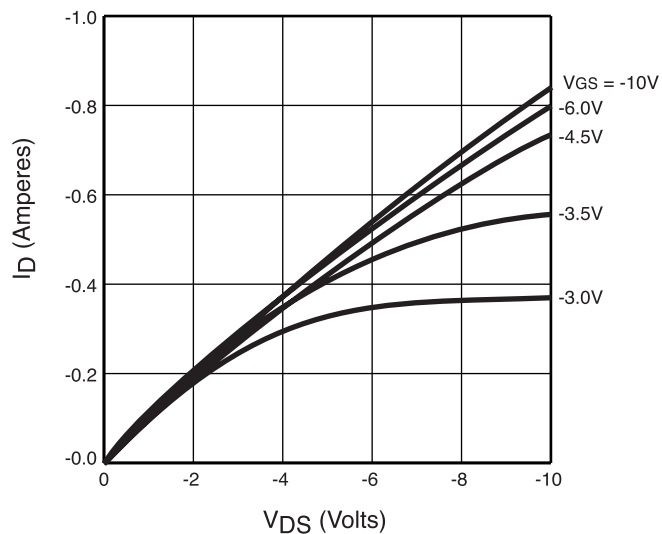


# Typical Performance Curves

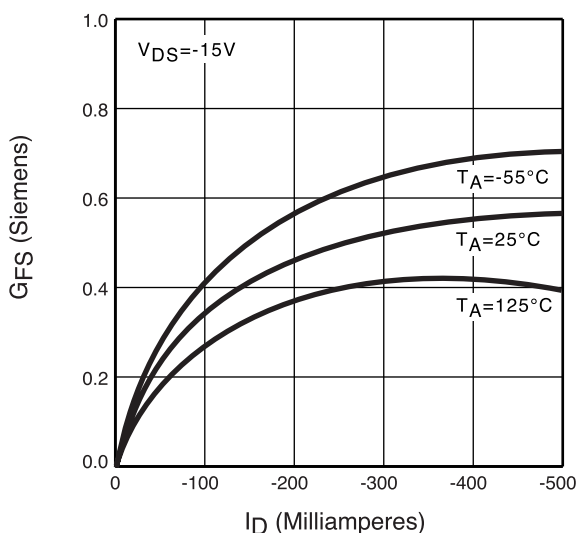
Output Characteristics



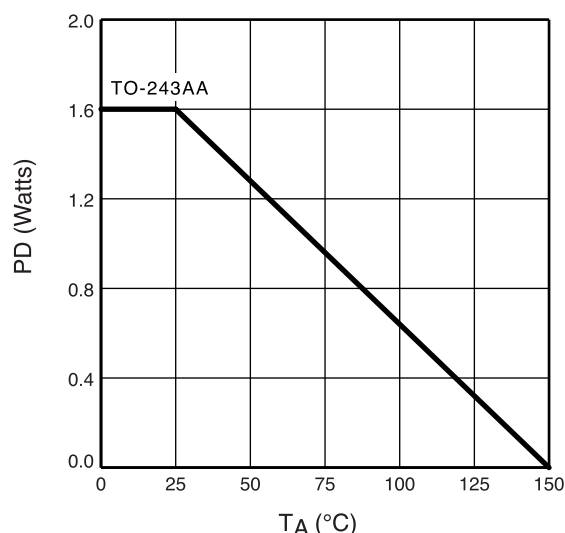
Saturation Characteristics



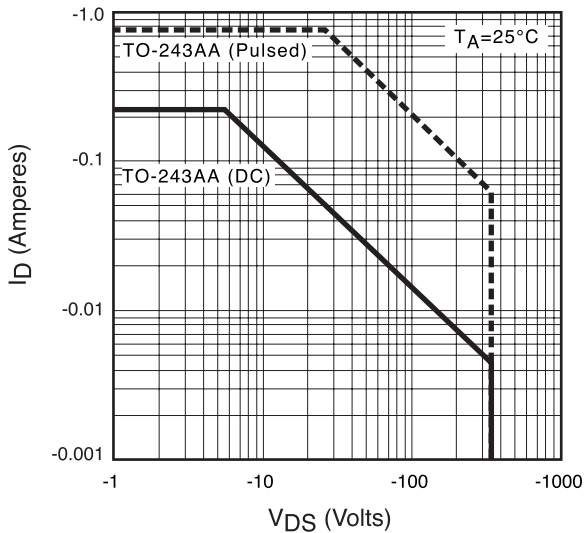
Transconductance vs. Drain Current



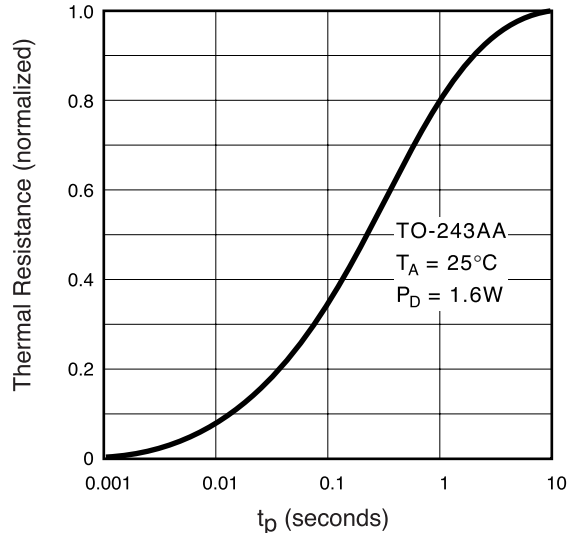
Power Dissipation vs. Ambient Temperature



Maximum Rated Safe Operating Area

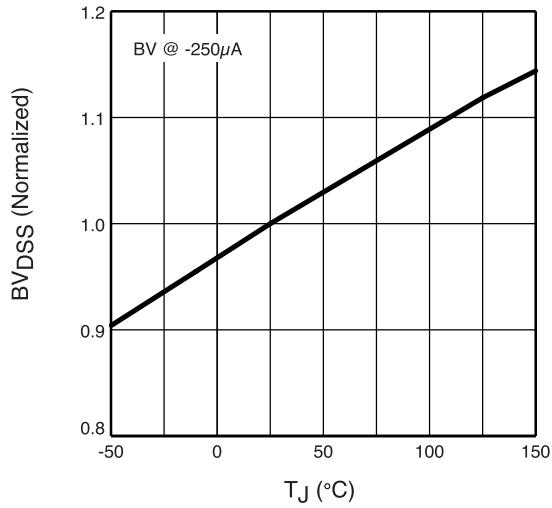


Thermal Response Characteristics

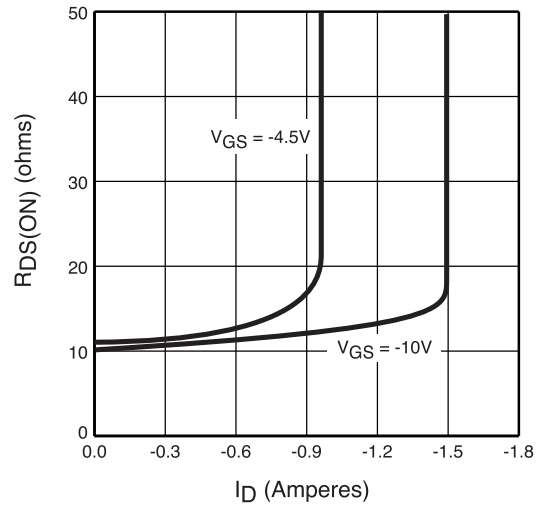


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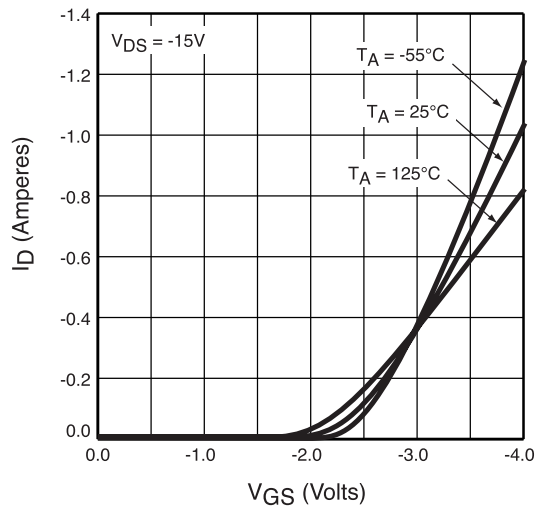
BV<sub>DSS</sub> Variation with Temperature



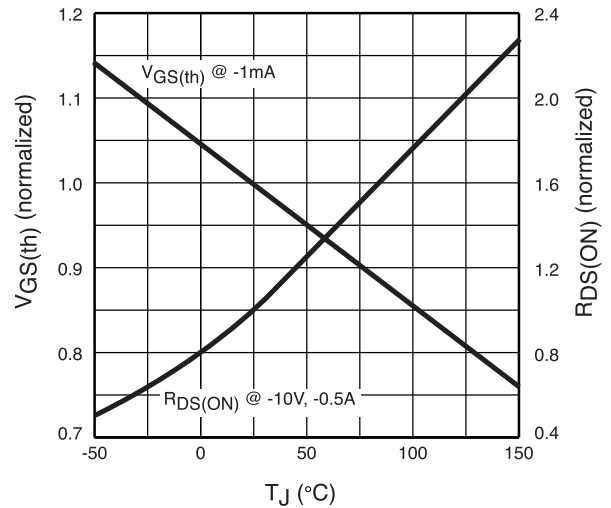
On Resistance vs. Drain Current



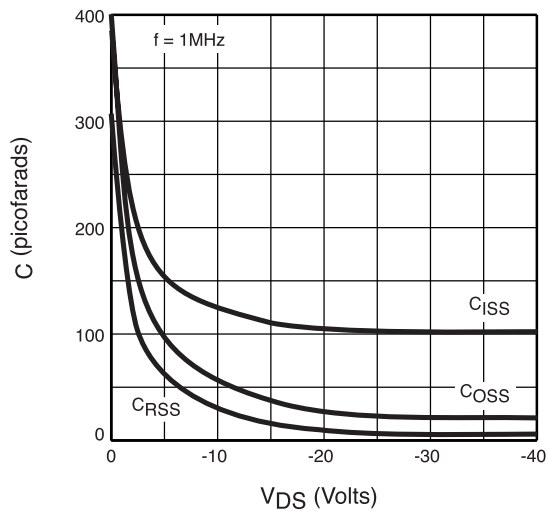
Transfer Characteristics



V<sub>GS(th)</sub> and R<sub>DS(ON)</sub> w/ Temperature



Capacitance vs. Drain Source Voltage



Gate Drive Dynamic Characteristics

