

N-Channel Depletion-Mode MOSFET

Ordering Information

BV _{DSX} /	R _{DS(ON)}	I _{DSS}	Order Number / Package			
BV _{DGX}	(max)	(min)	TO-92	TO-243AA*	Die	
500V	1.0KΩ	1.0mA	LND150N3	LND150N8	LND150ND	

^{*} Same as SOT-89. Product shipped on 2000 piece carrier tape reels.

Product marking for TO-243AA:					
	LN1E*				
Where * = 2-week alpha date code					

Features

- ESD gate protection
- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Excellent thermal stability
- Integral source-drain diode
- ☐ High input impedance and low C_{ISS}

Applications

- Solid state relays
- Normally-on switches
- Converters
- Power supply circuits
- Constant current sources
- Input protection circuits

Absolute Maximum Ratings

Drain-to-Source Voltage	BV _{DSX}
Drain-to-Gate Voltage	BV_{DGX}
Gate-to-Source Voltage	±20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

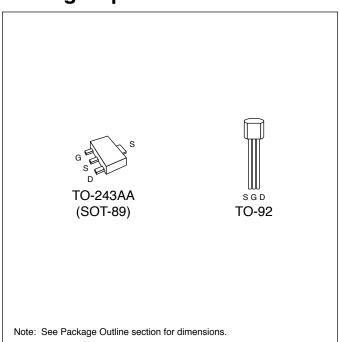
^{*} Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

The LND1 is a high voltage N-channel depletion mode (normally-on) transistor utilizing Supertex's lateral DMOS technology. The gate is ESD protected.

The LND1 is ideal for high voltage applications in the areas of normally-on switches, precision constant current sources, voltage ramp generation and amplification.

Package Options



12/13/01

Thermal Characteristics

Package	I _D (continuous)*	I _D (pulsed)	Power Dissipation @T _A = 25°C	θ _{jc} °C/W	θ _{ja} °C/W	l _{DR}	I _{DRM} *
TO-92	30mA	30mA	0.74W	125	170	30mA	30mA
TO-243AA	30mA	30mA	1.6W [†]	31	105†	30mA	30mA

^{*} In (continuous) is limited by max rated T

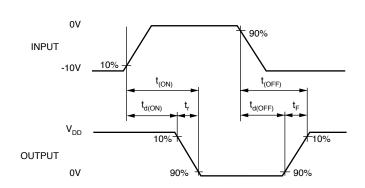
Electrical Characteristics (@ 25°C unless otherwise specified)

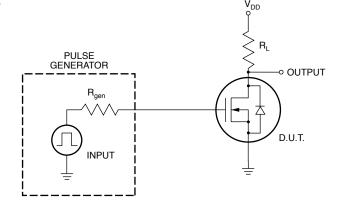
Symbol	Parameter	Min	Тур	Max	Unit	Conditions	
BV _{DSX}	Drain-to-Source Breakdown Voltage	500			V	$V_{GS} = -10V, I_D = 1.0mA$	
V _{GS(OFF)}	Gate-to-Source OFF Voltage	-1.0		-3.0	V	$V_{DS} = 25V, I_{D} = 100nA$	
$\Delta V_{GS(OFF)}$	Change in V _{GS(OFF)} with Temperature			5.0	mV/°C	$V_{DS} = 25V, I_{D} = 100nA$	
I _{GSS}	Gate Body Leakage Current			100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$	
I _{D(OFF)}	Drain-to-Source Leakage Current			100	nA	$V_{GS} = -10V, V_{DS} = 450V$	
				100	μΑ	$V_{GS} = -10V$, $V_{DS} = 0.8V$ max rating $T_A = 125$ °C	
I _{DSS}	Saturated Drain-to-Source Current	1.0		3.0	mA	$V_{GS} = 0V, V_{DS} = 25V$	
R _{DS(ON)}	Static Drain-to-Source ON-State Resistance		850	1000	Ω	$V_{GS} = 0V, I_D = 0.5mA$	
$\Delta R_{DS(ON)}$	Change in RDS(ON) with Temperature			1.2	%/°C	$V_{GS} = 0V, I_D = 0.5mA$	
G _{FS}	Forward Transconductance	1.0	2.0		m &	$V_{GS} = 0V, I_D = 1.0mA$	
C _{ISS}	Input Capacitance		7.5	10			
C _{OSS}	Output Capacitance		2.0	3.5	pF	$V_{GS} = -10V, V_{DS} = 25V$ f = 1 MHz	
C _{RSS}	Reverse Transfer Capacitance		0.5	1.0		I = I WINZ	
t _{d(ON)}	Turn-ON Delay Time		0.09				
tr	Rise Time		0.45			$V_{DD} = 25V, I_D = 1.0mA,$	
t _{d(OFF)}	Turn-OFF Delay Time		0.1		μS	$R_{GEN} = 25\Omega$	
t _f	Fall Time		1.3				
V _{SD}	Diode Forward Voltage Drop			0.9	V	$V_{GS} = -10V, I_{SD} = 1.0mA$	
t _{rr}	Reverse Recovery Time		200		ns	V _{GS} = -10V, I _{SD} = 1.0mA	

Notes:

- 1. All D.C. parameters 100% tested at 25 $^{\circ}$ C unless otherwise stated. (Pulse test: 300 μ s pulse, 2% duty cycle.)
- 2. All A.C. parameters sample tested.

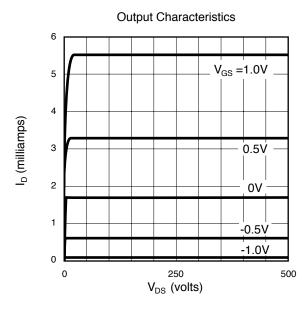
Switching Waveforms and Test Circuit



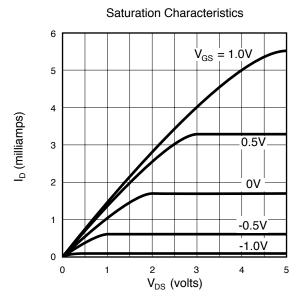


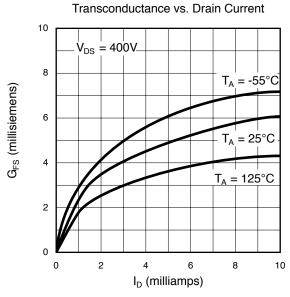
[†] Mounted on FR5 Board, 25mm x 25mm x 1.57mm. Significant P_n increase possible on ceramic substrate.

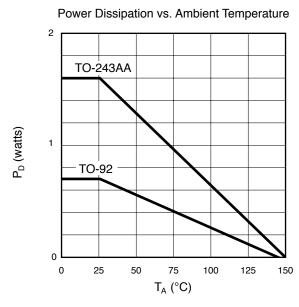
Typical Performance Curves

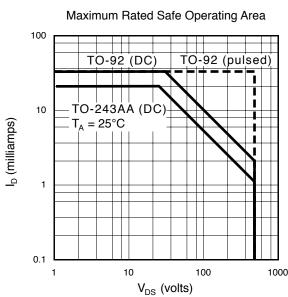


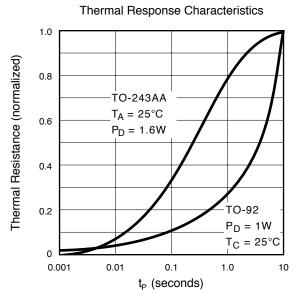




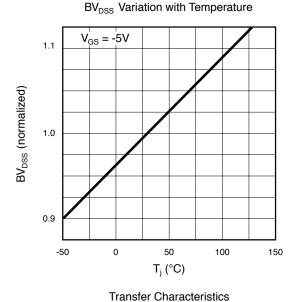


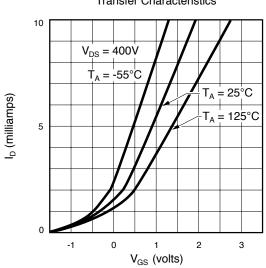


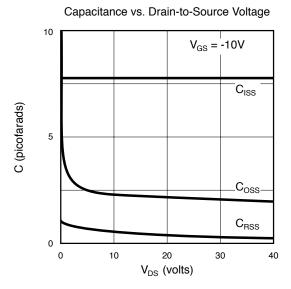


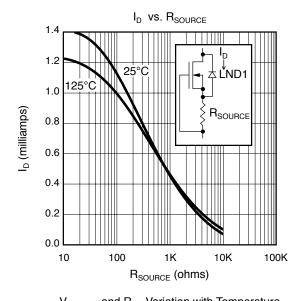


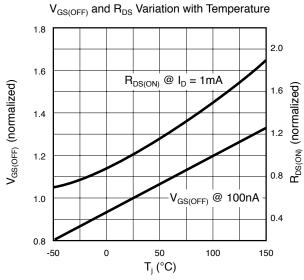
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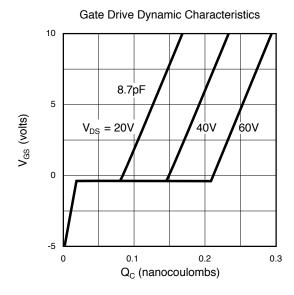












12/13/010