64-Channel Serial To Parallel Converter With P-Channel Open Drain Controllable Output Current

Ordering Information

Device	Package Options			
	80-Lead Quad Ceramic Gullwing	80 Lead Quad Plastic Gullwing	Die	80 Lead Quad Ceramic Gullwing (MIL-Std-833 Processed*)
HV57009	HV57009DG	HV57009PG	HV57009X	RBHV57009DG

* For Hi-Rel process flows, refer to page 5-3 of the Databook.

Features

- ❏ Processed with HVCMOS® technology
- ❏ 5V CMOS Logic
- ❏ Output voltage up to -85V
- ❏ Output current source control
- ❏ 16MHz equivalent data rate
- ❏ Latched data outputs
- ❏ Forward and reverse shifting options (DIR pin)
- ❏ Diode to V_{DD} allows efficient power recovery
- ❏ Hi-Rel processing available

Absolute Maximum Ratings

Supply voltage, V_{DD}[1]		-0.5V to +7.5V
Output Voltage, V_{NN}[1]		V_{DD} + 0.5V to -95V
Logic input levels[1]		-0.3V to V_{DD} +0.3V
Ground Current[2]		1.5A
Continuous total power dissipation[3]	Plastic	1200mW
	Ceramic	1900mW
Operating temperature range	Plastic	-40°C to +85°C
	Ceramic	-55°C to +125°C
Storage temperature range		-65°C to +150°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds		260°C

Notes:
1. All voltages are referenced to V_{SS}.
2. Limited by the total power dissipated in the package.
3. For operation above 25°C ambient derate linearly to maximum operating temperature at 20mW/°C for plastic and at 19mW/°C for ceramic.

General Description

The HV570 is a low-voltage serial to high-voltage parallel converter with P-channel open drain outputs. This device has been designed for use as a driver for plasma panels.

The device has two parallel 32-bit shift registers, permitting data rate twice the speed of one (they are clocked together). There are also 64 latches and control logic to perform the blanking of the outputs. $HV_{OUT}1$ is connected to the first stage of the first shift register through the blanking logic. Data is shifted through the shift registers on the logic low to high transition of the clock. The DIR pin causes CCW shifting when connected to V_{SS}, and CW shifting when connected to V_{DD}. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register ($HV_{OUT}64$). Operation of the shift register is not affected by the $\overline{LE}$ (latch enable), or the $\overline{BL}$ (blanking) inputs. Transfer of data from the shift registers to latches occurs when the $\overline{LE}$ input is high. The data in the latches is stored when $\overline{LE}$ is low.

The HV570 has 64 channels of output constant current sourcing capability. They are adjustable from 0.1 to 2.0mA through one external resistor or a current source.

03/12/02

Electrical Characteristics

DC Characteristics (All voltages are referenced to V_{SS}, V_{SS} = 0, TA = 25°C)

Symbol	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current			15	mA	$V_{DD} = V_{DD}$, max f_{CLK} = 8MHz
I_{NN}	High voltage supply current			-10	μA	Outputs off, HV_{OUT} = -85V (total of all outputs)
I_{DDQ}	Quiescent V_{DD} supply current			100	μA	All inputs = V_{DD}, except +IN = V_{SS} = GND
V_{OH}	High-level output	Data out	V_{DD} -0.5		V	I_O = -100μA
		HV_{OUT}	+1	V_{DD}	V	I_O = -2mA
V_{OL}	Low-level output	Data out		+0.5	V	I_O = 100μA
I_{IH}	High-level logic input current			1	μA	$V_{IH} = V_{DD}$
I_{IL}	Low-level logic input current			-1	μA	V_{IL} = 0V
I_{CS}	HV output source current			-2	mA	V_{REF} = 2V, R_{EXT} = 1K, see Figures 8a and 8b
			-0.1		mA	V_{REF} = 0.1V, R_{EXT} = 1K, see Figure 8a and 8b
ΔI_{CS}	HV output source current for I_{REF} = 2.0mA			10	%	V_{REF} = 2V, R_{EXT} = 1K

Notes 1: Current going out of the chip is considered negative.

AC Characteristics (Logic signal inputs and Data inputs have t_r, $t_f \leq$ 5ns [10% and 90% points] for measurements)

Symbol	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency	DC	8	MHz	Per register
t_{WL}, t_{WH}	Clock width high or low	62		ns	
t_{SU}	Data set-up time before clock rises	10		ns	
t_H	Data hold time after clock rises	15		ns	
t_{ON}, t_{OFF}	Time for latch enable to HV_{OUT}		500	ns	C_L = 15pF
t_{DHL}	Delay time clock to data high to low		70	ns	C_L = 15pF
t_{DLH}	Delay time clock to data low to high		70	ns	C_L = 15pF
t_{DLE}	Delay time clock to $\overline{LE}$ low to high	25		ns	
t_{WLE}	Width of $\overline{LE}$ pulse	25		ns	
t_{SLE}	$\overline{LE}$ set-up time before clock rises	0		ns	
t_r, t_f	Maximum allowable clock rise and fall time (10% and 90% points)		100	ns	

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{DD}	Logic supply voltage		4.5	5.5	V
HV_{OUT}	HV output off voltage		-85	V_{DD}	V
V_{IH}	High-level input voltage		V_{DD} - 1.2V	V_{DD}	V
V_{IL}	Low-level input voltage		0	1.2	V
f_{CLK}	Clock frequency per register		DC	8	MHz
T_A	Operating free-air temperature	Plastic	-40	+85	°C
		Ceramic	-55	+125	°C

Note:
Power-up sequence should be the following:

1. Connect ground.
2. Apply V_{DD}.
3. Set all inputs to a known state.

Power-down sequence should be the reverse of the above.

Figure 1: Input and Output Equivalent Circuits

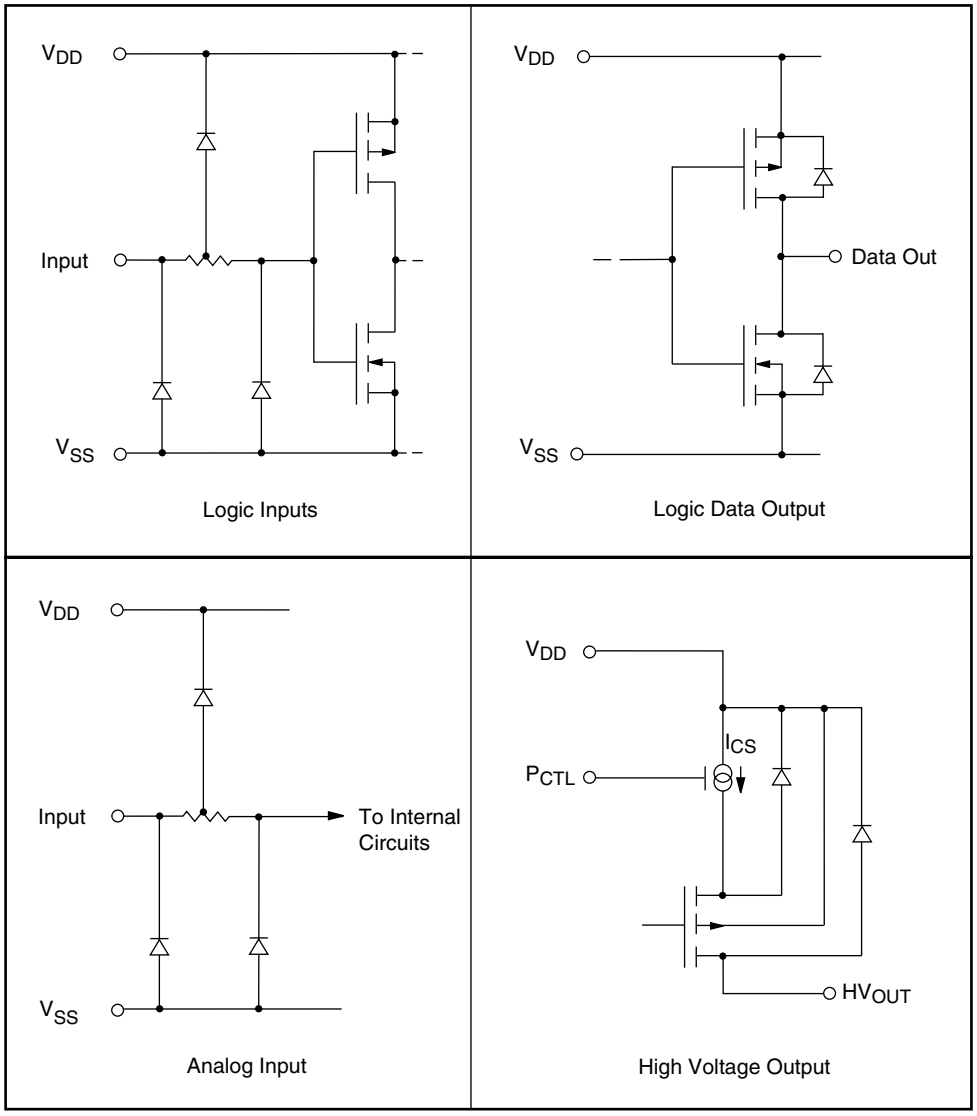


Figure 2: Switching Waveforms

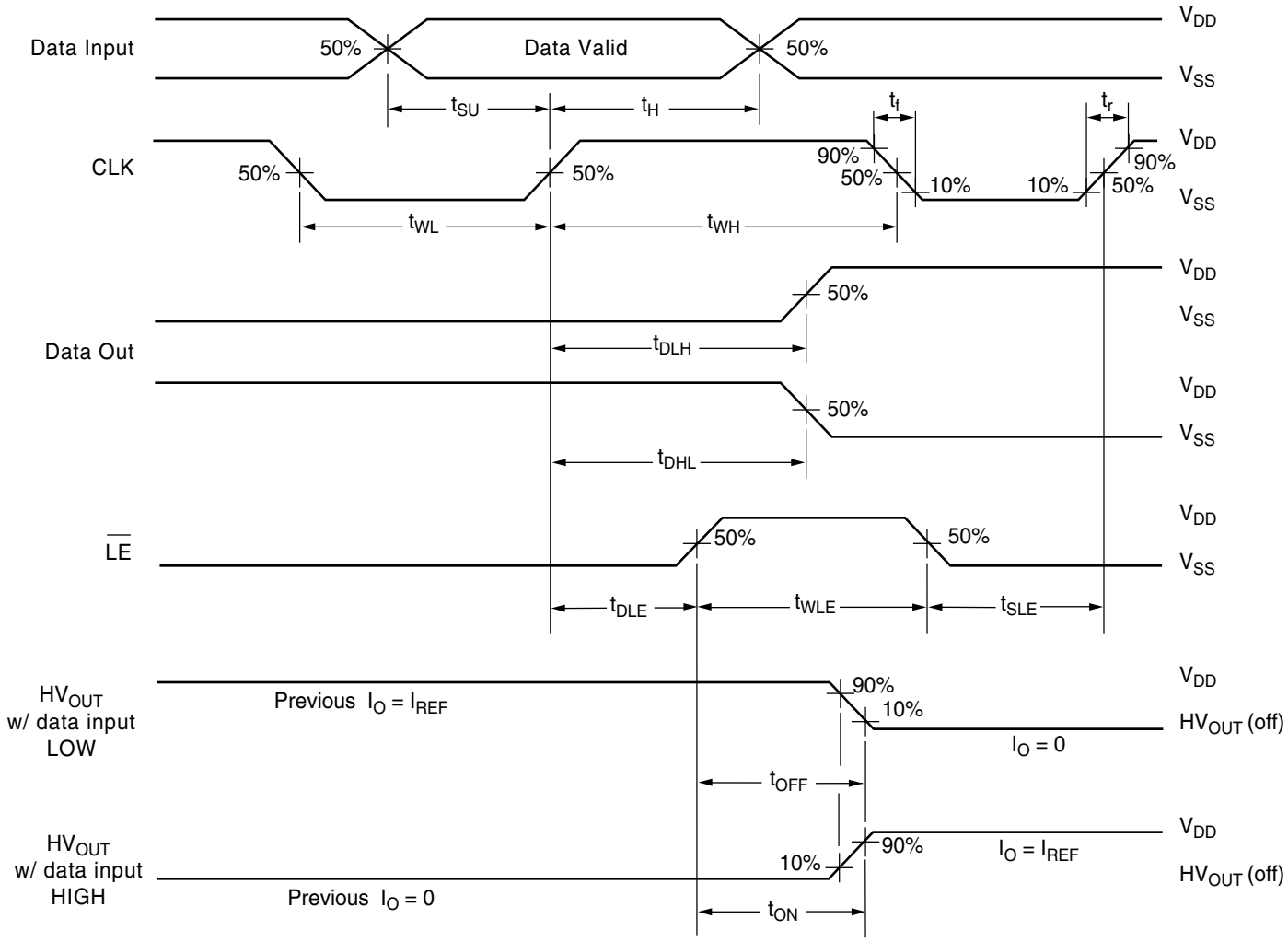
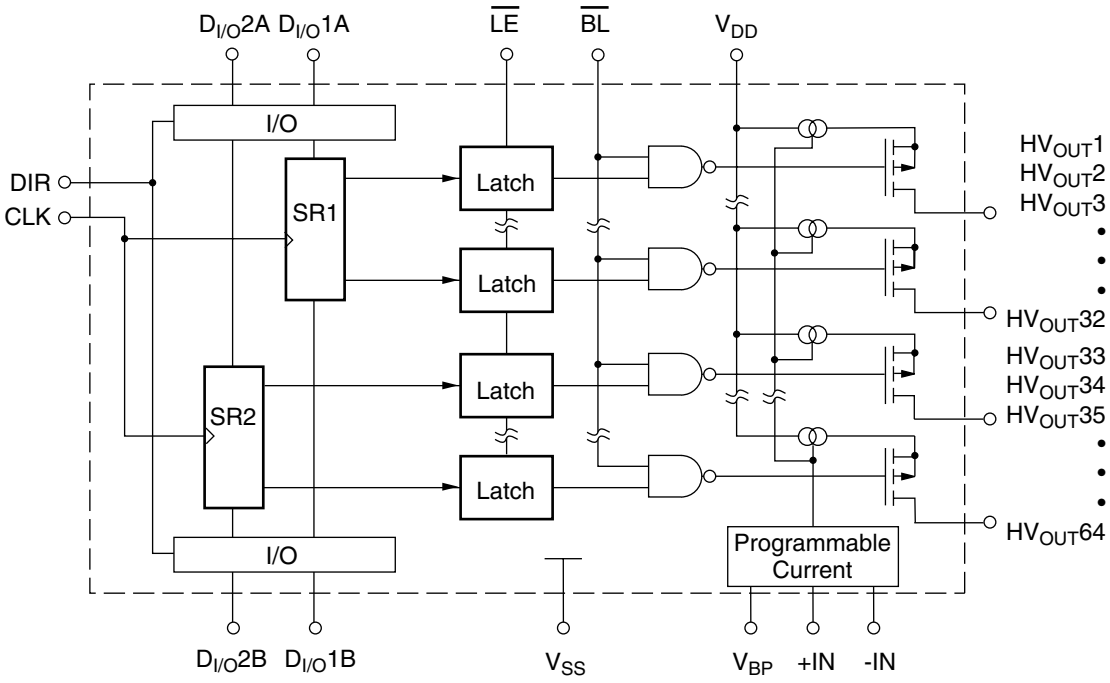


Figure 3: Functional Block Diagram



Note: Each SR (shift register) provides 32 outputs. SR1 supplies outputs 1 to 32 and SR2 supplies outputs 33 to 64.

Figure 4: Function Table

Function	Inputs					Outputs		
	Data In	CLK	$\overline{LE}$	$\overline{BL}$	DIR	Shift Reg	HV Outputs	Data Out
All O/P High	X	X	X	L	X	*	ON	*
Data Falls Through (Latches Tansparent)	L	↑	H	H	X	L....L	ON	L
	H	↑	H	H	X	H....H	OFF	H
Data Stored in Latches	X	X	L	H	X	*	Inversion of Stored Data	*
I/O Relation	$D_{I/O}$1-2A	↑	H	H	H	$Q_n \rightarrow Q_{n+1}$	New ON or OFF	$D_{I/O}$1-2B
	$D_{I/O}$1-2A	↑	L	H	H	$Q_n \rightarrow Q_{n+1}$	Previous ON or OFF	$D_{I/O}$1-2B
	$D_{I/O}$1-2B	↑	L	H	L	$Q_n \rightarrow Q_{n-1}$	Previous ON or OFF	$D_{I/O}$1-2A
	$D_{I/O}$1-2B	↑	H	H	L	$Q_n \rightarrow Q_{n-1}$	New ON or OFF	$D_{I/O}$1-2A

Notes:
* = dependent on previous stage's state. See Figure 7 for D_{IN} and D_{OUT} pin designation for CW and CCW shift.
H = V_{DD} (Logic)/V_{NN} (HV Outputs)
L = V_{SS}

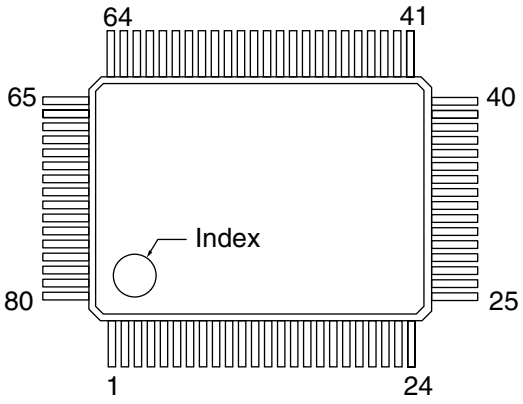
Figure 5: Pin Configurations

80-pin Gullwing Package

Pin	Function	Pin	Function
1	HV_{OUT} 24	41	HV_{OUT} 64
2	HV_{OUT} 23	42	HV_{OUT} 63
3	HV_{OUT} 22	43	HV_{OUT} 62
4	HV_{OUT} 21	44	HV_{OUT} 61
5	HV_{OUT} 20	45	HV_{OUT} 60
6	HV_{OUT} 19	46	HV_{OUT} 59
7	HV_{OUT} 18	47	HV_{OUT} 58
8	HV_{OUT} 17	48	HV_{OUT} 57
9	HV_{OUT} 16	49	HV_{OUT} 56
10	HV_{OUT} 15	50	HV_{OUT} 55
11	HV_{OUT} 14	51	HV_{OUT} 54
12	HV_{OUT} 13	52	HV_{OUT} 53
13	HV_{OUT} 12	53	HV_{OUT} 52
14	HV_{OUT} 11	54	HV_{OUT} 51
15	HV_{OUT} 10	55	HV_{OUT} 50
16	HV_{OUT} 9	56	HV_{OUT} 49
17	HV_{OUT} 8	57	HV_{OUT} 48
18	HV_{OUT} 7	58	HV_{OUT} 47
19	HV_{OUT} 6	59	HV_{OUT} 46
20	HV_{OUT} 5	60	HV_{OUT} 45
21	HV_{OUT} 4	61	HV_{OUT} 44
22	HV_{OUT} 3	62	HV_{OUT} 43
23	HV_{OUT} 2	63	HV_{OUT} 42
24	HV_{OUT} 1	64	HV_{OUT} 41
25	$D_{I/O}$1A	65	HV_{OUT} 40
26	$D_{I/O}$2A	66	HV_{OUT} 39
27	N/C	67	HV_{OUT} 38
28	N/C	68	HV_{OUT} 37
29	$\overline{LE}$	69	HV_{OUT} 36
30	CLK	70	HV_{OUT} 35
31	$\overline{BL}$	71	HV_{OUT} 34
32	V_{SS}	72	HV_{OUT} 33
33	DIR	73	HV_{OUT} 32
34	V_{DD}	74	HV_{OUT} 31
35	-IN	75	HV_{OUT} 30
36	$D_{I/O}$2B	76	HV_{OUT} 29
37	$D_{I/O}$1B	77	HV_{OUT} 28
38	N/C	78	HV_{OUT} 27
39	+IN	79	HV_{OUT} 26
40	V_{BP}	80	HV_{OUT} 25

Notes:
1. Pin designation for DIR = V_{DD}.
2. A 0.1µF capacitor is needed between V_{DD} and V_{BP} (pin 40) for better output current stability and to prevent transient cross-coupling between outputs. See Fig. 8a and 8b.

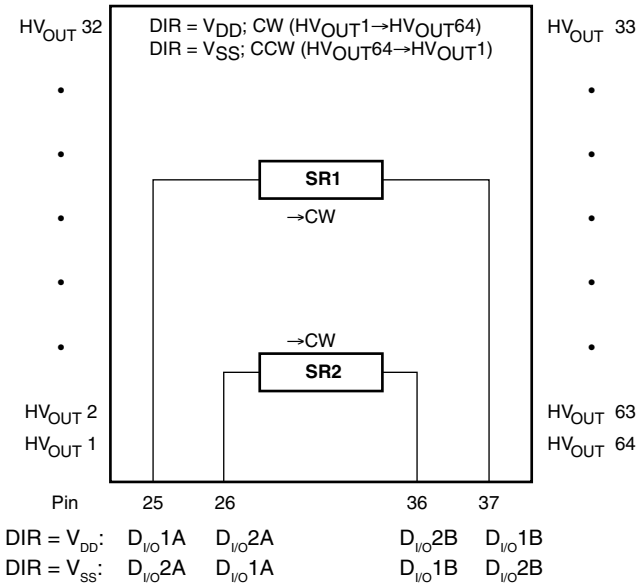
Figure 6: Package Outline



top view

80-pin Gullwing Package

Figure 7: Shift Register Operation



Typical Current Programming Circuits

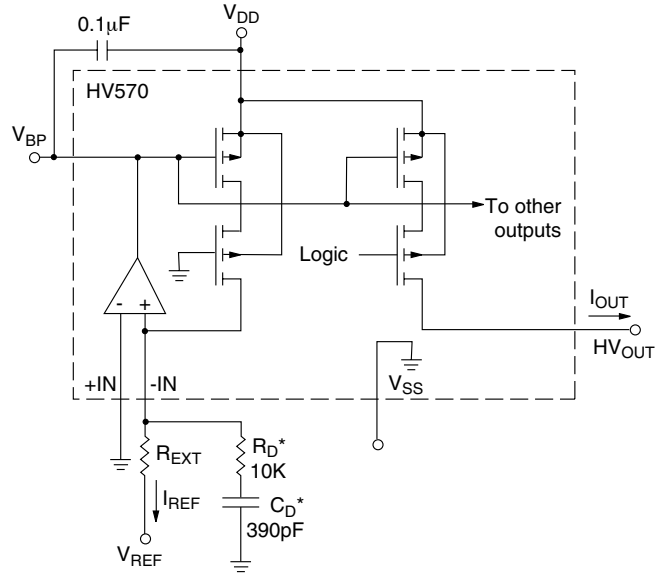


Figure 8a: Negative Control

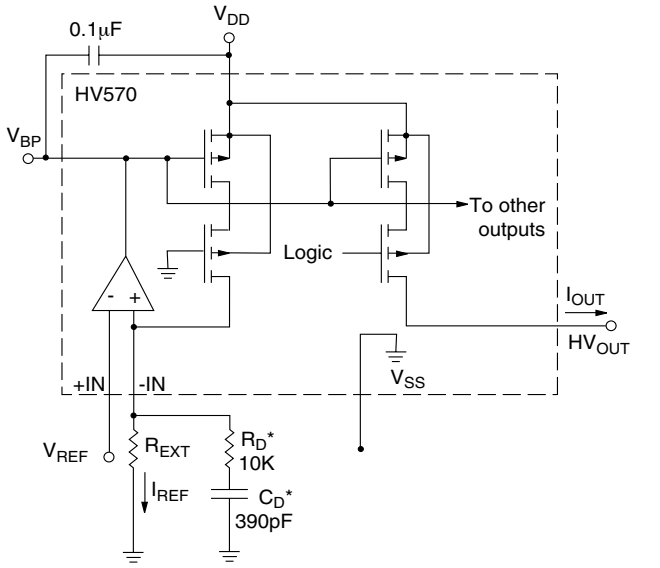


Figure 8b: Positive Control

*Required if R_{EXT} > 10K or R_{EXT} is replaced by a constant current source.

Since $I_{OUT} = I_{REF} = \frac{|V_{REF}|}{R_{EXT}}$

Therefore, if I_{OUT} = 2mA and V_{REF} = -5V → R_{EXT} = 2.5KΩ.

If I_{OUT} = 1mA and R_{EXT} = 1KΩ → V_{REF} = -1V.

If R_{EXT} >10KΩ, add series network R_D and C_D to ground for stability as shown.

This control method behaves linearly as long as the operational amplifier is not saturated. However, it requires a negative power source and needs to provide a current $I_{REF} = I_{OUT}$ for each HV570 chip being controlled.

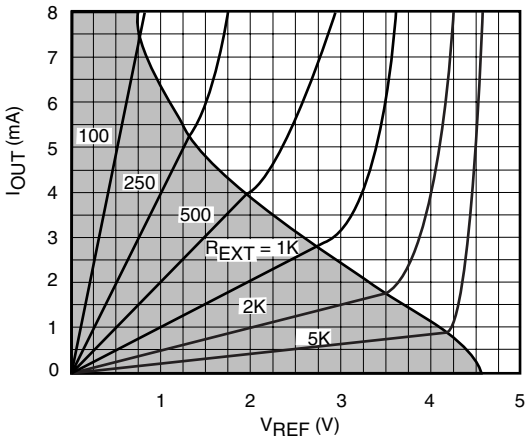
If $HV_{OUT} \geq +1V$, the HV_{OUT} cascode may no longer operate as a perfect current source, and the output current will diminish. This effect depends on the magnitude of the output current.

Given I_{OUT} and V_{REF}, the R_{EXT} can be calculated by using:

$$R_{EXT} = \frac{V_{REF}}{I_{REF}} = \frac{V_{REF}}{I_{OUT}}$$

The intersection of a set of I_{OUT} and V_{REF} values can be located in the graph shown below. The value picked for R_{EXT} must always be in the shaded area for linear operation. This control method has the advantage that V_{REF} is positive, and draws only leakage current. If R_{EXT} > 10K, add series network R_D and C_D to ground for stability as shown.

Note: Lower reference current I_{REF}, results in higher distortion, ΔI_{CS}, on the output.



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