WM9701A

Low Power AC'97 Multimedia Audio Codec

Production Data, January 2001, Rev 3.2

DESCRIPTION

The WM9701A is a high-quality stereo audio codec compliant with the Intel AC'97 Rev 1.03 specification. Forming the analogue component PC audio solution, it performs full-duplex 18-bit codec functions at 48 ksamples/s and offers excellent audio quality with high SNR.

In addition, the WM9701A provides a comprehensive analogue mixer with 4 sets of stereo inputs, plus phone, 2 microphone, and PC-beep inputs. On-chip reference circuits generate the necessary bias voltages for the device, and a 5-pin digital bi-directional serial interface allows transfer of control data and DAC and ADC words to and from the AC'97 controller.

The WM9701A is particularly suited to low power applications such as notebook PCs.

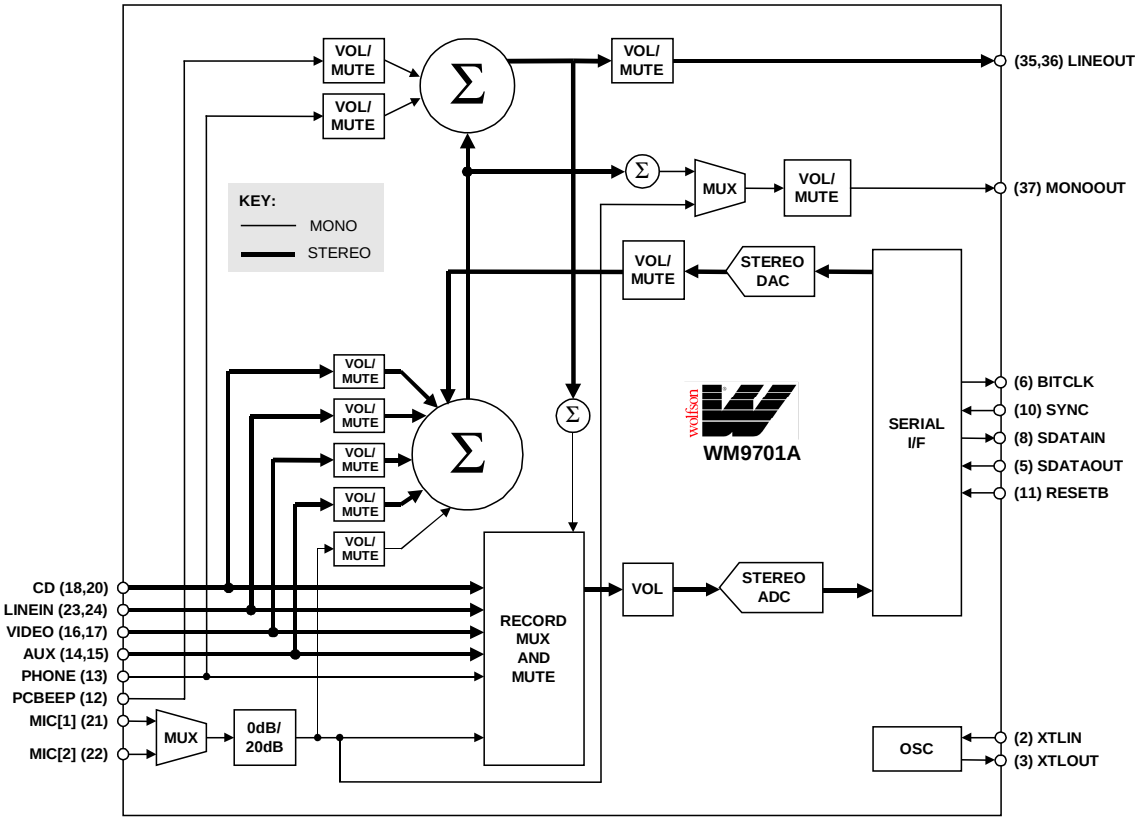
FEATURES

- 3.3V or 5V operation
- 18-bit stereo codec
- S/N ratio > 95dB
- Multiple stereo input mixer
- Mono and stereo volume control
- 48-pin TQFP package
- Power management features
- Very low standby power

APPLICATIONS

- Notebook PC
- PC sound cards
- Motherboards

BLOCK DIAGRAM



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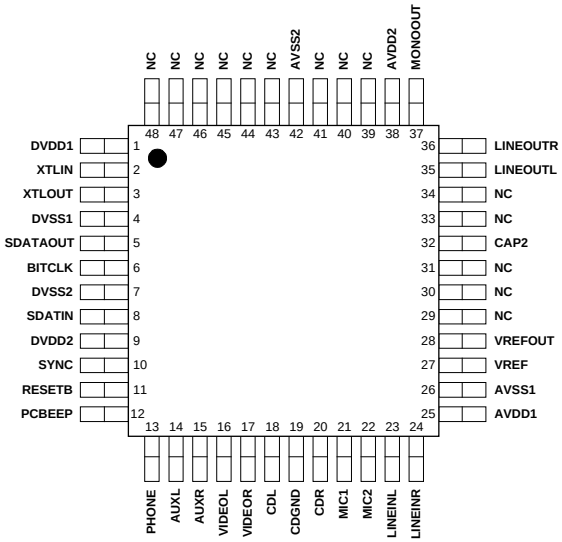
PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMP. RANGE	PACKAGE
WM9701ACFT/V	0^{o} to 70^{o}C	48-pin TQFP

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

As per specifications IPC/JEDEC J-STD-020A and JEDEC A113-B, this product requires specific storage conditions prior to surface mount assembly. It has been classified as having a Moisture Sensitivity Level of 2 and as such will be supplied in vacuum-sealed moisture barrier bags.

CONDITION	MIN	MAX
Digital supply voltage	-0.3V	+7V
Analogue supply voltage	-0.3V	+7V
Voltage range digital inputs	DVSS -0.3V	DVDD +0.3V
Voltage range analogue inputs	AVSS -0.3V	AVDD +0.3V
Operating temperature range, T_A	0^{o}C	$+70^{o}$C
Storage temperature	-65^{o}C	$+150^{o}$C
Package body temperature (soldering 10 seconds)		$+240^{o}$C
Package body temperature (soldering 2 minutes)		$+183^{o}$C

Note:

1. The digital supply voltage (DVDD) must always be less than or equal to the analogue supply voltage (AVDD).

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range	DVDD1, DVDD2	Note 1	-10%	3.3 to 5.0	+10%	V
Analogue supply range	AVDD1, AVDD2	Note 1	-10%	3.3 to 5.0	+10%	V
Digital ground	DVSS1, DVSS2			0		V
Analogue ground	AVSS1, AVSS2			0		V
Difference DVSS to AVSS			-0.3	0	+0.3	V
Analogue supply current		DVDD, AVDD = 5V		25		mA
Digital supply current		DVDD, AVDD = 5V		10		mA
Standby supply current (all PRs set)		DVDD, AVDD = 5V		30		µA
Analogue supply current		DVDD, AVDD = 3.3V		15		mA
Digital supply current		DVDD, AVDD = 3.3V		6		mA
Standby supply current (all PRs set)		DVDD, AVDD = 3.3V		20		µA

Note:

1. Both supplies should be powered on and off at the same time.

ELECTRICAL CHARACTERISTICS

Test Conditions:
AVDD = 5V, GND = 0V, DVDD = 3.3V, GND = 0V, T_A = 0°C to +70°C, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Logic Levels (DVDD = 3.3 or 5.0V)						
Input LOW level	V_{IL}		AVSS -0.3		0.8	V
Input HIGH level	V_{IH}		2.2		AVDD +0.3	V
Output LOW	V_{OL}				0.1 * VDD	V
Output HIGH	V_{OH}		0.9 * VDD			V
Analogue I/O Levels (Input Signals on any Inputs, Outputs on LINEOUT L, R and MONO)						
Input level		Minimum input impedance = 10k	AVSS -100mV		AVDD +100mV	V
Output level		Into 10kohm load	AVSS +100mV	Near rail to rail	AVDD -100mV	V
Reference Levels						
Reference input/output	CAP2		2/5 AVDD	AVDD/2	3/5 AVDD	V
CAP2 impedance				75		kohms
Mixer reference	VREF			Buffered CAP2		V
MIC reference	VREFOUT			Buffered CAP2		V
MIDBUFF current sink (pins VREF and VREFOUT)		AVDD = 5V	-5	-15		mA
MIDBUFF current source (pins VREF and VREFOUT)		AVDD = 5V	5	15		mA
MIDBUFF current source (pins VREF and VREFOUT)		AVDD = 3.3V		5		mA

Test Conditions:
AVDD = 5V, GND = 0V, DVDD = 3.3V, GND = 0V, T_A = 0°C to +70°C, unless otherwise stated.

DAC Circuit Specifications 48kHz Sampling						
SNR A-weighted (Note 1)		AVDD = 5V	85	96		dB
		AVDD = 3.3V		93		dB
Full scale output voltage		VREF = 2.5V		1.0		Vrms
		VREF = 1.65V		0.66		Vrms
THD		-3dBFS input	74 (0.2%)	90		dB
Frequency response			20		19,200	Hz
Transition band			19,200		28,800	Hz
Stop band			28,800			Hz
Out of band rejection				-40		dB
Spurious tone reduction				-100		dB
PSRR		20 to 20kHz		46		dB
ADC Circuit Specifications 48kHz Sampling						
SNR A-weighted (Note 1)		AVDD = 5V	75	92		dB
		AVDD = 3.3V		90		dB
ADC input for full scale output		VREF = 2.5V, AVDD = 5V		1.0		Vrms
		VREF = 1.65V, AVDD = 3.3V		0.66		Vrms
THD		-6dBV input	74	90		dB
Frequency response			20		19,200	Hz
Transition band			19,200		28,800	Hz
Stop band			28,800			Hz
Stop band rejection			-74 (0.2%)			dB
PSRR		20 to 20kHz		40		dB
Mixer Circuit Specifications 48kHz Sampling						
SNR CD path A-weighted (Note 1)		AVDD = 5V	90	95		dB
		AVDD = 3.3V		93		dB
SNR Other paths A-weighted (Note 1)		AVDD = 5V	85	95		dB
		AVDD = 3.3V		93		dB
Maximum input voltage			AVSS	1.0	AVDD	Vrms
				0.66		
Maximum output voltage on LINEOUT				1.0		Vrms
THD		0dBV input	-74 (0.2%)	-92		dB
Frequency response (+/-1dB)			20		20,000	Hz
Input impedance (CD inputs)		At any gain	10	15		kohm
Input impedance (other mixer inputs)		At max gain	10	20		kohm
		At 0db gain		100		kohm
Input impedance MIC inputs		At max gain		80		kohm
		At 0db gain	10	15		kohm
PSRR		20 to 20kHz		40		dB
Clock Frequency Range						
Crystal clock				24.576		MHz
BIT_CLK frequency				12.288		MHz
SYNC frequency				48.0		kHz

Note:

1. SNR is the ratio of 0dB full scale signal level to output level with no signal present, A-weighted and 20 - 20kHz bandwidth.

SERIAL INTERFACE

Test Conditions:
AVDD = 5V, GND = 0V, DVDD = 3.3V, GND = 0V, T_A = 0°C to +70°C, unless otherwise stated. All measurements are taken at 10% to 90% VDD, unless otherwise stated.

All the following timing information is guaranteed, not tested.

AC-LINK LOW POWER MODE

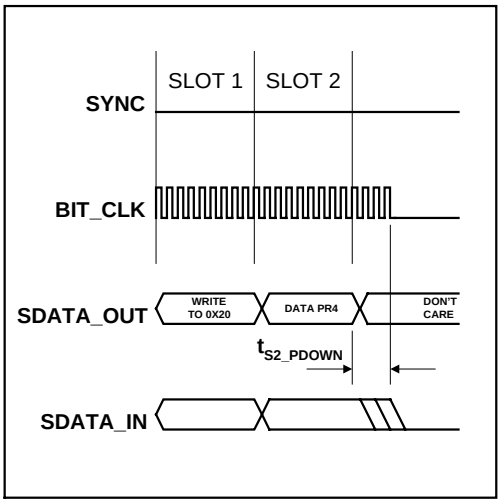


Figure 1 AC-Link Power down Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
End of slot 2 to BIT_CLK SDATA_IN low	t_{S2_PDOWN}			1.0	µs

COLD RESET

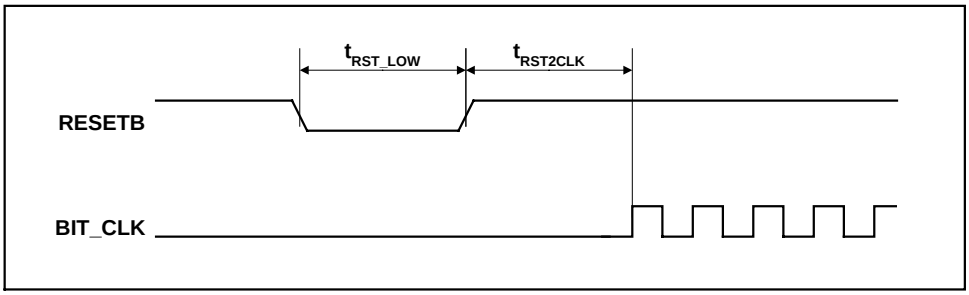


Figure 2 Cold Reset Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
RESETB active low pulse width	t_{RST_LOW}	1.0			µs
RESETB inactive to BIT_CLK startup delay	$t_{RST2CLK}$	162.8			ns

WARM RESET

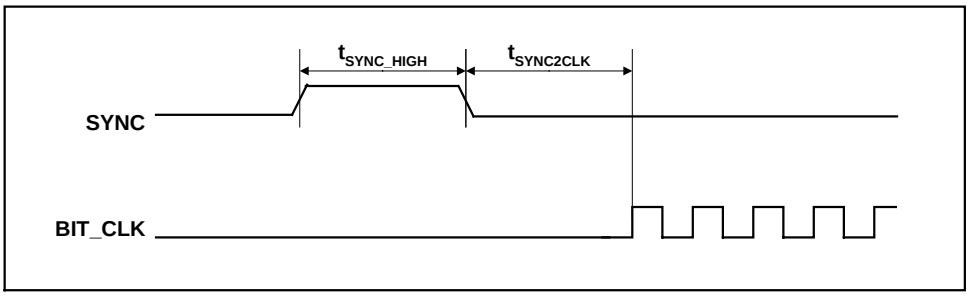


Figure 3 Warm Reset Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
SYNC active high pulse width	t_{SYNC_HIGH}		1.3		µs
SYNC inactive to BIT_CLK startup delay	$t_{SYNC2CLK}$	162.4			ns

CLOCK SPECIFICATIONS

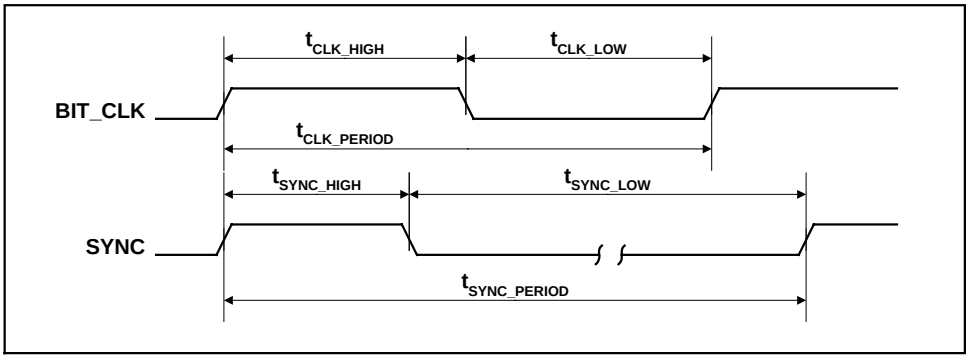


Figure 4 Clock Specifications (50pF External Load)

Note: Worst case duty cycle restricted to 40/60.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
BIT_CLK frequency			12.288		MHz
BIT_CLK period	t_{CLK_PERIOD}		81.4		ns
BIT_CLK output jitter				750	ps
BIT_CLK high pulse width (Note 1 on page 4)	t_{CLK_HIGH}	32.56	40.7	48.84	ns
BIT_CLK low pulse width (Note 1 on page 4)	t_{CLK_LOW}	32.56	40.7	48.84	ns
SYNC frequency			48.0		kHz
SYNC period	t_{SYNC_PERIOD}		20.8		µs
SYNC high pulse width	t_{SYNC_HIGH}		1.3		µs
SYNC low pulse width	t_{SYNC_LOW}		19.5		µs

DATA SETUP AND HOLD (50PF EXTERNAL LOAD)

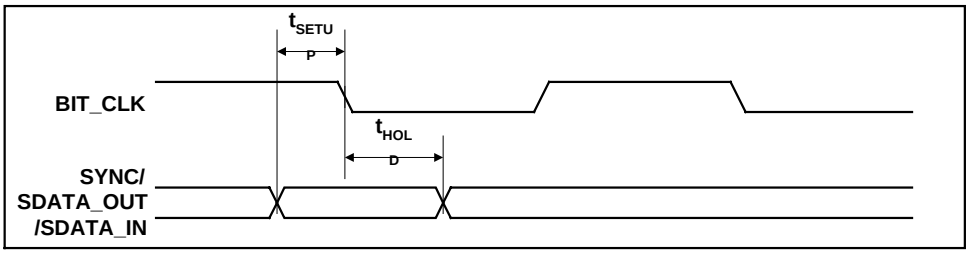


Figure 5 Data Setup and Hold (50pF External Load)

Note: Setup and hold time parameters for SDATA_IN are with respect to AC'97 Controller.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Setup to falling edge of BIT_CLK	t_{SETUP}	15.0			ns
Hold from falling edge of BIT_CLK	t_{HOLD}	5.0			ns

SIGNAL RISE AND FALL TIMES

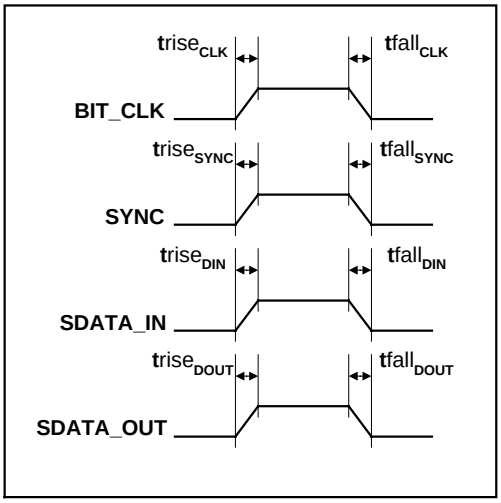


Figure 6 Signal Rise and Fall Times (50pF external load)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
BIT_CLK rise time	$trise_{CLK}$	2		6	ns
BIT_CLK fall time	$tfall_{CLK}$	2		6	ns
SYNC rise time	$trise_{SYNC}$	2		6	ns
SYNC fall time	$tfall_{SYNC}$	2		6	ns
SDATA_IN rise time	$trise_{DIN}$	2		6	ns
SDATA_IN fall time	$trise_{DIN}$	2		6	ns
SDATA_OUT rise time	$trise_{DOUT}$	2		6	ns
SDATA_OUT fall time	$tfall_{DOUT}$	2		6	ns

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	DVDD1	Supply	Digital positive supply
2	XTLIN	Digital input	Clock crystal connection or clock input (XTAL not used)
3	XTLOUT	Digital output	Clock crystal connection
4	DVSS1	Supply	Digital ground supply
5	SDATAOUT	Digital input	Serial data input
6	BITCLK	Digital output	Serial interface clock output to AC'97 controller
7	DVSS2	Supply	Digital ground supply
8	SDATAIN	Digital output	Serial data output to AC'97 controller
9	DVDD2	Supply	Digital positive supply
10	SYNC	Digital input	Serial interface sync pulse from AC'97 controller
11	RESETB	Digital input	NOT reset input (active low, resets registers)
12	PCBEEP	Analogue input	Mixer input, typically for PCBEEP signal
13	PHONE	Analogue input	Mixer input, typically for PHONE signal
14	AUXL	Analogue input	Mixer input, typically for AUX signal
15	AUXR	Analogue input	Mixer input, typically for AUX signal
16	VIDEOL	Analogue input	Mixer input, typically for VIDEO signal
17	VIDEOR	Analogue input	Mixer input, typically for VIDEO signal
18	CDL	Analogue input	Mixer input, typically for CD signal
19	CDGND	Analogue input	CD input common mode reference (ground)
20	CDR	Analogue input	Mixer input, typically for CD signal
21	MIC1	Analogue input	Mixer input with extra gain if required
22	MIC2	Analogue input	Mixer input with extra gain if required
23	LINEINL	Analogue input	Mixer input, typically for LINE signal
24	LINEINR	Analogue input	Mixer input, typically for LINE signal
25	AVDD1	Supply	Analogue positive supply
26	AVSS1	Supply	Analogue ground supply, chip substrate
27	VREF	Analogue output	Buffered CAP2, used as MIXER reference
28	VREFOUT	Analogue output	Reference for microphones; buffered CAP2
29	NC		No internal connection
30	NC		No internal connection
31	NC		No internal connection
32	CAP2	Analogue input	Reference input/output; pulls to midrail if not driven
33	NC		No internal connection
34	NC		No internal connection
35	LINEOUTL	Analogue output	Main analogue output for left channel
36	LINEOUTR	Analogue output	Main analogue output for right channel
37	MONOOUT	Analogue output	Main mono output
38	AVDD2	Supply	Analogue positive supply
39	NC		No internal connection
40	NC		No internal connection
41	NC		No internal connection
42	AVSS2	Supply	Analogue ground supply, chip substrate
43	NC		No internal connection
44	NC		No internal connection
45	NC		No internal connection
46	NC		No internal connection
47	NC		No internal connection
48	NC		No internal connection

DEVICE DESCRIPTION

INTRODUCTION

WM9701A is fully compatible with Rev 1.03 of the AC'97 specification.

WM9701A comprises a stereo 18-bit Codec, (that is, 2 ADCs and 2 DACs) plus a comprehensive analogue mixer with 4 sets of stereo inputs, plus phone, 2 microphone, and PC-beep inputs. Additionally, on-chip reference generation circuits generate the necessary bias voltages for the device, and a bi-directional serial interface allows transfer of control data and DAC and ADC words to and from the AC'97 controller. WM9701A supports 18-bit resolution within the DAC and ADC functions, but the AC'97 Codec serial interface specification allows any word length up to 20-bits to be written to, or read from, the AC'97 Codec. These words are MSB justified, and any LSBs not used will simply default to 0. Normally it is anticipated that 16-bit words will be used in most PC type systems. Therefore, for the DAC, 16-bit words will be downloaded into the Codec from the controller, along with padding of 0s to make the 16-bit word up to 20-bit length. In this case, WM9701A will process the 16-bit word along with 0 padding bits in the 2 LSB locations (to make 18-bit). At the ADC output, WM9701A will provide an 18-bit word, again with 0s in the two LSB locations (20-bit). The AC'97 controller will then ignore the 4 LSBs of the 20-bit word. When WM9701A is interrogated, it responds indicating it is an 18-bit device. However, a serial register controlled mode is available to allow these flags to be changed, making the device appear to be a 16-bit device.

The WM9701A has the ADC and DAC functions implemented using over sampled, or 'sigma-delta' converters, and uses on-chip digital filters to convert these 1-bit signals to and from the 48ks/s 16/18-bit PCM words that the AC'97 controller requires. The digital parts of the device are powered separately from the analogue to optimise performance, and 3.3V digital and 5V analogue supplies may be used on the same device to further optimise performance. Digital levels are 5V tolerant when the analogue supplies are 5V, so WM9701A may be connected to a controller running on 5V supplies, but using 3.3V for the digital section of WM9701A. WM9701A is also capable of operating with a 3.3V supply only (digital and analogue).

An internally generated mid-rail reference is provided at pin CAP2 which is used as the chip reference. This pin should be heavily decoupled.

The WM9701A is not limited to PC-only applications. The ability to power down sections of the device selectively, and the option to choose alternative master clock, and hence sample rates, means that many alternative applications in areas such as telecoms, may be anticipated. Internal connection of Pc-beep to the outputs in the case where the device is reset is supported.

CONTROL INTERFACE

A digital interface to control and transfer to and from the WM9701A has been provided. This serial interface is compatible with the Intel AC'97 specification as illustrated in the 'System Diagram'.

The main control interface functions are:

- Control of analogue gain and signal paths through the mixer.
- Bi-directional transfer of ADC and DAC words to and from AC'97 controller.
- Selection of power down modes.

AC-LINK DIGITAL SERIAL INTERFACE PROTOCOL

WM9701A incorporates a 5 pin digital serial interface that links it to the AC'97 controller. AC-link is a bi-directional, fixed rate, serial PCM digital stream. It handles multiple input, and output audio streams, as well as control register accesses employing a time division multiplexed (TDM) scheme. The AC-link architecture divides each audio frame into 12 outgoing and 12 incoming data streams, each with 20-bit sample resolution. With a minimum required DAC and ADC resolution of 16-bits, AC'97 may also be implemented with 18 or 20-bit DAC/ADC resolution, given the headroom that the AC-link architecture provides. WM9701A provides support for 18-bit operation.

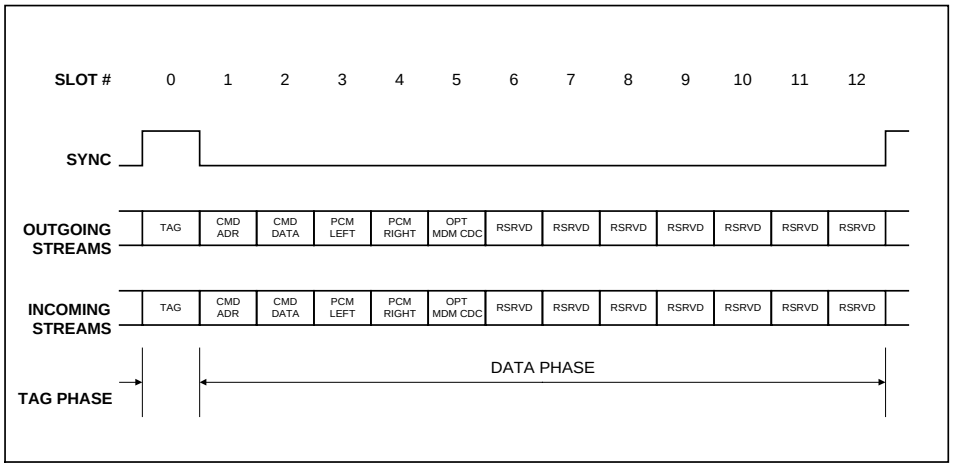


Figure 7 AC'97 Standard Bi-directional Audio Frame

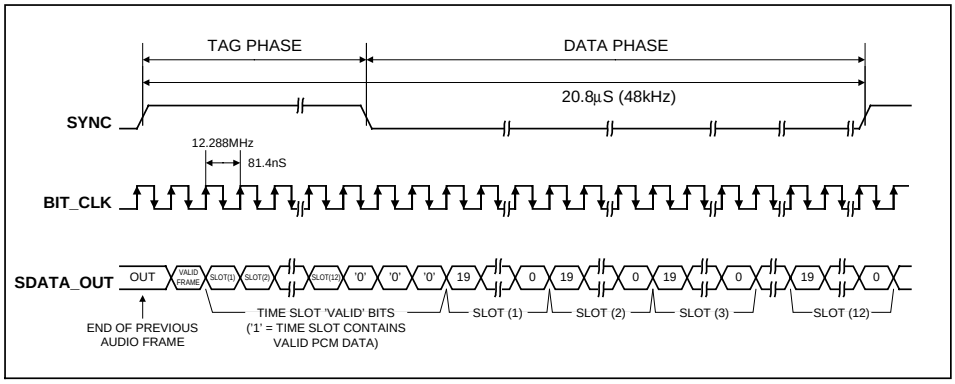


Figure 8 AC-link Audio Output Frame

The data streams currently defined by the AC'97 specification include:

PCM playback - 2 output slots	2 channel composite PCM output stream
PCM record data - 2 input slots	2 channel composite PCM input stream
Control 2 output slots	Control register write port
Status 2 input slots	Control register read port
Optional modem line Codec output - 1 output slot	Modem line Codec DAC input stream (Not supported by WM9701A)
Optional modem line Codec input - 1 input slot	Modem line Codec ADC output stream (Not supported by WM9701A)
Optional dedicated microphone input - 1 input slot	Dedicated microphone input stream in support of stereo AEC, and/or other voice applications. (Not supported by WM9701A)

Synchronisation of all AC-link data transactions is signalled by the WM9701A controller. WM9701A drives the serial bit clock onto AC-link, which the AC'97 controller then qualifies with a synchronisation signal to construct audio frames.

SYNC fixed at 48 kHz, is derived by dividing down the serial clock (BIT_CLK). BIT_CLK, fixed at 12.288 MHz, provides the necessary clocking granularity to support 12, 20-bit outgoing and incoming time slots. AC-link serial data is transitioned on each rising edge of BIT_CLK. The receiver of AC-link data, (WM9701A for outgoing data and the AC'97 controller for incoming data), samples each serial bit on the falling edges of BIT_CLK.

The AC-link protocol provides for a special 16-bit time slot (slot 0) wherein each bit conveys a valid tag for its corresponding time slot within the current audio frame. A 1 in a given bit position of slot 0 indicates that the corresponding time slot within the current audio frame has been assigned to a data stream, and contains valid data. If a slot is "tagged" invalid, it is the responsibility of the source of the data, (WM9701A for the input stream, AC'97 controller for the output stream); to stuff all bit positions with 0s during that slot's active time.

SYNC remains high for a total duration of 16 BIT CLKs at the beginning of each audio frame.

The portion of the audio frame where SYNC is high is defined as the “Tag Phase”. The remainder of the audio frame where SYNC is low is defined as the “Data Phase”. Additionally, for power savings, all clock, sync, and data signals can be halted. This requires that WM9701A be implemented as a static design to allow its register contents to remain intact when entering a power savings mode.

AC-LINK AUDIO OUTPUT FRAME (SDATA_OUT)

The audio output frame data streams correspond to the multiplexed bundles of all digital output data targeting WM9701A’s DAC inputs, and control registers. As briefly mentioned earlier, each audio output frame supports up to 12, 20-bit outgoing data time slots. Slot 0 is a special reserved time slot containing 16-bits, which are used for AC-link protocol infrastructure.

Within slot 0 the first bit is a global bit (SDATA_OUT slot 0, bit 15) which flags the validity for the entire audio frame. If the “Valid Frame” bit is a 1, this indicates that the current audio frame contains at least one time slot of valid data. The next 12-bit positions sampled by WM9701A indicate which of the corresponding 12 time slots contain valid data.

In this way data streams of differing sample rates can be transmitted across AC-link at its fixed 48 kHz audio frame rate. Figure 8 illustrates the time slot based AC-link protocol.

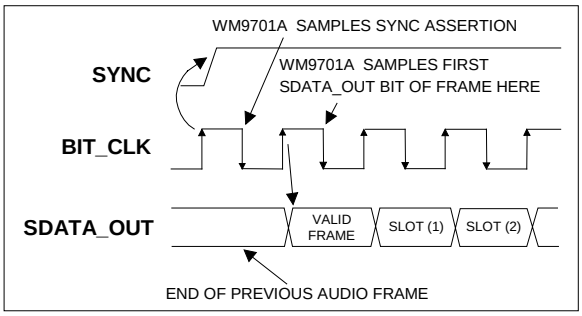


Figure 9 Start of an Audio Output Frame

A new audio output frame begins with a low to high transition of SYNC as shown in Figure 9. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, WM9701A samples the assertion of SYNC. This falling edge marks the time when both sides of AC-link are aware of the start of a new audio frame. On the next rising edge of BIT_CLK, AC’97 transitions SDATA_OUT into the first bit position of slot 0 (“Valid Frame” bit). Each new bit position is presented to AC-link on a rising edge of BIT_CLK, and subsequently sampled by the WM9701A on the following falling edge of BIT_CLK. This sequence ensures that data transitions and subsequent sample points for both incoming and outgoing data streams are time aligned.

Baseline AC’97 specified audio functionality MUST ALWAYS sample rate convert to and from a fixed 48 ks/s on the AC’97 controller.

This requirement is necessary to ensure that interoperability between the AC’97 controller and WM9701A, among other things, can be guaranteed by definition for baseline specified AC’97 features.

SDATA_OUT’s composite stream is MSB justified (MSB first) with all non-valid slot bit positions stuffed with 0s by the AC’97 controller.

In the event that there are less than 20 valid bits within an assigned and valid time slot, the AC’97 controller always stuffs all trailing non-valid bit positions of the 20-bit slot with 0s.

As an example, consider an 8-bit sample stream that is being played out to one of WM9701A’s DACs. The first 8-bit positions are presented to the DAC (MSB justified) followed by the next 12-bit-positions, which are stuffed with 0s by the AC’97 controller. This ensures that regardless of the resolution of the implemented DAC (16, 18 or 20-bit), no DC biasing will be introduced by the least significant bits.

When mono audio sample streams are output from the AC’97 controller, it is necessary that BOTH left and right sample stream time slots be filled with the same data.

SLOT 1: COMMAND ADDRESS PORT

The command port is used to control features, and monitor status for WM9701A functions including, but not limited to, mixer settings, and power management (refer to the register section). The control interface architecture supports up to 64, 16-bit read/write registers, addressable on even byte boundaries. Only the even registers (00h, 02h, etc.) are valid, odd register (01h, 03h, etc.) accesses are discouraged (if supported they should default to the preceding even byte boundary - i.e. a read to 01h will return the 16-bit contents of 00h. WM9701A's control register file is nonetheless readable as well as writeable to provide more robust testability.

Audio output frame slot 1 communicates control register address, and read/write command information to WM9701A.

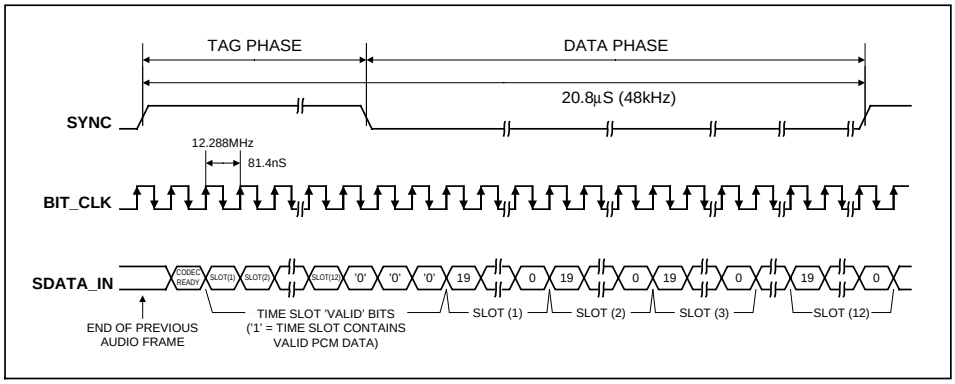


Figure 10 AC-link Audio Input Frame

COMMAND ADDRESS PORT BIT ASSIGNMENTS

Bit(19)	Read/write command (1 = read, 0 = write)
Bit(18:12)	Control register index (64 16-bit locations, addressed on even byte boundaries)
Bit(11:0)	Reserved (stuffed with 0s)

The first bit (MSB) sampled by WM9701A indicates whether the current control transaction is a read or write operation. The following 7 bit positions communicate the targeted control register address. The trailing 12 bit positions within the slot are reserved and must be stuffed with 0s by the AC'97 controller.

SLOT 2: COMMAND DATA PORT

The command data port is used to deliver 16-bit control register write data in the event that the current command port operation is a write cycle. (As indicated by slot 1, bit 19)

Bit(19:4)	Control register write data (stuffed with 0s if current operation is a read)
Bit(3:0)	Reserved (stuffed with 0s)

If the current command port operation is a read then the entire time slot must be stuffed with 0s by the AC'97 controller.

SLOT 3: PCM PLAYBACK LEFT CHANNEL

Audio output frame slot 3 is the composite digital audio left playback stream. In a typical 'Games Compatible' PC this slot is composed of standard PCM (.wav) output samples digitally mixed (on the AC'97 controller or host processor) with music synthesis output samples. If a sample stream of resolution less than 20-bits is transferred, the AC'97 controller must stuff all trailing non-valid bit positions within this time slot with 0s.

SLOT 4: PCM PLAYBACK RIGHT CHANNEL

Audio output frame slot 4 is the composite digital audio right playback stream. In a typical 'Games Compatible' PC this slot is composed of standard PCM (.wav) output samples digitally mixed (on the AC'97 controller or host processor) with music synthesis output samples.

If a sample stream of resolution less than 20-bits is transferred, the AC'97 controller must stuff all trailing non-valid bit positions within this time slot with 0s.

SLOT 5: OPTIONAL MODEM LINE CODEC

Audio output frame slot 5 contains the MSB justified modem DAC input data. This optional AC'97 feature is not supported in WM9701A, and if data is written to this location it is ignored. This may be determined by the AC'97 controller interrogating the WM9701A Vendor ID registers.

SLOTS 6-12: RESERVED

Audio output frame slots 6-12 are reserved for future use and are always stuffed with 0s by the AC'97 controller.

AC-LINK AUDIO INPUT FRAME (SDATA_IN)

The audio input frame data streams correspond to the multiplexed bundles of all digital input data targeting the AC'97 controller. As is the case for audio output frame, each AC-link audio input frame consists of 12, 20-bit time slots.

Slot 0 is a special reserved time slot containing 16-bits, which are used for AC-link protocol infrastructure.

Within slot 0 the first bit is a global bit (SDATA_IN slot 0, bit 15) which flags whether WM9701A is in the "Codec Ready" state or not. If the "Codec Ready" bit is a 0, this indicates that WM9701A is not ready for normal operation. This condition is normal following the desertion of power on reset for example, while WM9701A's voltage references settle. When the AC-link "Codec Ready" indicator bit is a 1 it indicates that the AC-link and WM9701A control and status registers are in a fully operational state. The AC'97 controller must further probe the power down Control/Status Register to determine exactly which subsections, if any, are ready.

Prior to any attempts at putting WM9701A into operation the AC'97 controller should poll the first bit in the audio input frame (SDATA_IN slot 0, bit 15) for an indication that WM9701A has gone "Codec Ready".

Once WM9701A is sampled "Codec Ready" then the next 12 bit positions sampled by the AC'97 controller indicate which of the corresponding 12 time slots are assigned to input data streams, and that they contain valid data. Figure 10 illustrates the time slot based AC-link protocol.

There are several subsections within WM9701A that can independently go busy/ready. It is the responsibility of the WM9701A controller to probe more deeply into the WM9701A register file to determine which WM9701A subsections are actually ready.

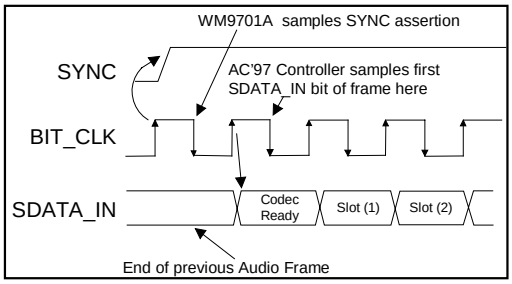


Figure 11 Start of an Audio Input Frame

A new audio input frame begins with a low to high transition of SYNC as shown in Figure 11. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, WM9701A samples the assertion of SYNC. This falling edge marks the time when both sides of AC-link are aware of the start of a new audio frame. On the next rising edge of BIT_CLK, the AC'97 controller transitions SDATA_IN into the first bit position of slot 0 (valid frame bit). Each new bit position is presented to AC-link on a rising edge of BIT_CLK, and subsequently sampled by the AC'97 controller on the following falling edge of BIT_CLK. This sequence ensures that data transitions and subsequent sample points for both incoming and outgoing data streams are time aligned.

SDATA_IN's composite stream is MSB justified (MSB first) with all non-valid bit positions (for assigned and/or unassigned time slots) stuffed with 0's by WM9701A. SDATA_IN is sampled on the falling edges of BIT_CLK .

SLOT 1: STATUS ADDRESS PORT

The status port is used to monitor status for WM9701A functions including, but not limited to, mixer settings, and power management.

Audio input frame slot 1 echoes the control register index, for historical reference, for the data to be returned in slot 2. (Assuming that slots 1 and 2 had been tagged "valid" by WM9701A during slot 0).

STATUS ADDRESS PORT BIT ASSIGNMENTS*:*

Bit(19)	RESERVED (stuffed with 0s)
Bit(18:12)	Control register index (echo of register index for which data is being returned)
Bit(11:0)	RESERVED (stuffed with 0s)

The first bit (MSB) generated by WM9701A is always stuffed with a 0. The following 7 bit positions communicate the associated control register address, and the trailing 12-bit positions are stuffed with 0s by WM9701A.

SLOT 2: STATUS DATA PORT

The status data port delivers 16-bit control register read data.

Bit(19:4)	Control register read data (stuffed with 0s if tagged "invalid" by WM9701)
Bit(3:0)	RESERVED (stuffed with 0s)

If slot 2 is tagged "invalid" by WM9701A, then the entire slot will be stuffed with 0s by WM9701A.

SLOT 3: PCM RECORD LEFT CHANNEL

Audio input frame slot 3 is the left channel output of WM9701A's input Mux, post-ADC.

WM9701A's ADCs can be implemented to support 16, 18, or 20-bit resolution. WM9701A ships out its ADC output data (MSB first), and stuffs any trailing non-valid bit positions with 0s to fill out its 20-bit time slot.

SLOT 4: PCM RECORD RIGHT CHANNEL

Audio input frame slot 4 is the right channel output of WM9701A's input Mux, post-ADC.

WM9701A's ADCs can be implemented to support 16, 18, or 20-bit resolution.

WM9701A ships out its ADC output data (MSB first), and stuffs any trailing non-valid bit positions with 0s to fill out its 20-bit time slot.

SLOT 5: OPTIONAL MODEM LINE CODEC

Audio input frame slot 5 contains MSB justified modem ADC output data. This optional feature is not supported by WM9701A. This may be determined by the AC'97 controller interrogating the WM9701A Vendor ID register.

SLOT 6: OPTIONAL DEDICATED MICROPHONE RECORD DATA

Audio input frame slot 6 is an optional (post-ADC) third PCM system input channel available for dedicated use by a desktop microphone. This optional AC'97 feature is not supported by WM9701A. This may be determined by the AC'97 controller interrogating the WM9701A Vendor ID register.

SLOTS 7-12: RESERVED

Audio input frame slots 7-12 are reserved for future use and are always stuffed with 0s by WM9701A.

AC-LINK LOW POWER MODE

The AC-link signals can be placed in a low power mode. When WM9701A's power down Register (26h), is programmed to the appropriate value, both BIT_CLK and SDATA_IN will be brought to, and held at a logic low voltage level.

BIT_CLK and SDATA_IN are transitioned low immediately following the decode of the write to the power down Register (26h) with PR4. When the AC'97 controller driver is at the point where it is ready to program the AC-link into its low power mode, slots 1 and 2 are assumed to be the only valid

stream in the audio output frame. At this point in time it is assumed that all sources of audio input have also been neutralised.

The AC'97 controller should also drive SYNC and SDATA_OUT low after programming WM9701A to this low power, "halted" mode.

Once WM9701A has been instructed to halt BIT_CLK, a special "wake up" protocol must be used to bring the AC-link to the active mode since normal audio output and input frames can not be communicated in the absence of BIT_CLK.

WAKING UP THE AC-LINK

There are 2 methods for bringing the AC-link out of a low power, halted mode. Regardless of the method, it is the AC'97 controller that performs the wake up task.

AC-link protocol provides for a "Cold WM9701A Reset", and a "Warm WM9701A Reset".

The current power down state would ultimately dictate which form of WM9701A reset is appropriate. Unless a "cold" or "register" reset (a write to the Reset register) is performed, wherein the WM9701A registers are initialised to their default values, registers are required to keep state during all power down modes.

Once powered down, re-activation of the AC-link via re-assertion of the SYNC signal must not occur for a minimum of 4 audio frame times following the frame in which the power down was triggered. When AC-link powers up it indicates readiness via the Codec Ready bit (input slot 0, bit 15).

COLD WM9701A RESET

A cold reset is achieved by asserting RESETB for the minimum specified time. By driving RESETB low, BIT_CLK, and SDATA_OUT will be activated, or re-activated as the case may be, and all WM9701A control registers will be initialised to their default power on reset values.

RESETB is an asynchronous WM9701A input.

WARM WM9701A RESET

A warm WM9701A reset will re-activate the AC-link without altering the current WM9701A register values. A warm reset is signaled by driving SYNC high for a minimum of 1µS in the absence of BIT_CLK.

Within normal audio frames SYNC is a synchronous WM9701A input. However, in the absence of BIT_CLK, SYNC is treated as an asynchronous input used in the generation of a warm reset to WM9701A. WM9701A will not respond with the activation of BIT_CLK until SYNC has been sampled low again by WM9701A. This will preclude the false detection of a new audio frame.

SERIAL INTERFACE REGISTER MAP DESCRIPTION

(See Table 10)

The serial interface bits perform control functions described as follows: The register map is fully specified by the AC'97 specification, and this description is simply repeated below, with optional unsupported features omitted.

RESET REGISTER (INDEX 00h)

Writing any value to this register performs a register reset, which causes all registers to revert to their default values. Reading this register returns the ID code of the part, indication of modem support (not supported by WM9701A) and a code for the type of 3D Stereo Enhancement (not supported by WM9701A).

The ID decodes the capabilities of WM9701A based on the following:

BIT	FUNCTION	VALUE ON WM9701A
ID0	Dedicated Mic PCM in channel	0
ID1	Modem line Codec support	0
ID2	Bass and treble control	0
ID3	Simulated stereo (mono to stereo)	0
ID4	Headphone out support	0
ID5	Loudness (bass boost) support	0
ID6	18-bit DAC resolution	1
ID7	20-bit DAC resolution	0
ID8	18-bit ADC resolution	1
ID9	20-bit ADC resolution	0
SE4....SE0	No stereo enhancement	00000

Table 1 Reset Register Function

Note that WM9701A defaults to indicate 18-bit compatibility. However, a control bit may be set in the vendor - specific registers that changes bits ID6 and ID8 to be '0', indicating a 16-bit device. It is unlikely that this function will be required, however, as the MSB justification of the ADC and DAC data means that a nominally 18-bit device should be fully compatible with controllers that only provide 16-bit support. (Most PC type applications will only require 16-bit operation).

PLAY MASTER VOLUME REGISTERS (INDEX 02h, 04h AND 06h)

These registers manage the output signal volumes. **Register 02h** controls the stereo master volume (both right and left channels), **Register 04h** controls the optional stereo headphone out, and **Register 06h** controls the mono volume output. Each step corresponds to 1.5dB. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at -∞dB.

ML5 to ML0 is for left channel level, MR5 through MR0 is for the right channel and MM5 to MM0 is for the mono out channel.

Support for the MSB of the level is not provided by WM9701A. If the MSB is written to then WM9701A detects when that bit is set and sets all 4 LSBs to 1s. Example: If the driver writes a 1xxxxx WM9701A interprets that as x11111. It will also respond when read with x11111 rather than 1xxxxx, the value written to it. The driver can use this feature to detect if support for the 6th bit is there or not.

The default value of both the mono and the stereo registers is 8000h (1000 0000 0000 0000), which corresponds to 0dB gain with mute on.

MUTE	MX4...MX0	FUNCTION
0	0 0000	0dB attenuation
0	0 0001	1.5dB attenuation
0	1 1111	46.5dB attenuation
1	x xxxx	∞dB attenuation

Table 2 Volume Register Function

MASTER TONE CONTROL REGISTERS (INDEX 08h)

Optional register for support of tone controls (bass and treble). WM9701A does not support bass and treble and writing to this register will have no effect, reading will result in all don't care values.

PC BEEP REGISTER (INDEX 0Ah)

This controls the level for the PC-beep input. Each step corresponds to approximately 3dB of attenuation. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at -∞dB.

WM9701A defaults to the PC-beep path being muted, so an external speaker should be provided within the PC to alert the user to power on self-test problems.

MUTE	PV3...PV0	FUNCTION
0	0000	0dB attenuation
0	1111	45dB attenuation
1	xxxx	∞dB attenuation

Table 3 PC-beep Register Function

ANALOGUE MIXER INPUT GAIN REGISTERS (INDEX 0CH - 18h)

This controls the gain/attenuation for each of the analogue inputs. Each step corresponds to approximately 1.5dB. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at -∞dB.

REGISTER 0EH (MIC VOLUME REGISTER)

This has an extra bit that is for a 20dB boost. When bit 6 is set to 1 the 20dB boost is on. The default value is 8008, which corresponds to 0dB gain with mute on.

The default value for the mono registers is 8008h, which corresponds to 0dB gain with mute on. The default value for stereo registers is 8808h, which corresponds to 0dB gain with mute on.

MUTE	GX4...GX0	FUNCTION
0	00000	+12dB gain
0	01000	0dB gain
0	11111	-34.5dB gain
1	xxxxx	-∞dB gain

Table 4 Mixer Gain Control Register Function

RECORD SELECT CONTROL REGISTER (INDEX 1Ah)

Used to select the record source independently for right and left. (see Table 5 for legend). The default value is 0000h, which corresponds to Mic in.

SR2 -SR0	RIGHT RECORD SOURCE	SL2-SL0	LEFT RECORD SOURCE
0	Mic	0	Mic
1	CD in (R)	1	CD in (L)
2	Video in (R)	2	Video in (L)
3	Aux in (R)	3	Aux in (L)
4	Line in (R)	4	Line in (L)
5	Stereo mix (R)	5	Stereo mix (L)
6	Mono mix	6	Mono mix
7	Phone	7	Phone

Table 5 Record Select Register Function

RECORD GAIN REGISTERS (INDEX 1Ch AND 1Eh)

1Ch is for the stereo input and 1Eh is for the optional special purpose correlated audio Mic channel. Each step corresponds to 1.5dB. 22.5dB corresponds to 0F0Fh and 000Fh respectively. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel(s) is set at -∞dB.

The default value is 8000h, which corresponds to 0dB gain with mute on.

MUTE	GX3...GX0	FUNCTION
0	1111	+22.5dB gain
0	0000	0dB gain
1	xxxxx	-∞dB gain

Table 6 Record Gain Register Function

GENERAL PURPOSE REGISTER (INDEX 20h)

This register is used to control several miscellaneous functions of the WM9701A.

Below is a summary of each bit and its function. Only the MIX, MS and LPBK bits are supported by WM9701A. The MS bit controls the Mic selector. The LPBK bit enables loop back of the ADC output to the DAC input without involving the AC-link, allowing for full system performance measurements. The function default value is 0000h which is all off.

BIT	FUNCTION	WM9701A SUPPORT
POP	PCM out path and mute, 0 = pre 3D, 1 = post 3D	No
ST	Simulated stereo enhancement, on/off 1 = on	No
3D	3D stereo enhancement on/off, 1 = on	No
LD	Loudness (bass boost) on/off, 1 = on	No
LLBK	Local loop back - for modem, line Codec	No
RLBK	Remote loop back - for modem, line Codec	No
MIX	Mono output select 0 = Mix, 1 = Mic	Yes
MS	Mic select 0 = Mic1, 1 = Mic2	Yes
LPBK	ADC/DAC/ loop back mode	Yes

Table 7 General Purpose Register Function

3D CONTROL REGISTER (INDEX 22h)

This optional register is used to control the centre and/or depth of the 3D stereo enhancement function built into of the AC'97 component. This feature is not supported by the WM9701A.

MODEM SAMPLE RATE REGISTER (INDEX 24h)

This register controls what sample rate AC'97 is sending or receiving samples for the optional Modem in and out. This feature is not supported by WM9701A.

POWER DOWN CONTROL/STATUS REGISTER (INDEX 26h)

This read/write register is used to program power down states and monitor subsystem readiness. The lower half of this register is read only status, a 1 indicating that the subsection is "*ready*". *Ready* is defined as the subsection able to perform in its nominal state. When this register is written to the bit values that come in on AC-link will have no effect on read only bits 0 to 7.

When the AC-link "Codec Ready" indicator bit (SDATA_IN slot 0, bit 15) is a 1 it indicates that the AC-link and WM9701A control and status registers are in a fully operational state. The AC'97 controller must further probe this power down Control/Status Register to determine exactly which subsections, if any, are ready.

READ BIT	FUNCTION
MDM	Modem section ready – not supported
REF	VREFs up to nominal level
ANL	Analogue mixers, etc ready
DAC	DAC section ready to accept data
ADC	ADC section ready to transmit data

Table 8 Power Down Status Register Function

The power down modes are as follows. The first three bits are to be used individually rather than in combination with each other. The last bit PR3 can be used in combination with PR2 or by itself. PR0 and PR1 control the PCM ADCs and DACs only. PR7 independently controls the optional modem ADC and DAC, not supported by WM9701A.

WRITE BIT	FUNCTION
PR0	PCM in ADCs and input Mux power down
PR1	PCM out DACs power down
PR2	Analogue mixer power down (VREF still on)
PR3	Analogue mixer power down (VREF off)
PR4	Digital interface (AC-Link) power down (external clock off)
PR5	Internal clock disable
PR6	HP amp power down - not supported
PR7	Modem ADC/DAC off - not supported

Table 9 Power Down Control Register Function

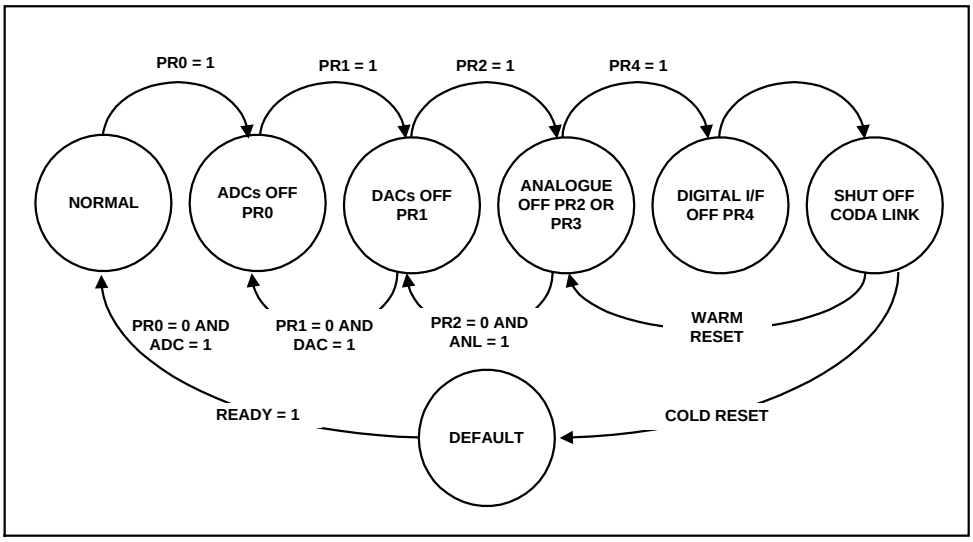


Figure 12 An Example of WM9701A Power Down/Power up Flow

Figure 12 illustrates one example procedure to do a complete power down of WM9701A. From normal operation sequential writes to the power down Register are performed to power down WM9701A a piece at a time. After everything has been shut off, a final write (of PR4) can be executed to shut down the WM9701A's digital interface (AC-link).

The part will remain in sleep mode with all its registers holding their static values. To wake up WM9701A, the AC'97 controller will send a pulse on the sync line issuing a warm reset. This will restart WM9701A's digital interface (resetting PR4 to 0). WM9701A can also be woken up with a cold reset. A cold reset will cause a loss of values of the registers, as a cold reset will set them to their default states. When a section is powered back on, the power down Control/Status register (index 26h) should be read to verify that the section is ready (i.e. stable) before attempting any operation that requires it.

Alternatively if RESETB is held low, all PR bits are held set so the device is held powered off until RESETB is taken high again.

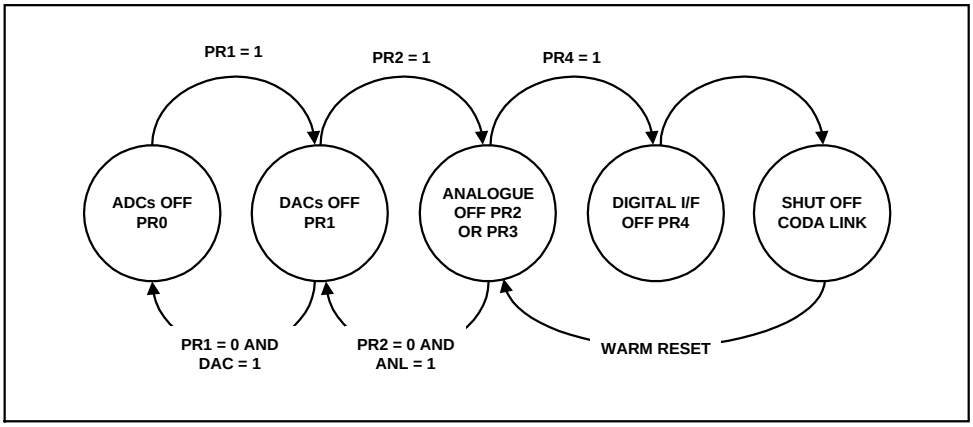


Figure 13 WM9701A Power Down/Flow with Analogue Still Alive

Figure 13 illustrates a state when all the mixers should work with the static volume settings that are contained in their associated registers. This is used when the user could be playing a CD (or external LINE_IN source) through WM9701A to the speakers but have most of the system in low power mode. The procedure for this follows the previous except that the analogue mixer is never shut down.

POWERDOWN CONTROL/STATUS REGISTER (INDEX 26H)

Also when RESETB pin is asserted low, all PR bits are over-ridden and the entire device is powered off to ultra low power state for as long as RESETB = low. On releasing RESETB, the device is reset (all active) and powered up.

RESERVED REGISTERS (INDEX 28h - 58h)

These registers are reserved by AC'97 and have no function on WM9701A.

VENDOR RESERVED REGISTERS (INDEX 5AH - 7Ah)

These are reserved for future use and are vendor specific. Do not write to these registers unless the Vendor ID register has been checked first to ensure that the driver knows the source of the AC'97 component. Values stored in this register are used to provide test modes for the manufacturer.

VENDOR SPECIFIC GAIN CONTROL REGISTERS – (INDEX 70H TO 74H)

Not used in the WM9701A.

VENDOR ID REGISTERS (INDEX 7Ch - 7Eh)

This register is for specific vendor identification if so desired. The ID method is Microsoft's Plug and Play Vendor ID code. The first character of that ID is F7 to F0, the second character S7 to S0 and the third T7 to T0. These three characters are ASCII encoded. The REV7 to REV0 field is for the Vendor Revision number. In WM9701A the vendor ID is set to WML0.

Wolfson is a registered Microsoft Plug and Play vendor.

SERIAL INTERFACE REGISTER MAP

The following table shows the function and address of the various control bits that are loaded through the serial interface during write operations.

Reg. Num.	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	X	SE4	SE3	SE2	SE1	SEO	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	0140h
02h	Master Volume	Mute	X	X	ML4	ML3	ML2	ML1	ML0	X	X	X	MR4	MR3	MR2	MR1	MM0	8000h
06h	Master Vol. Mono	Mute	X	X	X	X	X	X	X	X	X	X	MM4	MM3	MM2	MM1	MM0	8000h
0Ah	PCBEEP Volume	Mute	X	X	X	X	X	X	X	X	X	X	PV3	PV2	PV2	PV0	X	8000h
OCh	Phone Volume	Mute	X	X	X	X	X	X	X	X	X	X	GN4	GN3	GN2	GN1	GN0	8008h
OEh	Mic Volume	Mute	X	X	X	X	X	X	X	X	20 dB	X	GN4	GN3	GN2	GN1	GN0	8008h
10h	Line In Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
12h	CD Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
14h	Video Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
16h	Aux Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
18h	PCM Out Vol.	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
1Ah	Record Select	X		X	X	X	SL2	SL1	SL0	X	X	X	X	X	SR2	SR1	SR0	0000h
1Ch	Record Gain	Mute	X	X	X	GL3	GL2	GL1	GL0	X	X	X	X	GR3	GR2	GR1	GR0	8000h
20h	General Purpose	X	X	X	X	X	X	MIX	MS	LPBK	X	X	X	X	X	X	X	0000h
26H	Power-down Ctrl/Stat	X	X	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	000Fh
28h	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
5Ah	Vendor Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
7Ah	Vendor Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	574D
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	REV 7	REV 6	REV 5	REV 4	REV 3	REV 2	REV 1	REV 0	4COO

Table 10 Serial Interface Register Map Description

RECOMMENDED EXTERNAL COMPONENTS

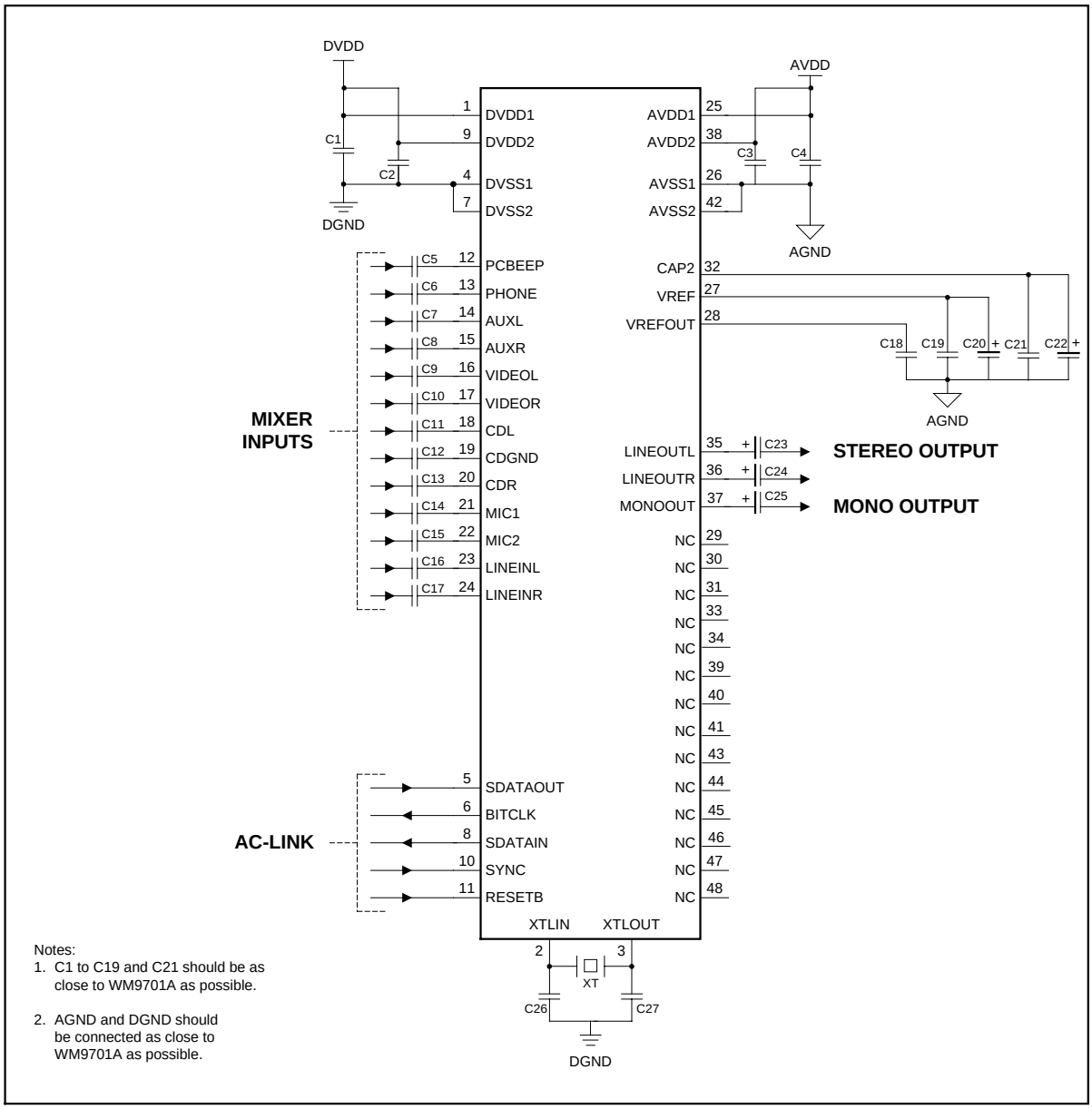


Figure 14 External Components Diagram

RECOMMENDED EXTERNAL COMPONENTS VALUES

COMPONENT REFERENCE	SUGGESTED VALUE	DESCRIPTION
C1 to C4	10nF	De-coupling for DVDD and AVDD
C5 to C17	470nF	AC coupling capacitors for setting DC level of analogue inputs. Value chosen to give corner frequency below 20Hz for minimum 10K input impedance.
C18	1µF	Reference de-coupling capacitors for ADC, DAC, Mixer and CAP2 references. Ceramic type or similar.
C19	0.1µF	
C20	10µF	
C21	0.1µF	
C22	10µF	
C23 to C25	10µF	Output AC coupling caps to remove VREF DC level from outputs.
C26 and C27	22pF	Optional capacitors for better crystal frequency stability.
XT	24.576 MHz	AC'97 master clock frequency. A bias resistor is not required, but if connected will not affect operation if value is large (above 1MΩ).

Table 11 External Component Recommendations

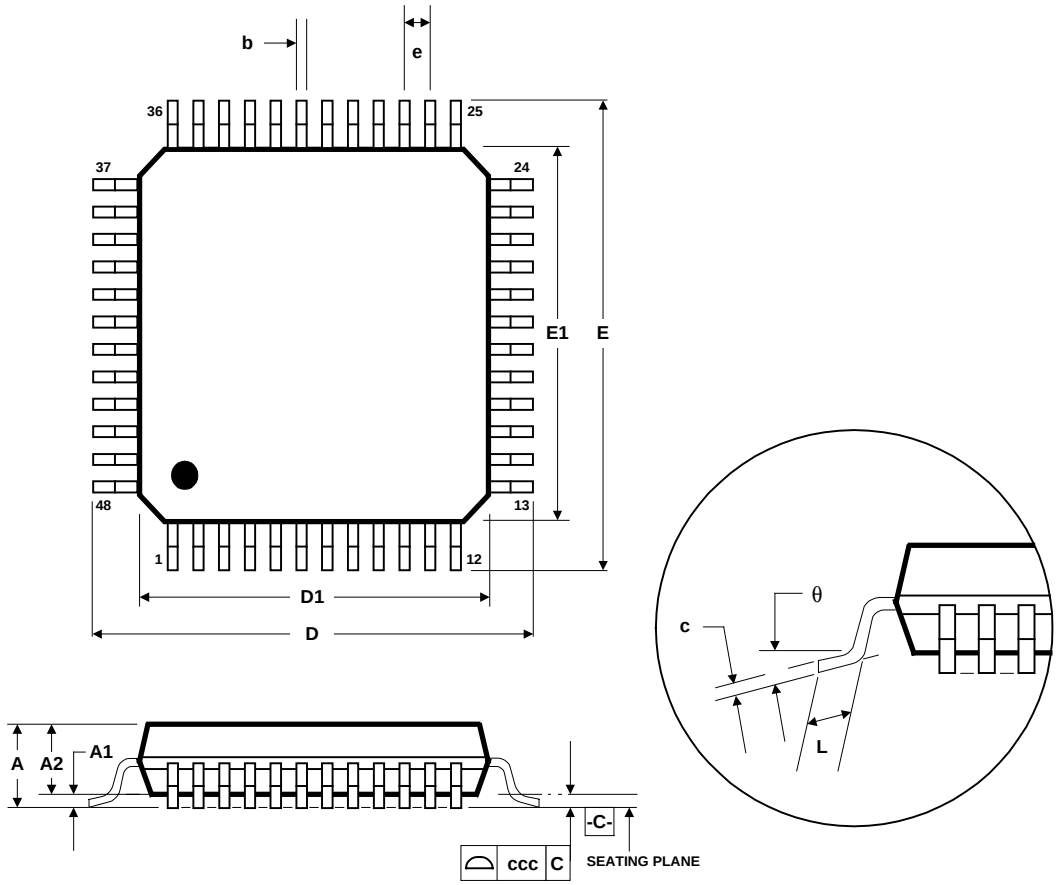
RECOMMENDATIONS FOR 3.3V OPERATION

The device's performance with AVDD = 3.3V is shown in Electrical Characteristics.

In 3.3V analogue operation, mid-rail reference scales to 1.5V. All ADC and DAC references are 3/5^{ths} of their nominal 5V value. Input and output signals that are 1Vrms in 5V applications, scale to 660mVrms in 3.3V applications. If 1Vrms output is required, the mixer gain adjust PGAs need to be increased by 3 times 1.5dB steps.

PACKAGE DIMENSIONS

FT: 48 PIN TQFP (7 x 7 x 1.4 mm) **DM003.B**



Symbols	Dimensions (mm)		
	MIN	NOM	MAX
A	-----	-----	1.60
A_1	0.05	-----	0.15
A_2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	-----	0.20
D	9.00 BSC		
D_1	7.00 BSC		
E	9.00 BSC		
E_1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
θ	0^o	3.5^o	7^o
Tolerances of Form and Position			
ccc	0.08		
REF:	JEDEC.95, MS-026		

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM.
D. MEETS JEDEC.95 MS-026, VARIATION = BBC. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.