# ANALOG DEVICES

# Ultracompact Precision 10 V/5 V/2.5 V/3.0 V Voltage References

## ADR01/ADR02/ADR03/ADR06

### FEA E

C70-5/ -5

L

IC-8: 3 /°C

C70-5/ -5: 9 /°C

I 0.1%

L 10 - (0.1 H 10 H )

AD 01: 12 40

AD 02: 7 40

AD 03: 4.5 40

AD 06: 5.0 40

H 10 A

: 40°C +125°C

AD 01/AD 02/AD 03 -
EF01/ EF02/ EF03[1]

### A LICA I

H

I

CMCIA

### ELEC I G IDE

| | |
|---|---|
| ADR01 | 10.0 V |
| ADR02 | 5.0 V |
| ADR03 | 2.5 V |
| ADR06 | 3.0 V |

[1] ADR01, ADR02, and ADR03 are component-level compatible with REF01, REF02, and REF03, respectively. No guarantees for system-level compatibility are implied. SOIC-8 versions of ADR01/ADR02/ADR03 are pin-to-pin compatible with SOIC-8 versions of REF01/REF02/REF03, respectively, with the additional temperature monitoring function.

### I C FIG A I

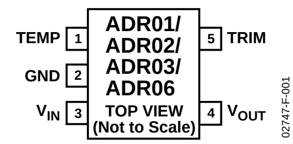


*Figure 1. 5-Lead SC70/TSOT Surface-Mount Packages*

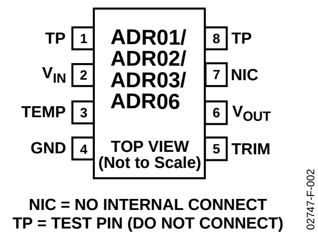


*Figure 2. 8-Lead SOIC Surface-Mount Package*

### GE E AL DE C I I

The ADR01, ADR02, ADR03, and ADR06 are precision 10 V, 5 V, 2.5 V, and 3.0 V band gap voltage references featuring high accuracy, high stability, and low power. The parts are housed in tiny SC70-5 and TSOT-5 packages, as well as the SOIC-8 versions. The SOIC-8 versions of the ADR01, ADR02, and ADR03 are drop-in replacements[1] to the industry-standard REF01, REF02, and REF03. The small footprint and wide operating range make the ADR0x references ideally suited for general-purpose and space-constraint applications.

With an external buffer and a simple resistor network, the TEMP terminal can be used for temperature sensing and approximation. A TRIM terminal is provided on the devices for fine adjustment of the output voltage.

The ADR01, ADR02, ADR03, and ADR06 are compact, low drift voltage references that provide an extremely stable output voltage from a wide supply voltage range. They are available in SC70-5, TSOT-5, and SOIC-8 packages with A and B grade selections. All parts are specified over the extended industrial (–40°C to +125°C) temperature range.




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# SPECIFICATIONS

## AD 01 ELEC ICAL CHA AC E I IC

$V_{IN}$ = 12 V to 40 V, $T_A$ = 25°C, unless otherwise noted.

**Table 1.**

| | | C | M | | M | |
|---|---|---|---|---|---|---|
| Output Voltage | $V_O$ | A and C grades | 9.990 | 10.000 | 10.010 | V |
| Initial Accuracy | $V_{OERR}$ | A and C grades | | | 10 | mV |
| | | | | | 0.1 | % |
| Output Voltage | $V_O$ | B grade | 9.995 | 10.000 | 10.005 | V |
| Initial Accuracy | $V_{OERR}$ | B grade | | | 5 | mV |
| | | | | | 0.05 | % |
| Temperature Coefficient | $TCV_O$ | A grade, SOIC-8, –40°C < $T_A$ < +125°C | | 3 | 10 | ppm/°C |
| | | A grade, TSOT-5, –40°C < $T_A$ < +125°C | | | 25 | ppm/°C |
| | | A grade, SC70-5, –40°C < $T_A$ < +125°C | | | 25 | ppm/°C |
| | | B grade, SOIC-8, –40°C < $T_A$ < +125°C | | 1 | 3 | ppm/°C |
| | | B grade, TSOT-5, –40°C < $T_A$ < +125°C | | | 9 | ppm/°C |
| | | B grade, SC70-5, –40°C < $T_A$ < +125°C | | | 9 | ppm/°C |
| | | C grade, SOIC-8, –40°C < $T_A$ < +125°C | | 10 | 40 | ppm/°C |
| Supply Voltage Headroom | $V_{IN} – V_O$ | | 2 | | | V |
| Line Regulation | $\Delta V_O/\Delta V_{IN}$ | $V_{IN}$ = 12 V to 40 V, –40°C < $T_A$ < +125°C | | 7 | 30 | ppm/V |
| Load Regulation | $\Delta V_O/\Delta I_{LOAD}$ | $I_{LOAD}$ = 0 to 10 mA, –40°C < $T_A$ < +125°C, $V_{IN}$ = 15 V | | 40 | 70 | ppm/mA |
| Quiescent Current | $I_{IN}$ | No load, –40°C < $T_A$ < +125°C | | 0.65 | 1 | mA |
| Voltage Noise | $e_{N\ p\text{-}p}$ | 0.1 Hz to 10 Hz | | 20 | | µV p-p |
| Voltage Noise Density | $e_N$ | 1 kHz | | 510 | | nV/√Hz |
| Turn-On Settling Time | $t_R$ | | | 4 | | µs |
| Long-Term Stability[1] | $\Delta V_O$ | 1,000 hours | | 50 | | ppm |
| Output Voltage Hysteresis | $\Delta V_{O\_HYS}$ | | | 70 | | ppm |
| Ripple Rejection Ratio | RRR | $f_{IN}$ = 10 kHz | | −75 | | dB |
| Short Circuit to GND | $I_{SC}$ | | | 30 | | mA |
| Voltage Output at TEMP Pin | $V_{TEMP}$ | | | 550 | | mV |
| Temperature Sensitivity | $TCV_{TEMP}$ | | | 1.96 | | mV/°C |

[1] The long-term stability specification is noncumulative. The drift in subsequent 1,000 hour periods is significantly lower than in the first 1,000 hour period.

## AD 02 ELEC ICAL CHA AC E I IC

$V_{IN}$ = 7 V to 40 V, $T_A$ = 25°C, unless otherwise noted.

**Table 2.**

| | | C | M | | M | |
|---|---|---|---|---|---|---|
| Output Voltage | $V_O$ | A and C grades | 4.995 | 5.000 | 5.005 | V |
| Initial Accuracy | $V_{OERR}$ | A and C grades | | | 5 | mV |
| | | | | | 0.1 | % |
| Output Voltage | $V_O$ | B grade | 4.997 | 5.000 | 5.003 | V |
| Initial Accuracy | $V_{OERR}$ | B grade | | | 3 | mV |
| | | | | | 0.06 | % |
| Temperature Coefficient | $TCV_O$ | A grade, SOIC-8, –40°C < $T_A$ < +125°C | | 3 | 10 | ppm/°C |
| | | A grade, TSOT-5, –40°C < $T_A$ < +125°C | | | 25 | ppm/°C |
| | | A grade, SC70-5, –40°C < $T_A$ < +125°C | | | 25 | ppm/°C |
| | | A grade. SC70-5, -55ºC < TA < +125ºC | | | 30 | ppm/°C |
| | | B grade, SOIC-8, –40°C < $T_A$ < +125°C | | 1 | 3 | ppm/°C |
| | | B grade, TSOT-5, –40°C < $T_A$ < +125°C | | | 9 | ppm/°C |
| | | B grade, SC70-5, –40°C < $T_A$ < +125°C | | | 9 | ppm/°C |
| | | C grade, SOIC-8, –40°C < $T_A$ < +125°C | | 10 | 40 | ppm/°C |
| Supply Voltage Headroom | $V_{IN} – V_O$ | | 2 | | | V |
| Line Regulation | $\Delta V_O/\Delta V_{IN}$ | $V_{IN}$ = 7 V to 40 V, –40°C < $T_A$ < +125°C | | 7 | 30 | ppm/V |
| | | $V_{IN}$ = 7 V to 40 V, –55°C < $T_A$ < +125°C | | 7 | 40 | ppm/V |
| Load Regulation | $\Delta V_O/\Delta I_{LOAD}$ | $I_{LOAD}$ = 0 to 10 mA, –40°C < $T_A$ < +125°C, $V_{IN}$ = 10 V | | 40 | 70 | ppm/mA |
| | | $I_{LOAD}$ = 0 to 10 mA, –55°C < $T_A$ < +125°C, $V_{IN}$ = 10 V | | 45 | 80 | ppm/mA |
| Quiescent Current | $I_{IN}$ | No load, –40°C < $T_A$ < +125°C | | 0.65 | 1 | mA |
| Voltage Noise | $e_{N\ p\text{-}p}$ | 0.1 Hz to 10 Hz | | 10 | | µV p-p |
| Voltage Noise Density | $e_N$ | 1 kHz | | 230 | | nV/√Hz |
| Turn-On Settling Time | $t_R$ | | | 4 | | µs |
| Long-Term Stability[1] | $\Delta V_O$ | 1,000 hours | | 50 | | ppm |
| Output Voltage Hysteresis | $\Delta V_{O\_HYS}$ | | | 70 | | ppm |
| | | –55°C < $T_A$ < +125°C | | 80 | | ppm |
| Ripple Rejection Ratio | RRR | $f_{IN}$ = 10 kHz | | –75 | | dB |
| Short Circuit to GND | $I_{SC}$ | | | 30 | | mA |
| Voltage Output at TEMP Pin | $V_{TEMP}$ | | | 550 | | mV |
| Temperature Sensitivity | $TCV_{TEMP}$ | | | 1.96 | | mV/°C |

[1] The long-term stability specification is noncumulative. The drift in subsequent 1,000 hour periods is significantly lower than in the first 1,000 hour period.

## AD 03 ELEC ICAL CHA AC E I IC

$V_{IN}$ = 4.5 V to 40 V, $T_A$ = 25°C, unless otherwise noted.

**Table 3.**

| | | C | M | | M | |
|---|---|---|---|---|---|---|
| Output Voltage | $V_O$ | A and C grades | 2.495 | 2.500 | 2.505 | V |
| Initial Accuracy | $V_{OERR}$ | A and C grades | | | 5 | mV |
| | | | | | 0.2 | % |
| Output Voltage | $V_O$ | B grades | 2.4975 | 2.5000 | 2.5025 | V |
| Initial Accuracy | $V_{OERR}$ | B grades | | | 2.5 | mV |
| | | | | | 0.1 | % |
| Temperature Coefficient | $TCV_O$ | A grade, SOIC-8, –40°C < $T_A$ < +125°C | | 3 | 10 | ppm/°C |
| | | A grade, TSOT-5, –40°C < $T_A$ < +125°C | | | 25 | ppm/°C |
| | | A grade, SC70-5, –40°C < $T_A$ < +125°C | | | 25 | ppm/°C |
| | | A grade, SC70-5, –55°C < $T_A$ < +125°C | | | 30 | ppm/°C |
| | | B grade, SOIC-8, –40°C < $T_A$ < +125°C | | 1 | 3 | ppm/°C |
| | | B grade, TSOT-5, –40°C < $T_A$ < +125°C | | | 9 | ppm/°C |
| | | B grade, SC70-5, –40°C < $T_A$ < +125°C | | | 9 | ppm/°C |
| | | C grade, SOIC-8, –40°C < $T_A$ < +125°C | | 10 | 40 | ppm/°C |
| Supply Voltage Headroom | $V_{IN} – V_O$ | | 2 | | | V |
| Line Regulation | $\Delta V_O/\Delta V_{IN}$ | $V_{IN}$ = 7.5 V to 40 V, –40°C < $T_A$ < +125°C | | 7 | 30 | ppm/V |
| | | $V_{IN}$ = 7.5 V to 40 V, –55°C < $T_A$ < +125°C | | 7 | 40 | ppm/V |
| Load Regulation | $\Delta V_O/\Delta I_{LOAD}$ | $I_{LOAD}$ = 0 mA to 10 mA, –40°C < $T_A$ < +125°C, $V_{IN}$ = 7.0 V | | 25 | 70 | ppm/mA |
| | | $I_{LOAD}$ = 0 mA to 10 mA, –55°C < $T_A$ < +125°C, $V_{IN}$ = 7.0 V | | 45 | 80 | ppm/mA |
| Quiescent Current | $I_{IN}$ | No load, –40°C < $T_A$ < +125°C | | 0.65 | 1 | mA |
| Voltage Noise | $e_{N\ p\text{-}p}$ | 0.1 Hz to 10 Hz | | 6 | | µV p-p |
| Voltage Noise Density | $e_N$ | 1 kHz | | 230 | | nV/√Hz |
| Turn-On Settling Time | $t_R$ | | | 4 | | µs |
| Long-Term Stability[1] | $\Delta V_O$ | 1,000 hours | | 50 | | ppm |
| Output Voltage Hysteresis | $\Delta V_{O\_HYS}$ | | | 70 | | ppm |
| | | –55°C < $T_A$ < +125°C | | 80 | | ppm |
| Ripple Rejection Ratio | RRR | $f_{IN}$ = 10 kHz | | –75 | | dB |
| Short Circuit to GND | $I_{SC}$ | | | 30 | | mA |
| Voltage Output at TEMP Pin | $V_{TEMP}$ | | | 550 | | mV |
| Temperature Sensitivity | $TCV_{TEMP}$ | | | 1.96 | | mV/°C |

[1] The long-term stability specification is noncumulative. The drift in subsequent 1,000 hour periods is significantly lower than in the first 1,000 hour period.

## AD 06 ELEC ICAL CHA AC E I IC

$V_{IN}$ = 5.0 V to 40 V, $T_A$ = 25°C, unless otherwise noted.

**Table 4.**

| | | C | M | | M | |
|---|---|---|---|---|---|---|
| Output Voltage | $V_O$ | A and C grades | 2.994 | 3.000 | 3.006 | V |
| Initial Accuracy | $V_{OERR}$ | A and C grades | | | 6 | mV |
| | | | | | 0.2 | % |
| Output Voltage | $V_O$ | B grade | 2.997 | 3.000 | 3.003 | V |
| Initial Accuracy | $V_{OERR}$ | B grade | | | 3 | mV |
| | | | | | 0.1 | % |
| Temperature Coefficient | $TCV_O$ | A grade, SOIC-8, –40°C < $T_A$ < +125°C | | 3 | 10 | ppm/°C |
| | | A grade, TSOT-5, –40°C < $T_A$ < +125°C | | | 25 | ppm/°C |
| | | A grade, SC70-5, –40°C < $T_A$ < +125°C | | | 25 | ppm/°C |
| | | B grade, SOIC-8, –40°C < $T_A$ < +125°C | | 1 | 3 | ppm/°C |
| | | B grade, TSOT-5, –40°C < $T_A$ < +125°C | | | 9 | ppm/°C |
| | | B grade, SC70-5, –40°C < $T_A$ < +125°C | | | 9 | ppm/°C |
| | | C grade, SOIC-8, –40°C < $T_A$ < +125°C | | 10 | 40 | ppm/°C |
| Supply Voltage Headroom | $V_{IN} - V_O$ | | 2 | | | V |
| Line Regulation | $\Delta V_O/\Delta V_{IN}$ | $V_{IN}$ = 15 V to 40 V, –40°C < $T_A$ < +125°C | | 7 | 30 | ppm/V |
| Load Regulation | $\Delta V_O/\Delta I_{LOAD}$ | $I_{LOAD}$ = 0 to 10 mA, –40°C < $T_A$ < +125°C, $V_{IN}$ = 7.0 V | | 40 | 70 | ppm/mA |
| Quiescent Current | $I_{IN}$ | No load, –40°C < $T_A$ < +125°C | | 0.65 | 1 | mA |
| Voltage Noise | $e_{N\ p\text{-}p}$ | 0.1 Hz to 10 Hz | | 10 | | µV p-p |
| Voltage Noise Density | $e_N$ | 1 kHz | | 510 | | nV/√Hz |
| Turn-On Settling Time | $t_R$ | | | 4 | | µs |
| Long-Term Stability[1] | $\Delta V_O$ | 1,000 hours | | 50 | | ppm |
| Output Voltage Hysteresis | $\Delta V_{O\_HYS}$ | | | 70 | | ppm |
| Ripple Rejection Ratio | RRR | $f_{IN}$ = 10 kHz | | –75 | | dB |
| Short Circuit to GND | $I_{SC}$ | | | 30 | | mA |
| Voltage Output AT TEMP Pin | $V_{TEMP}$ | | | 550 | | mV |
| Temperature Sensitivity | $TCV_{TEMP}$ | | | 1.96 | | mV/°C |

[1] The long-term stability specification is noncumulative. The drift in subsequent 1,000 hour periods is significantly lower than in the first 1,000 hour period.

## DICE ELEC ICAL CHA AC E I IC

$V_{IN}$ = up to 40 V, $T_A$ = 25°C, unless otherwise noted.

**Table 5.**

| | | C | M | | M | |
|---|---|---|---|---|---|---|
| Output Voltage | | | | | | |
| ADR01NBC | $V_O$ | 25°C | 9.995 | 10.004 | 10.005 | V |
| ADR02NBC | $V_O$ | 25°C | 4.997 | 5.002 | 5.003 | V |
| Temperature Coefficient | $TCV_O$ | $-40°C < T_A < +125°C$ | | 10 | | ppm/°C |
| Line Regulation | | | | | | |
| ADR01NBC | $\Delta V_O/\Delta V_{IN}$ | $V_{IN}$ = 15 V to 40 V | | 7 | | ppm/V |
| ADR02NBC | $\Delta V_O/\Delta V_{IN}$ | $V_{IN}$ = 7 V to 40 V | | 7 | | ppm/V |
| Load Regulation | $\Delta V_O/\Delta I_{LOAD}$ | $I_{LOAD}$ = 0 to 10 mA | | 40 | | ppm/mA |
| Quiescent Current | $I_{IN}$ | No load | | 0.65 | | mA |
| Voltage Noise | $e_{N\ p\text{-}p}$ | 0.1 Hz to 10 Hz | | 25 | | µV p-p |

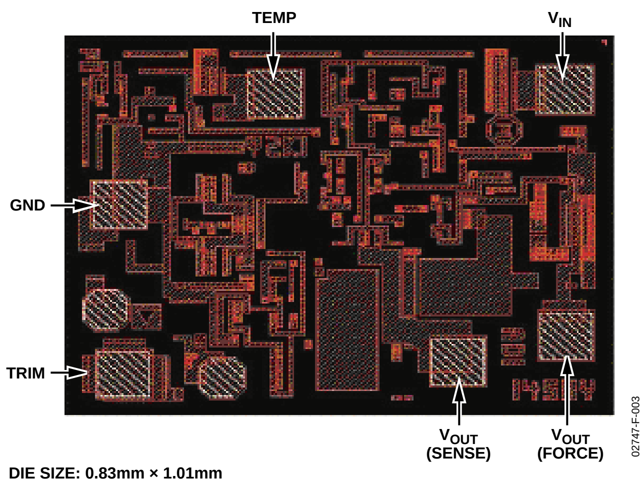


*Figure 3. Die Layout*

## ABSOLUTE MAXIMUM RATINGS

Ratings at 25°C, unless otherwise noted.

**Table 6.**

| | |
|---|---|
| Supply Voltage | 40 V |
| Output Short-Circuit Duration to GND | Indefinite |
| Storage Temperature Range | −65°C to +150°C |
| Operating Temperature Range | −40°C to +125°C |
| Junction Temperature Range: KS, UJ, and R Packages | −65°C to +150°C |
| Lead Temperature Range (Soldering, 60 Sec) | 300°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 7. Thermal Resistance**

| k | $\theta_{JA}$[1] | $\theta_{JC}$ | |
|---|---|---|---|
| SC70-5 (KS-5) | 376 | 189 | °C/W |
| TSOT-5 (UJ-5) | 230 | 146 | °C/W |
| SOIC-8 (R-8) | 130 | 43 | °C/W |

[1] $\theta_{JA}$ is specified for the worst-case conditions, that is, $\theta_{JA}$ is specified for devices soldered in circuit boards for surface-mount packages.

### E DCA I

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although these products feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

# PARAMETER DEFINITIONS

### *Temperature Coefficient*

The change of output voltage with respect to operating temperature changes normalized by the output voltage at 25°C. This parameter is expressed in ppm/°C and can be determined by the following equation:

$$TCV_O[ppm/°C] = \frac{V_O(T_2) - V_O(T_1)}{V_O(25°C) \times T_2 - T_1} \times 10^6$$

where:
$V_O(25°C) = V_O$ at 25°C
$V_O(T_1) = V_O$ at Temperature 1
$V_O(T_2) = V_O$ at Temperature 2

### *Line Regulation*

The change in output voltage due to a specified change in input voltage. This parameter accounts for the effects of self-heating. Line regulation is expressed in either percent per volt, parts-per-million per volt, or microvolts per volt change in input voltage.

### *Load Regulation*

The change in output voltage due to a specified change in load current. This parameter accounts for the effects of self-heating. Load regulation is expressed in either microvolts per milliampere, parts-per-million per milliampere, or ohms of dc output resistance.

### *Long-Term Stability*

Typical shift of output voltage at 25°C on a sample of parts subjected to a test of 1,000 hours at 25°C:

$$\Delta V_O = V_O(t_0) - V_O(t_1)$$

$$\Delta V_O[ppm] = \frac{V_O(t_0) - V_O(t_1)}{V_O(t_0)} \times 10^6$$

where:
$V_O(t_0) = V_O$ at 25°C at Time 0
$V_O(t_1) = V_O$ at 25°C after 100 hours of operation at 25°C

The majority of the shift is seen in the first 200 hours, and, as time goes by, the drift decreases significantly. So for the subsequent 1,000 hours' time points, this drift is much smaller than the first.

### *Thermal Hysteresis*

Defined as the change of output voltage after the device is cycled through temperature from +25°C to −40°C to +125°C and back to +25°C. This is a typical value from a sample of parts put through such a cycle.

$$V_{O\_HYS} = V_O(25°C) - V_{O\_TC}$$

$$V_{O\_HYS}[ppm] = \frac{V_O(25°C) - V_{O\_TC}}{V_O(25°C)} \times 10^6$$

where:
$V_O(25°C) = V_O$ at 25°C
$V_{O\_TC} = V_O$ at 25°C after temperature cycle at +25°C to −40°C to +125°C and back to +25°C

E

### *Input Capacitor*

Input capacitors are not required on the ADR01/ADR02/ADR03/ADR06. There is no limit for the value of the capacitor used on the input, but a 1 μF to 10 μF capacitor on the input improves transient response in applications where the supply suddenly changes. An additional 0.1 μF in parallel also helps to reduce noise from the supply.

### *Output Capacitor*

The ADR01/ADR02/ADR03/ADR06 do not require output capacitors for stability under any load condition. An output capacitor, typically 0.1 μF, filters out any low level noise voltage and does not affect the operation of the part. On the other hand, the load transient response can be improved with an additional 1 μF to 10 μF output capacitor in parallel. A capacitor here acts as a source of stored energy for a sudden increase in load current. The only parameter that degrades by adding an output capacitor is the turn-on time, and it depends on the size of the capacitor chosen.

## TYPICAL PERFORMANCE CHARACTERISTICS

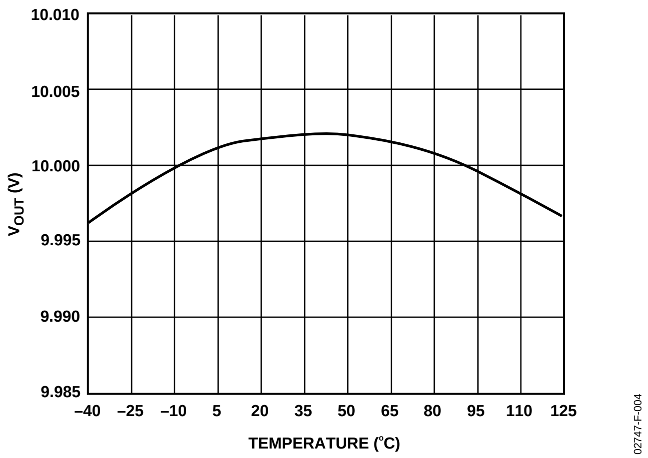


*Figure 4. ADR01 Typical Output Voltage vs. Temperature*

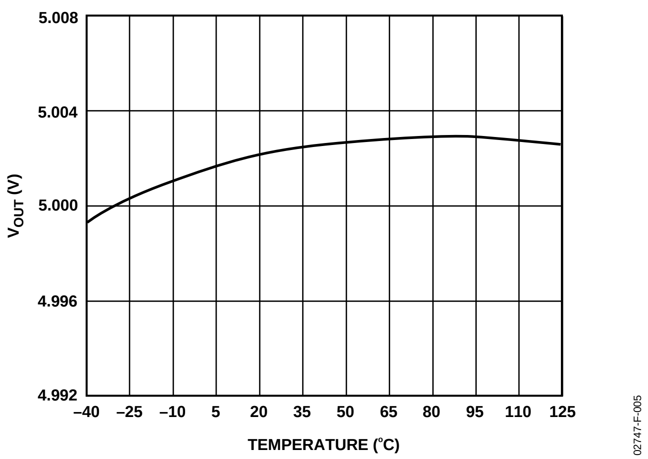


*Figure 5. ADR02 Typical Output Voltage vs. Temperature*

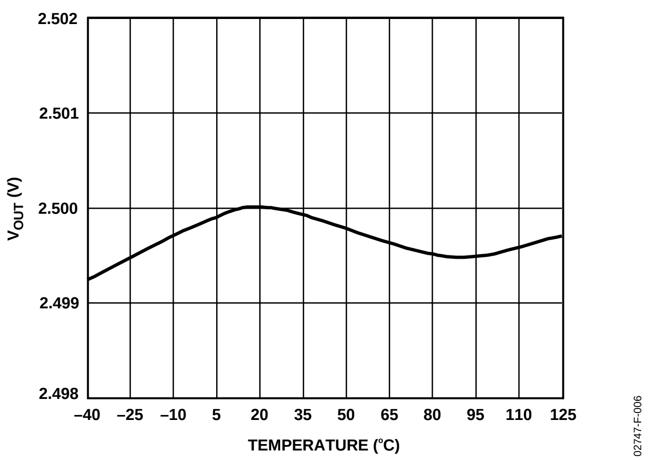


*Figure 6. ADR03 Typical Output Voltage vs. Temperature*

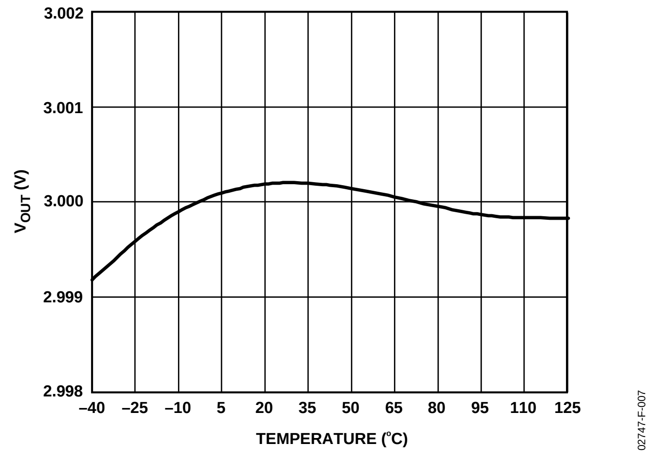


*Figure 7. ADR06 Typical Output Voltage vs. Temperature*

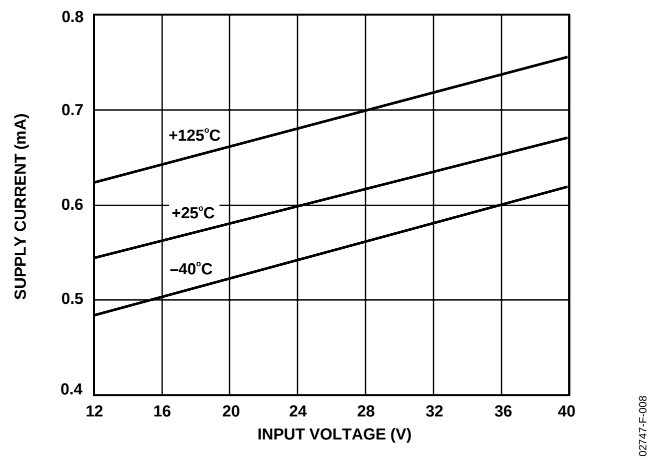


*Figure 8. ADR01 Supply Current vs. Input Voltage*

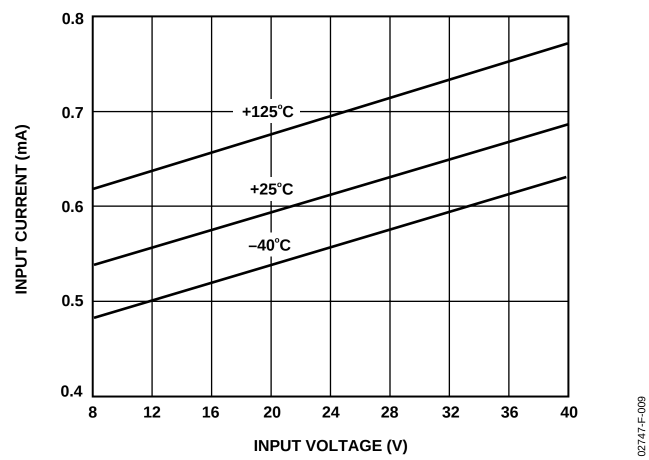


*Figure 9. ADR02 Supply Current vs. Input Voltage*

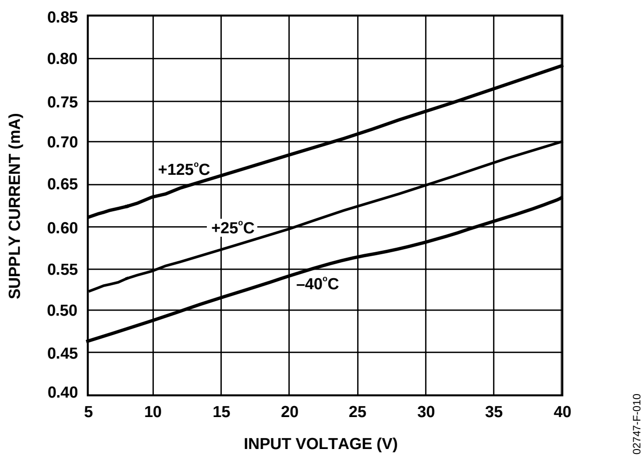


*Figure 10. ADR03 Supply Current vs. Input Voltage*

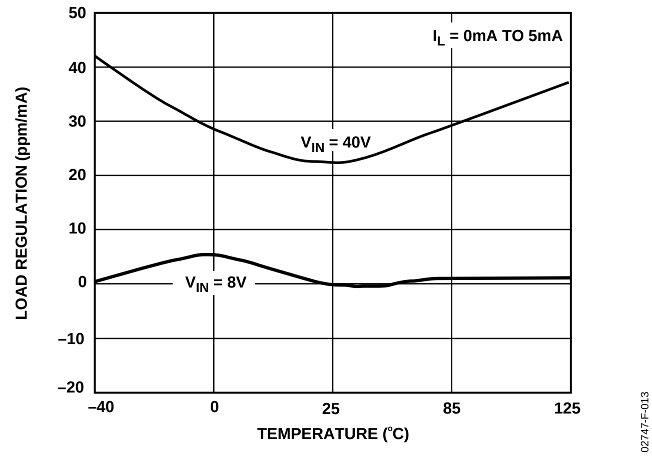


*Figure 13. ADR02 Load Regulation vs. Temperature*

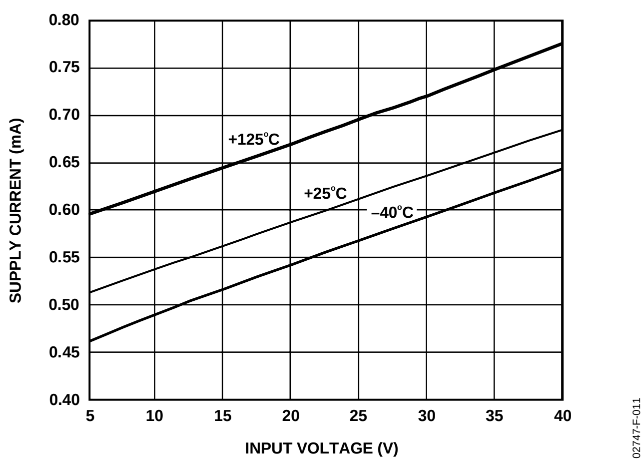


*Figure 11. ADR06 Supply Current vs. Input Voltage*

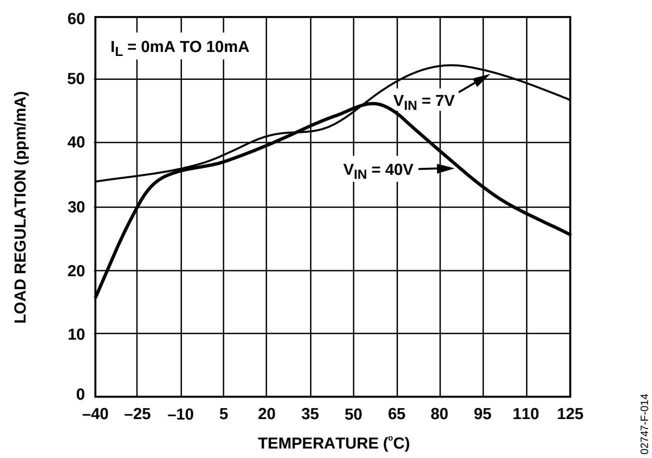


*Figure 14. ADR03 Load Regulation vs. Temperature*

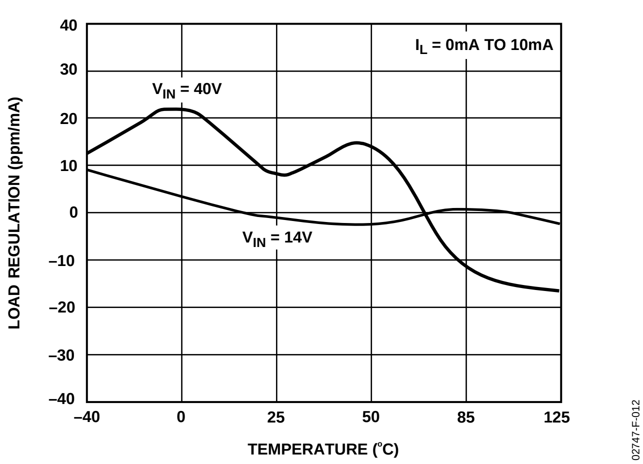


*Figure 12. ADR01 Load Regulation vs. Temperature*

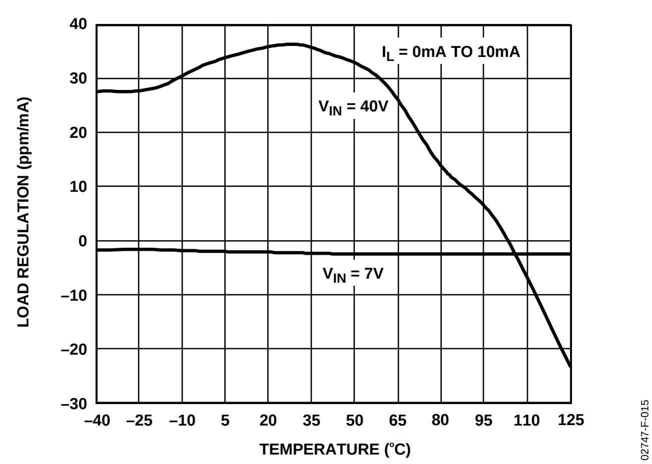


*Figure 15. ADR06 Load Regulation vs. Temperature*

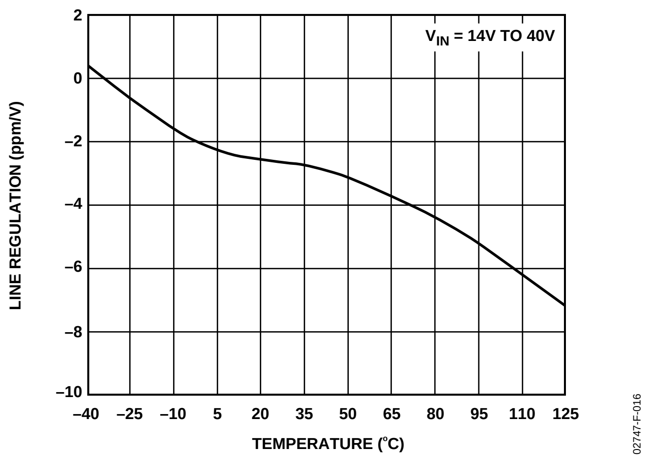


Figure 16. ADR01 Line Regulation vs. Temperature

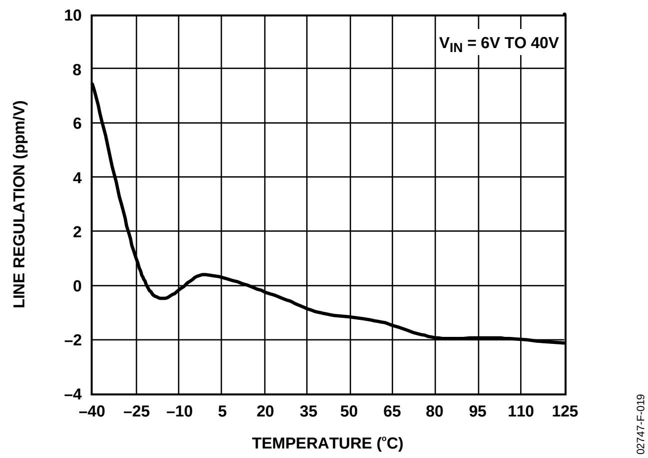


Figure 19. ADR06 Line Regulation vs. Temperature

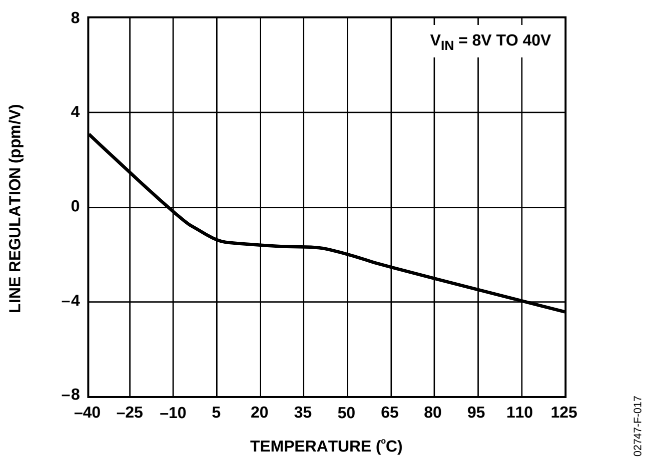


Figure 17. ADR02 Line Regulation vs. Temperature

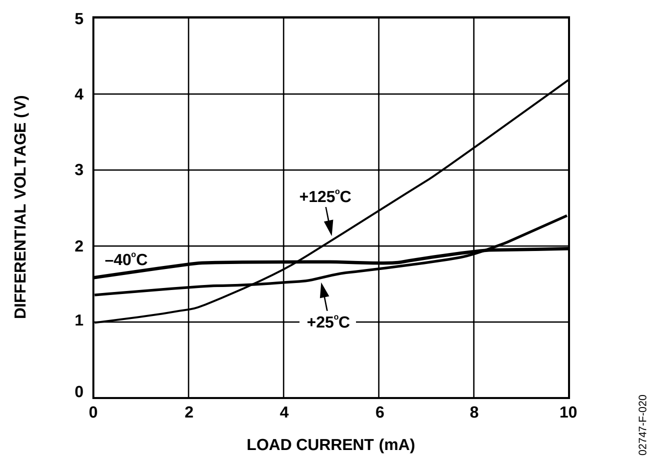


Figure 20. ADR01 Minimum Input-Output Voltage Differential vs. Load Current

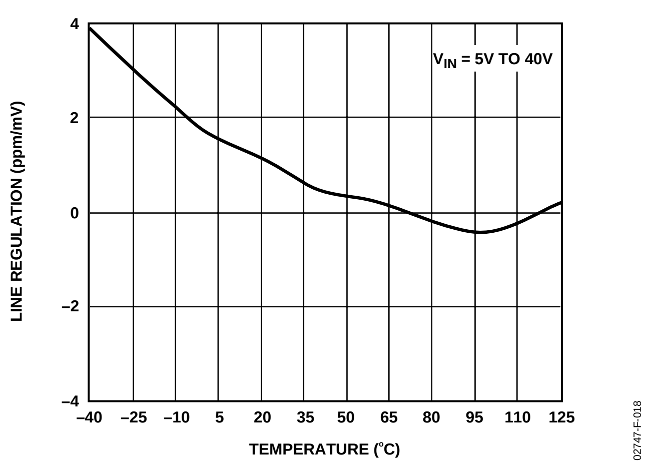


Figure 18. ADR03 Line Regulation vs. Temperature

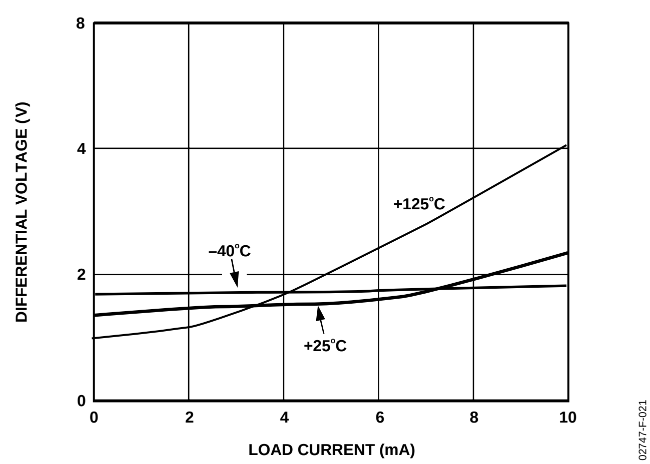


Figure 21. ADR02 Minimum Input-Output Voltage Differential vs. Load Current

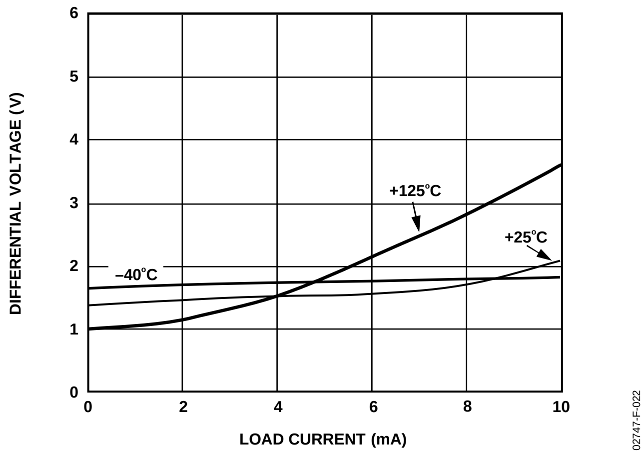


Figure 22. ADR03 Minimum Input-Output Voltage Differential vs. Load Current

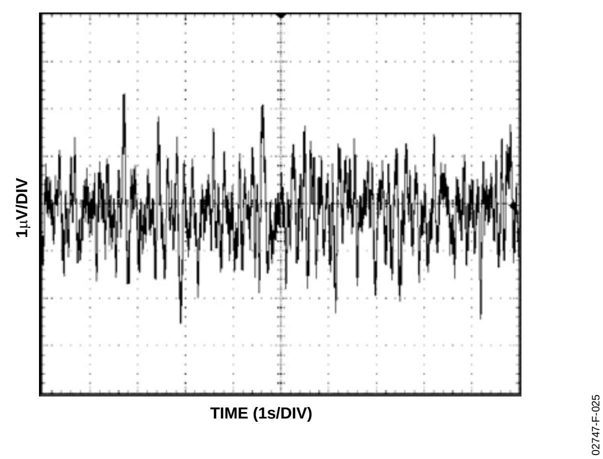


Figure 25. ADR02 Typical Noise Voltage 0.1 Hz to 10 Hz

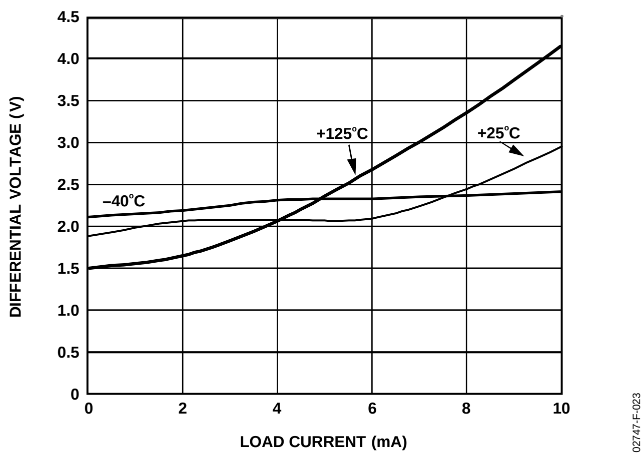


Figure 23. ADR06 Minimum Input-Output Voltage Differential vs. Load Current

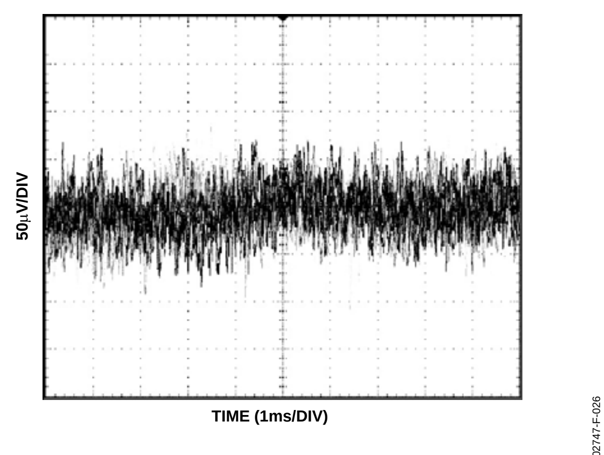


Figure 26. ADR02 Typical Noise Voltage 10 Hz to 10 KHz

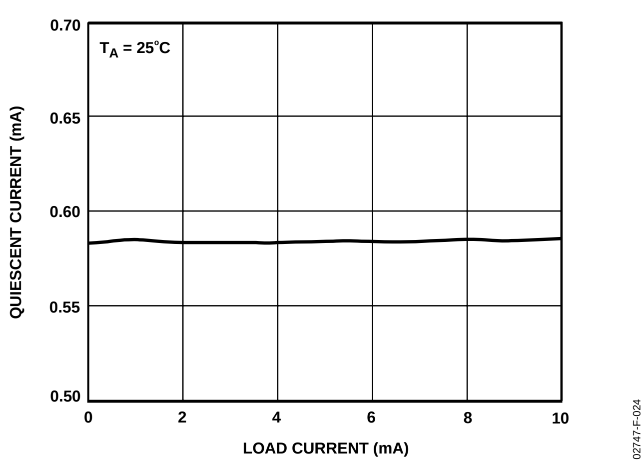


Figure 24. ADR01 Quiescent Current vs. Load Current

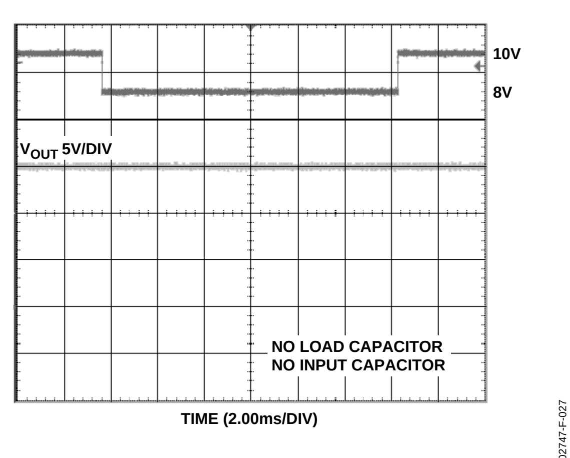


Figure 27. ADR02 Line Transient Response

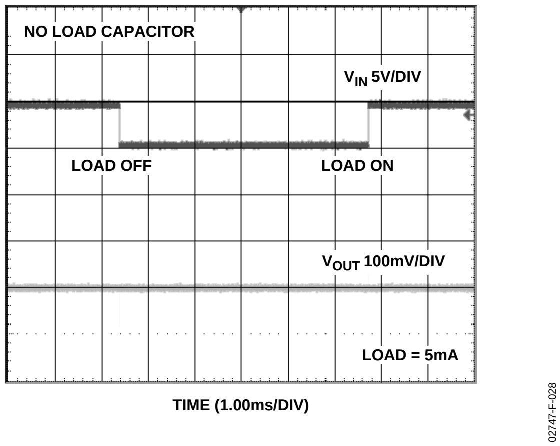


Figure 28. ADR02 Load Transient Response

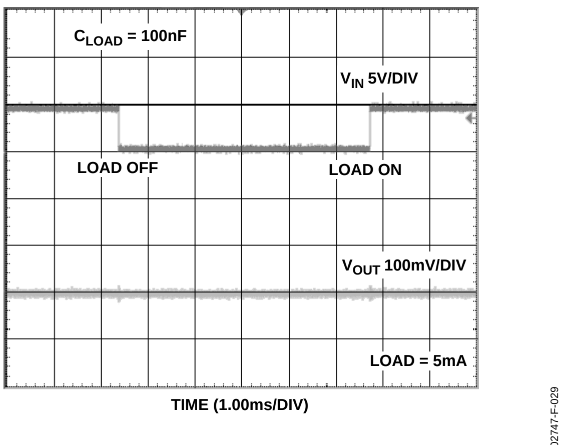


Figure 29. ADR02 Load Transient Response

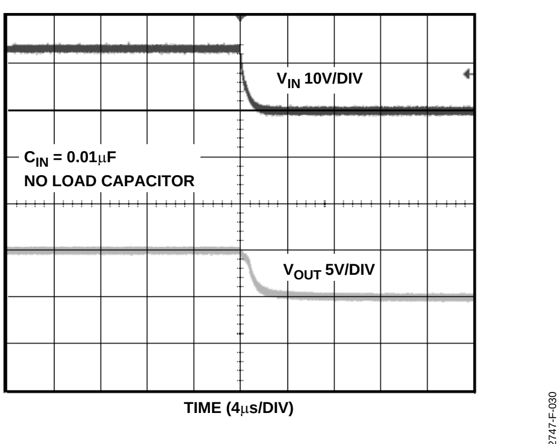


Figure 30. ADR02 Turn-Off Response

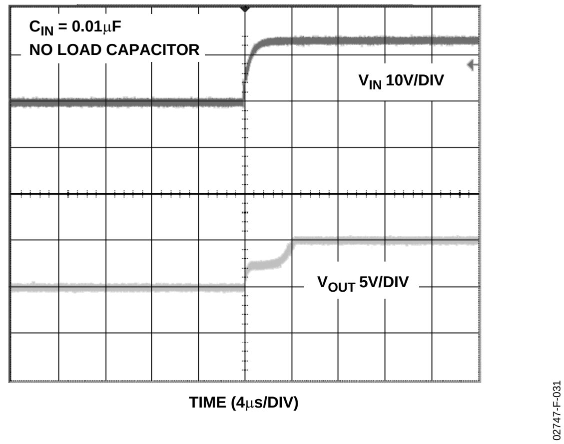


Figure 31. ADR02 Turn-On Response

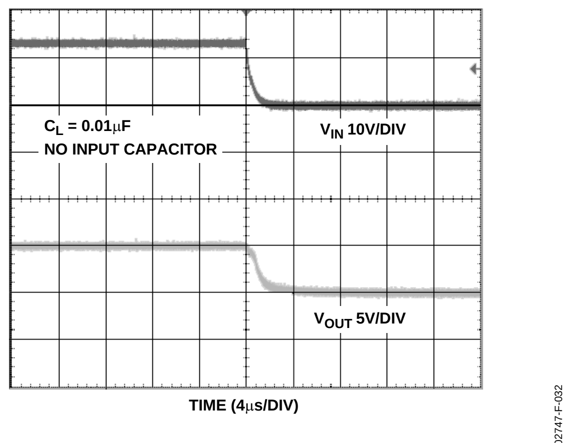


Figure 32. ADR02 Turn-Off Response

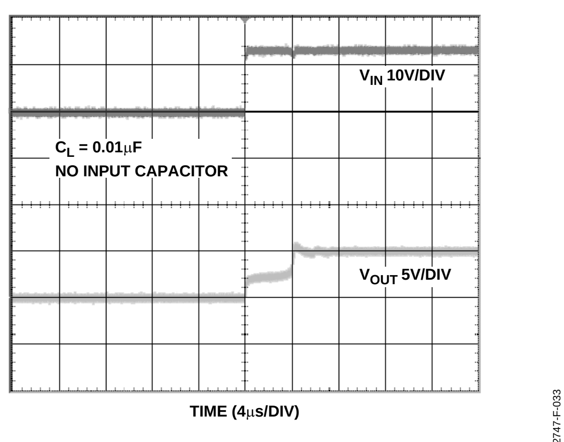


Figure 33. ADR02 Turn-On Response

# APPLICATIONS

The ADR01/ADR02/ADR03/ADR06 are high precision, low drift 10 V, 5 V, 2.5 V, and 3.0 V voltage references available in an ultracompact footprint. The SOIC-8 version of the devices is a drop-in replacement of the REF01/REF02/ REF03 sockets with improved cost and performance.

These devices are standard band gap references. The band gap cell contains two NPN transistors (Q18 and Q19) that differ in emitter area by 2×. The difference in their $V_{BE}$ produces a proportional-to-absolute temperature current (PTAT) in R14, and, when combined with the $V_{BE}$ of Q19, produces a band gap voltage, $V_{BG}$, that is almost constant in temperature. With an internal op amp and the feedback network of R5 and R6, $V_O$ is set precisely at 10 V, 5 V, 2.5 V, and 3.0 V for the ADR01, ADR02, ADR06, and ADR03, respectively. Precision laser trimming of the resistors and other proprietary circuit techniques are used to further enhance the initial accuracy, temperature curvature, and drift performance of the ADR01/ADR02/ADR03/ADR06.

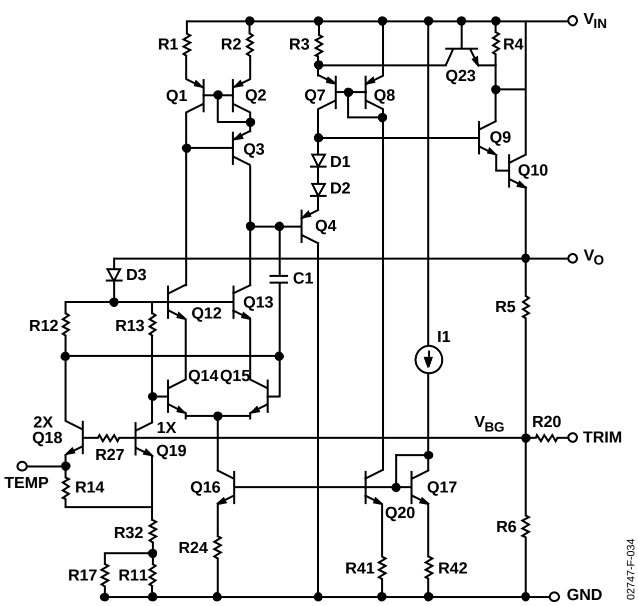


*Figure 34. Simplified Schematic Diagram*

The PTAT voltage is made available at the TEMP pin of the ADR01/ADR02/ADR03/ADR06. It has a stable 1.96 mV/°C temperature coefficient, such that users can estimate the temperature change of the device by knowing the voltage change at the TEMP pin.

## A L I G HEAD 01/AD 02/AD 03/AD 06

The devices can be used without any external components to achieve the specified performance. Because of the internal op amp amplifying the band gap cell to 10 V/5 V/2.5 V/3.0 V, power supply decoupling helps the transient response of the ADR01/ADR02/ADR03/ADR06. As a result, a 0.1 µF ceramic type decoupling capacitor should be applied as close as possible to the input and output pins of the device. An optional 1 µF to 10 µF bypass capacitor can also be applied at the $V_{IN}$ node to maintain the input under transient disturbance.

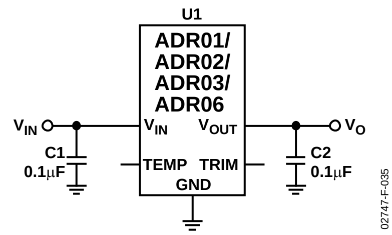


*Figure 35. Basic Configuration*

### *Output Adjustment*

The ADR01/ADR02/ADR03/ADR06 trim terminal can be used to adjust the output voltage over a nominal voltage. This feature allows a system designer to trim system errors by setting the reference to a voltage other than 10 V/5 V/2.5 V/3.0 V. For finer adjustment, a series resistor of 470 kΩ can be added. With the configuration shown in Figure 36, the ADR01 can be adjusted from 9.70 V to 10.05 V, the ADR02 can be adjusted from 4.95 V to 5.02 V, the ADR06 can be adjusted from 2.8 V to 3.3 V, and the ADR03 can be adjusted from 2.3 V to 2.8 V. Adjustment of the output does not significantly affect the temperature performance of the device, provided the temperature coefficients of the resistors are relatively low.

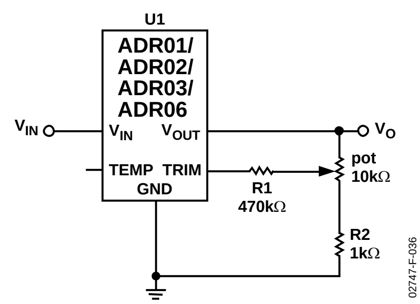


*Figure 36. Optional Trim Adjustment*

### *Temperature Monitoring*

As described previously, the ADR01/ADR02/ADR03/ADR06 provide a TEMP output (Pin 3) that varies linearly with temperature. This output can be used to monitor the temperature change in the system. The voltage at VTEMP is approximately 550 mV at 25°C, and the temperature coefficient is approximately 1.96 mV/°C (see Figure 37). A voltage change of 39.2 mV at the TEMP pin corresponds to a 20°C change in temperature.

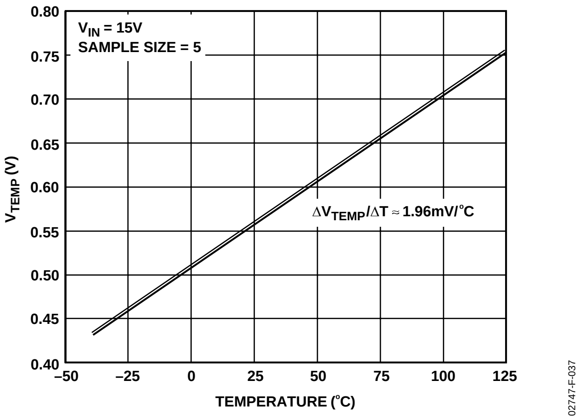


*Figure 37. Voltage at TEMP Pin vs. Temperature*

The TEMP function is provided as a convenience rather than a precise feature. Because the voltage at the TEMP node is acquired from the band gap core, current pulling from this pin has a significant effect on $V_{OUT}$. Care must be taken to buffer the TEMP output with a suitable low bias current op amp, such as the AD8601, AD820, or OP1177, all of which would result in less than a 100 µV change in $\Delta V_{OUT}$ (see Figure 38). Without buffering, even tens of microamps drawn from the TEMP pin can cause $V_{OUT}$ to fall out of specification.

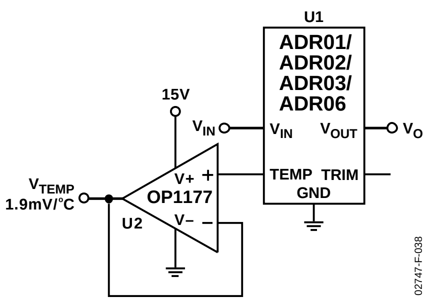


*Figure 38. Temperature Monitoring*

## EGA I E EFE E CE

Without using any matching resistors, a negative reference can be configured as shown in Figure 39. For the ADR01, the voltage difference between $V_{OUT}$ and GND is 10 V. Because $V_{OUT}$ is at virtual ground, U2 closes the loop by forcing the GND pin to be the negative reference node. U2 should be a precision op amp with a low offset voltage characteristic.

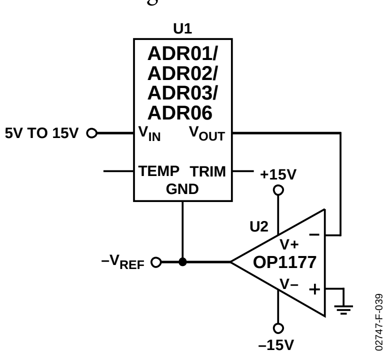


*Figure 39. Negative Reference*

## L C C E CE

Unlike most references, the ADR01/ADR02/ADR03/ADR06 employ an NPN Darlington in which the quiescent current remains constant with respect to the load current, as shown in Figure 24. As a result, a current source can be configured as shown in Figure 40 where $I_{SET} = (V_{OUT} – V_L)/R_{SET}$. $I_L$ is simply the sum of $I_{SET}$ and $I_Q$. Although simple, $I_Q$ varies typically from 0.55 to 0.65 mA, limiting this circuit to general-purpose applications.

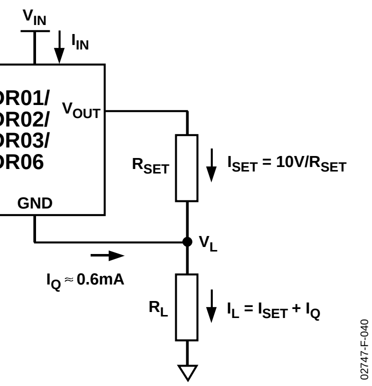


*Figure 40. Low Cost Current Source*

## ECI I C E CE I H ADJ ABLE

A precision current source, on the other hand, can be implemented with the circuit shown in Figure 41. By adding a mechanical or digital potentiometer, this circuit becomes an adjustable current source. If a digital potentiometer is used, the load current is simply the voltage across terminals B to W of the digital potentiometer divided by $R_{SET}$.

$$I_L = \frac{V_{REF} \times D}{R_{SET}} \tag{1}$$

where *D* is the decimal equivalent of the digital potentiometer input code.

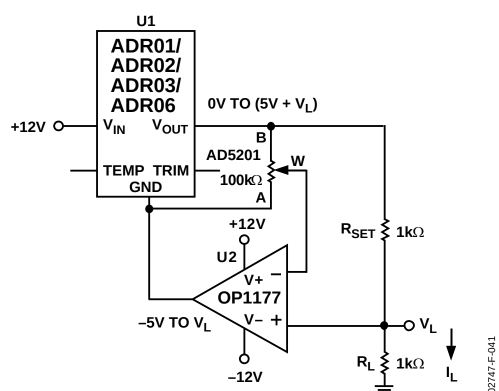


*Figure 41. Programmable 0 to 5 mA Current Source*

To optimize the resolution of this circuit, dual-supply op amps should be used because the ground potential of ADR02 can swing from –5 V at zero scale to $V_L$ at full scale of the potentiometer setting.

### G AMMABLE 4 20 A C E A MI E

Because of their precision, adequate current handling, and small footprint, the devices are suitable as the reference sources for many high performance converter circuits. One of these applications is the multichannel 16-bit 4 to 20 mA current transmitter in the industrial control market (see Figure 42). This circuit employs a Howland current pump at the output, which yields better efficiency, a lower component count, and a higher voltage compliance than the conventional design with op amps and MOSFETs. In this circuit, if the resistors are matched such that R1 = R1′, R2 = R2′, R3 = R3′, the load current is

$$I_L = \frac{(R2 + R3)/R1}{R3'} \times \frac{V_{REF} \times D}{2^N} \tag{2}$$

where $D$ is similarly the decimal equivalent of the DAC input code and $N$ is the number of bits of the DAC.

According to Equation 2, R3′ can be used to set the sensitivity. R3′ can be made as small as necessary to achieve the current needed within U4 output current driving capability. On the other hand, other resistors can be kept high to conserve power.

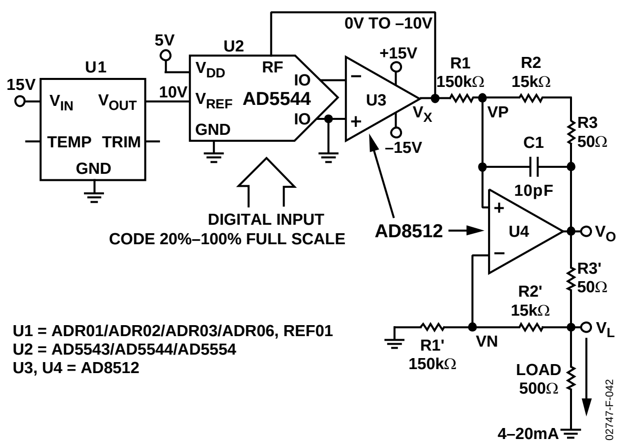


*Figure 42. Programmable 4 to 20 mA Transmitter*

In this circuit, the AD8512 is capable of delivering 20 mA of current, and the voltage compliance approaches 15 V.

The Howland current pump yields a potentially infinite output impedance, which is highly desirable, but resistance matching is critical in this application. The output impedance can be determined using Equation 3. As can be seen by this equation, if the resistors are perfectly matched, $Z_O$ is infinite. On the other hand, if they are not matched, $Z_O$ is either positive or negative. If the latter is true, oscillation may occur. For this reason, a capacitor, C1, in the range of 1 pF to 10 pF should be connected between VP and the output terminal of U4, to filter any oscillation.

$$Z_O = \frac{V_t}{I_t} = \frac{R1'}{\left(\frac{R1'R2}{R1R2'} - 1\right)} \tag{3}$$

In this circuit, an ADR01 provides the stable 10.000 V reference for the AD5544 quad 16-bit DAC. The resolution of the adjustable current is 0.3 µA/step, and the total worst-case INL error is merely 4 LSB. Such error is equivalent to 1.2 µA or a 0.006% system error, which is well below most systems' requirements. The result is shown in Figure 43 with measurement taken at 25°C and 70°C; total system error of 4 LSB at both 25°C and 70°C.

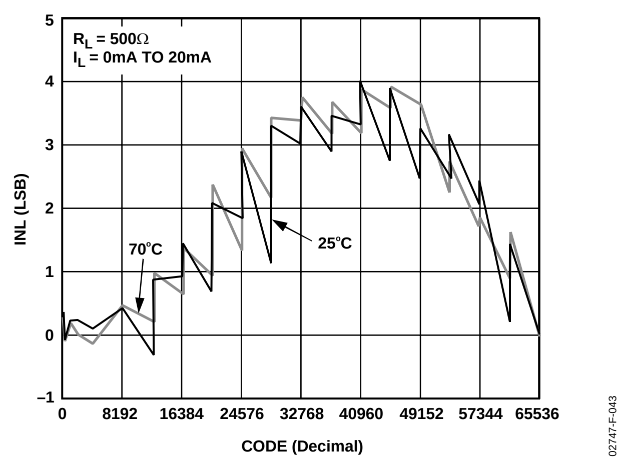


*Figure 43. Result of Programmable 4 to 20 mA Current Transmitter*

### *Precision Boosted Output Regulator*

A precision voltage output with boosted current capability can be realized with the circuit shown in Figure 44. In this circuit, U2 forces $V_O$ to be equal to $V_{REF}$ by regulating the turn-on of N1, thereby making the load current furnished by $V_{IN}$. In this configuration, a 50 mA load is achievable at $V_{IN}$ of 15 V. Moderate heat is generated on the MOSFET, and higher current can be achieved with a replacement of a larger device. In addition, for a heavy capacitive load with a fast edging input signal, a buffer should be added at the output to enhance the transient response.

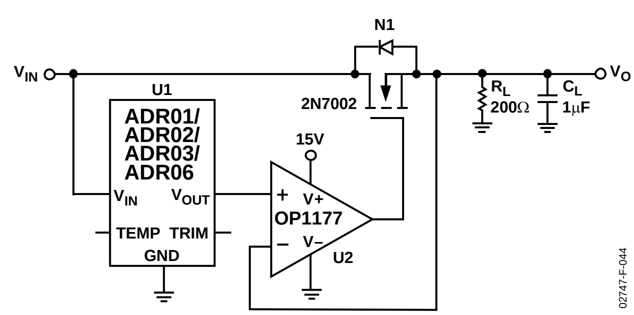


*Figure 44. Precision Boosted Output Regulator*

## OUTLINE DIMENSIONS

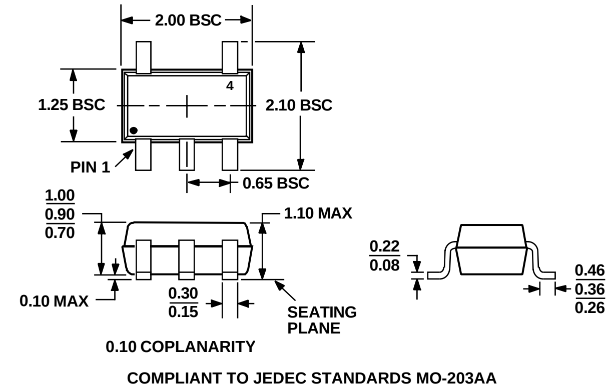


*Figure 45. 5-Lead Thin Shrink Small Outline Transistor Package [SC70]*
*(KS-5)*
*Dimensions shown in millimeters*

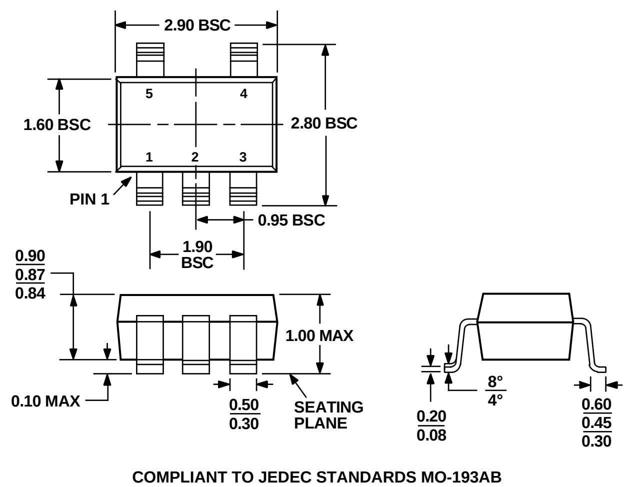


*Figure 46. 5-Lead Thin Small Outline Transistor Package [TSOT]*
*(UJ-5)*
*Dimensions shown in millimeters*

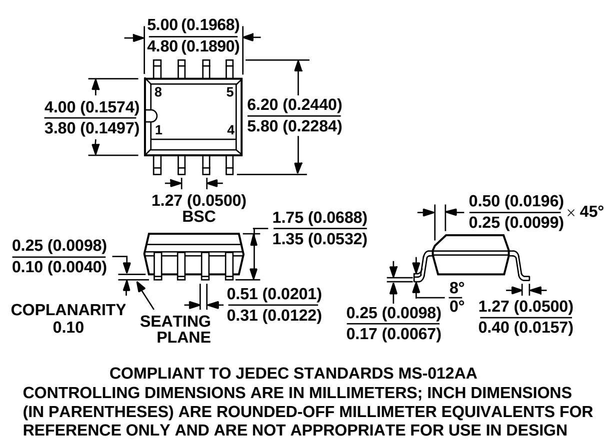


*Figure 47. 8-Lead Standard Small Outline Package [SOIC]*
*Narrow Body (R-8)*
*Dimensions shown in millimeters and (inches)*

# ORDERING GUIDES

## AD 01 DE I G G IDE

| M | ( ) | I A ( ) | (%) | C ( /°C) | k D | k | M k[1] | / | (°C) |
|---|---|---|---|---|---|---|---|---|---|
| ADR01AR | 10 | 10 | 0.1 | 10 | SOIC-8 | R-8 | ADR01 | 98 | −40 to +125 |
| ADR01AR-REEL7 | 10 | 10 | 0.1 | 10 | SOIC-8 | R-8 | ADR01 | 1,000 | −40 to +125 |
| ADR01BR | 10 | 5 | 0.05 | 3 | SOIC-8 | R-8 | ADR01 | 98 | −40 to +125 |
| ADR01BR-REEL7 | 10 | 5 | 0.05 | 3 | SOIC-8 | R-8 | ADR01 | 1,000 | −40 to +125 |
| ADR01AUJ-REEL7 | 10 | 10 | 0.1 | 25 | TSOT-23-5 | UJ-5 | R8A | 3,000 | −40 to +125 |
| ADR01AUJ-R2 | 10 | 10 | 0.1 | 25 | TSOT-23-5 | UJ-5 | R8A | 250 | −40 to +125 |
| ADR01BUJ-REEL7 | 10 | 5 | 0.05 | 9 | TSOT-23-5 | UJ-5 | R8B | 3,000 | −40 to +125 |
| ADR01BUJ-R2 | 10 | 5 | 0.05 | 9 | TSOT-23-5 | UJ-5 | R8B | 250 | −40 to +125 |
| ADR01AKS-REEL7 | 10 | 10 | 0.1 | 25 | SC70 | KS-5 | R8A | 3,000 | −40 to +125 |
| ADR01AKS-R2 | 10 | 10 | 0.1 | 25 | SC70 | KS-5 | R8A | 250 | −40 to +125 |
| ADR01BKS-REEL7 | 10 | 5 | 0.05 | 9 | SC70 | KS-5 | R8B | 3,000 | −40 to +125 |
| ADR01BKS-R2 | 10 | 5 | 0.05 | 9 | SC70 | KS-5 | R8B | 250 | −40 to +125 |
| ADR01CRZ[2] | 10 | 10 | 0.1 | 40 | SOIC-8 | R-8 | ADR01 | 98 | −40 to +125 |
| ADR01CRZ-REEL[2] | 10 | 10 | 0.1 | 40 | SOIC-8 | R-8 | ADR01 | 2,500 | −40 to +125 |
| ARR01NBC | 10 | 5 | 0.05 | 10 (Typ) | Dice | | | 360 | |

[1] First line shows part number ADR01; second line shows A or B for the grade, with the YYMM date code; third line shows the lot number.
[2] Z = Pb-free part.

## AD 02 DE I G G IDE

| M | ( ) | I A ( ) | (%) | C ( /°C) | k D | k | M k[1] | / | (°C) |
|---|---|---|---|---|---|---|---|---|---|
| ADR02AR | 5 | 5 | 0.1 | 10 | SOIC-8 | R-8 | ADR02 | 98 | −40 to +125 |
| ADR02AR-REEL | 5 | 5 | 0.1 | 10 | SOIC-8 | R-8 | ADR02 | 1,000 | −40 to +125 |
| ADR02AR-REEL7 | 5 | 5 | 0.1 | 10 | SOIC-8 | R-8 | ADR02 | 1,000 | −40 to +125 |
| ADR02ARZ[2] | 5 | 5 | 0.1 | 10 | SOIC-8 | R-8 | ADR02 | 98 | −40 to +125 |
| ADR02ARZ-REEL[2] | 5 | 5 | 0.1 | 10 | SOIC-8 | R-8 | ADR02 | 2,500 | −40 to +125 |
| ADR02BR | 5 | 3 | 0.06 | 3 | SOIC-8 | R-8 | ADR02 | 98 | −40 to +125 |
| ADR02BR-REEL7 | 5 | 3 | 0.06 | 3 | SOIC-8 | R-8 | ADR02 | 1,000 | −40 to +125 |
| ADR02AUJ-REEL7 | 5 | 5 | 0.1 | 25 | TSOT-23-5 | UJ-5 | R9A | 3,000 | −40 to +125 |
| ADR02AUJ-R2 | 5 | 5 | 0.1 | 25 | TSOT-23-5 | UJ-5 | R9A | 250 | −40 to +125 |
| ADR02BUJ-REEL7 | 5 | 3 | 0.06 | 9 | TSOT-23-5 | UJ-5 | R9B | 3,000 | −40 to +125 |
| ADR02BUJ-R2 | 5 | 3 | 0.06 | 9 | TSOT-23-5 | UJ-5 | R9B | 250 | −40 to +125 |
| ADR02AKS-REEL7 | 5 | 5 | 0.1 | 25 | SC70 | KS-5 | R9A | 3,000 | −40 to +125 |
| ADR02AKS-R2 | 5 | 5 | 0.1 | 25 | SC70 | KS-5 | R9A | 250 | −40 to +125 |
| ADR02BKS-REEL7 | 5 | 3 | 0.06 | 9 | SC70 | KS-5 | R9B | 3,000 | −40 to +125 |
| ADR02BKS-R2 | 5 | 3 | 0.06 | 9 | SC70 | KS-5 | R9B | 250 | −40 to +125 |
| ADR02CRZ[2] | 5.0 | 5 | 0.1 | 40 | SOIC-8 | R-8 | ADR02 | 98 | −40 to +125 |
| ADR02CRZ-REEL[2] | 5.0 | 5 | 0.1 | 40 | SOIC-8 | R-8 | ADR02 | 2500 | −40 to +125 |
| ARR02NBC | 5 | 3 | 0.06 | 10 (Typ) | Dice | | | 360 | |

[1] First line shows part number ADR02; second line shows A or B for the grade, with the YYMM date code; third line shows the lot number.
[2] Z = Pb-free part.

## AD 03 DE I G G IDE

| M | ( ) | I A ( ) | (%) | C ( /°C) | k D | k | M k[1] | / | (°C) |
|---|---|---|---|---|---|---|---|---|---|
| ADR03AR | 2.5 | 5 | 0.2 | 10 | SOIC-8 | R-8 | ADR03 | 98 | −40 to +125 |
| ADR03AR-REEL7 | 2.5 | 5 | 0.2 | 10 | SOIC-8 | R-8 | ADR03 | 1,000 | −40 to +125 |
| ADR03BR | 2.5 | 2.5 | 0.1 | 3 | SOIC-8 | R-8 | ADR03 | 98 | −40 to +125 |
| ADR03BR-REEL7 | 2.5 | 2.5 | 0.1 | 3 | SOIC-8 | R-8 | ADR03 | 1,000 | −40 to +125 |
| ADR03AUJ-REEL7 | 2.5 | 5 | 0.2 | 25 | TSOT-23-5 | UJ-5 | RFA | 3,000 | −40 to +125 |
| ADR03AUJ-R2 | 2.5 | 5 | 0.2 | 25 | TSOT-23-5 | UJ-5 | RFA | 250 | −40 to +125 |
| ADR03BUJ-REEL7 | 2.5 | 2.5 | 0.1 | 9 | TSOT-23-5 | UJ-5 | RFB | 3,000 | −40 to +125 |
| ADR03BUJ-R2 | 2.5 | 2.5 | 0.1 | 9 | TSOT-23-5 | UJ-5 | RFB | 250 | −40 to +125 |
| ADR03AKS-REEL7 | 2.5 | 5 | 0.2 | 25 | SC70 | KS-5 | RFA | 3,000 | −40 to +125 |
| ADR03AKS-R2 | 2.5 | 5 | 0.2 | 25 | SC70 | KS–5 | RFA | 250 | −40 to +125 |
| ADR03BKS–REEL7 | 2.5 | 2.5 | 0.1 | 9 | SC70 | KS–5 | RFB | 3,000 | −40 to +125 |
| ADR03BKS–R2 | 2.5 | 2.5 | 0.1 | 9 | SC70 | KS–5 | RFB | 250 | −40 to +125 |
| ADR03BKSZ–REEL7[2] | 2.5 | 2.5 | 0.1 | 9 | SC70 | KS–5 | RFB | 3,000 | −40 to +125 |
| ADR03CRZ[2] | 2.5 | 5 | 0.1 | 40 | SOIC-8 | R-8 | ADR02 | 98 | −40 to +125 |
| ADR03CRZ-REEL[2] | 2.5 | 5 | 0.1 | 40 | SOIC-8 | R-8 | ADR02 | 2500 | −40 to +125 |

[1] First line shows part number ADR03; second line shows A or B for the grade, with the YYMM date code; third line shows the lot number.
[2] Z = Pb-free part.

## AD 06 DE I G G IDE

| M | ( ) | I A ( ) | (%) | C ( /°C) | k D | k | M k[1] | / | (°C) |
|---|---|---|---|---|---|---|---|---|---|
| ADR06AR | 3.0 | 6 | 0.2 | 10 | SOIC-8 | R-8 | ADR06 | 98 | −40 to +125 |
| ADR06AR-REEL7 | 3.0 | 3 | 0.2 | 10 | SOIC-8 | R-8 | ADR06 | 1,000 | −40 to +125 |
| ADR06BR | 3.0 | 6 | 01 | 3 | SOIC-8 | R-8 | ADR06 | 98 | −40 to +125 |
| ADR06BR-REEL7 | 3.0 | 3 | 0.1 | 3 | SOIC-8 | R-8 | ADR06 | 1,000 | −40 to +125 |
| ADR06AUJ-R2 | 3.0 | 6 | 0.2 | 25 | TSOT-23-5 | UJ-5 | RWA | 250 | −40 to +125 |
| ADR06AUJ-REEL7 | 3.0 | 6 | 0.2 | 25 | TSOT-23-5 | UJ-5 | RWA | 3,000 | −40 to +125 |
| ADR06BUJ–R2 | 3.0 | 3 | 0.1 | 9 | TSOT-23-5 | UJ-5 | RWB | 250 | −40 to +125 |
| ADR06BUJ-REEL7 | 3.0 | 3 | 0.1 | 9 | TSOT-23-5 | UJ-5 | RWB | 3,000 | −40 to +125 |
| ADR06AKS-R2 | 3.0 | 6 | 0.2 | 25 | SC70 | KS-5 | RWA | 250 | −40 to +125 |
| ADR06AKS-REEL7 | 3.0 | 6 | 0.2 | 25 | SC70 | KS–5 | RWA | 3,000 | −40 to +125 |
| ADR06BKS-R2 | 3.0 | 3 | 0.1 | 9 | SC70 | KS-5 | RWB | 250 | −40 to +125 |
| ADR06BKS–REEL7 | 3.0 | 3 | 0.1 | 9 | SC70 | KS–5 | RWB | 3,000 | −40 to +125 |
| ADR06CRZ[2] | 3.0 | 6 | 0.2 | 40 | SOIC-8 | R-8 | ADR06 | 98 | −40 to +125 |
| ADR06CRZ-REEL[2] | 3.0 | 6 | 0.2 | 40 | SOIC-8 | R-8 | ADR06 | 2500 | −40 to +125 |

[1] First line shows part number ADR06; second line shows A or B for the grade, with the YYMM date code; third line shows the lot number.
[2] Z = Pb-free part.