National Semiconductor

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LMC6482
CMOS Dual Rail-To-Rail Input and Output Operational Amplifier

General Description

The LMC6482 provides a common-mode range that extends to both supply rails. This rail-to-rail performance combined with excellent accuracy, due to a high CMRR, makes it unique among rail-to-rail input amplifiers.

It is ideal for systems, such as data acquisition, that require a large input signal range. The LMC6482 is also an excellent upgrade for circuits using limited common-mode range amplifiers such as the TLC272 and TLC277.

Maximum dynamic signal range is assured in low voltage and single supply systems by the LMC6482's rail-to-rail output swing. The LMC6482's rail-to-rail output swing is guaranteed for loads down to 600Ω.

Guaranteed low voltage characteristics and low power dissipation make the LMC6482 especially well-suited for battery-operated systems.

LMC6482 is also available in MSOP package which is almost half the size of a SO-8 device.

See the LMC6484 data sheet for a Quad CMOS operational amplifier with these same features.

Features

(Typical unless otherwise noted)

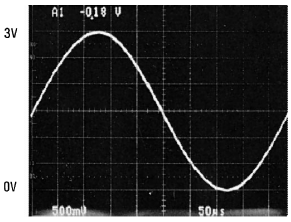
- Rail-to-Rail Input Common-Mode Voltage Range (Guaranteed Over Temperature)
- Rail-to-Rail Output Swing (within 20 mV of supply rail, 100 kΩ load)
- Guaranteed 3V, 5V and 15V Performance
- Excellent CMRR and PSRR: 82 dB
- Ultra Low Input Current: 20 fA
- High Voltage Gain (R_L = 500 kΩ): 130 dB
- Specified for 2 kΩ and 600Ω loads
- Available in MSOP Package

Applications

- Data Acquisition Systems
- Transducer Amplifiers
- Hand-held Analytic Instruments
- Medical Instrumentation
- Active Filter, Peak Detector, Sample and Hold, pH Meter, Current Source
- Improved Replacement for TLC272, TLC277

3V Single Supply Buffer Circuit

Rail-To-Rail Input



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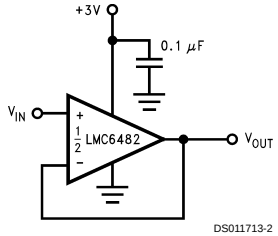

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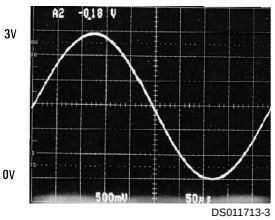
Rail-To-Rail Output



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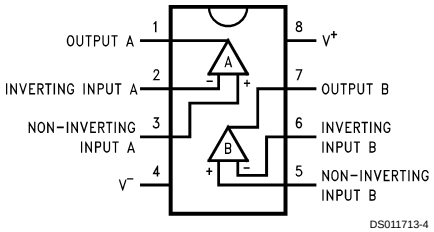
Connection Diagram



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Ordering Information

Package	Temperature Range		NSC Drawing	Transport Media	Package Marking
	Military −55˚C to +125˚C	Industrial −40˚C to +85˚C			
8-Pin Molded DIP	LMC6482MN	LMC6482AIN, LMC6482IN	N08E	Rail	LMC6482MN, LMC6482AIN, LMC6482IN
8-pin Small Outline		LMC6482AIM, LMC6482IM	M08A	Rail Tape and Reel	LMC6482AIM, LMC6482IM
8-pin Ceramic DIP	LMC6482AMJ/883		J08A	Rail	LMC6482AMJ/883Q5962-9453401MPA
8-pin Mini SO		LMC6482IMM	MUA08A	Rail Tape and Reel	A10

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	1.5 kV
Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	(V^+) +0.3V, (V^-) −0.3V
Supply Voltage $(V^+ - V^-)$	16V
Current at Input Pin (Note 12)	±5 mA
Current at Output Pin (Notes 3, 8)	±30 mA
Current at Power Supply Pin	40 mA
Lead Temperature (Soldering, 10 sec.)	260˚C
Storage Temperature Range	−65˚C to +150˚C
Junction Temperature (Note 4)	150˚C

Operating Ratings (Note 1)

Supply Voltage	3.0V ≤ V+ ≤ 15.5V
Junction Temperature Range	
LMC6482AM	$-55^\circ C \le T_J \le +125^\circ C$
LMC6482AI, LMC6482I	$-40^\circ C \le T_J \le +85^\circ C$
Thermal Resistance (θ_{JA})	
N Package, 8-Pin Molded DIP	90˚C/W
M Package, 8-Pin Surface Mount	155˚C/W
MSOP package, 8-Pin Mini SO	194˚C/W

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = 5V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and R_L > 1M. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Typ (Note 5)	LMC6482AI Limit (Note 6)	LMC6482I Limit (Note 6)	LMC6482M Limit (Note 6)	Units
V_{OS}	Input Offset Voltage			0.11	0.750 **1.35**	3.0 **3.7**	3.0 **3.8**	mV max
TCV_{OS}	Input Offset Voltage Average Drift			1.0				µV/˚C
I_B	Input Current	(Note 13)		0.02	**4.0**	**4.0**	**10.0**	pA max
I_{OS}	Input Offset Current	(Note 13)		0.01	**2.0**	**2.0**	**5.0**	pA max
C_{IN}	Common-Mode Input Capacitance			3				pF
R_{IN}	Input Resistance			>10				TeraΩ
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 15.0V V^+ = 15V		82	70 **67**	65 **62**	65 **60**	dB min
		0V ≤ V_{CM} ≤ 5.0V V^+ = 5V		82	70 **67**	65 **62**	65 **60**	
+PSRR	Positive Power Supply Rejection Ratio	5V ≤ V^+ ≤ 15V, V^- = 0V V_O = 2.5V		82	70 **67**	65 **62**	65 **60**	dB min
−PSRR	Negative Power Supply Rejection Ratio	−5V ≤ V^- ≤ −15V, V^+ = 0V V_O = −2.5V		82	70 **67**	65 **62**	65 **60**	dB min
V_{CM}	Input Common-Mode Voltage Range	V^+ = 5V and 15V For CMRR ≥ 50 dB		V^- − 0.3	− 0.25 **0**	− 0.25 **0**	− 0.25 **0**	V max
				V^+ + 0.3V	V^+ + 0.25 **V^+**	V^+ + 0.25 **V^+**	V^+ + 0.25 **V^+**	V min
A_V	Large Signal Voltage Gain	R_L = 2 kΩ (Notes 7, 13)	Sourcing	666	140 **84**	120 **72**	120 **60**	V/mV min
			Sinking	75	35 **20**	35 **20**	35 **18**	V/mV min
		R_L = 600Ω (Notes 7, 13)	Sourcing	300	80 **48**	50 **30**	50 **25**	V/mV min
			Sinking	35	20 **13**	15 **10**	15 **8**	V/mV min

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1M. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6482AI Limit (Note 6)	LMC6482I Limit (Note 6)	LMC6482M Limit (Note 6)	Units
V_O	Output Swing	V^+ = 5V R_L = 2 kΩ to $V^+/2$	4.9	4.8 **4.7**	4.8 **4.7**	4.8 **4.7**	V min
			0.1	0.18 **0.24**	0.18 **0.24**	0.18 **0.24**	V max
		V^+ = 5V R_L = 600Ω to $V^+/2$	4.7	4.5 **4.24**	4.5 **4.24**	4.5 **4.24**	V min
			0.3	0.5 **0.65**	0.5 **0.65**	0.5 **0.65**	V max
		V^+ = 15V R_L = 2 kΩ to $V^+/2$	14.7	14.4 **14.2**	14.4 **14.2**	14.4 **14.2**	V min
			0.16	0.32 **0.45**	0.32 **0.45**	0.32 **0.45**	V max
		V^+ = 15V R_L = 600Ω to $V^+/2$	14.1	13.4 **13.0**	13.4 **13.0**	13.4 **13.0**	V min
			0.5	1.0 **1.3**	1.0 **1.3**	1.0 **1.3**	V max
I_{SC}	Output Short Circuit Current V^+ = 5V	Sourcing, V_O = 0V	20	16 **12**	16 **12**	16 **10**	mA min
		Sinking, V_O = 5V	15	11 **9.5**	11 **9.5**	11 **8.0**	mA min
I_{SC}	Output Short Circuit Current V^+ = 15V	Sourcing, V_O = 0V	30	28 **22**	28 **22**	28 **20**	mA min
		Sinking, V_O = 12V (Note 8)	30	30 **24**	30 **24**	30 **22**	mA min
I_S	Supply Current	Both Amplifiers V^+ = +5V, V_O = $V^+/2$	1.0	1.4 **1.8**	1.4 **1.8**	1.4 **1.9**	mA max
		Both Amplifiers V^+ = 15V, V_O = $V^+/2$	1.3	1.6 **1.9**	1.6 **1.9**	1.6 **2.0**	mA max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = $V^+/2$, and R_L > 1M. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6482AI Limit (Note 6)	LMC6482I Limit (Note 6)	LMC6482M Limit (Note 6)	Units
SR	Slew Rate	(Note 9)	1.3	1.0 **0.7**	0.9 **0.63**	0.9 **0.54**	V/µs min
GBW	Gain-Bandwidth Product	V^+ = 15V	1.5				MHz
ϕ_m	Phase Margin		50				Deg
G_m	Gain Margin		15				dB
	Amp-to-Amp Isolation	(Note 10)	150				dB
e_n	Input-Referred Voltage Noise	F = 1 kHz V_{cm} = 1V	37				nV/√Hz
i_n	Input-Referred Current Noise	F = 1 kHz	0.03				pA/√Hz

AC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = $V^+/2$, and R_L > 1M. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6482AI Limit (Note 6)	LMC6482I Limit (Note 6)	LMC6482M Limit (Note 6)	Units
T.H.D.	Total Harmonic Distortion	F = 10 kHz, A_V = −2 R_L = 10 kΩ, V_O = 4.1 V_{PP}	0.01				%
		F = 10 kHz, A_V = −2 R_L = 10 kΩ, V_O = 8.5 V_{PP} V^+ = 10V	0.01				%

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = 3V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1M.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6482AI Limit (Note 6)	LMC6482I Limit (Note 6)	LMC6482M Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.9	2.0 **2.7**	3.0 **3.7**	3.0 **3.8**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		2.0				µV/˚C
I_B	Input Bias Current		0.02				pA
I_{OS}	Input Offset Current		0.01				pA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 3V	74	64	60	60	dB min
PSRR	Power Supply Rejection Ratio	3V ≤ V^+ ≤ 15V, V^- = 0V	80	68	60	60	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50 dB	V^- −0.25	0	0	0	V max
			V^+ + 0.25	V^+	V^+	V^+	V min
V_O	Output Swing	R_L = 2 kΩ to $V^+/2$	2.8				V
			0.2				V
		R_L = 600Ω to $V^+/2$	2.7	2.5	2.5	2.5	V min
			0.37	0.6	0.6	0.6	V max
I_S	Supply Current	Both Amplifiers	0.825	1.2 **1.5**	1.2 **1.5**	1.2 **1.6**	mA max

AC Electrical Characteristics

Unless otherwise specified, V^+ = 3V, V^- = 0V, V_{CM} = V_O = $V^+/2$, and R_L > 1M.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6482AI Limit (Note 6)	LMC6482I Limit (Note 6)	LMC6482M Limit (Note 6)	Units
SR	Slew Rate	(Note 11)	0.9				V/µs
GBW	Gain-Bandwidth Product		1.0				MHz
T.H.D.	Total Harmonic Distortion	F = 10 kHz, A_V = −2 R_L = 10 kΩ, V_O = 2 V_{PP}	0.01				%

Note 1: Absolute Maximum Ratings indicate limts beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF. All pins rated per method 3015.6 of MIL-STD-883. This is a Class 1 device rating.

AC Electrical Characteristics (Continued)

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150˚C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: V^+ = 15V, V_{CM} = 7.5V and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 3.5V ≤ V_O ≤ 7.5V.

Note 8: Do not short circuit output to V^+, when V^+ is greater than 13V or reliability will be adversely affected.

Note 9: V^+ = 15V. Connected as Voltage Follower with 10V step input. Number specified is the slower of either the positive or negative slew rates.

Note 10: Input referred, V^+ = 15V and R_L = 100 kΩ connected to 7.5V. Each amp excited in turn with 1 kHz to produce V_O = 12 V_{PP}.

Note 11: Connected as voltage Follower with 2V step input. Number specified is the slower of either the positive or negative slew rates.

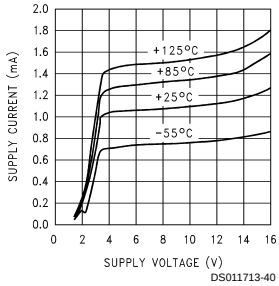
Note 12: Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.

Note 13: Guaranteed limits are dictated by tester limitations and not device performance. Actual performance is reflected in the typical value.

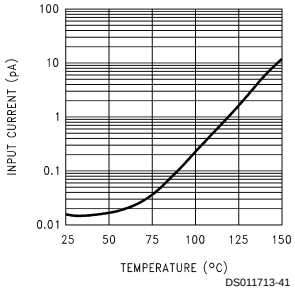
Note 14: For guaranteed Military Temperature parameters see RETS6482X.

Typical Performance Characteristics V_S = +15V, Single Supply, T_A = 25˚C unless otherwise specified

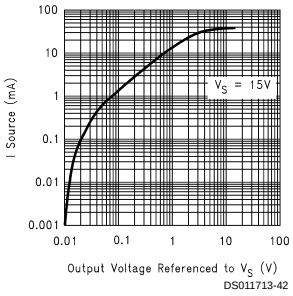
Supply Current vs Supply Voltage



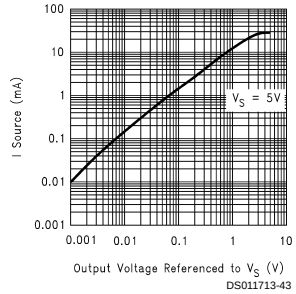
Input Current vs Temperature



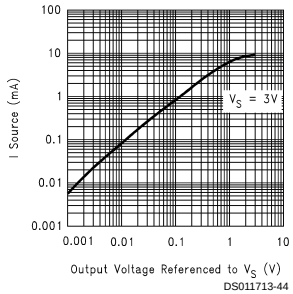
Sourcing Current vs Output Voltage



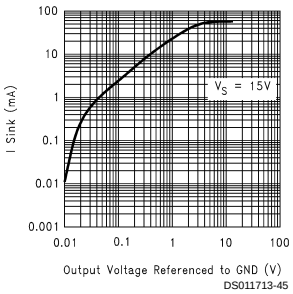
Sourcing Current vs Output Voltage



Sourcing Current vs Output Voltage

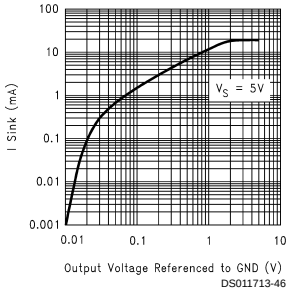


Sinking Current vs Output Voltage



Typical Performance Characteristics V_S = +15V, Single Supply, T_A = 25˚C unless otherwise specified (Continued)

Sinking Current vs Output Voltage



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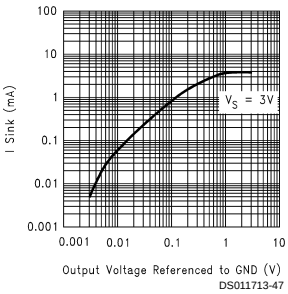
Sinking Current vs Output Voltage



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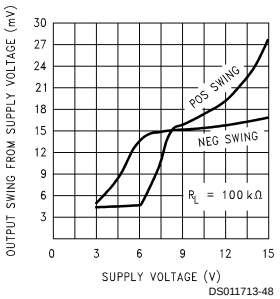
Output Voltage Swing vs Supply Voltage



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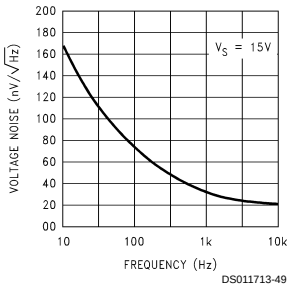
Input Voltage Noise vs Frequency



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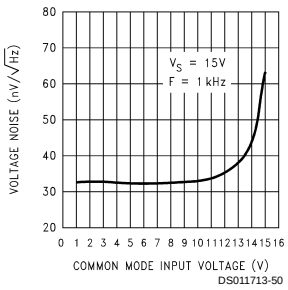
Input Voltage Noise vs Input Voltage



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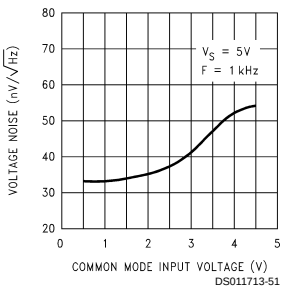
Input Voltage Noise vs Input Voltage



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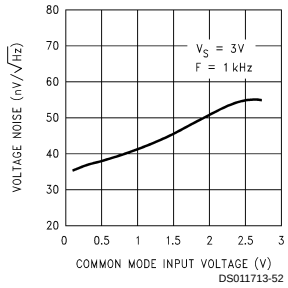
Input Voltage Noise vs Input Voltage



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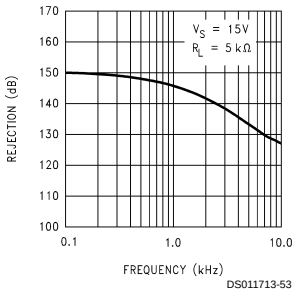
Crosstalk Rejection vs Frequency



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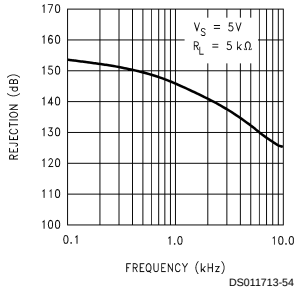
Typical Performance Characteristics V_S = +15V, Single Supply, T_A = 25˚C unless otherwise specified (Continued)

Crosstalk Rejection vs Frequency



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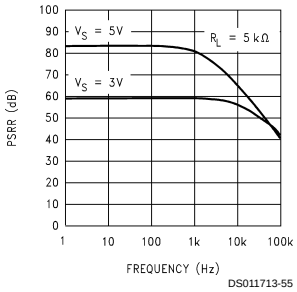
Positive PSRR vs Frequency



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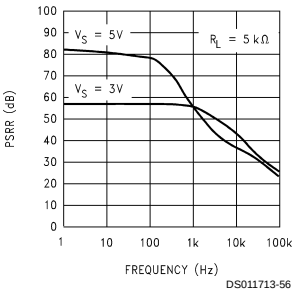
Negative PSRR vs Frequency



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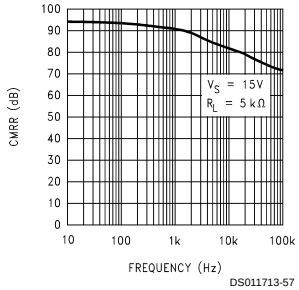
CMRR vs Frequency



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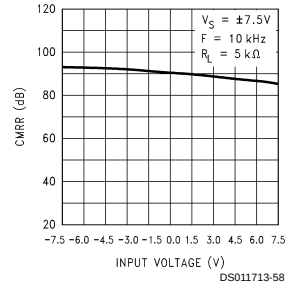
CMRR vs Input Voltage



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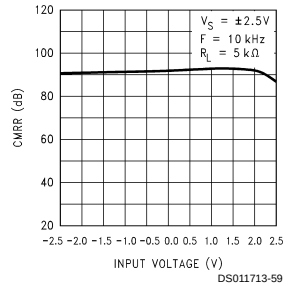
CMRR vs Input Voltage



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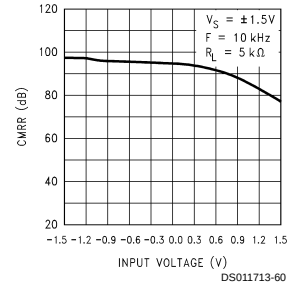
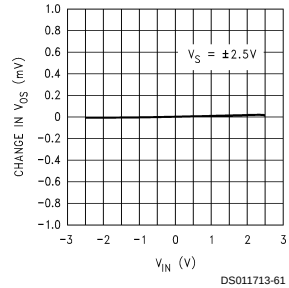
CMRR vs Input Voltage



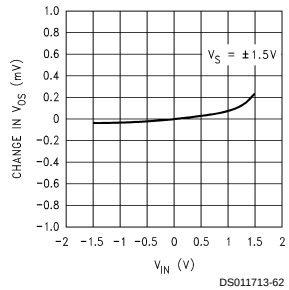
DS011713-60

ΔV_{OS} vs CMR



DS011713-61

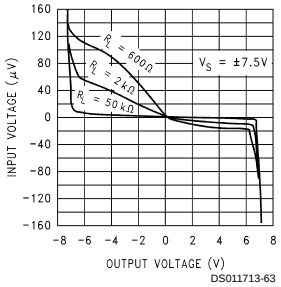
ΔV_{OS} vs CMR



DS011713-62

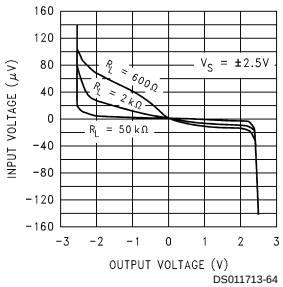
Typical Performance Characteristics V_S = +15V, Single Supply, T_A = 25˚C unless otherwise specified (Continued)

Input Voltage vs Output Voltage



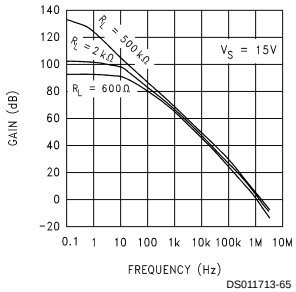
DS011713-63

Input Voltage vs Output Voltage



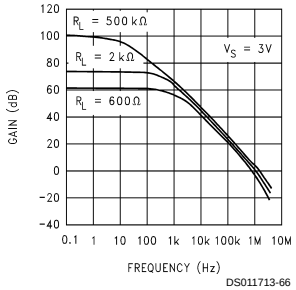
DS011713-64

Open Loop Frequency Response



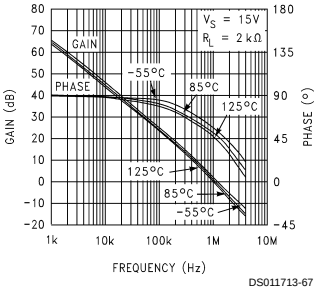
DS011713-65

Open Loop Frequency Responce



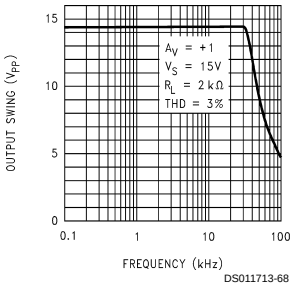
DS011713-66

Open Loop Frequency Response vs Temperature



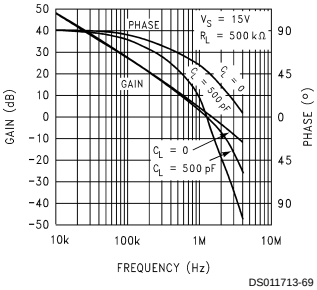
DS011713-67

Maximum Output Swing vs Frequency



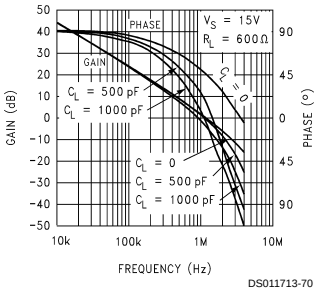
DS011713-68

Gain and Phase vs Capacitive Load



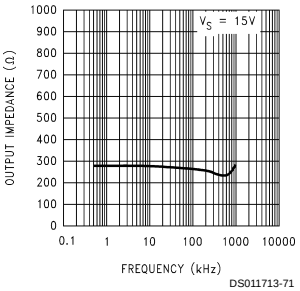
DS011713-69

Gain and Phase vs Capacitive Load



DS011713-70

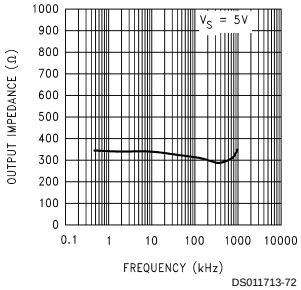
Open Loop Output Impedance vs Frequency



DS011713-71

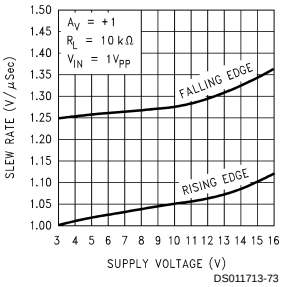
Typical Performance Characteristics V_S = +15V, Single Supply, T_A = 25˚C unless otherwise specified (Continued)

Open Loop Output Impedance vs Frequency



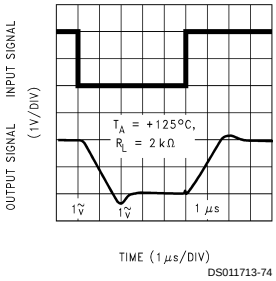
DS011713-72

Slew Rate vs Supply Voltage



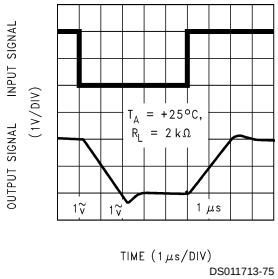
DS011713-73

Non-Inverting Large Signal Pulse Response



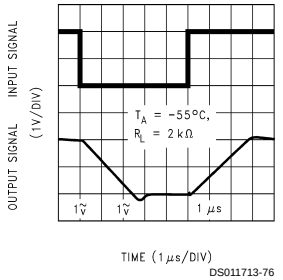
DS011713-74

Non-Inverting Large Signal Pulse Response



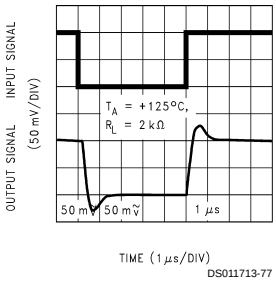
DS011713-75

Non-Inverting Large Signal Pulse Response



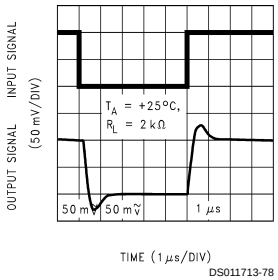
DS011713-76

Non-Inverting Small Signal Pulse Response



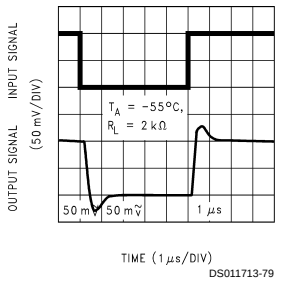
DS011713-77

Non-Inverting Small Signal Pulse Response



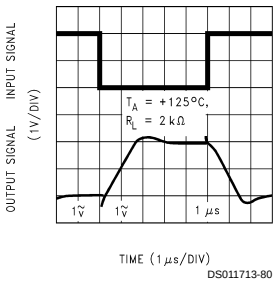
DS011713-78

Non-Inverting Small Signal Pulse Response



DS011713-79

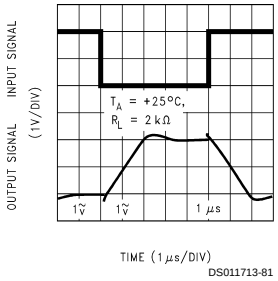
Inverting Large Signal Pulse Response



DS011713-80

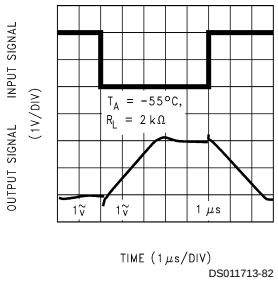
Typical Performance Characteristics V_S = +15V, Single Supply, T_A = 25˚C unless otherwise specified (Continued)

Inverting Large Signal Pulse Response



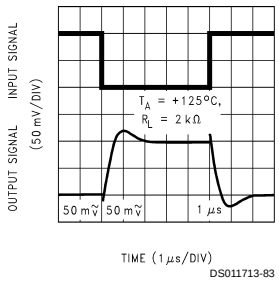
DS011713-81

Inverting Large Signal Pulse Response



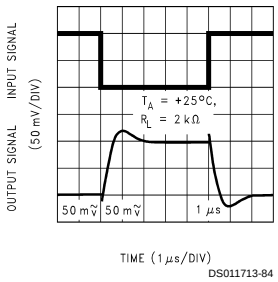
DS011713-82

Inverting Small Signal Pulse Response



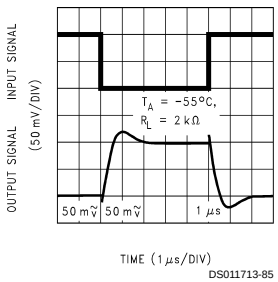
DS011713-83

Inverting Small Signal Pulse Response



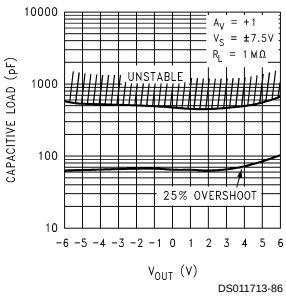
DS011713-84

Inverting Small Signal Pulse Response



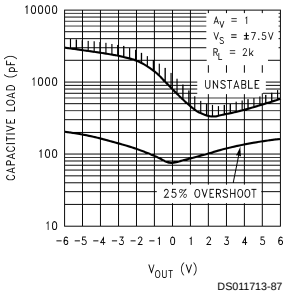
DS011713-85

Stability vs Capacitive Load



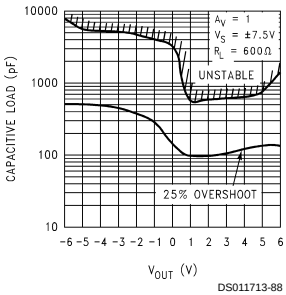
DS011713-86

Stability vs Capacitive Load



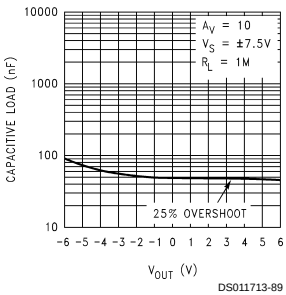
DS011713-87

Stability vs Capacitive Load



DS011713-88

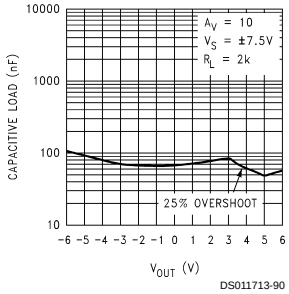
Stability vs Capacitive Load



DS011713-89

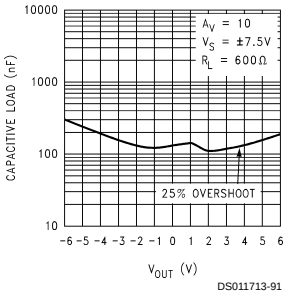
Typical Performance Characteristics V_S = +15V, Single Supply, T_A = 25˚C unless otherwise specified (Continued)

Stability vs Capacitive Load



DS011713-90

Stability vs Capacitive Load



DS011713-91

Application Information

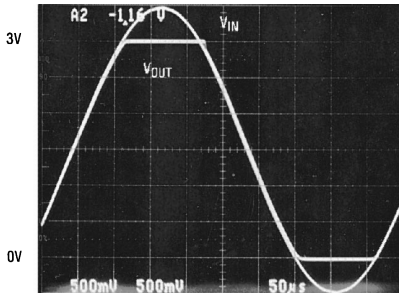
1.0 Amplifier Topology

The LMC6482 incorporates specially designed wide-compliance range current mirrors and the body effect to extend input common mode range to each supply rail. Complementary paralleled differential input stages, like the type used in other CMOS and bipolar rail-to-rail input amplifiers, were not used because of their inherent accuracy problems due to CMRR, cross-over distortion, and open-loop gain variation.

The LMC6482's input stage design is complemented by an output stage capable of rail-to-rail output swing even when driving a large load. Rail-to-rail output swing is obtained by taking the output directly from the internal integrator instead of an output buffer stage.

2.0 Input Common-Mode Voltage Range

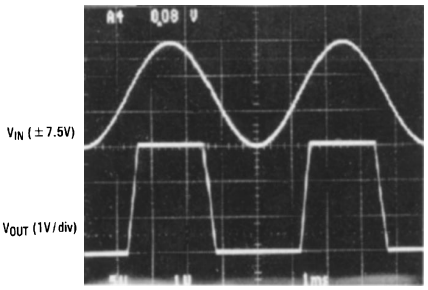
Unlike Bi-FET amplifier designs, the LMC6482 does not exhibit phase inversion when an input voltage exceeds the negative supply voltage. *Figure 1* shows an input voltage exceeding both supplies with no resulting phase inversion on the output.



DS011713-10

FIGURE 1. An Input Voltage Signal Exceeds the LMC6482 Power Supply Voltages with No Output Phase Inversion

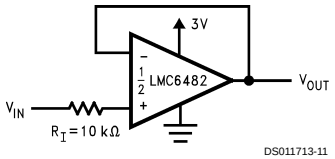
The absolute maximum input voltage is 300 mV beyond either supply rail at room temperature. Voltages greatly exceeding this absolute maximum rating, as in *Figure 2*, can cause excessive current to flow in or out of the input pins possibly affecting reliability.



DS011713-39

FIGURE 2. A ±7.5V Input Signal Greatly Exceeds the 3V Supply in *Figure 3* Causing No Phase Inversion Due to R_I

Applications that exceed this rating must externally limit the maximum input current to ±5 mA with an input resistor (R_I) as shown in *Figure 3*.



DS011713-11

FIGURE 3. R_I Input Current Protection for Voltages Exceeding the Supply Voltages

3.0 Rail-To-Rail Output

The approximated output resistance of the LMC6482 is 180Ω sourcing and 130Ω sinking at Vs = 3V and 110Ω sourcing and 80Ω sinking at Vs = 5V. Using the calculated output resistance, maximum output voltage swing can be estimated as a function of load.

4.0 Capacitive Load Tolerance

The LMC6482 can typically directly drive a 100 pF load with V_S = 15V at unity gain without oscillating. The unity gain follower is the most sensitive configuration. Direct capacitive loading reduces the phase margin of op-amps. The combi-

Application Information (Continued)

nation of the op-amp's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation.

Capacitive load compensation can be accomplished using resistive isolation as shown in *Figure 4*. This simple technique is useful for isolating the capacitive inputs of multiplexers and A/D converters.

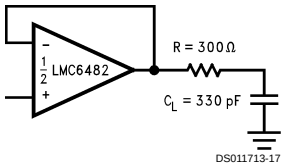


FIGURE 4. Resistive Isolation of a 330 pF Capacitive Load

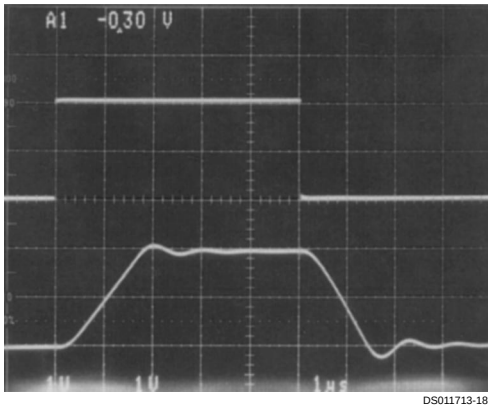


FIGURE 5. Pulse Response of the LMC6482 Circuit in *Figure 4*

Improved frequency response is achieved by indirectly driving capacitive loads, as shown in *Figure 6*.

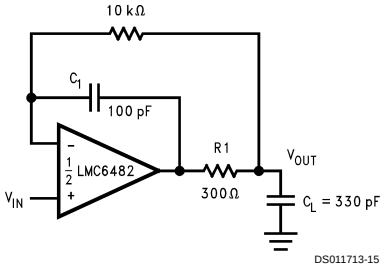


FIGURE 6. LMC6482 Noninverting Amplifier, Compensated to Handle a 330 pF Capacitive Load

R1 and C1 serve to counteract the loss of phase margin by feeding forward the high frequency component of the output signal back to the amplifiers inverting input, thereby preserving phase margin in the overall feedback loop. The values of R1 and C1 are experimentally determined for the desired pulse response. The resulting pulse response can be seen in *Figure 7*.

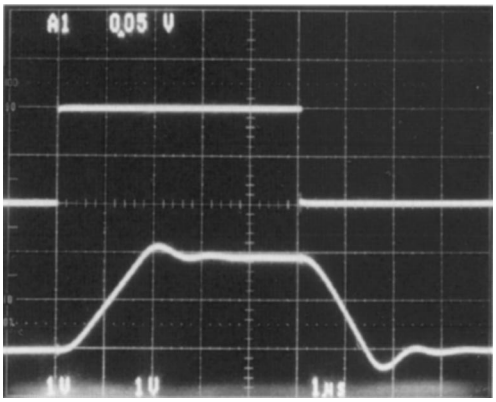


FIGURE 7. Pulse Response of LMC6482 Circuit in *Figure 6*

5.0 Compensating for Input Capacitance

It is quite common to use large values of feedback resistance with amplifiers that have ultra-low input current, like the LMC6482. Large feedback resistors can react with small values of input capacitance due to transducers, photodiodes, and circuits board parasitics to reduce phase margins.

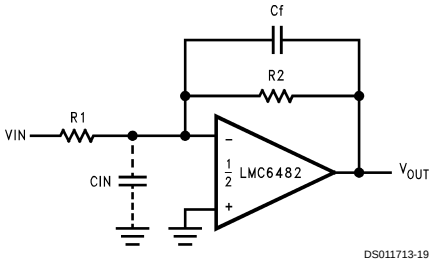


FIGURE 8. Canceling the Effect of Input Capacitance

The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in *Figure 8*), C_f, is first estimated by:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

or

$$R_1 C_{IN} \leq R_2 C_f$$

which typically provides significant overcompensation.

Printed circuit board stray capacitance may be larger or smaller than that of a bread-board, so the actual optimum value for C_f may be different. The values of C_f should be checked on the actual circuit. (Refer to the LMC660 quad CMOS amplifier data sheet for a more detailed discussion.)

Application Information (Continued)

6.0 Printed-Circuit-Board Layout for High-Impedance Work

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low input current of the LMC6482, typically less than 20 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even through it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LM6482's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in *Figure 9.* To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 250 times degradation from the LMC6482's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See *Figure 10* for typical connections of guard rings for standard op-amp configurations.

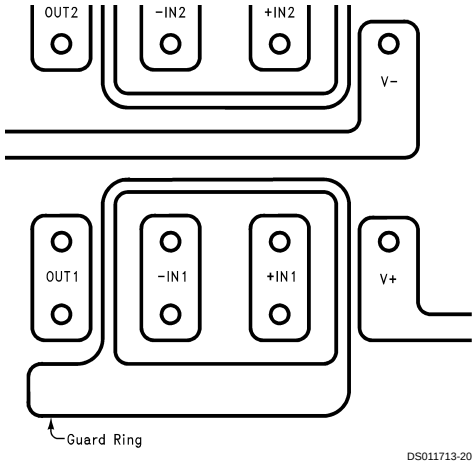


FIGURE 9. Example of Guard Ring in P.C. Board Layout

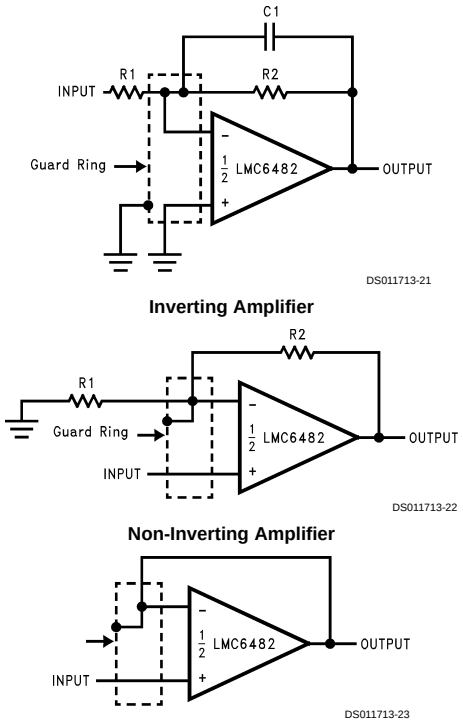
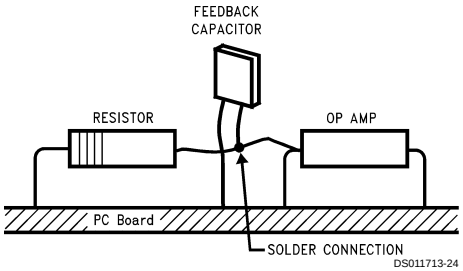


FIGURE 10. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 11.*



(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 11. Air Wiring

Application Information (Continued)

7.0 Offset Voltage Adjustment

Offset voltage adjustment circuits are illustrated in *Figure 12 Figure 13*. Large value resistances and potentiometers are used to reduce power consumption while providing typically ±2.5 mV of adjustment range, referred to the input, for both configurations with V_S = ±5V.

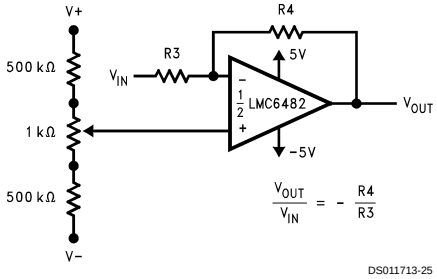


FIGURE 12. Inverting Configuration Offset Voltage Adjustment

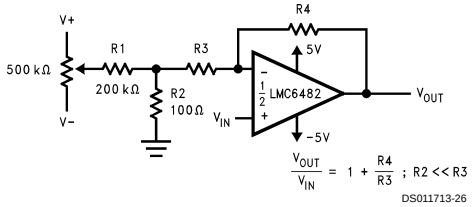


FIGURE 13. Non-Inverting Configuration Offset Voltage Adjustment

8.0 Upgrading Applications

The LMC6484 quads and LMC6482 duals have industry standard pin outs to retrofit existing applications. System performance can be greatly increased by the LMC6482's features. The key benefit of designing in the LMC6482 is increased linear signal range. Most op-amps have limited input common mode ranges. Signals that exceed this range generate a non-linear output response that persists long after the input signal returns to the common mode range.

Linear signal range is vital in applications such as filters where signal peaking can exceed input common mode ranges resulting in output phase inverison or severe distortion.

9.0 Data Acquisition Systems

Low power, single supply data acquisition system solutions are provided by buffering the ADC12038 with the LMC6482 (*Figure 14*). Capable of using the full supply range, the LMC6482 does not require input signals to be scaled down to meet limited common mode voltage ranges. The LMC4282 CMRR of 82 dB maintains integral linearity of a 12-bit data acquisition system to ±0.325 LSB. Other rail-to-rail input amplifiers with only 50 dB of CMRR will degrade the accuracy of the data acquisition system to only 8 bits.

Application Information (Continued)

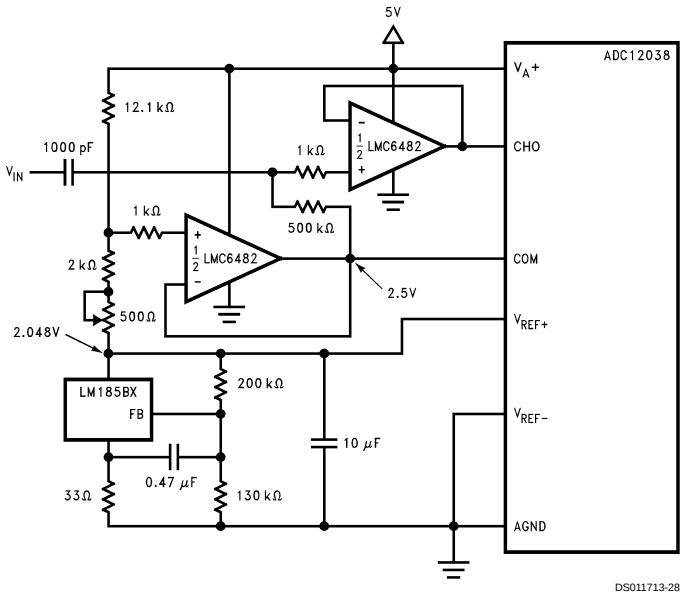


FIGURE 14. Operating from the same Supply Voltage, the LMC6482 buffers the ADC12038 maintaining excellent accuracy

10.0 Instrumentation Circuits

The LMC6482 has the high input impedance, large common-mode range and high CMRR needed for designing instrumentation circuits. Instrumentation circuits designed with the LMC6482 can reject a larger range of common-mode signals than most in-amps. This makes instrumentation circuits designed with the LMC6482 an excellent choice of noisy or industrial environments. Other applications that benefit from these features include analytic medical instruments, magnetic field detectors, gas detectors, and silicon-based tranducers.

A small valued potentiometer is used in series with R_g to set the differential gain of the 3 op-amp instrumentation circuit in *Figure 15*. This combination is used instead of one large valued potentiometer to increase gain trim accuracy and reduce error due to vibration.

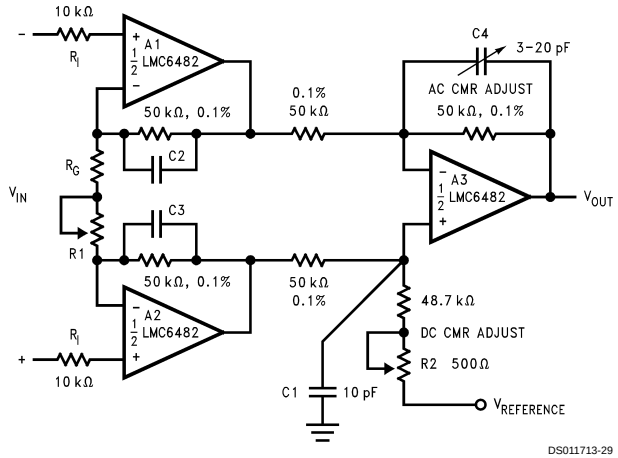


FIGURE 15. Low Power 3 Op-Amp Instrumentation Amplifier

A 2 op-amp instrumentation amplifier designed for a gain of 100 is shown in *Figure 16*. Low sensitivity trimming is made

Application Information (Continued)

for offset voltage, CMRR and gain. Low cost and low power consumption are the main advantages of this two op-amp circuit.

Higher frequency and larger common-mode range applications are best facilitated by a three op-amp instrumentation amplifier.

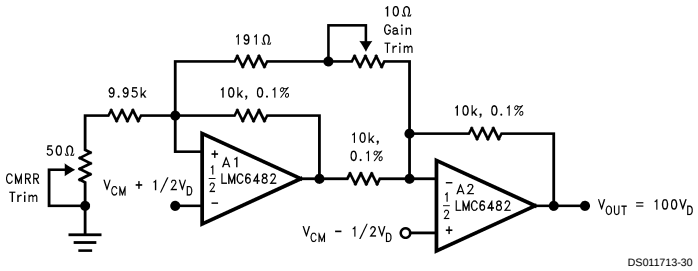


FIGURE 16. Low-Power Two-Op-Amp Instrumentation Amplifier

11.0 Spice Macromodel

A spice macromodel is available for the LMC6482. This model includes accurate simulation of:

- Input common-mode voltage range
- Frequency and transient response
- GBW dependence on loading conditions
- Quiescent and dynamic supply current
- Output swing dependence on loading conditions

and many more characteristics as listed on the macromodel disk.

Contact your local National Semiconductor sales office to obtain an operational amplifier spice model library disk.

Typical Single-Supply Applications

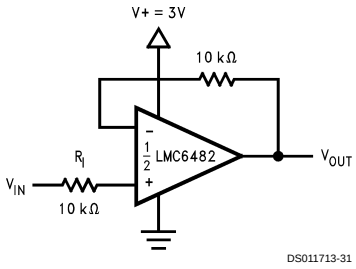


FIGURE 17. Half-Wave Rectifier with Input Current Protection (RI)

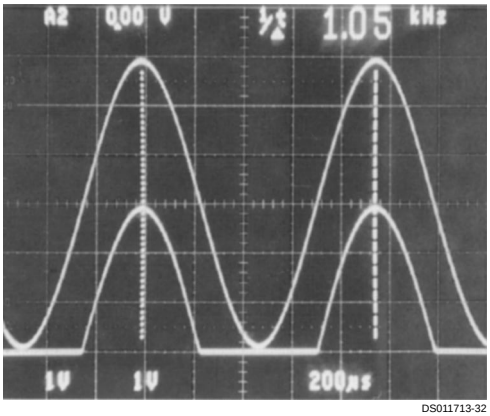


FIGURE 18. Half-Wave Rectifier Waveform

The circuit in *Figure 17* uses a single supply to half wave rectify a sinusoid centered about ground. R_I limits current into the amplifier caused by the input voltage exceeding the supply voltage. Full wave rectification is provided by the circuit in *Figure 19*.

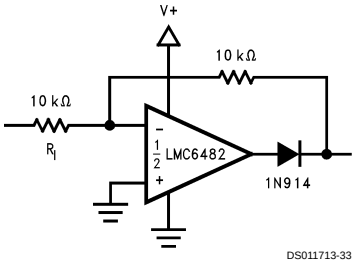
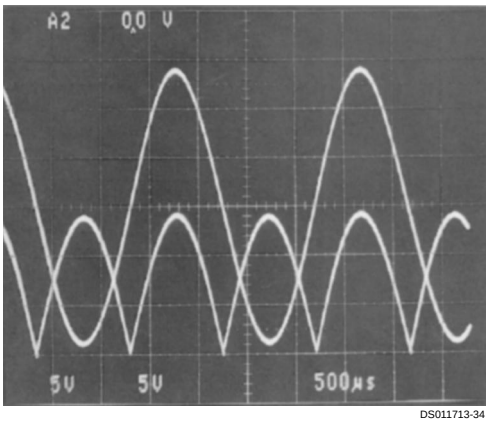


FIGURE 19. Full Wave Rectifier with Input Current Protection (R_I)

Typical Single-Supply Applications (Continued)



DS011713-34

FIGURE 20. Full Wave Rectifier Waveform

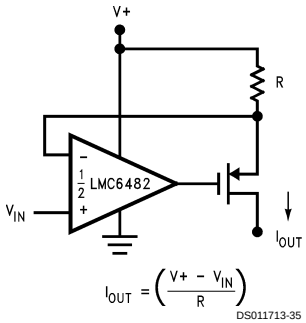


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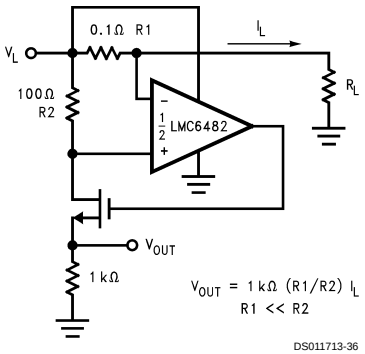
FIGURE 21. Large Compliance Range Current Source



DS011713-36

FIGURE 22. Positive Supply Current Sense

Typical Single-Supply Applications (Continued)

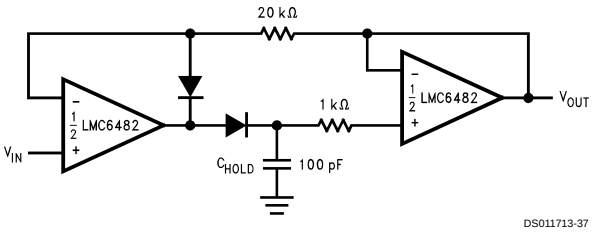


FIGURE 23. Low Voltage Peak Detector with Rail-to-Rail Peak Capture Range

In *Figure 23* dielectric absorption and leakage is minimized by using a polystyrene or polyethylene hold capacitor. The droop rate is primarily determined by the value of C_H and diode leakage current. The ultra-low input current of the LMC6482 has a negligible effect on droop.

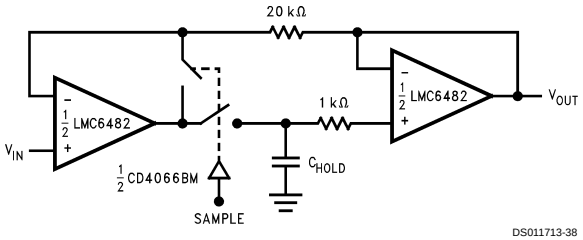
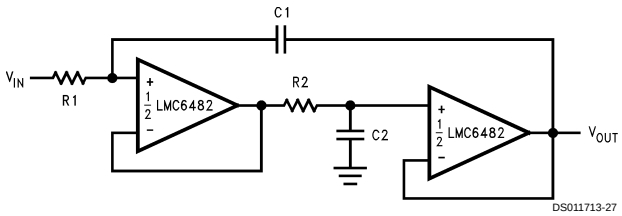


FIGURE 24. Rail-to-Rail Sample and Hold

The LMC6482's high CMRR (82 dB) allows excellent accuracy throughout the circuit's rail-to-rail dynamic capture range.

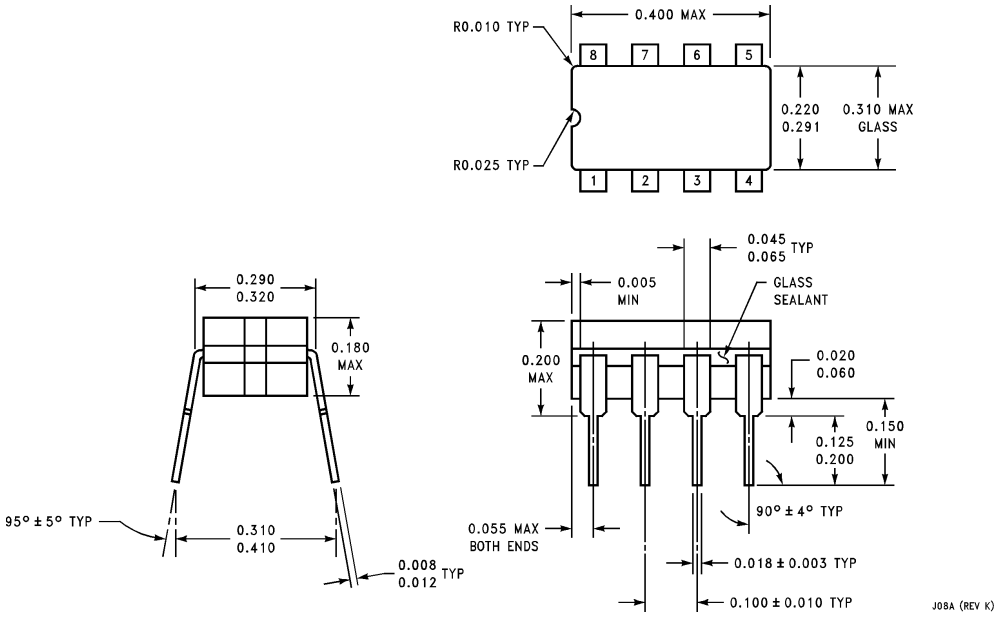


$$R1 = R2,\ C1 = C2;\ f = \frac{1}{2\pi R1\ C1};\ DF = \tfrac{1}{2}\sqrt{\frac{C_2}{C_1}}\sqrt{\frac{R_2}{R_1}}$$

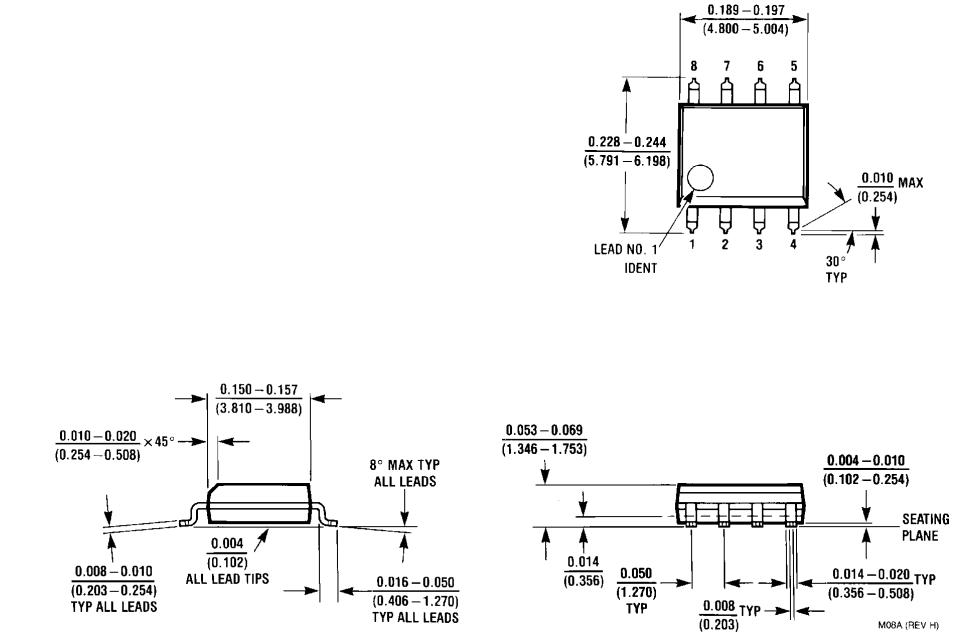
FIGURE 25. Rail-to-Rail Single Supply Low Pass Filter

The low pass filter circuit in *Figure 25* can be used as an anti-aliasing filter with the same voltage supply as the A/D converter. Filter designs can also take advantage of the LMC6482 ultra-low input current. The ultra-low input current yields negligible offset error even when large value resistors are used. This in turn allows the use of smaller valued capacitors which take less board space and cost less.

Physical Dimensions inches (millimeters) unless otherwise noted

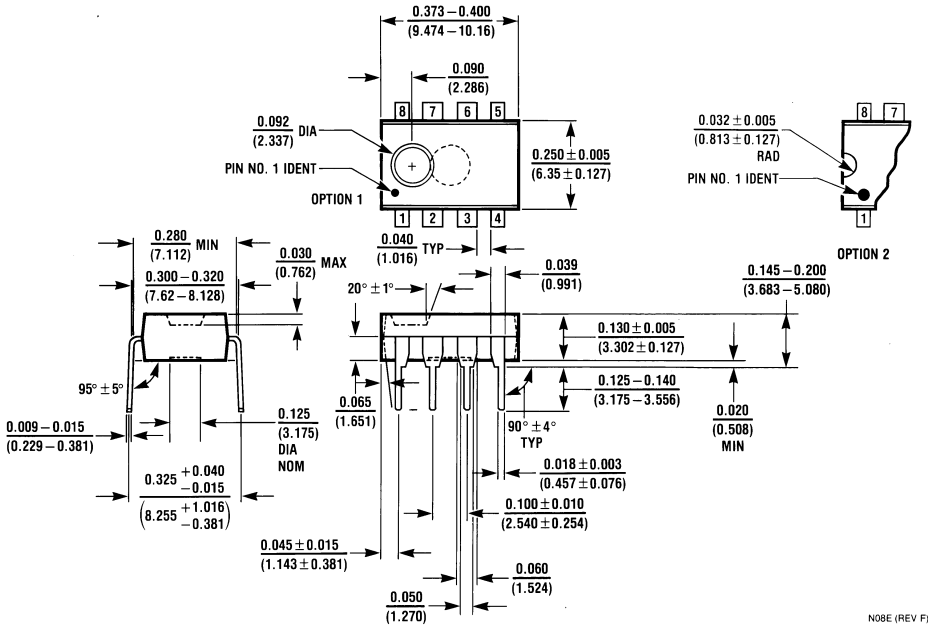


8-Pin Ceramic Dual-In-Line Package
Order Number LMC6482AMJ/883
NS Package Number J08A



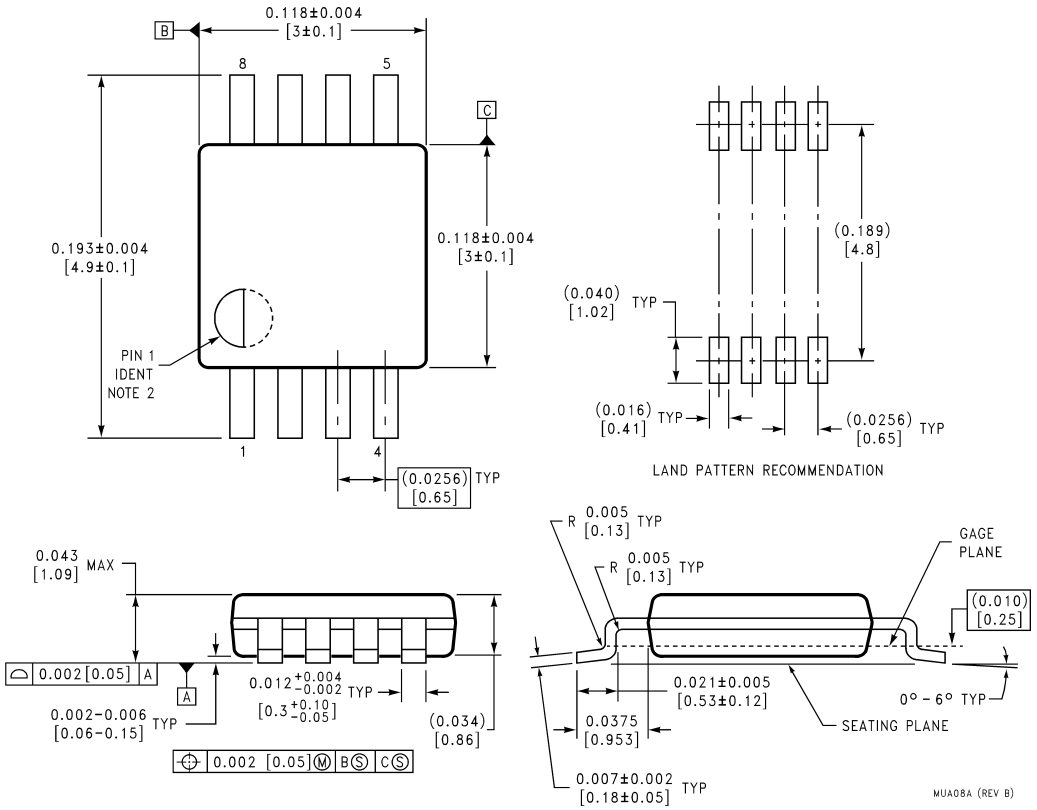
8-Pin Small Outline Package
Order Package Number LMC6482AIM or LMC6482IM
NS Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



8-Pin Molded Dual-In-Line Package
Order Package Number LMC6482AIN, LMC6482IN or LMC6482MN
NS Package Number N08E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



8-Lead Mini Small Outline Molded Package, JEDEC
Order Number LMC6482IMM, or LMC6482IMMX
NS Package Number MUA08A

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