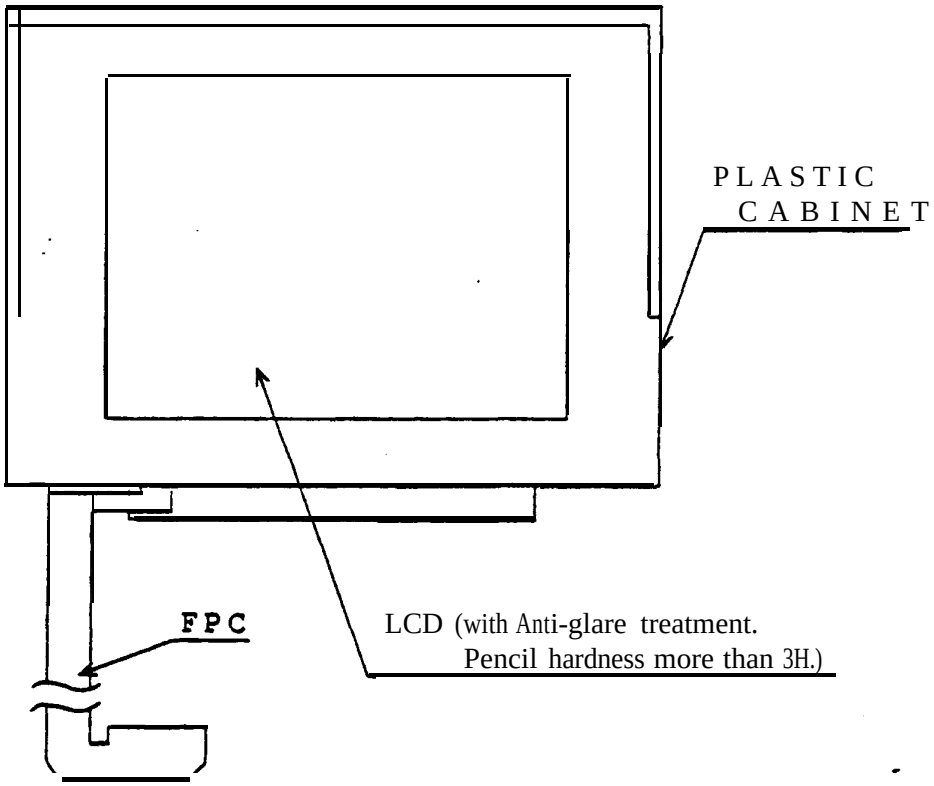
1. Application

This data sheet is to introduce the specification of LM641521, Passive Matrix type LCD Unit.

2. Construction and Outline

Construction: 640X480 dots display unit consisting of an LCD panel, PWB (printed wiring board) with electric components mounted onto, tab (tape automated bonding) to coaaect the LCD panel and PWB electrically, and plastic cabinets to fix them mechanically.



Outline : See lit 8

Connect ioa : See Fig. 8 and Table 8

3. Mechanical Specifications

Table 1

Parameter	Specifications	Unit
Outline dimensions	279.4 (W) × 196.85 (H) × 24.59 MAX (D) *1	mm
Effective viewing Area	196 (W) × 147.6 (H)	mm
Display format	640 (W) × 480 (H) full dot	—
Dot size	0.27 × 0.27	mm
Dot spacing	0.03	mm
*2 Dot color	Black*3	—
*2 Background color	White*3	—
Weight	Approx. 380	g

1# 1 Excluded PPC.

#2 Due to the characteristics of the LC material the colors varr with environmental temperature.

#3 Positive-type display
Displayed data *H*: Dots ON : Black
Displayed data *L*: Dots off: White

4. Absolute Maximum Ratings

4-L Electrical absolute maximum ratings

Table 2

Parueter	Symbol	MIN.	MAX.	Unit	Remark
Sample voltage (Logic)	Vdd-Vss	0	6.0	V	Ta=25 C
Supply voltage (LCD drive)	Vdd-Vzz	0	30.0	V	Ta=2 SC
Input voltage	VIN	0			Ta=25°C

4-2 Environmental Conditions

Table 3

Item	Tstg		Topr		Remark
	MIN.	Max.	Min.	MAX.	
Ambient temperatuer	-25 C	+60 C	0C	+45C	Note 2
Humidi ty	Note		Note *1*		*No* condensat ion
Vibration	Note 2		Note 2		3 directions (X/Y/Z)
Shock	Note 3		Note 3..		6 directions (+X+Y+Z)

Note 1) Ta<40 C. . . . .95% RH Max

Ta>40C . . . ..Absolute humidity shall be less than Ta=40 C/95% RH.

Note 2)

Frequency	5Hz~23Hz	23Hz~500Hz
I Vibratioo level	-	1. OG
Vibration width	1. 0mm	-
Interval	5Hz~500Hz~5Hz/26. 6min	

2 hoars for each direction of X/Y/Z (6 hoars as total)

Note 3) Accerelation : 50G

Pulse width : 11ms

3 times *for* each direction *of +X/+Y/+Z*

Note 4) Care **should** be taken so that the LCD Unit maynot be subjected to the temperature out of this specification

5. Electrical Specifications

5-1 Electrical characteristics

Tabel 4 Ta=25°C,Vdd=5V+ 5%

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	V_{DD}-V_{SS}		4.75	5.0	5.25	V
Supply voltage (LCD drive)	V_{EE}-V_{SS}	Note 1) Note 2)	-23.0	-18.7	-14.1	V
Input signal vol tage	V_{IH}	'H' level	0.8V_{DD}	—	V_{DD}	V
		'L' level	0	—	0.2V_{DD}	V
Input leakage current	I_{IL}	'H' level	—	—	250	μA
		'L' level	-250	—	—	μA
Supply current (Logic)	I_{DD}	Note 3)	—	23.0	33.0	mA
Supply currect (LCD dirve)	I_{EE}		—	17.5	27.0	mA
Power consumption	Pd		—	450	680	mW

Note 1) The viewing angle _ at which the optimum contrast is obtained by adjusting V_{EE}-V_{SS}. Refer to Fig.4 for the definition of θ.

Note 2) Max. end Min. valaes are specified as the Hat and Min. voltage within the condition of operational temperature range (0~45℃). Typ. values are specified as the typical voltage at 25℃.

Note 3) Display high frequency pattern.

V_{DD} = 5V, V_{EE} - V_{SS} = -18.7V, Frame frequency = 85Hz, Display pattern = 4bit checker

display ■■■■□□□□■■■■□□□□■■■■□□□□

pattern □□□□■■■■□□□□■■■■□□□□■■■■

■■■■□□□□■■■■□□□□■■■■□□□□

5-2 Input capacitance

Table 5

Signal	Input capacitance
S	40pF TYP
CP1, DISP	250pF TYP
CP2	200pF TYP
DU0~DU3	200pF TYP
DL0~DL3	200pF TYP

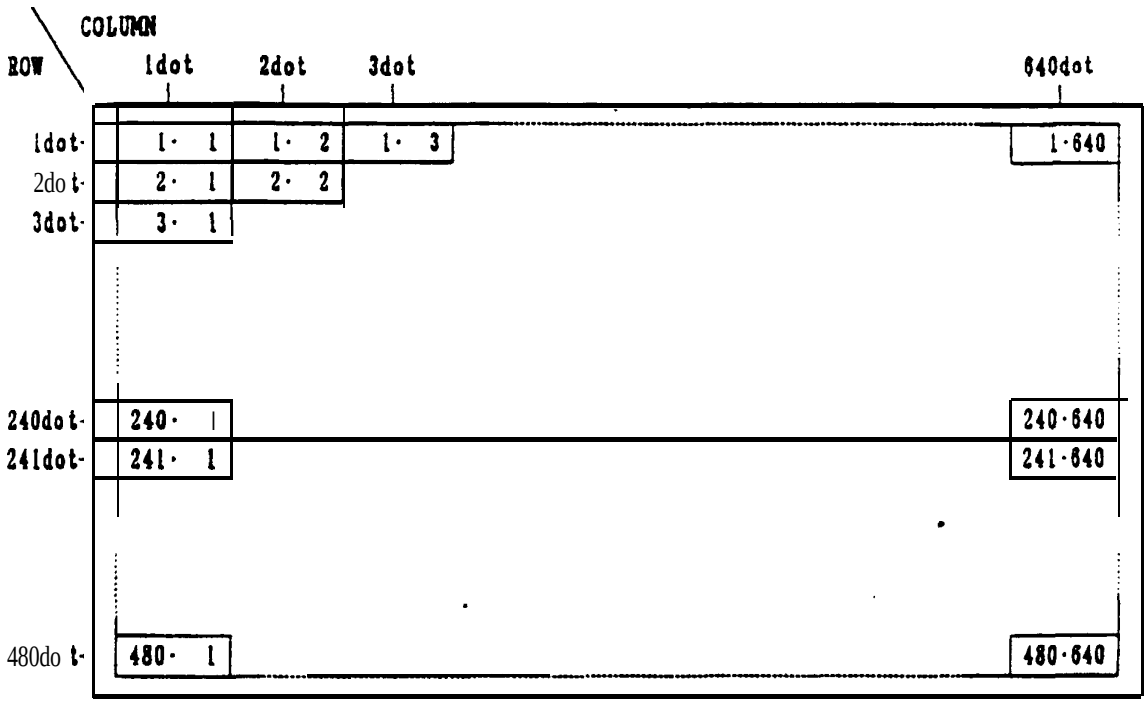
5-3 Interface signals

fable 6

Used connector : 1mm Pitch PPC (27pins)

Pin No	Symbol	Description	Level
1	V_{SS}	Ground potential	
2	V_{SS}	Ground potential	
3	V_{SS}	Ground potential	
4	s	Scan start-up signal	'H'
5	CP1	Input data latch signal	H→L
6	CP2	Data input clock signal	H→L
7	DISP	Display *control* signal	Display on..'H' off..'L'
a	V_{DD}	Parer supply *for* logic and LCD (+5V)	-
9	V_{SS}	Ground potential	
10	V_{EE}	Power supply for LCD I-1	
11	DUO	Display data signal (Upper half)	H (ON), L (OFF)
12	DU1		
13	DU2		
14	DU3		
15	DLO	Display drtr signal (Lower half)	H (ON), L (OFF)
16	DL1		
17	DL2		
18	DL3		
19	V_{SS}	Ground potential	-
20	V_{SS}	Ground potential	-
21	V_{SS}	Ground potential	-
22~27	-	(Not to connected with LCD circuit1	

Note) Pin No. and its locrtior are shown in Fig. 8.



Note) 1·2 means 1st row 2nd column dot.

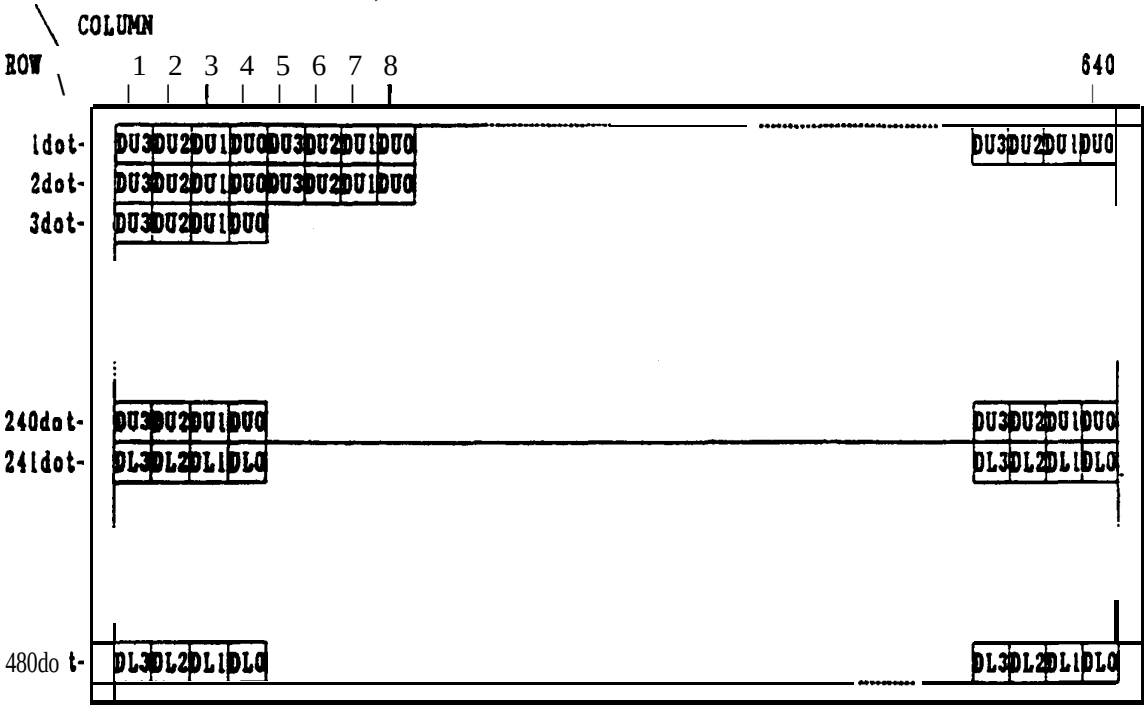


Fig. Dot chart of display area

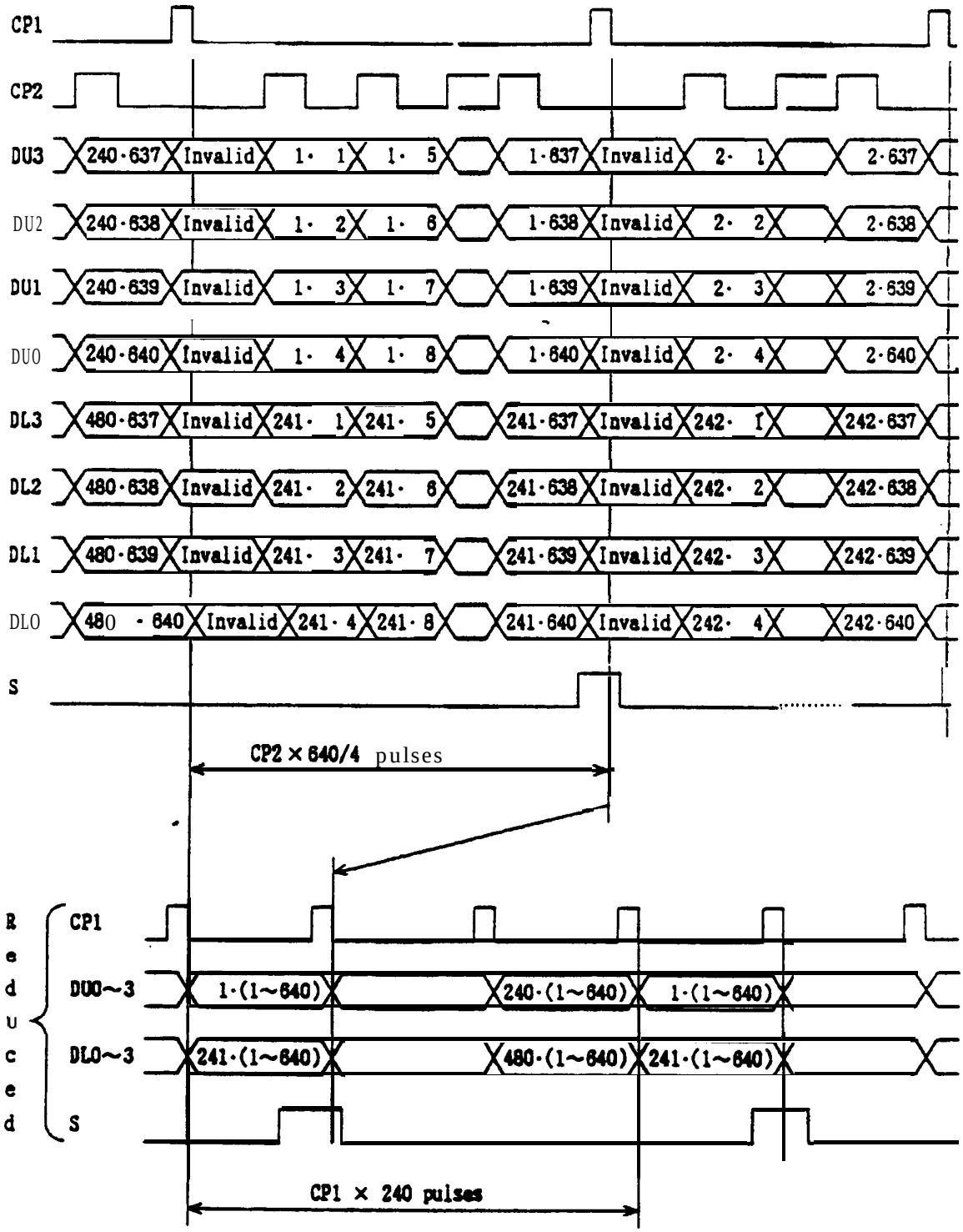


Fig.2 Data input timing

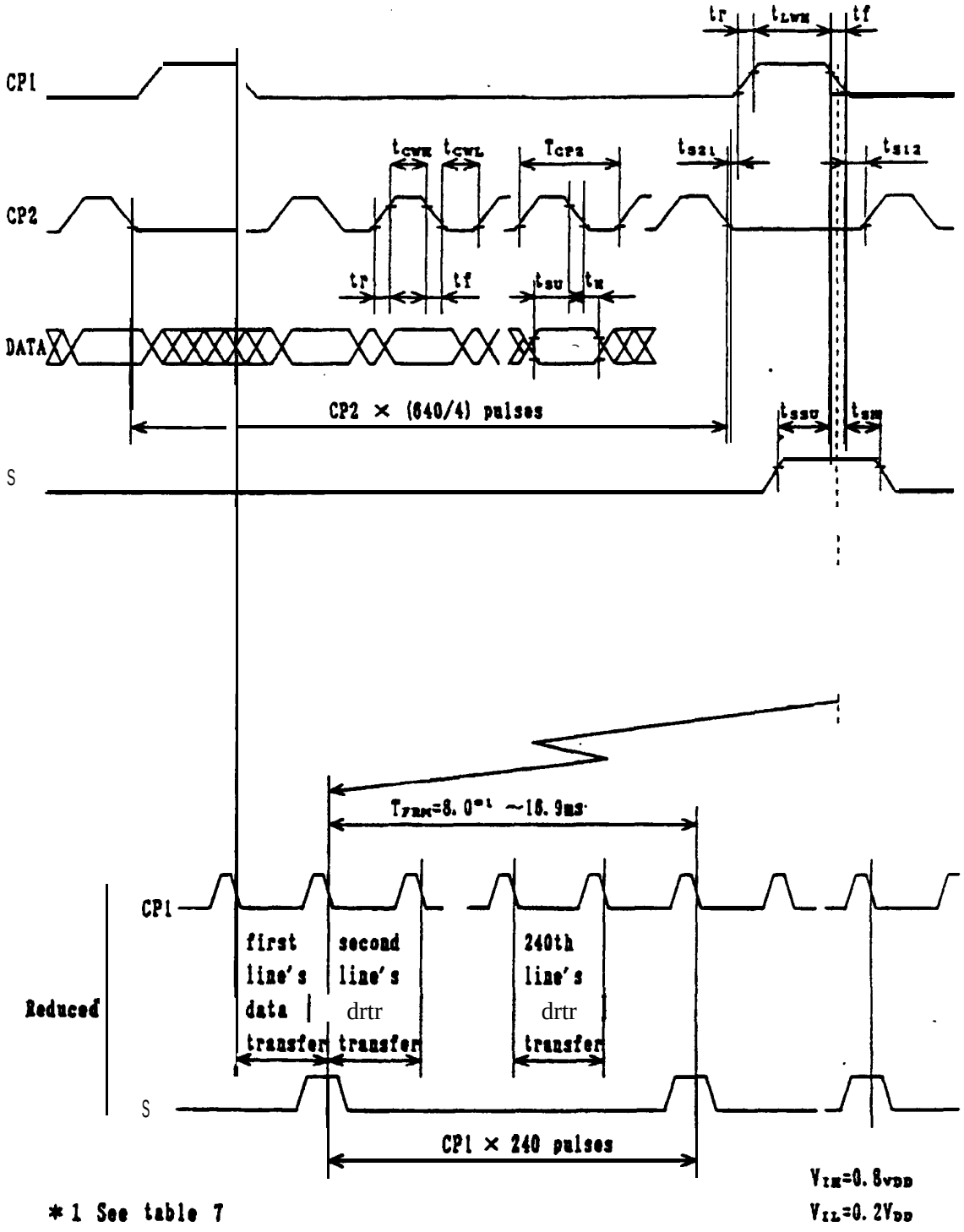


Fig.3 Interface timing chart

Table 7 Interface timing ratings

Item	Symbol	Bating MIN.	TYP.	MAX.	Unit
Frame cycle	T_{FRM}	8.0*1		16.9	ns
CP2 clock crclr	T_{CP2}	152			ns
.H' level clock width	t_{CWH}	65			ns
'L' level clock width	t_{CWL}	65			as
● H' level latch clock width	t_{LWH}	T0			ns
Data set up time	t_{SU}	50			ns
Data hold tire	t_H	40		.	ns
S set up time	t_{SSU}	100			as
S hold time	t_{SH}	100			ns
CP2↑ clock allowance time from CP1↓	t_{S21}	0			ns
CP1↑ clock allowance tire from CP2↓	t_{S12}	0			ns
Clock rise/fall time	tr, tf			t_{rf}*2	ns

*1 : LCD unit functions at the ● inirum frame cycle of 8 ms (Maximum franc frequency *of* 125Hz). Owing to the characteristics of LCD unit, . shadowing' will become more eminent as frame frequency goes up, while flicker will be reduced.

According to our experiments, frame cycle of 11.7 ms Min. or frame frequency of 85 Hz Max. will demonstrate optimum display quality in terms of flicker and . shadowing' . But since judgement of display quality is subjective and display quality such as 'shadowing' is pattern dependent, it is recommended that decision of frame cycle or frame frequency, to which power consumption of the LCD rait is propotional, be made based on your own through testing on the LCD unit with every possible patterns displayed on it.

*2 : $t_{rf} = 50$ in case $t_{CT} = (T_{CP2} - t_{CWH} - t_{CWL})/2 \geq 50$

$t_{rf} = t_{CT}$ in case $t_{CT} = (T_{CP2} - t_{CWH} - t_{CWL})/2 < 50$

8. Unit Driving Method

8.1 Circuit configuration

tic. 7 shows the block diagram of the Unit's circaitrr.

8. 2 Display Face Configuration

The display face electrically consists of txo (upper and lower) display segments so that the unit may offer higher contrast by reducing drive duty ratio. Zach display segment (640×240 dots) is driven at 1/240 duty ratio.

8. 3 Input Data and Control Signal

The LCD driver is 80 bits LSI, consisting of shift registers, latch circnits and LCD driver circuits.

Display data which are externally divided into data for each row (640dots) will be sequentially transferred in the form of I-bit parallel data through shift registers by Clock Signal CP2 from the left top of the display face.

When data of oae row (640dots) have been input, they will be latched in the form of parallel data for 640 lines of signal electrodes by latch signal CP1. Thea the corresponding drive signal will be transmitted to the 640 liars of column electrodes of the LCD *panel* by the LCD drive circuits.

At this tire, scan start-or signal S hu been transferred from the scan signal driver to the 1st row of scan electrodes, and the contents of the data signals are displayed oa the 1st rows of upper ad lower half of the display face according to the combinations of voltages applied to the scan and signal electrodes of the LCD.

While the 1st ron of data are being displayed, the 2nd rows of data are entered. When 640 dots of data have been transferred thaa latched on the falling edge of CP1 clock, t&e display face proceeds to the 2nd rows of display.

Such drtr input will be repeated up to the 240th row of each display segment, from upper to lower rows, to complete one frame of display by time sharing method. Then data input proceeds to the next display face.

Scan start-w signal S generates scan signal to drive horizontal electrodes.

Since DC voltage, if applied to LCD panel, causes chemical reaction which will deteriorate LCD panel, drive waveform shall be inverted at every display frame to prevent the generation of such DC voltage. Control Signal M plays suchrole.

Because of the characteristics of the CMOS driver LSI, the power consumption of the aait goes up as the operating frequency CP2 increases. Thus the driver LSI applies the system of tranferring 4-bits parallel data through the 4 lines of shift registers to reduce the data transfer speed CP2. Thanks to the LSI, the power coasuaptioa of the unit will be minimized.

In this circuit configuration, I-bit display data shall be therefore input to data input pins of DU_{0-3} (upper display segment) sad DL_{0-3} (lower display segment).

Furthermore the LCD unit adopts bus line system for data input to minimize the power consumption. In this system data input terminal of each driver LSI rctivrted only when relevant data input' is fed.

Data input for column electrodes of both the upper and ths lower display segment and chip select of driver LSI are made as follows:

The driver LSI at the left end of the display fro is first selected, and the adjacent driver LSI of the right side is selected when 80 dots data (20CP2) is fed. This process is sequentially continued until data is fed to the driver LSI at the right end of the display face.

This process is simultaneously followed at the column drivers LSI's of both the upper and the lower display segments. Thus data input for both the upper sad the lower display repeats must be fed through 4-bit bus line sequentially from the left end of the display face.

Since this graphic display unit coatrire no ret leeh RAM. it requires data and timing pulse inputs even for static dieplu.

The timing chart of input signals are shown in Fig. 3 and Table 7.

7. Optical Characteristics

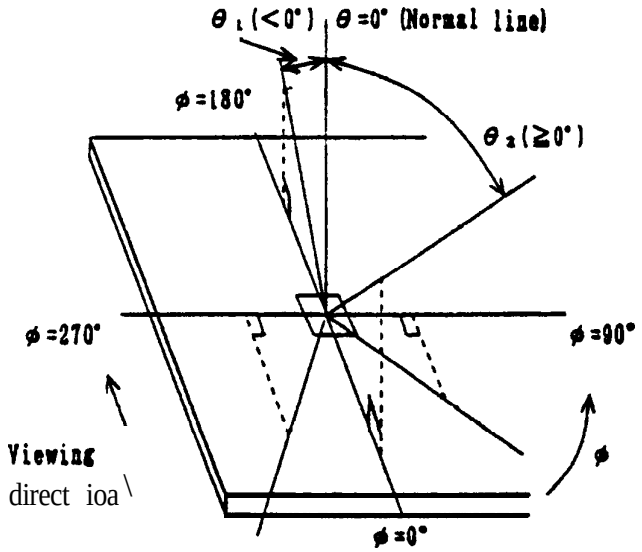
Ta=25℃, V_{DD}=5.0V, V_{EE}-V_{SS}=-18.7V TYP

Table 8

Following specs are based upon the electrical measuring conditions, on which the contrast of perpendicular direction (θ=0°) will be MAX.

Parameter		Symbol	Condition		MIN.	TYP.	MAX.	Unit	Remark
Viewing angle range		$\theta_2-\theta_1$	ϕ=0°	Co≧2.0	45	-	-	dgr.	Note 1
		θ_1	$\theta_1<\theta_2$	Co=2.0	-	-	-15	dgr.	
		θ_2			25	-	-	dgr.	
		$\theta_2-\theta_1$	ϕ=90°	Co≧2.0	55	-	-	dgr.	
		θ_1	$\theta_1<\theta_2$	Co=2.0	-	-	-25	dgr.	
		θ_2			25	-	-	dgr.	
Contrast ratio		Co	θ=0°, ϕ=0°		3.0	6.0	-	-	Note 2
Response time	Rise	τr	θ=0°, ϕ=0°		-	120	170	ms	
	Decay	τd	θ=0°, ϕ=0°		-	130	180	ms	Note 3

Note 1) The viewing angle range is defined as shorn below.



* Angle θ_1, θ_2 and ϕ shell fall within the range over which the displayed character can be read.

Fig 4. Definition of Viewing Angle

Mote 2) Contrast ratio is defined as follows:

Contrast ratio is calculated by using the following formula when the waveform voltage (Fig. 6) is applied in the optical chrrrcteristics test method (Fig. 5).

$$Co = \frac{\text{Photo-detector output voltage with non-select waveform being replied}}{\text{Photo-detector output voltage with select waveform being replied}}$$

Note 31 The response characteristics of photodetector output are measured as shon in tic. 6, assuming that input signals are applied so as to select and deselect the dots to be ● eesured, in the optical characteristics test method shown in Fig. 5

Note 4) Table 8 shows the optical characterisrics detected when the LCD applied voltage waveforms are in the highest frequency*.

* The most critical condition for the characteristics of LCD.

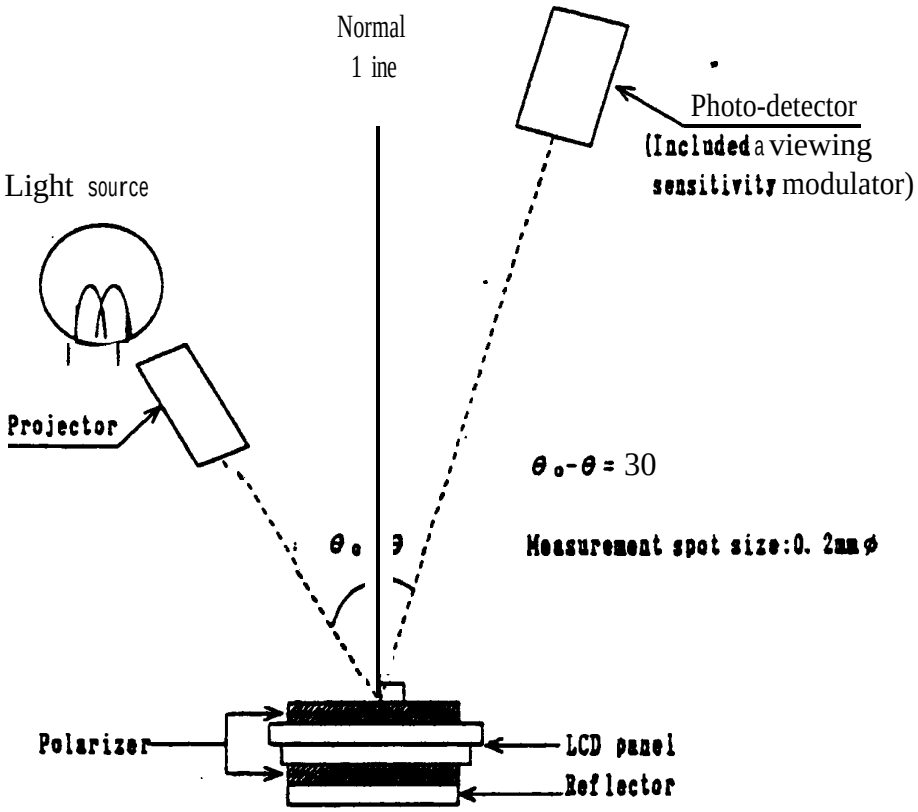


Fig 5. Optical Characteristics Test Method

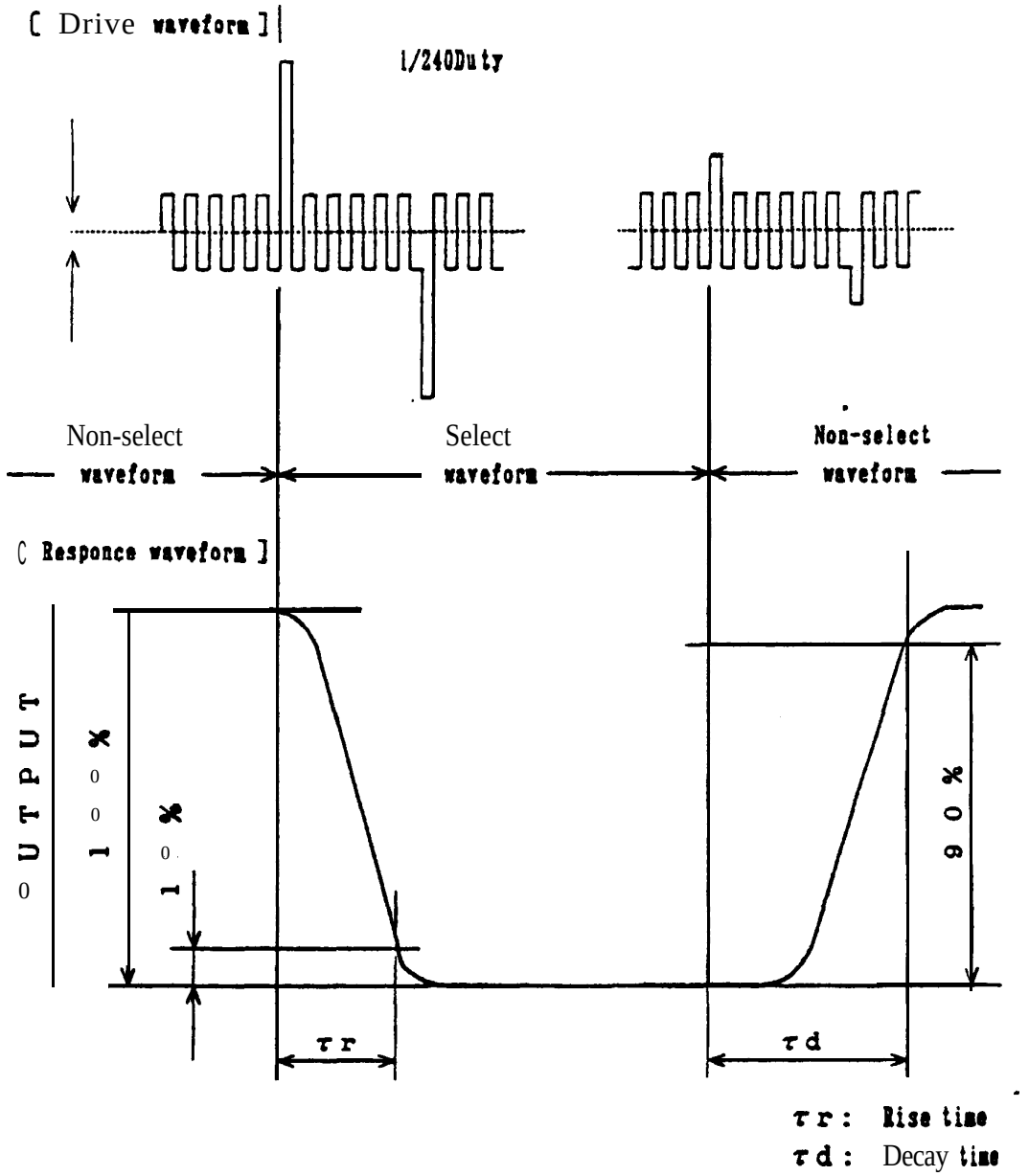
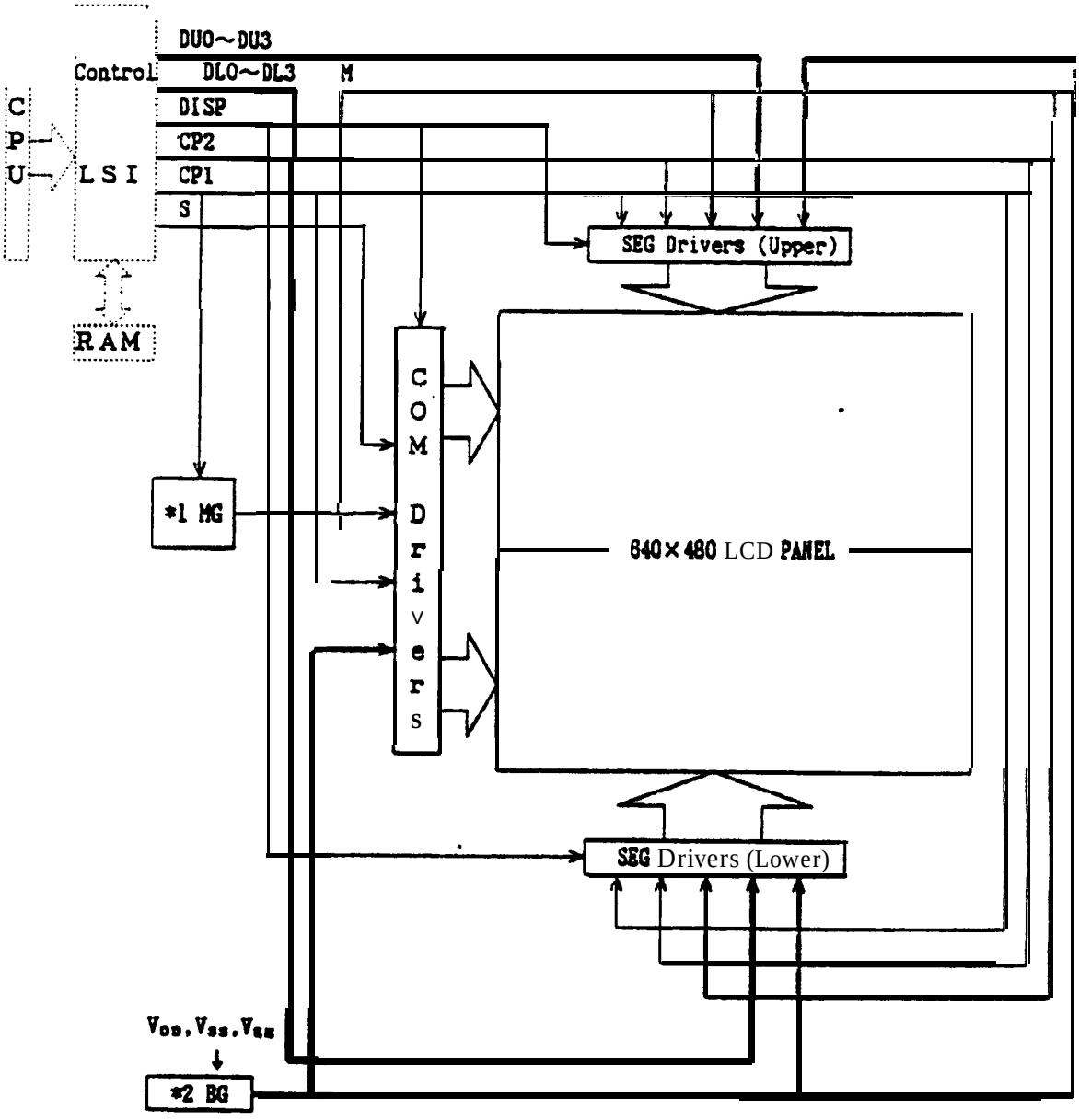


Fig.6 Difinition of Response Time



*1 MG: M GENERATOR CIRCUIT
*2 BG: BIAS GENERATOR CIRCUIT

Fig.7 Circuit block diagram

SHARP

SPEC No.	MODEL No.	PAGE
LC92517	LM641521	18

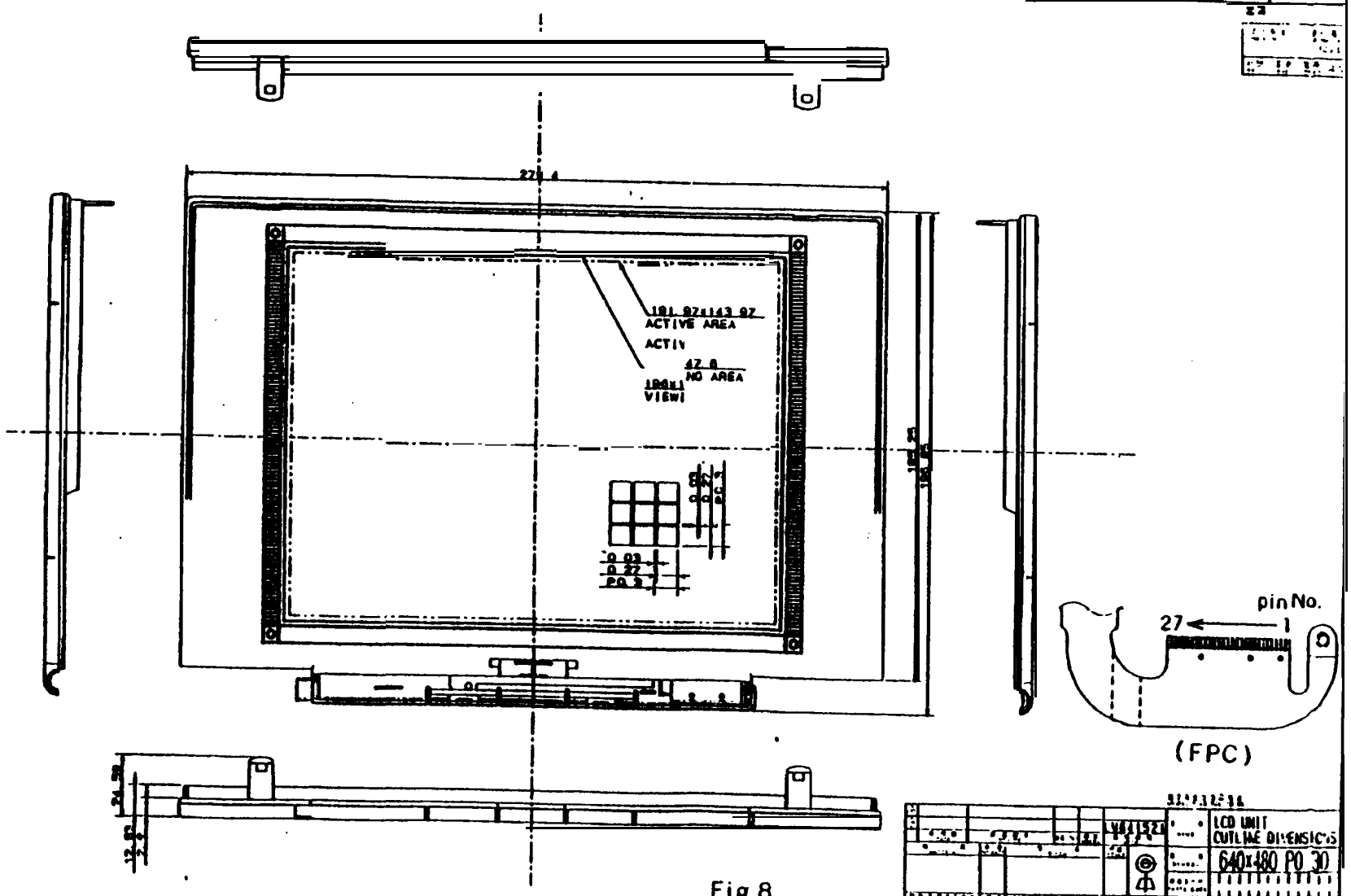


Fig.8

8. Precautions

1) Industrial (Mechanical) design of the product in which this LCD unit will be incorporated mast be so made tbat the viewing angle charactrrirtics of the LCD may be optimized.

This unit's viewing angle is ill&rated in Fig. 9.

θ_1 < viewing angle < θ_2 ($\theta_1 < 0°$, $\theta_2 \geq 0°$)

(For the specif ic values of θ_1, θ_2, refer to the tablr 8.)

Please consider thr optimum viewing cooditioas according to the purpose when installing the unit.

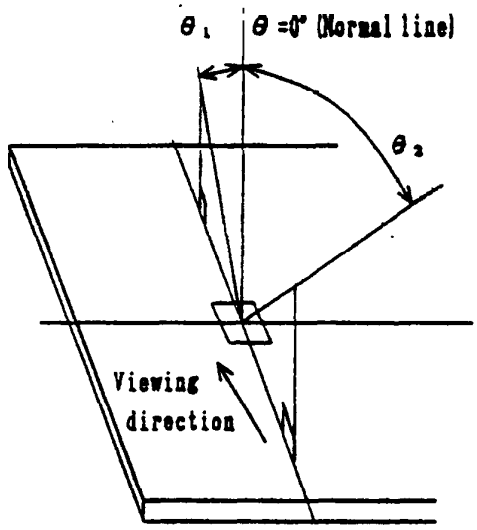


Fig 9. Dot matrix LCD viewing angle

2) This unit is installed using mounting tabs at the foar corners of PCB or bezel.

Thor installing the unit, pay attention and handle carefully aot to allow any undue stress such u twist or bend.

A transparent acrylic resin board or other type of protective panel should be attached to the front of the unit to protect the polarizer, LCD cells, etc.

3) Since the front polarizer is easily damaged, please pay attention not to scratch on its face.

4) *If* the *surface of* the LCD ceils aeeds to be cleaned, ripe it swiftly with cotton or other *soft* cloth. *If* still aot completely clear, blow oa its and wipe.

5) later droplets, etc. must be wiped off immediately since they may cause *color* changer. staining, etc. if reuioed for a long time.

6) Since LCD is made of glass plates, dropping the unit or banging it against hard objects may cause cracking or fragmentation.

7) CMOS LSIs are equipped in this unit, so care must be taken to avoid the electro static charge, by earthing human body, etc. Take the following measures, to protect the unit from the electric discharge via mounting tabs **fror** the main systen the electrified with static electricity.

(1) Earth the retrllic case *of* the main system (contact of the unit and main sys tem).

(2) Insulate the unit and uia system by attaching insulating rashers made of bakelite or nylon, etc.

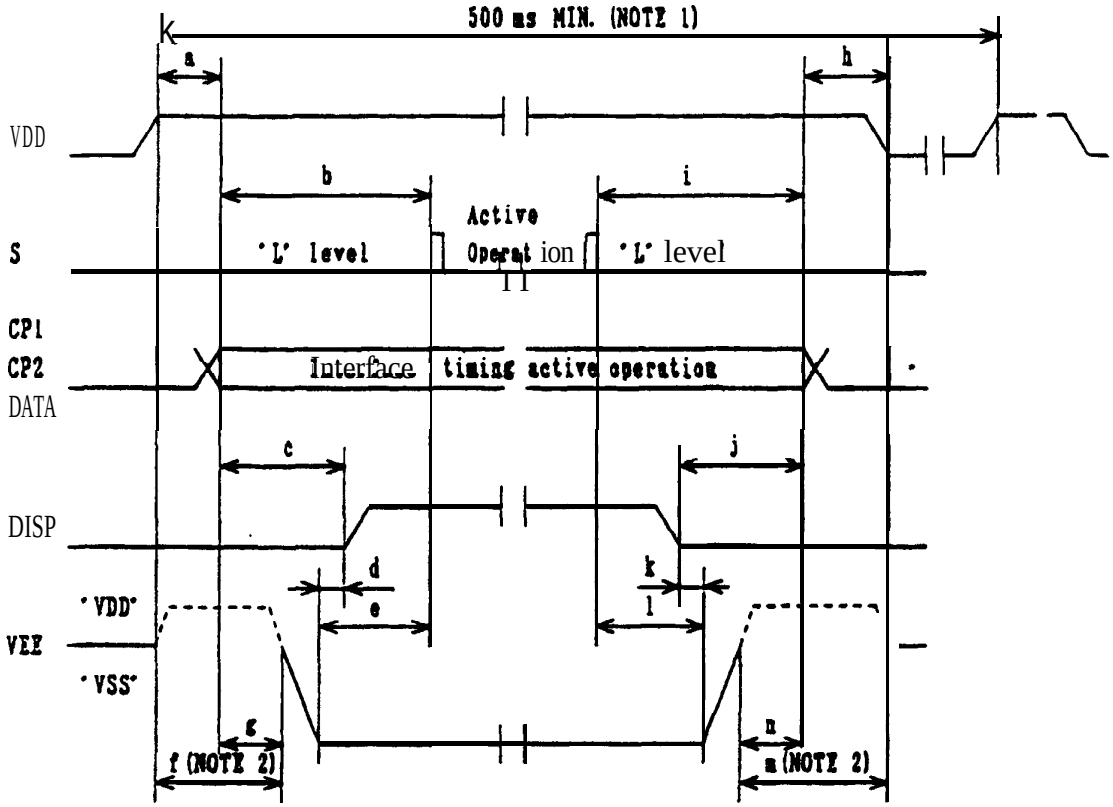
81 The unit should be driven according to the specified ratings to avoid malfunction of permanent damage. DC voltage drive leads to rapid deterioration *of* LC, so **ensure** that the drive is alternating waveform by coatinoas application of the signal M. Especially the power ON/OFF sequence shorn on next page is strongly recommended to avoid latch-up of driver LSIs and application of DC voltage to LCD panel.

9) Avoid to expose the unit to the direct sun-light, strong ultra-violet light, etc. *for* a long time.

10) If stored at temperatures below specified storage temperature, the LC MY freeze and be deteriorated. If storage temperature exceed the specified rating, the molecular orieatatioa of the LC may change to that of a liquid, and they may not revert to their original state. As far as possible always store at normal room temperature.

11) Disassembling the LCD unit can cause permanent damage and should be strictly avoided.

Supply voltage sequence condition



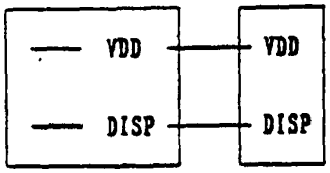
POWER ON			POWER OFF		
SYMBOL	With DISP control	Without DISP control	SYMBOL	With DISP control	Without DISP control
a	0 ns MIN.	0 ns MIN. 20 u MAX.	h	0 ns MIN.	0 ns MIN. 20 ns MAX.
b	0 ns MIN.	20 ns MIN.	i	0 ns MIN.	20 ns MIN.
c	20 ns MIN.	-	j	20 ns MIN.	-
d	0 ns MIN.	-	k	0 ns MIN.	-
e		0 u MIN.	l	-	0 ns MIN.
f	0 ns MIN.	(NOTE2)	m	0 ns MIN.	(NOTE2)
g	-	0 ns MIN. 100 ns MAX.	n	-	100 ns MIN.

(Note 1) Power ON/OFF cycle time. All signals ud power line shallbe in accordance with above sequence in case of power ON/OFF.

(Note 2 VEE to be set at 'VDD level' or 'open'. VEE shorld be in accordance with the dotted line when DISP (display control signal) is not used.

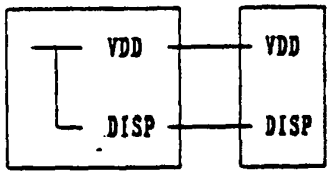
(note3) Connection of DISP (pin No. 4)

○With DISP control
input DISP control signal shown on page.19



Control Circuit LCD UNIT

○Without DISP control
DISP to be connected with VDD.



Control Circuit LCD UNIT

9. Applicable inooectioa standard
The LCD unit shall meet the following inspection standard
:S-U-012-01

10. This specification describes display quality in case of no gray scale.
Since display quality can be affected by gray scale methods, display quality shall be carefully evaluated for the usability of the LCD UNIT in case gray scale is displayed oa the LCD UNIT.

WARNING

DON'T USE ANY MATERIALS WHICH EMIT FOLLOWING GAS FROM EPOXY RESIN (AMINE) HARDENER) AND SILICONE ADHESIVE AGENT (DEALCOHOL OR DEOXIM) TO PREVENT CHANGE POLARIZER COLOR OWING TO GAS.