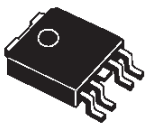
L4987 SERIES

VERY LOW DROP VOLTAGE REGULATORS WITH INHIBIT AND DROPOUT CONTROL FLAG

- VERY LOW DROPOUT VOLTAGE (0.25V TYP.)
- DROPOUT CONTROL FLAG
- VERY LOW QUIESCENT CURRENT (TYP. 90 µA IN OFF MODE, 500µA IN ON MODE)
- OUTPUT CURRENT UP TO 200 mA
- LOGIC-CONTROLLED ELECTRONIC SHUTDOWN
- OUTPUT VOLTAGES OF 3V, 5V 8.7V 12V
- INTERNAL CURRENT AND THERMAL LIMIT
- ONLY 2.2µF FOR STABILITY
- AVAILABLE IN ± 2% SELECTION AT 25 °C
- SUPPLY VOLTAGE REJECTION: 70 dB (TYP.)

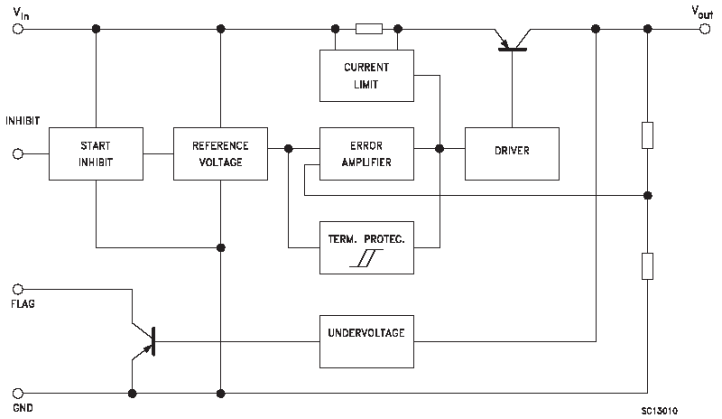


PPAK

DESCRIPTION

The L4987 is a very low drop regulator available in PPAK. The very low drop-voltage (0.5V Max at 200 mA) and the very low quiescent current make it particularly suitable for low noise, low power applications, and in battey powered systems. The input dump protection up to 40V makes it ideal for automotive applications. a shutdown Logic Control function is available (pin2, TTL compatible). This means that when the device is used as a local regulator, it is possible to put a part of the boad in standby, decreasing the total power consumption. The regulator employs an output pin (open collector) providing a logic signal when the pass transistor is in saturation at low input voltage, this signal can be used to prevent the pop-up phenomenon in the car radio. In battery powered systems (the cellular phone, notebook) it is possible to use the flag to monitor the battery charge status through the dropout of the regulator.

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

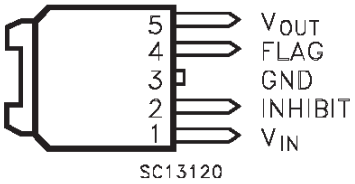
Symbol	Parameter	Value	Unit
V_i	DC Input Voltage	40	V
I_o	Output Current	Internally limited	mA
P_{tot}	Power Dissipation	Internally limited	mW
T_{stg}	Storage Temperature Range	- 40 to 150	^oC
T_{op}	Operating Junction Temperature Range	- 40 to 125	^oC

Absolute Maximum Rating are those values beyond wich damage to the device may occur. Functional operation under these conditions is not implied.

THERMAL DATA

Symbol	Parameter	DPAK/PPAK	Unit
$R_{thj-case}$	Thermal Resistance Junction-case	8	$^oC/W$
$R_{thj-amb}$	Thermal Resistance Junction-ambient	100	$^oC/W$

CONNECTION DIAGRAM (top view)



ORDERING NUMBERS

Type	Output Voltage
L4987CPT30 (*)	3 V
L4987CPT50 (*)	5 V
L4987CPT87 (*)	8.7 V
L4987CPT120 (*)	12 V

(*) Available even in tape & reel

ELECTRICAL CHARACTERISTICS FOR L4987CPT30 (refer to the test circuits, V_I = 6 V, I_{OUT} = 5 mA, T_j = 25 °C, C_i = 0.1 µF, C_o = 2.2 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	I_o = 200 mA, V_i = 6 V I_o = 200 mA, V_i = 6 V -40<T_J<125 °C	2.94 2.88	3	3.06 3.12	V V
V_i	Operating Input Voltage	I_o = 200 mA	3.62		18	V
I_{out}	Output Current Limit		250			A
ΔV_o	Line Regulation	V_i = 4.3 to 18 V, I_o = 0.5 mA		2.4	14	mV
ΔV_o	Load Regulation	V_i = 4.1 V I_o = 0.5 to 200 mA		3	20	mV
I_d	Quiescent Current	ON MODE V_i = 4.3 to 18 V I_o = 0 mA V_i = 4.3 to 18 V I_o = 200 mA		 0.7 1.5	 1 6	 mA mA
		OFF MODE V_i = 12 V		90	180	µA
SVR	Supply Voltage Rejection	I_o = 5 mA V_i = 5.3 V ± 1V f = 120 Hz f = 1 KHz f = 10 KHz		 80 75 60		 dB dB dB
V_d	Dropout Voltage	I_o = 200 mA I_o = 200 mA -40 < T_J < 125 °C		0.25	0.5 0.7	V V
V_{il}	Control Input Logic Low	-40 < T_J < 125 °C			0.8	V
V_{ih}	Control Input Logic High	-40 < T_J < 125 °C	2			V
I_i	Control Input Current			10		µA
C_O	Output Bypass Capacitance	ESR = 0.5 to 10 Ω I_o = 0 to 200 mA -40 < T_J < 125 °C	2	10		µF
V_{fl}	Control Flag Output Low	V_i - V_o < V_{cesat} power, I_{fl} = 6 mA I_o = 200 mA			0.5	V
I_{fh}	Control Flag Output High Leakage Current	V_i > 3.62 V V_{oh} = 15 V			10	µA

ELECTRICAL CHARACTERISTICS FOR L4987CPT50 (refer to the test circuits, V_I = 8 V, I_{OUT} = 5mA, T_j = 25 °C, C_i = 0.1 µF, C_o = 2.2 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	I_o = 200 mA, V_i = 8 V I_o = 200 mA, V_i = 8 V -40<T_J<125 °C	4.9 4.8	5	5.1 5.2	V V
V_i	Operating Input Voltage	I_o = 200 mA	5.7		18	V
I_{out}	Output Current Limit		250			A
ΔV_o	Line Regulation	V_i = 6.3 to 18 V, I_o = 0.5 mA		3	20	mV
ΔV_o	Load Regulation	V_i = 3.6 V I_o = 0.5 to 200 mA		3	20	mV
I_d	Quiescent Current	ON MODE V_i = 6.3 to 18 V I_o = 0 mA V_i = 6.3 to 18 V I_o = 200 mA		 0.7 1.5	 1 6	 mA mA
		OFF MODE V_i = 12 V		90	180	µA
SVR	Supply Voltage Rejection	I_o = 5 mA V_i = 7.3 V ± 1V f = 120 Hz f = 1 KHz f = 10 KHz		 76 71 58		 dB dB dB
V_d	Dropout Voltage	I_o = 200 mA I_o = 200 mA -40 < T_J < 125 °C		0.3	0.5 0.7	V V
V_{il}	Control Input Logic Low	-40 < T_J < 125 °C			0.8	V
V_{ih}	Control Input Logic High	-40 < T_J < 125 °C	2			V
I_i	Control Input Current			10		µA
C_O	Output Bypass Capacitance	ESR = 0.5 to 10 Ω I_o = 0 to 200 mA -40 < T_J < 125 °C	2	10		µF
V_{fl}	Control Flag Output Low	V_i - V_o < V_{cesat} power, I_{fl} = 6 mA I_o = 200 mA			0.5	V
I_{fh}	Control Flag Output High Leakage Current	V_i > 5.85 V V_{oh} = 15 V			10	µA

ELECTRICAL CHARACTERISTICS FOR L4987CPT87 (refer to the test circuits, V_I = 11.7V, I_{OUT} = 5mA, T_j = 25 °C, C_i = 0.1 µF, C_o = 2.2 µF unless otherwise specified)

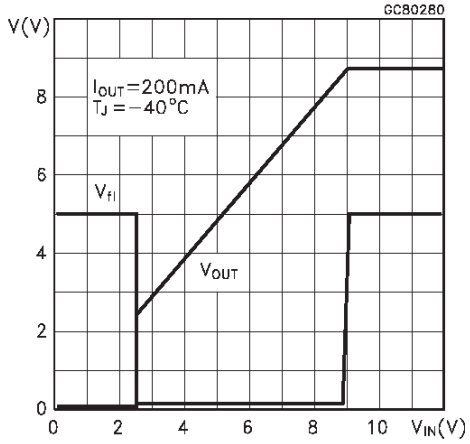
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	I_o = 200 mA, V_i =11.7 V I_o = 200 mA, V_i =11.7 V -40<T_J<125°C	8.526 8.35	8.7	8.874 9.05	V V
V_i	Operating Input Voltage	I_o = 200 mA	9.55		18	V
I_{out}	Output Current Limit		250			A
ΔV_o	Line Regulation	V_i = 10 to 18 V, I_o = 0.5 mA		4	24	mV
ΔV_o	Load Regulation	V_i = 10 V I_o = 0.5 to 200 mA		3	20	mV
I_d	Quiescent Current	ON MODE V_i = 10 to 18 V I_o = 0 mA V_i = 10 to 18 V I_o = 200 mA		 0.5 3	 1 6	 mA mA
		OFF MODE V_i = 12 V		90	180	µA
SVR	Supply Voltage Rejection	I_o = 5 mA V_i = 11 V ± 1V f = 120 Hz f = 1 KHz f = 10 KHz		 71 68 55		 dB dB dB
V_d	Dropout Voltage	I_o = 200 mA I_o = 200 mA -40 < T_J < 125 °C		0.3	0.5 0.7	V V
V_{il}	Control Input Logic Low	-40 < T_J < 125 °C			0.8	V
V_{ih}	Control Input Logic High	-40 < T_J < 125 °C	2			V
I_i	Control Input Current			10		µA
C_O	Output Bypass Capacitance	ESR = 0.5 to 10 Ω I_o = 0 to 200 mA -40 < T_J < 125 °C	2	10		µF
V_{fl}	Control Flag Output Low	V_i - V_o < V_{cesat} power, I_{fl} = 6 mA I_o = 200 mA			0.5	V
I_{fh}	Control Flag Output High Leakage Current	V_i > 9.55 V V_{oh} = 15 V			10	µA

ELECTRICAL CHARACTERISTICS FOR L4987CPT120 (refer to the test circuits, V_I = 15V, I_{OUT} = 5mA, T_j = 25 °C, C_i = 0.1 µF, C_o = 2.2 µF unless otherwise specified)

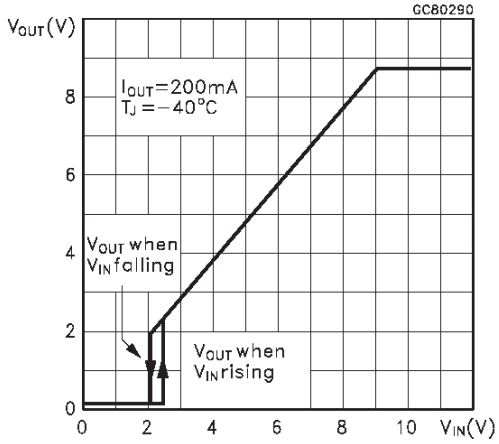
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	I_o = 200 mA, V_i =15 V I_o = 200 mA, V_i =15 V -40<T_J<125°C	11.76 11.52	12	8.874 9.05	V V
V_i	Operating Input Voltage	I_o = 200 mA	12.75		18	V
I_{out}	Output Current Limit		250			A
ΔV_o	Line Regulation	V_i = 13.5 to 18 V, I_o = 0.5 mA		5	30	mV
ΔV_o	Load Regulation	V_i = 13.5 V I_o = 0.5 to 200 mA		3	20	mV
I_d	Quiescent Current	ON MODE V_i = 13.5 to 18 V I_o = 0 mA V_i = 13.5 to 18 V I_o = 200 mA		 0.5 3	 1 6	 mA mA
		OFF MODE V_i = 12 V		90	180	µA
SVR	Supply Voltage Rejection	I_o = 5 mA V_i = 14.5 V ± 1V f = 120 Hz f = 1 KHz f = 10 KHz		 67 64 51		 dB dB dB
V_d	Dropout Voltage	I_o = 200 mA I_o = 200 mA -40 < T_J < 125 °C		0.3	0.5 0.7	V V
V_{il}	Control Input Logic Low	-40 < T_J < 125 °C			0.8	V
V_{ih}	Control Input Logic High	-40 < T_J < 125 °C	2			V
I_i	Control Input Current			10		µA
C_O	Output Bypass Capacitance	ESR = 0.5 to 10 Ω I_o = 0 to 200 mA -40 < T_J < 125 °C	2	10		µF
V_{fl}	Control Flag Output Low	V_i - V_o < V_{cesat} power, I_{fl} = 6 mA I_o = 200 mA			0.5	V
I_{fh}	Control Flag Output High Leakage Current	V_i > 12.75 V V_{oh} = 15 V			10	µA

TYPICAL PERFORMANCE CHARACTERISTICS (unless otherwise specified T_J=25°C, C_{IN}=C_{OUT}=1µF)

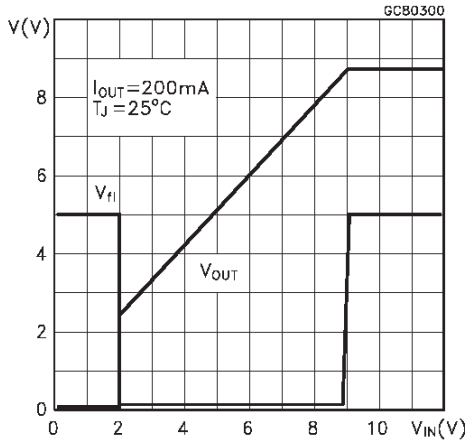
Output and Flag Voltage vs Input Voltage



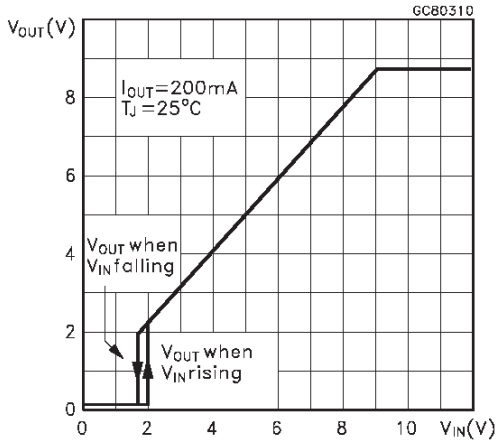
Output Voltage vs Input Voltage



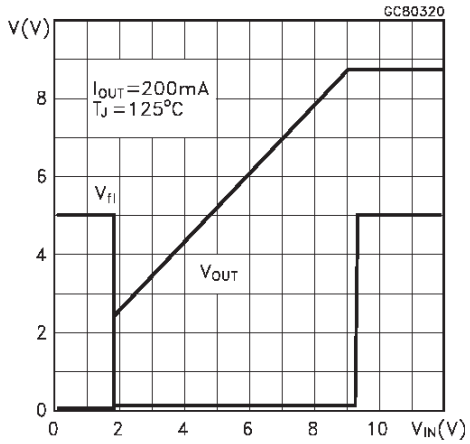
Output and Flag Voltage vs Input Voltage



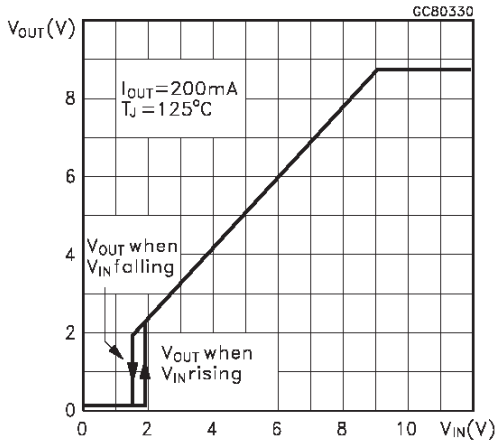
Output Voltage vs Input Voltage



Output and Flag Voltage vs Input Voltage



Output Voltage vs Input Voltage



APPLICATION HINT OF L4987CPT30

How to use the control flag

The flag produces a logic "low" whenever the output fall out out of regulation. An "out of regulation condition can result from:

1) Low Input Voltage ($V_{IN} \leq V_{OUT} + V_{DROP}$)

2) Curent Limiting

3) Thermal Limiting

Figure 1 to 2 show the typical behaviour of the output voltage and the control flag versus the input voltage and the temperatre. No hysteresis is implemented; so the response of V_{OUT} and V_{FLAG} are the same either when the V_{IN} ramps up or down.

The control flag is an open collector which requires an external pull-up resistor. This may be connected to the regulator output (Figure 3) or some other supply voltage (Figure 4).

Using the regulator output prevents an invalid "high" on the flag which occurs if it is pulled up to an external voltage while the regulator input voltage is reduced below about 2V (Figue 5).

Concerning the pull-up resistor its value must be properly chosen as suggested below. When "low" as it is possible to see in figure 6 the control flag voltage is:

$V_{FLAG(LOW)} = V_{CE} = 0.5 = V_{SUPPLY} - R_{PULL} \times I_{FL}$

V_{SUPPLY} is chosen by design and, thus is known, while I_{FL} must be at maximum 10mA. Then

$0.5V \geq V_{SUPPLY} - R_{PULL} \times 10mA$

The minimum value of R_{PULL}, is, so, determined by the following equation:

$$R_{PULL(min)} \geq V_{SUPPLY} - \frac{0.5}{10\ mA}$$

Regarding the maximum value of R_{PULL} note that its value depends of the type of logic used (CMOS, TTL etc.), the transistor leackage current and the presence or not of a load on V_{FLAG}.

The following example shows how to determine the R_{PULL} max in the case of CMOS logic, no load and 10µA (for L4978 it is the maximum value of I_{FH}) of control flag leakage current.

Becaause of CMOS logic:

$$V_{FLAG(HIGH)} \geq \frac{2}{3} V_{SUPPLY}$$

But:

$$V_{FLAG(HIGH)} = V_{SUPPLY} - R_{PULL} \times I_{FH} \geq \frac{2}{3} V_{SUPPLY}$$

so, the maximum value is determined by the following equation:

$$R_{PULL(MAX)} \leq \frac{\frac{1}{3} V_{SUPPLY}}{10\ A}$$

Figure 1: Output and Flag Voltage vs Input

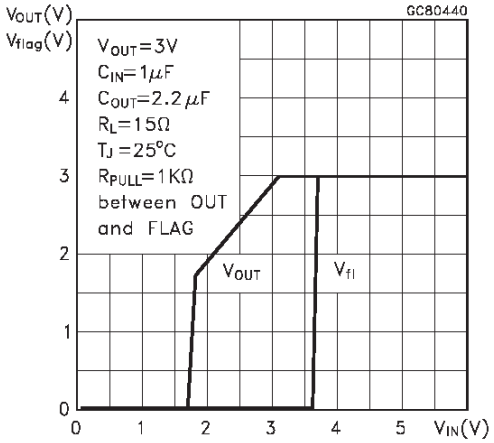


Figure 2: Flag Voltage vs Input

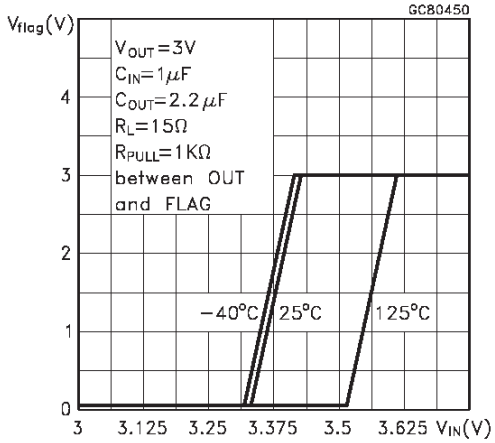


Figure 3: Test Circuit

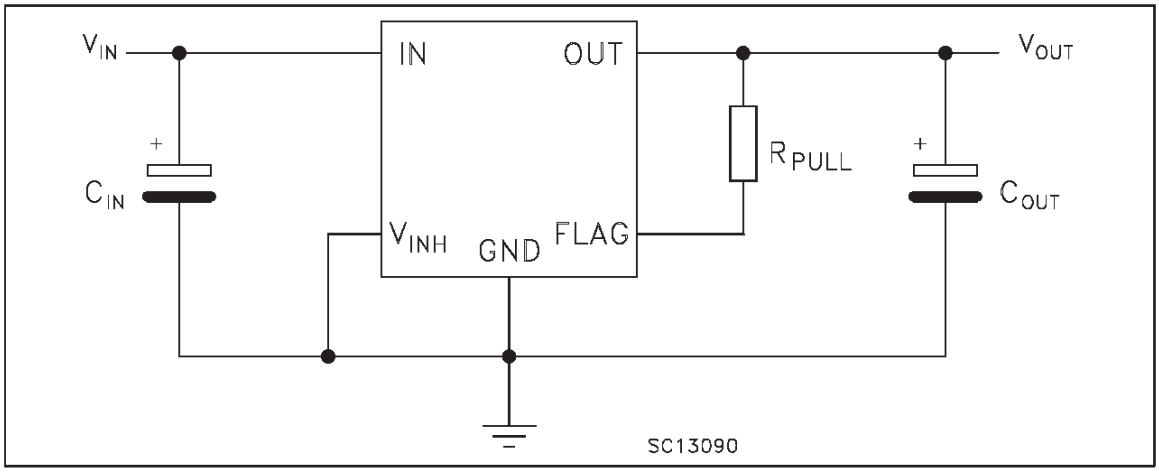


Figure 4: Test Circuit

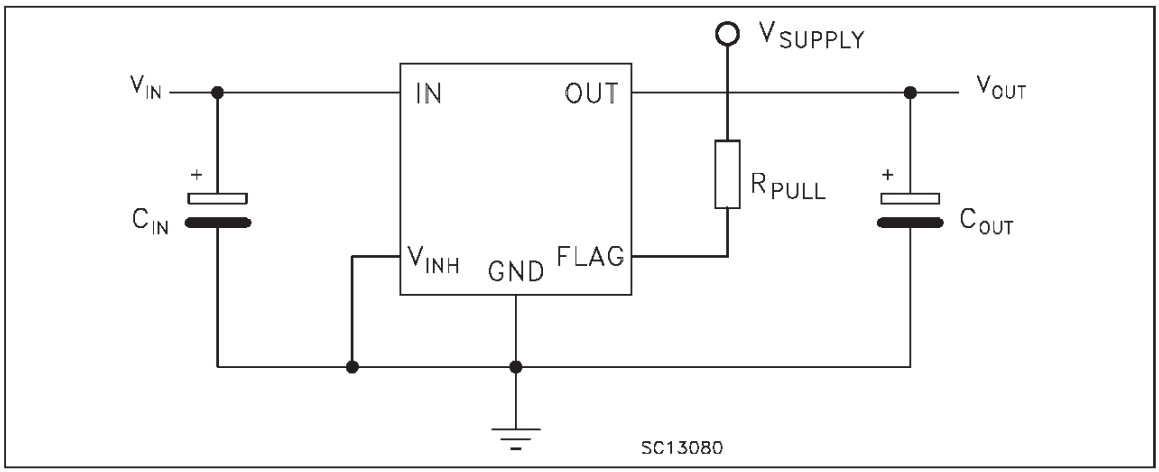


Figure 5: Output and Flag Voltage vs Input

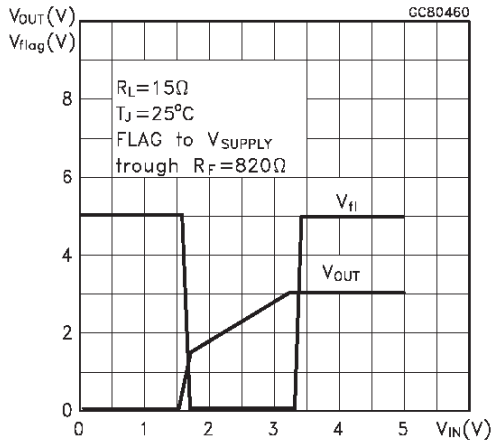
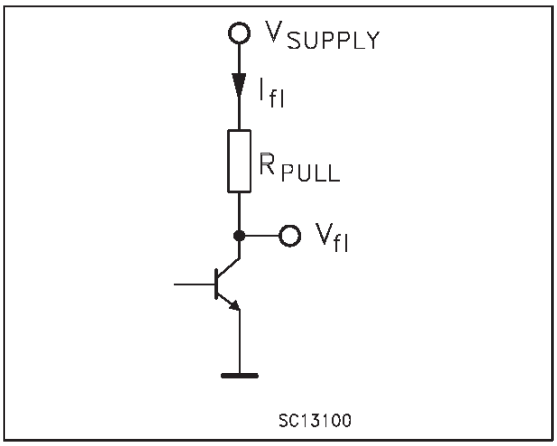
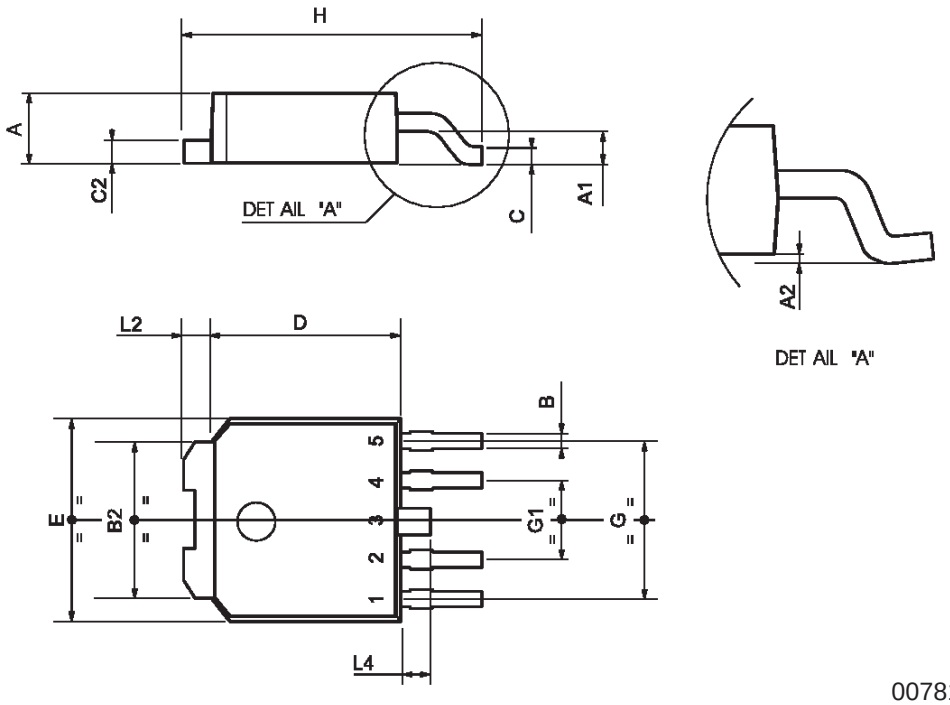


Figure 6: Equivalent Output Circuit



PPAK MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.4		0.6	0.015		0.023
B2	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.9		5.25	0.193		0.206
G1	2.38		2.7	0.093		0.106
H	9.35		10.1	0.368		0.397
L2		0.8	1		0.031	0.039
L4	0.6		1	0.023		0.039



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