

## Features

- Clocking Speeds Up To 40MHz
- 4 Channels
- 12 ns tr/TF at 1000pF Cload
- 1ns Rise and Fall Time Mismatch
- 1.5ns Prop Delay Mismatch
- Low Quiescent Current, <1mA
- Fast Output Enable Function, 12ns
- Wide Output Voltage Range
- $8V \geq V_L \geq -5V$
- $-2V \leq V_H \leq 15V$
- 2A Peak Drive
- 3Ω On Resistance
- Input Level Shifters
- TTL/CMOS Input Compatible

## Applications

- CCD Drivers
- Digital Cameras
- Pin Drivers
- Clock / Line Drivers
- Ultrasound Transducer Drivers
- Ultrasonic and RF Generators
- Level Shifting

## Ordering Information

Part No.	Temp. Range	Package	Outline #
EL7457CU	-40°C to +85°C	16-Pin QSOP	MDP0040
EL7457CS	-40°C to +85°C	16-Pin SO	MDP0027

## General Description

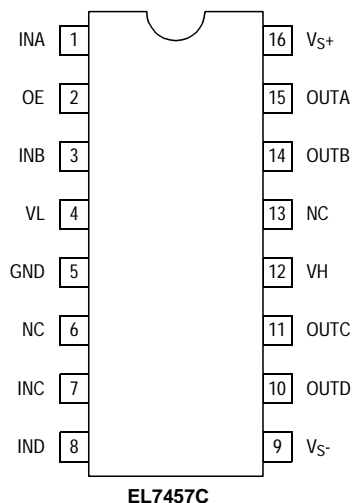
The EL7457C is an ultra-high speed, non-inverting quad CMOS driver. It is capable of running at clock rates up to 40MHz and features 2A peak drive capability and a nominal on-resistance of just 3Ω. The EL7457C is ideal for driving highly capacitive loads, such as storage and vertical clocks in CCD applications. It is also well suited to ATE pin driving, level-shifting and clock-driving applications.

The EL7457C is capable of running from single or dual power supplies while using ground referenced inputs. Each output can be switched to either the high (VH) or low (VL) supply pins, depending on the related input pin. The inputs are compatible with both 3V and 5V CMOS and TTL logic. The output enable (OE) pin can be used to put the outputs into a high-impedance state. This is especially useful in CCD applications, where the driver should be disabled during power down.

The EL7457C also features very fast rise and fall times which are matched to within 1ns. The propagation delay is also matched between rising and falling edges to within 2ns.

The EL7457C is available in both the 16-Pin QSOP and 16-Pin SOIC packages. It is specified for operation over the -40°C to +85°C temperature range.

## Pin Layout Diagram



# EL7457C

## 40MHz Non-Inverting Quad CMOS Driver

### Absolute Maximum Ratings (T<sub>A</sub> = 25°C)

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Voltage (V<sub>S+</sub> to GND) +16.5V  
 Input Voltage GND -0.3V, V<sub>S+</sub> +0.3V

Continuous Output Current 100mA  
 Storage Temperature Range -65°C to +150°C  
 Ambient Operating Temperature -40°C to +85°C  
 Operating Junction Temperature 125°C  
 Power Dissipation: See Curves  
 Maximum ESD 2kV

#### Important Note:

All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: T<sub>J</sub> = T<sub>C</sub> = T<sub>A</sub>.

### Electrical Characteristics

V<sub>S+</sub> = +5V, V<sub>S-</sub> = -5V, V<sub>H</sub> = +5V, V<sub>L</sub> = -5V, T<sub>A</sub> = 25°C, unless otherwise specified

Parameter	Description	Condition	Min	Typ	Max	Units
<b>Input</b>						
V <sub>IH</sub>	Logic "1" Input Voltage		2.0			V
I <sub>IH</sub>	Logic "1" Input Current	V <sub>IH</sub> = 5V		0.1	10	μA
V <sub>IL</sub>	Logic "0" Input Voltage				0.8	V
I <sub>IL</sub>	Logic "0" Input Current	V <sub>IL</sub> = 0V		0.1	10	μA
C <sub>in</sub>	Input Capacitance			3.5		pF
R <sub>in</sub>	Input Resistance			50		MΩ
<b>Output</b>						
R <sub>OV1</sub>	ON Resistance V <sub>H</sub> to OUT <sub>x</sub>	I <sub>OUT</sub> = -100mA		4.5	6	Ω
R <sub>OV2</sub>	ON Resistance V <sub>L</sub> to OUT <sub>x</sub>	I <sub>OUT</sub> = +100mA		4	6	Ω
I <sub>Leak</sub>	Output Leakage Current	V <sub>H</sub> = V <sub>S+</sub> , V <sub>L</sub> = V <sub>S-</sub>		0.1	10	μA
I <sub>PK</sub>	Peak Output Current	Source		2.0		A
		Sink		2.0		A
<b>Power Supply</b>						
I <sub>S</sub>	Power Supply Current	Inputs = V <sub>S+</sub>		0.5	1.5	mA
<b>Switching Characteristics</b>						
t <sub>R</sub>	Rise Time	C <sub>L</sub> = 1000pF		13.5		ns
t <sub>F</sub>	Fall Time	C <sub>L</sub> = 1000pF		13		ns
t <sub>RFdelta</sub>	t <sub>R</sub> , t <sub>F</sub> Mismatch	C <sub>L</sub> = 1000pF		0.5		ns
t <sub>D-1</sub>	Turn-Off Delay Time	C <sub>L</sub> = 1000pF		12.5		ns
t <sub>D-2</sub>	Turn-On Delay Time	C <sub>L</sub> = 1000pF		14.5		ns
t <sub>Ddelta</sub>	t <sub>D-1</sub> - T <sub>D-2</sub> Mismatch	C <sub>L</sub> = 1000pF		2		ns
T <sub>enable</sub>	Enable Delay Time			12		ns
T <sub>disable</sub>	Disable Delay Time			12		ns

# EL7457C

## 40MHz Non-Inverting Quad CMOS Driver

EL7457C

### Electrical Characteristics

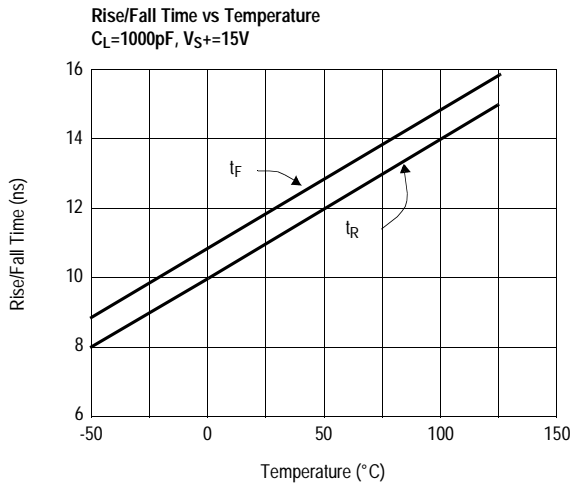
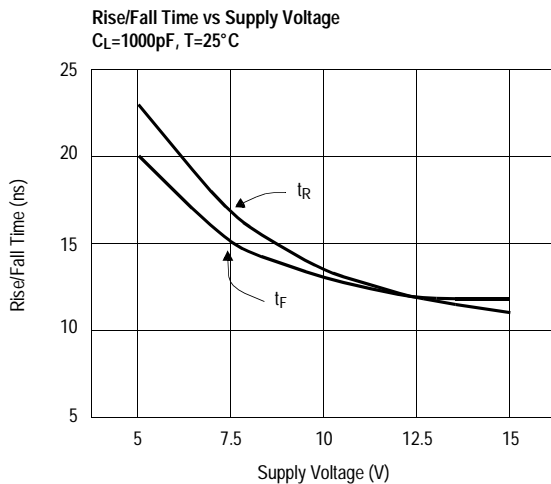
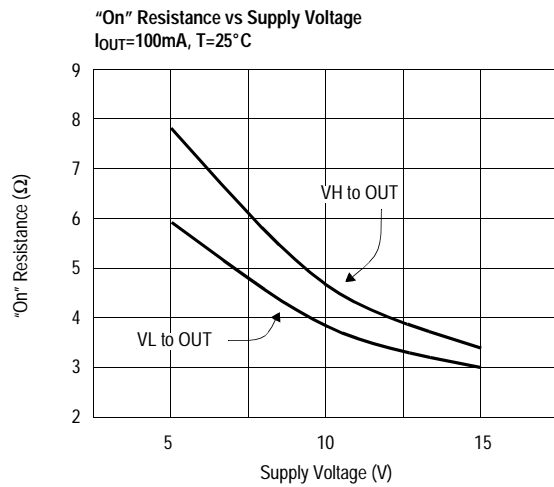
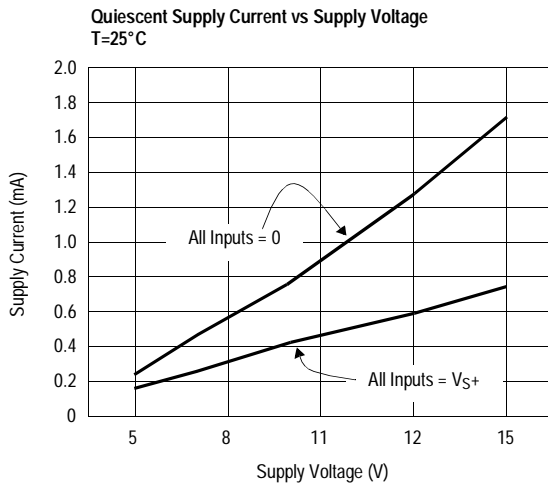
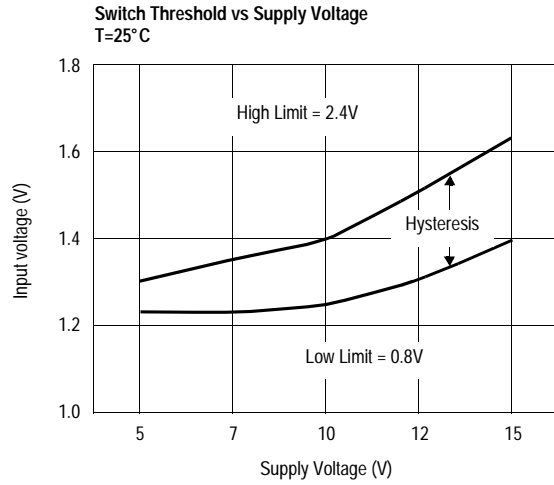
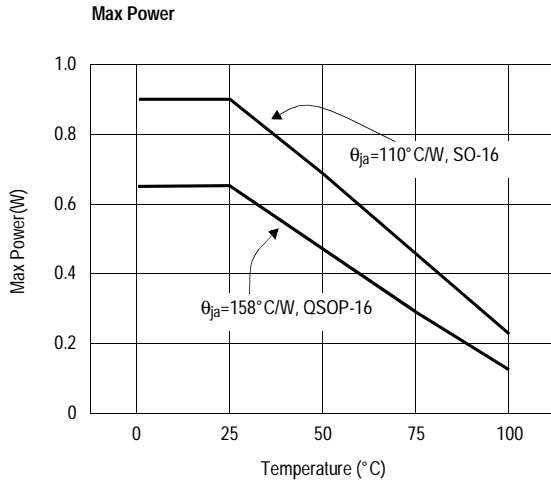
$V_{S+} = +15V$ ,  $V_{S-} = 0V$ ,  $V_H = +15V$ ,  $V_L = 0V$ ,  $T_A = 25^\circ C$ , unless otherwise specified

Parameter	Description	Condition	Min	Typ	Max	Units
<b>Input</b>						
$V_{IH}$	Logic "1" Input Voltage		2.4			V
$I_{IH}$	Logic "1" Input Current	$V_{IH} = 5V$		0.1	10	$\mu A$
$V_{IL}$	Logic "0" Input Voltage				0.8	V
$I_{IL}$	Logic "0" Input Current	$V_{IL} = 0V$		0.1	10	$\mu A$
$C_{in}$	Input Capacitance			3.5		pF
$R_{in}$	Input Resistance			50		M $\Omega$
<b>Output</b>						
$R_{OV1}$	ON Resistance $V_H$ to OUT	$I_{OUT} = -100mA$		3.5	5	$\Omega$
$R_{OV2}$	ON Resistance $V_L$ to OUT	$I_{OUT} = +100mA$		3	5	$\Omega$
$I_{leak}$	Output Leakage Current	$V_H = V_{S+}$ , $V_L = V_{S-}$		0.1	10	$\mu A$
$I_{PK}$	Peak Output Current	Source		2.0		A
		Sink		2.0		A
<b>Power Supply</b>						
$I_S$	Power Supply Current	Inputs = $V_{S+}$		0.8	2	mA
<b>Switching Characteristics</b>						
$t_R$	Rise Time	$C_L = 1000pF$		11		ns
$t_F$	Fall Time	$C_L = 1000pF$		12		ns
$t_{RF\Delta}$	$t_R$ , $t_F$ Mismatch	$C_L = 1000pF$		1		ns
$t_{D-1}$	Turn-Off Delay Time	$C_L = 1000pF$		11.5		ns
$t_{D-2}$	Turn-On Delay Time	$C_L = 1000pF$		13		ns
$t_{D\Delta}$	$t_{D-1} - t_{D-2}$ Mismatch	$C_L = 1000pF$		1.5		ns
$T_{enable}$	Enable Delay Time			12		ns
$T_{disable}$	Disable Delay Time			12		ns

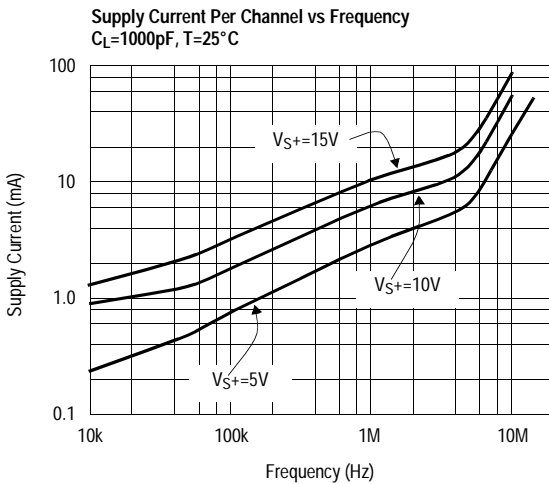
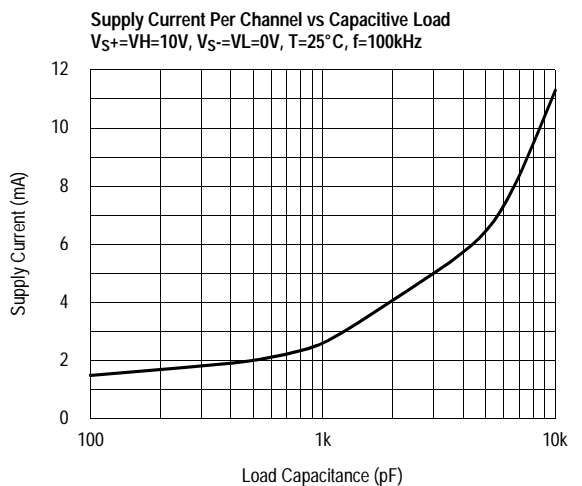
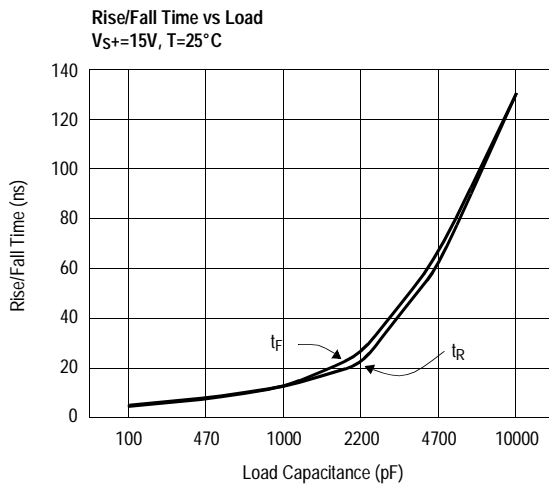
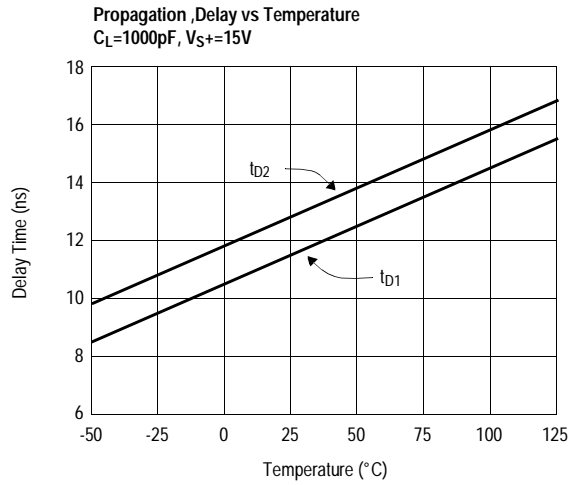
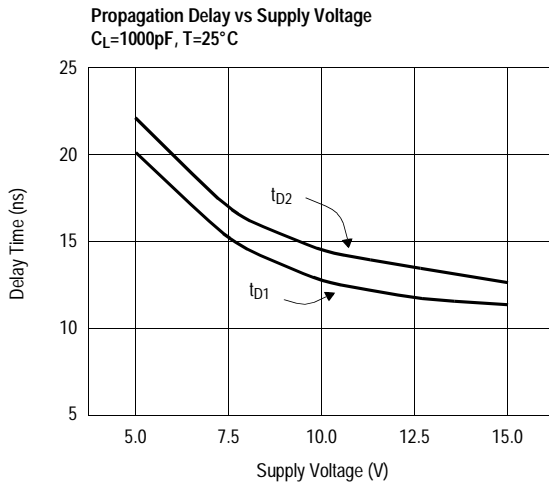
# EL7457C

## 40MHz Non-Inverting Quad CMOS Driver

### Typical Performance Curves



### Typical Performance Curves (cont.)



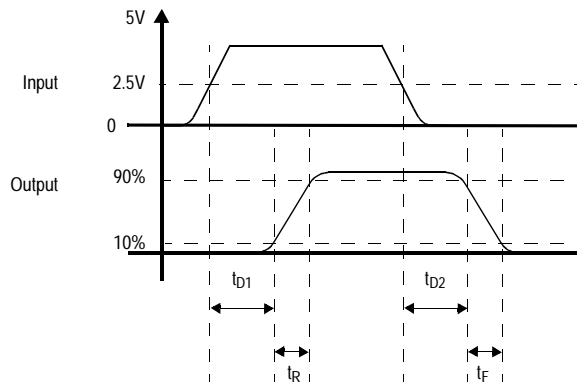
# EL7457C

## 40MHz Non-Inverting Quad CMOS Driver

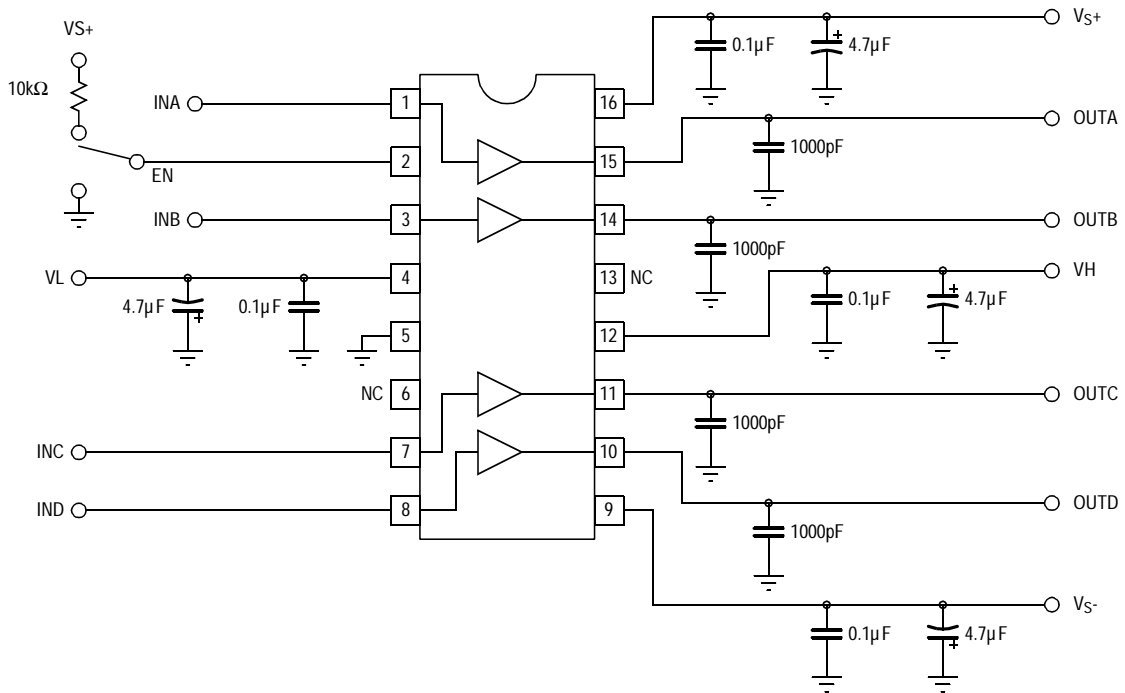
### Nominal Operating Voltage Range

PIN	MIN	MAX
$V_{S+}$ to $V_{S-}$	5V	15V
$V_{S-}$ to GND	-5V	0V
VH	$V_{S-} + 2.5V$	$V_{S+}$
VL	$V_{S-}$	$V_{S+}$
VH to VL	0V	15V
VL to $V_{S-}$	0V	8V

### Timing Diagrams



### Standard Test Configuration

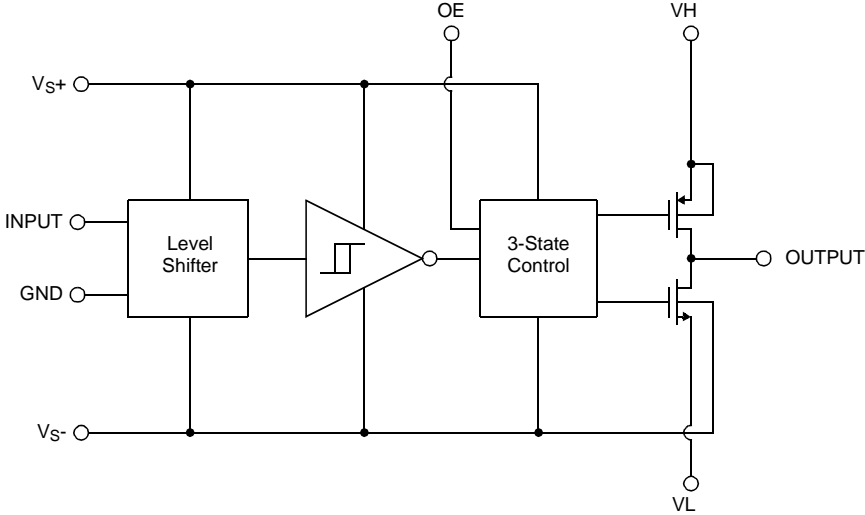


**EL7457C****40MHz Non-Inverting Quad CMOS Driver****Pin Description**

Pin	Name	Function	Equivalent Circuit
1	INA	Input Channel A	<p>Circuit 1</p>
2	OE	Output Enable	(Reference Circuit 1)
3	INB	Input Channel B	(Reference Circuit 1)
4	VL	Low Voltage Input Pin	
5	GND	Input Logic Ground	
6	NC	No Connection	
7	INC	Input Channel C	(Reference Circuit 1)
8	IND	Input Channel D	(Reference Circuit 1)
9	V <sub>S-</sub>	Negative Supply Voltage	
10	OUTD	Output Channel D	<p>Circuit 2</p>
11	OUTC	Output Channel C	(Reference Circuit 2)
12	V <sub>H</sub>	High Voltage Input Pin	
13	NC	No Connection	
14	OUTB	Output Channel B	(Reference Circuit 2)
15	OUTA	Output Channel A	(Reference Circuit 2)
16	V <sub>S+</sub>	Positive Supply Voltage	



**Block Diagram**



# EL7457C

## 40MHz Non-Inverting Quad CMOS Driver

### Application Information:

#### Product Description

The EL7457C is a high performance 40MHz ultra-high speed quad driver. Each channel of the EL7457C consists of a single P-channel high side driver and a single N-channel low side driver. These 3Ω devices will pull the output (OUT<sub>X</sub>) to either the high or low voltage, on VH and VL respectively, depending on the input logic signal (IN<sub>X</sub>). It should be noted that there is only one set of high and low voltage pins.

A common output enable (OE) pin is available on the EL7457C. This pin, when pulled low will put all outputs in to the high impedance state.

The EL7457C is available in both the 16-pin SOIC and the space saving 16-pin QSOP packages. The relevant package should be chosen depending on the calculated power dissipation.

#### Supply Voltage Range and Input Compatibility

The EL7457C is designed for operation on supplies from 5V to 15V with 10% tolerance (i.e. 4.5V to 16.5V). The table on page 6 shows the specifications for the relationship between the V<sub>S+</sub>, V<sub>S-</sub>, VH, VL and GND pins. The EL7457C does not contain a true analog switch and therefore VL should always be less than VH.

All input pins are compatible with both 3V and 5V CMOS signals. With a positive supply (V<sub>S+</sub>) of 5V, the EL7457C is also compatible with TTL inputs.

#### Power Supply Bypassing

When using the EL7457C, it is very important to use adequate power supply bypassing. The high switching currents developed by the EL7457C necessitate the use of a bypass capacitor on both the positive and negative supplies. It is recommended that a 4.7μF tantalum capacitor be used in parallel with a 0.1μF low-inductance ceramic MLC capacitor. These should be placed as close to the supply pins as possible. It is also recommended that the VH and VL pins have some level of bypassing, especially if the EL7457C is driving highly capacitive loads.

#### Power Dissipation Calculation

When switching at high speeds, or driving heavy loads, the EL7457C drive capability is limited by the rise in die temperature brought about by internal power dissipation. For reliable operation die temperature must be kept below T<sub>jmax</sub> (125°C). It is necessary to calculate the power dissipation for a given application prior to selecting the package type.

Power dissipation may be calculated:

$$PD = (V_S \times I_S) + \sum_1^4 (C_{INT} \times V_S^2 \times f) + (C_L \times V_{OUT}^2 \times f)$$

where:

- V<sub>S</sub> is the total power supply to the EL7457C (from V<sub>S+</sub> to V<sub>S-</sub>),
- V<sub>out</sub> is the swing on the output (VH - VL),
- C<sub>L</sub> is the load capacitance,
- C<sub>INT</sub> is the internal load capacitance (50pF max.),
- I<sub>S</sub> is the quiescent supply current (3mA max.) and
- f is frequency

Having obtained the application's power dissipation, a maximum package thermal coefficient may be determined, to maintain the internal die temperature below T<sub>jmax</sub>.

$$\theta_{ja} = \frac{(T_{jmax} - T_{max})}{PD}$$

where:

- T<sub>jmax</sub> is the maximum junction temperature (125°C),
- T<sub>max</sub> is the maximum operating temperature,
- PD is the power dissipation calculated above.

Using the value of θ<sub>ja</sub>, a suitable package for the application may be selected.

In applications with a θ<sub>ja</sub> greater than 158°C/W, a 16-pin QSOP may be used. A 16-pin SOIC is suitable for applications with a θ<sub>ja</sub> value greater than 110°C/W. However,

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EL7457C

if the calculated value of  $\theta_{ja}$  is less than  $110^{\circ}\text{C}/\text{W}$ , the application must be derated to prevent premature failure of the device, either by reducing the switching fre-

quency, the capacitive load or the maximum operating temperature.

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40MHz Non-Inverting Quad CMOS Driver

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# **élantec**

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