LX1660/1661

ADVANCED PWM CONTROLLER

PRODUCTION DATA SHEET

LINFINITY MICROELECTRONICS

THE INFINITE POWER OF INNOVATION

DESCRIPTION

The LX1660 and LX1661 Are Monolithic Switching Regulator Controller ICs designed to provide low-cost, high-performance adjustable power supply for microprocessors and other applications requiring a fast transient response and a high degree of accuracy. They provide an adjustable synchronous Pulse Width Modulator output suitable for a power supply for Pentium® or other microprocessors.

Synchronous Rectifier Driver For CPU Core. The devices can drive dual MOSFETs resulting in typical efficiencies of 85 - 90%, even with loads in excess of 10A. Synchronous shutdown results in increased efficiency in light load applications.

Short-Circuit Current Limiting Without Expensive Current Sense Resistors. The current sensing mechanism can use a PCB trace resistance or the parasitic resistance of the main inductor. For applications requiring a high degree of accuracy, a conventional sense resistor can be used.

Hiccup Mode Fault Protection. The hiccup mode is programmable and with pulse-by-pulse current limiting will help protect the power supply system and load in the even of a short circuit.

Ultra-Fast Transient Response Reduces System Cost. The fixed frequency modulated off-time architecture results in the fastest transient response for a given inductor. Adaptive voltage positioning (LX1661 only) requires fewer low-ESR capacitors to meet stringent transient over- and under-shoot specifications.

KEY FEATURES

- Designed To Drive A Synchronous Rectifier Stage — Can Also Be Used In Non-Synchronous Applications
- Soft-Start Capability
- Hiccup-Mode Fault Protection
- No Current-Sense Resistor Required For Current Limiting
- Modulated Constant Off-Time Control Mechanism For Fast Transient Response And Simple System Design
- 2V, 0.5% Internal Voltage Reference Brought Out

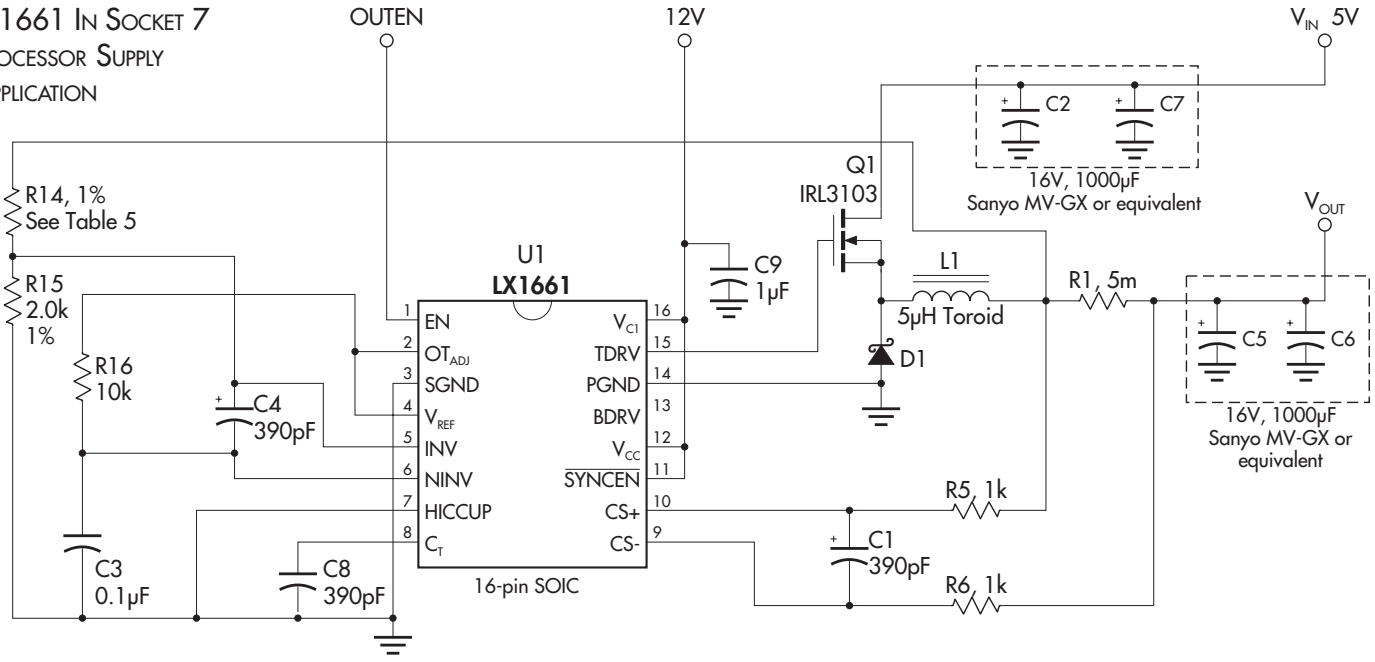
APPLICATIONS

- Pentium Processor Supplies
- AMD-K6™ Supplies
- Cyrix® 6x86™ Supplies
- Voltage Regulator Modules
- General Purpose DC:DC Supplies

IMPORTANT: For the most current data, consult LinFinity's web site: **http://www.linfinity.com.**

PRODUCT HIGHLIGHT

LX1661 IN SOCKET 7 PROCESSOR SUPPLY APPLICATION



PACKAGE ORDER INFORMATION

T_A (°C)	N Plastic DIP 16-pin	D Plastic SOIC 16-pin
0 to 70	LX166xCN	LX166xCD

Note: All surface-mount packages are available in Tape & Reel. Append the letter "T" to part number. (i.e. LX166xCDT)

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ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage 25V
Output Peak Current Source (500ns) 1.5A
Output Peak Current Sink (500ns) 1.5A
Analog Inputs ..... -0.3 to +6V
Power Dissipation at T_A = 25°C
  N Package 1.5W
  D Package 830mW
Operating Junction Temperature
  Plastic (N, D Packages) ..... 150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal. Pin numbers refer to DIL packages only.

THERMAL DATA

N PACKAGE:

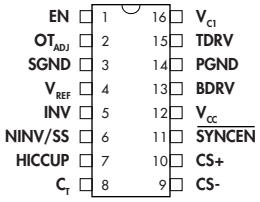
THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	65°C/W

D PACKAGE:

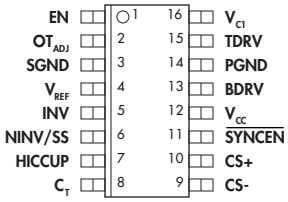
THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	120°C/W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system.
All of the above assume no ambient airflow

PACKAGE PIN OUTS



N PACKAGE
(Top View)



D PACKAGE
(Top View)

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, 10.8 < V_{CC} < 13.2, 0°C ≤ T_A ≤ 85°C. Test conditions: V_{CC} = 12V, T = 25°C.)

Parameter	Symbol	Test Conditions	LX1660			LX1661			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Reference Section									
Initial Output Voltage		V_{CC} = 12V, I_L = 100µA	1.98	2	2.02	1.98	2	2.02	V
Load Regulation		V_{CC} = 12V, I_L = 10µA to 5mA		2			2		mV
Short Circuit Current I_{SH}		V_{REF} = 1.96V		24			24		mA
Timing Section									
Off Time Initial	OT	OT_{ADJ} = 1.8V, C_T = 390pF		2			2		µS
		OT_{ADJ} = 3.5V, C_T = 390pF		1			1		µS
Off Time Temp Stability		OT_{ADJ} = 1.8V to 3.5V		2			2		%
Discharging Current	I_{DIS}	V_{NINV} = 1.8V, V_{CT} = 1.5V	180	210	240	180	210	240	µA
		V_{NINV} = 3.5V, V_{CT} = 1.75V	180	210	240	180	210	240	µA
Ramp Peak	V_P			2			2		V
Ramp Peak-Valley	V_{RPP}	OT_{ADJ} = 1.8V	0.8	0.9	1.0	0.8	0.9	1.0	V
		OT_{ADJ} = 3.5V	0.475	0.5	0.525	0.475	0.5	0.525	V
Ramp Valley Delay to Output		10% Overdrive		100			100		nS
Turn Off Threshold	V_{OFF}	(Voltage at OT_{ADJ} Pin)	0.6	0.9	1.2	0.6	0.9	1.2	V
Error Comparator Section									
Input Bias Current	I_B	V_{FB} = V_{SET}		0.1	1.0		0.1	1.0	µA
Input Offset Voltage	V_{IO}			2		36	42	48	mV
E_C Delay to Output		10% Overdrive		150			150		nS
Synchronous Control Section									
Synchronous Enable Threshold	S_{YCEN}		0.5	0.7	0.9	0.5	0.7	0.9	V
Current Sense Section									
Input Bias Current	I_B	1.8V < V_{CS}+ = V_{CS} < 3.5V		0.1	1		0.1	1	µA
Pulse By Pulse C_L	V_{CLP}	Initial Accuracy	80	90	100	80	90	100	mV
C_S Delay to Output		10% Overdrive		150			150		nS
Output Drivers Section									
Output Rise Time	T_R	V_{CL} = V_{C2} = 12V, C_L = 3000pF		70			70		nSec
Output Fall Time	T_F	V_{CL} = V_{C2} = 12V, C_L = 3000pF		70			70		nSec
Output Pull Down	V_{PD}	V_{CC} = V_C = 0, $I_{PULL\ UP}$ = 2mA		1			1		V
Peak Current	I_{PK}	t_{PULSE} = 500ns			1.0			1.0	A
UVLO and S.S. Section									
Start-Up Threshold	V_{ST}		9.85	10.15	10.45	9.85	10.15	10.45	V
Hysteresis	V_{HYST}			0.31			0.31		V
S.S. Sink Current	I_{SD}	V_{CL} = 10.1V	2	3		2	3		mA
S.S. Sat Voltage	V_{OL}	V_{CL} = 9V, I_{SD} = 20µA		0.2	0.6		0.2	0.6	V
Enable Shutdown Threshold	V_{EN}		1.3	1.4	1.5	1.3	1.4	1.5	V
Enable Bias Current	I_{EN}	I_{EN} (Low), V_{EN} = 0V		-0.5	-1		-0.5	-1	µA
		I_{EN} (High), V_{EN} = 2V		0.5	1		0.5	1	µA
Enable Hysteresis			0.14	0.16	0.18	0.14	0.16	0.18	V
Supply Current Section									
Dynamic Operating Current	I_{CD}	V_{CC} = V_C = 12V, Out Freq = 200kHz, C_L = 0			25			25	mA
Start-Up Current	I_{ST}	V_{CL} = 10V		500	1000		500	1000	µA
Hiccup Section									
Hiccup Factor "ON" Time		(C_{HICCUP} = 0.1µF typ.)		100			100		mS/µF
Hiccup Duty Cycle				10			10		%

BLOCK DIAGRAM

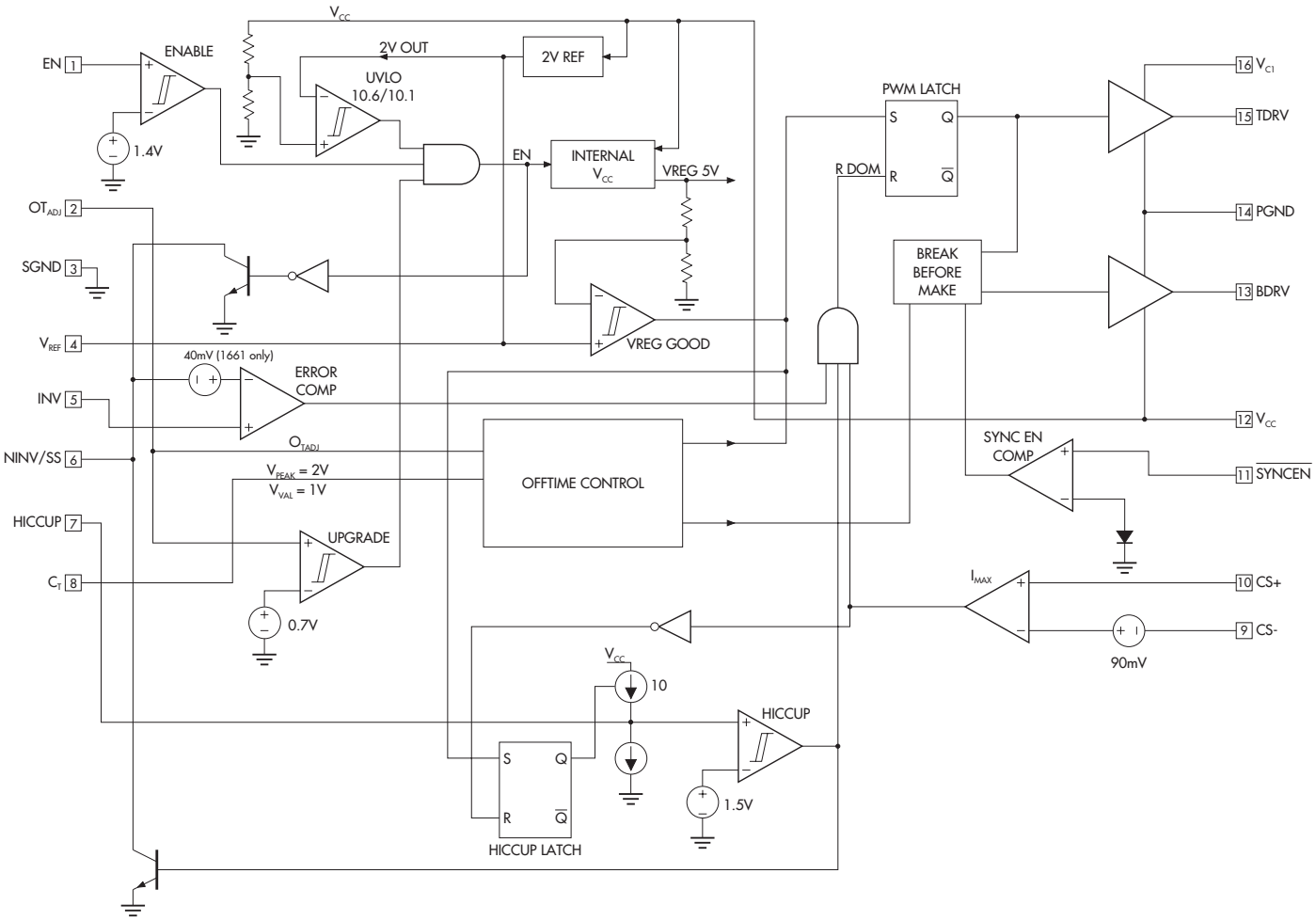


FIGURE 1 — Block Diagram

FUNCTIONAL PIN DESCRIPTION

Pin	#	Description
EN	1	A low voltage at this pin puts the IC in sleep-mode.
OT_{ADJ}	2	The purpose of this pin is to allow modulation of the OFF-time relative to the reference voltage. The OFF-time is inversely proportional to the reference voltage. The inverting input of the upgrade voltage comparator is also connected to this pin, when the voltage at this pin is below 0.7V, the controller shuts down.
SGND	3	This pin is the signal ground of the IC.
V_{REF}	4	2V reference.
INV	5	This pin is the inverting input of the error comparator.
NINV/SS	6	This pin is the non-inverting input of the error comparator (LX1661 only: 40mV offset between this pin and error comparator). This pin is pulled low during sleep-mode to allow soft-start function during start up.
HICCUP	7	A hiccup-mode capacitor connected to this pin adjusts duty cycle.
C_T	8	The OFF-time is programmed by connecting a capacitor from this pin to ground.
CS-	9	This is the inverting input of the pulse-by-pulse current comparator.
CS+	10	This is the non-inverting input of the pulse-by-pulse current comparator.
$\overline{\text{SYNCEN}}$	11	This pin enables the synchronous (bottom) driver. A high voltage at this pin disables the synchronous driver.
V_{CC}	12	This is the IC supply voltage as well as the supply to the bottom MOSFET.
BDRV	13	This is the gate drive to the bottom MOSFET
PGND	14	This is a separate ground for the top and bottom MOSFET.
TDRV	15	This is the gate drive to the top MOSFET.
V_{C1}	16	This pin is a separate power supply input for the top drive.

THEORY OF OPERATION

IC OPERATION

Referring to the block diagram and typical application circuit, the output turns ON the top MOSFET, allowing the inductor current to increase. At the error comparator threshold, the PWM latch is reset, the top MOSFET turns OFF and the synchronous MOSFET turns ON. The OFF-time capacitor C_T is now allowed to discharge. At the valley voltage, the synchronous MOSFET turns OFF and the top MOSFET turns on. A special break-before-make circuit prevents simultaneous conduction of the two MOSFETs.

To minimize frequency variation with varying output voltage, the OFF-time is modulated as a function of the voltage at the OT_{ADJ} pin. The OT_{ADJ} pin is also being monitored for a minimum voltage of 0.7V. Below 0.7V the controller will shut down. A low voltage at the EN pin or the OT_{ADJ} pin will put the controller in a sleep mode. During the sleep mode the NINV pin is pulled low. This discharges the external bypass capacitor on this pin and allows for a soft-start.

Regulation

LX1660 Only: The INV pin is connected to the negative side of the sense resistor (i.e. the actual voltage supplied to the load) — See Figure 2. The LX1660 will achieve a high DC set-point accuracy, since it regulates at the load, but it will have greater transient voltage over- and under-shoots than the LX1661.

LX1661 Only: The INV pin is connected to the positive side of the sense resistor (between the inductor and the sense resistor) — See Figure 2. The LX1661 has a 40mV offset to the NINV pin to enhance transient response, as shown in Figure 3 below.

- The peak voltage at the V_{FB} pin is 40mV higher than the set voltage and its average is the peak voltage minus the ripple voltage at V_{FB} pin.
- The output voltage is the voltage at the V_{FB} pin minus the voltage drop across the current sensing resistor ($I * R_{SENSE}$).
- At light loads, the voltage drop across the sensing resistor is small; hence, the output voltage is approximately the voltage at the V_{FB} pin (approximately 40mV higher than the nominal set-point voltage, V_{SET}).
- At heavy loads, larger current flows in the sense resistor, therefore, the voltage drop is higher and the output voltage is lower.

This adaptive positioning of the output voltage as the load changes allows a greater output voltage excursion during a fast step-load transient and requires fewer output capacitors to meet the transient-response specification.

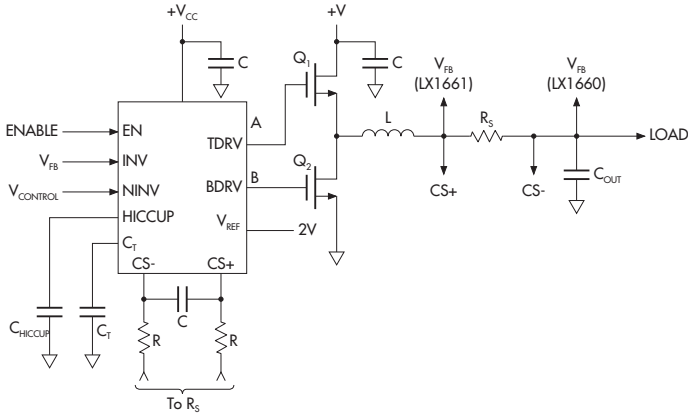


Figure 2 — LX1660 / 1661 General Circuit Configuration

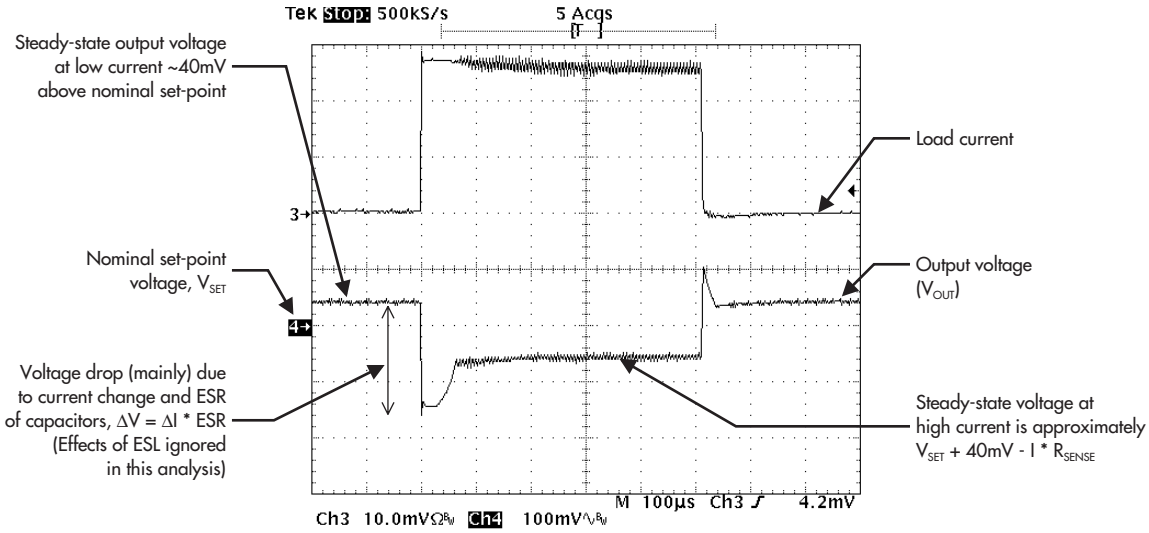


Figure 3 — Adaptive Voltage Positioning

THEORY OF OPERATION (continued)

ERROR VOLTAGE COMPARATOR

The error voltage comparator compares the feedback voltage at the positive side of the sense resistor to the set voltage (set voltage plus 40mV in LX1661). An external filter is recommended for high-frequency noise.

CURRENT LIMIT AND HICCUP SECTIONS

Current limiting is performed by sensing the inductor current across the sense resistor. Exceeding this threshold turns the output drive OFF and latches it OFF until the PWM latch set input goes high again. To reduce stress on the external MOSFET and SCR during output shorts or heavy-load conditions, a hiccup circuit is incorporated, which provides 10% duty cycle. The hiccup time is programmed via a capacitor at the HICCUP pin. A low voltage at this pin disables the hiccup function.

OFF TIME CONTROL TIMING SECTION

The timing capacitor C_T allows programming of the OFF-time. The timing capacitor is quickly charged during the ON time of the top MOSFET and allowed to discharge when the top MOSFET is OFF.

OFF TIME CONTROL TIMING SECTION (continued)

In order to minimize frequency variations while providing different supply voltages, the discharge current is modulated by the voltage at the OT_{ADJ} pin. The OFF-time is inversely proportional to the OT_{ADJ} voltage. If the OT_{ADJ} voltage drops below 0.7V, the IC shuts down into a low quiescent current mode.

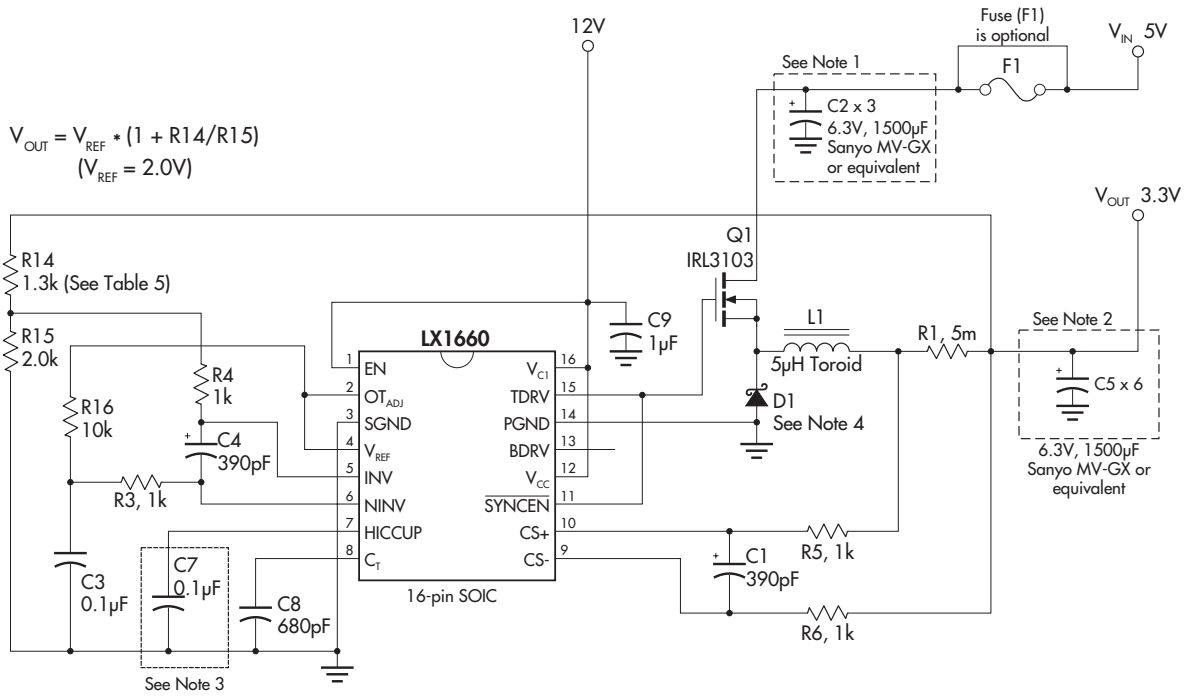
UNDER VOLTAGE LOCKOUT AND SHUTDOWN SECTION

The purpose of the UVLO is to keep the output drive off and to maintain low quiescent current until the input voltage reaches the start-up threshold. At voltages below the start-up voltage, the UVLO comparator disables the internal biasing, and turns off the output drives. The NINV pin is pulled low.

SYNCHRONOUS CONTROL SECTION

The synchronous control section incorporates a unique break-before-make function to ensure that the primary switch and the synchronous switch are not turned on at the same time. Approximately 100 nanoseconds of deadtime is provided by the break-before-make circuitry to protect the MOSFET switches.

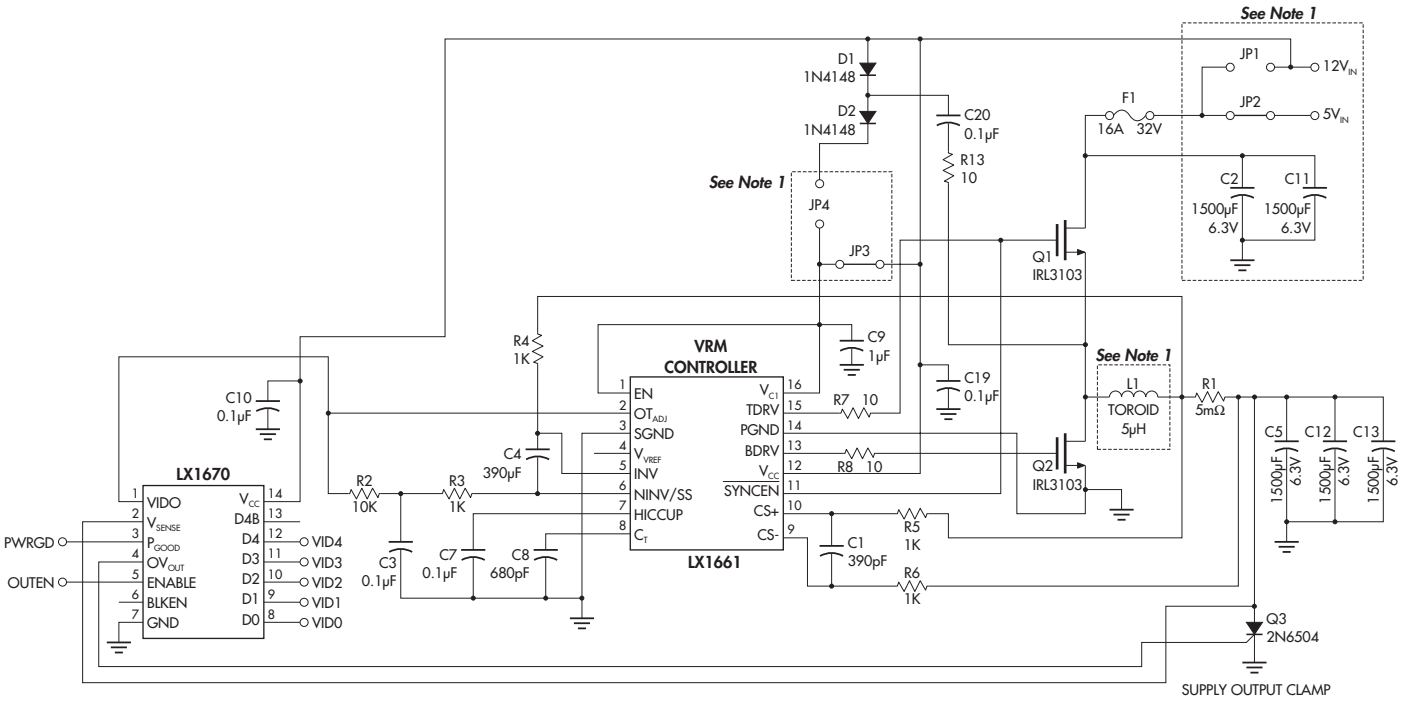
APPLICATION INFORMATION



Notes
1. The number of capacitors within this bank may be reduced for cost savings at a penalty of increased ripple on the input bus.
2. The number of capacitors in the output filter bank may be reduced by two in a typical application; more may be removed for systems with lesser transient requirements.
3. If pulse-by-pulse current limiting is desired, remove C7 and short LX1660 pin 7 to ground.
4. D1 is Motorola MBR1035 for 10A capability; downsize as per required current.

Figure 4 — LX1660 Controller Used In A Typical Stand-Alone High-Current 5V To 3.3V Regulator Application

APPLICATION INFORMATION



Note 1. Setup shown is for 5V application. For 12V input change the following:
- **Close** JP1 and JP4
- **Open** JP2 and JP3
- For C2 and C11, use 16V/850µF capacitors instead
- Inductor L1 = 10µH

Figure 5 — Full Featured Voltage Regulator Using LX1661 Controller And LX1670 Programmable Reference / DAC Chip For Pentium Pro Processor Or Pentium II Processor Applications

APPLICATION INFORMATION

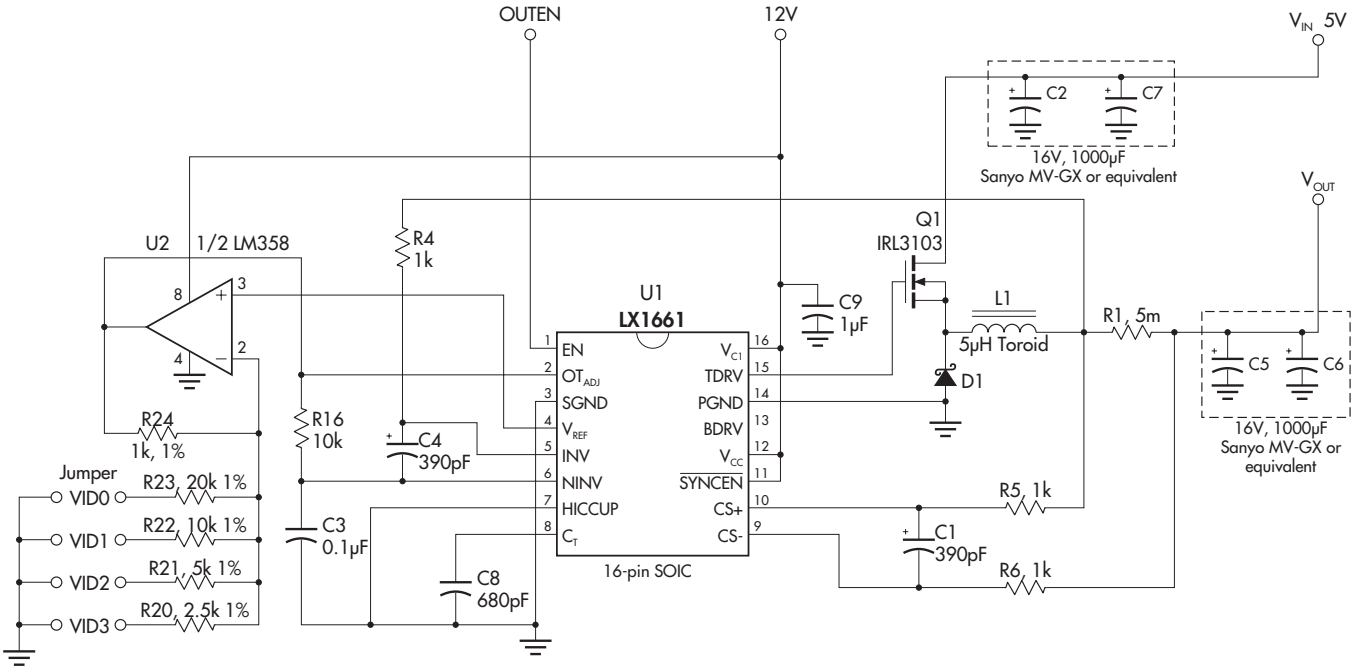


Figure 6 — Low Cost Programmable Power Supply For Socket 7 Processors

TABLE 1 - Voltage Identification Code (VID)

VID3	VID2	VID1	VID0	Output Voltage
1	1	1	1	2.0V
1	1	1	0	2.1V
1	1	0	1	2.2V
1	1	0	0	2.3V
1	0	1	1	2.4V
1	0	1	0	2.5V
1	0	0	1	2.6V
1	0	0	0	2.7V
0	1	1	1	2.8V
0	1	1	0	2.9V
0	1	0	1	3.0V
0	1	0	0	3.1V
0	0	1	1	3.2V
0	0	1	0	3.3V
0	0	0	1	3.4V
0	0	0	0	3.5V

Note: Costs are estimates only. Check with suppliers for exact quotation.

Setting The Output Voltage

The output voltage is set by means of a 4-bit digital VID code. For processors that do not have VID coded into the package, the VID code can be set by means of a jumper or DIP switch. For low or '0' signal, connect the VID pin to ground (DIP switch ON). For high or '1', leave open (DIP switch OFF).

USING THE LX1660/61 DEVICES

The LX1660/61 devices are very easy to design with, requiring only a few simple calculations to implement a given design. The following procedures and considerations should provide effective operation for virtually all applications. Refer to the **Application Information** section for component reference designators.

SELECTING BETWEEN THE LX1660 AND THE LX1661

In order to provide maximum user versatility, the Advanced PWM Controller is offered in two versions: the LX1660 and the LX1661.

The LX1661 has a 40mV offset built-in which compensates for the current sense resistor voltage drop. This allows optimal transient response for high-speed systems, such as Pentium Pro processor power supplies. Overall system design could be more economical with the LX1661, since output capacitance requirements could be eased.

The LX1660 provides a very accurate DC set-point, since the 40mV offset is not included in the device. This device is good for critical DC applications, such as core power in slower microprocessors and related systems.

See "Theory Of Operation" section earlier in this data sheet.

OUTPUT INDUCTOR

The output inductor should be selected to meet the requirements of the output voltage ripple in steady-state operation and the inductor current slew-rate during transient.

The peak-to-peak output voltage ripple is:

$$V_{RIPPLE} = ESR * I_{RIPPLE}$$

where,

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{f_{SW} * L} * \frac{V_{OUT}}{V_{IN}}$$

I_{RIPPLE} is the inductor ripple current, L is the output inductor value and ESR is the Effective Series Resistance of the output capacitor.

I_{RIPPLE} should typically be in the range of 20% to 40% of the maximum output current. Higher inductance results in lower output voltage ripple, allowing slightly higher ESR to satisfy the transient specification. Higher inductance also slows the inductor current slew rate in response to the load-current step change, ΔI, resulting in more output-capacitor voltage droop. The inductor-current slew rates at rise and fall edges are:

$$T_{RISE} = L * \Delta I / (V_{IN} - V_{OUT})$$

and,

$$T_{FALL} = L * \Delta I / V_{OUT}$$

When using electrolytic capacitors, the capacitor voltage droop is usually negligible, due to the large capacitance.

INPUT INDUCTOR

In order to supply faster transient load changes, a smaller output inductor is needed. However, reducing the size of the output inductor will result in a higher ripple voltage on the input supply. This noise on the 5V rail can affect other system components, such as graphic cards. In this case, it is recommended that a 1 - 1.5µH inductor is used on the input to the regulator, to filter the ripple on the 5V supply. Ensure that this inductor has the same current rating as the output inductor.

OUTPUT CAPACITOR

The output capacitor is sized to meet ripple and transient performance specifications. Effective Series Resistance (ESR) is a critical parameter. When a step load current occurs, the output voltage will have a step that equals the product of the ESR and the current step, ΔI. In an advance microprocessor power supply, the output capacitor is usually selected for ESR instead of capacitance or RMS current capability. A capacitor that satisfies the ESR requirement usually has a larger capacitance and current capability than strictly needed. The allowed ESR can be found by:

$$ESR * (I_{RIPPLE} + \Delta I) < V_{EX}$$

where I_{RIPPLE} is the inductor ripple current, ΔI is the maximum load current step change, and V_{EX} is the allowed output voltage excursion in the transient. Adaptive voltage positioning increases the value of V_{EX}, allowing a higher ESR value and reducing the cost of the output capacitor.

Typically, the positioning voltage is 40mV, using the LX1661, and the transient tolerance is 100mV, resulting in a V_{EX} of 140mV (See Figure 3). The LX1660 does not have the positioning voltage offset, so V_{EX} is 100mV maximum.

Electrolytic capacitors can be used for the output capacitor, but are less stable with age than tantalum capacitors. As they age, their ESR degrades, reducing the system performance and increasing the risk of failure. It is recommended that multiple parallel capacitors be used, so that, as ESR increases with age, overall performance will still meet the processor's requirements.

There is frequently strong pressure to use the least expensive components possible, however, this could lead to degraded long-term reliability, especially in the case of filter capacitors. Linfinity's demonstration boards use Sanyo MV-GX filter capacitors, which are aluminum electrolytic, and have demonstrated reliability. The Oscon series from Sanyo generally provides the very best performance in terms of long term ESR stability and general reliability, but at a substantial cost penalty. The MV-GX series provides excellent ESR performance at a reasonable cost. Beware of off-brand, very low-cost filter capacitors, which have been shown to degrade in both ESR and general electrolytic characteristics over time.

USING THE LX1660/61 DEVICES

INPUT CAPACITOR

The input capacitor and the input inductor are to filter the pulsating current generated by the buck converter to reduce interference to other circuits connected to the same 5V rail. In addition, the input capacitor provides local de-coupling of the buck converter. The capacitor should be rated to handle the RMS current requirement. The RMS current is:

$$I_{RMS} = I_L \sqrt{d(1-d)}$$

where I_L is the inductor current and d is the duty cycle. The maximum value, when d = 50%, $I_{RMS} = 0.5I_L$. For 5V input and output in the range of 2 to 3V, the required RMS current is very close to $0.5I_L$.

A high-frequency (ceramic) capacitor should be placed across the drain of the top MOSFET and the source of the bottom one to avoid ringing due to the parasitic inductor being switched ON and OFF. See capacitor C_7 in the Product Highlight on the first page of this data sheet.

TIMING CAPACITOR SELECTION

The frequency of operation of the LX1660 / 1661 is a function of the duty cycle and OFF-time. The OFF-time is proportional to the timing capacitor (connected to Pin 8, C_T), and is modulated to minimize frequency variations with duty cycle. The frequency is constant, during steady-state operation, due to the modulation of the OFF-time.

The timing capacitor (C_T) should be selected using the following equation:

$$C_T = \frac{(1 - V_{OUT} / V_{IN}) * I_{DIS}}{f_S (1.52 - 0.29 * V_{OUT})}$$

where I_{DIS} is fixed at 200µA and f_S is the switching frequency (recommended to be around 200kHz for optimal operation and component selection).

When using a 5V input voltage, the switching frequency (f_S) can be approximated as follows:

$$C_T = 0.621 * \frac{I_{DIS}}{f_S}$$

Choosing a 680pF timing capacitor will result in an operating frequency of 183kHz at V_{OUT} = 2.8V. When a 12V power input is used, the capacitor value must be changed (the optimal timing capacitor for 12V input will be in the range of 1000 - 1500pF).

CURRENT LIMIT

Current limiting occurs when a sensed voltage, proportional to load current, exceeds the current-sense comparator threshold value (90mV). The current can be sensed either by using a fixed sense resistor in series with the inductor to cause a voltage drop proportional to current, or by using a resistor and capacitor in parallel with the inductor to sense the voltage drop across the

CURRENT LIMIT (continued)

parasitic resistance of the inductor. One should include an RC filter at the CS+ and CS- inputs, as shown in the **Application Information** section, to eliminate jitter and noise.

For most applications, the resistors R5, R6 can be set at 1kΩ, and C1 can be in the 300-500pF range as a starting point. If a fine trim or adjustment of the current trip level is required, C1 may be shunted by a resistor. C1 will introduce a small delay into the current limit trip point, which effectively raises the threshold.

Sense Resistor

The current sense resistor (R1) is selected according to the formula:

$$R1 = V_{TRIP} / I_{TRIP}$$

Where V_{TRIP} is the current sense comparator threshold (100mV) and I_{TRIP} is the desired current limit. Typical choices are shown below.

TABLE 2 - Current Sense Resistor Selection Guide

Load	Sense Resistor Value
Pentium-Class Processor (<10A)	5mΩ
Pentium II Class (>10A)	2.5mΩ

A smaller sense resistor will result in lower heat dissipation (I^2R) and also a smaller output voltage droop at higher currents.

There are several alternative types of sense resistor. The surface-mount metal "staple" form of resistor has the advantage of exposure to free air to dissipate heat and its value can be controlled very tightly. Its main drawback, however, is cost. An alternative is to construct the sense resistor using a copper PCB trace. Although the resistance cannot be controlled as tightly, the PCB trace is very low cost.

PCB Sense Resistor

A PCB sense resistor should be constructed as shown in Figure 7. By attaching directly to the large pads for the capacitor and inductor, heat is dissipated efficiently by the larger copper masses. Connect the current sense lines as shown to avoid any errors.

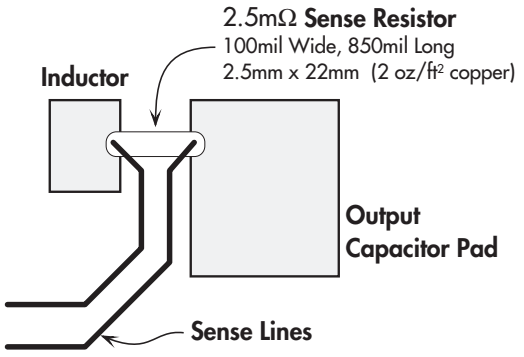


FIGURE 7 — Sense Resistor Construction Diagram

USING THE LX1660/61 DEVICES

CURRENT LIMIT (continued)

Recommended sense resistor sizes are given in the following table:

TABLE 3 - PCB Sense Resistor Selection Guide

Copper Weight	Copper Thickness	Desired Resistor Value	Dimensions (w x l) mm	inches
2 oz/ft²	68µm	2.5mΩ	2.5 x 22	0.1 x 0.85
		5mΩ	2.5 x 43	0.1 x 1.7

Loss-Less Current Sensing Using Resistance of Inductor

Any inductor has a parasitic resistance, R_L, which causes a DC voltage drop when current flows through the inductor. Figure 8 shows a sensor circuit comprising of a surface mount resistor, R_S, and capacitor, C_S, in parallel with the inductor, eliminating the current sense resistor.

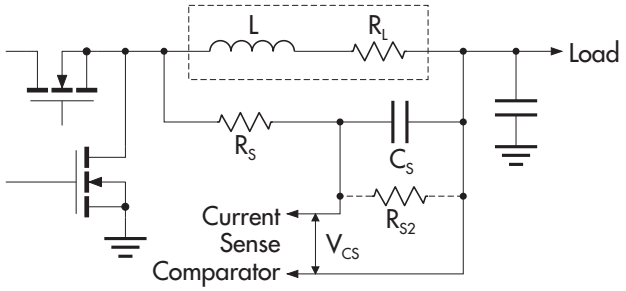


FIGURE 8 — Current Sense Circuit

The current flowing through the inductor is a triangle wave. If the sensor components are selected such that:

$$L/R_L = R_S * C_S$$

The voltage across the capacitor will be equal to the current flowing through the resistor, i.e.

$$V_{CS} = I_L R_L$$

Since V_{CS} reflects the inductor current, by selecting the appropriate R_S and C_S, V_{CS} can be made to reach the comparator voltage at the desired trip current.

Design Example

(Pentium II circuit, with a maximum static current of 14.2A)

The gain of the sensor can be characterized as:

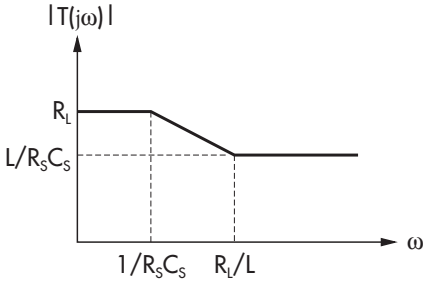


FIGURE 9 — Sensor Gain

CURRENT LIMIT (continued)

The dc/static tripping current $I_{trip,S}$ satisfies:

$$I_{trip,S} = \frac{V_{trip}}{R_L}$$

Select $L/R_S C_S \le R_L$ to have higher dynamic tripping current than the static one. The dynamic tripping current $I_{trip,d}$ satisfies:

$$I_{trip,d} = \frac{V_{trip}}{L/(R_S C_S)}$$

General Guidelines for Selecting R_S, C_S, and R_L

$$R_L = \frac{V_{trip}}{I_{trip,S}} \qquad \text{Select: } R_S \le 10\ \text{k}\Omega$$

and C_S according to: $$C_{S\,n} = \frac{L_n}{R_L R_S}$$

The above equation has taken into account the current-dependency of the inductance. Typical values are: R_L = 3mΩ, R_S = 9kΩ, C_S = 0.1µF, and L is 2.5µH at 0A current.

In cases where R_L is so large that the trip point current would be lower than the desired short-circuit current limit, a resistor (R_{S2}) can be put in parallel with C_S, as shown in Figure 8. The selection of components is as follows:

$$\frac{R_{L\,(Required)}}{R_{L\,(Actual)}} = \frac{R_{S2}}{R_{S2} + R_S}$$

$$C_S = \frac{L}{R_{L\,(Actual)} * (R_{S2} // R_S)} = \frac{L}{R_{L\,(Actual)}} * \frac{R_S + R_{S2}}{R_{S2} * R_S}$$

Again, select (R_{S2}//R_S) < 10kΩ.

C4 ERROR COMPARATOR INPUT BYPASS CAPACITOR

The LX1660/61 device has a unique topology which results in extremely fast response to transient disturbances. Actual loop closure is around a comparator. A capacitor should be placed between the INV and NINV Error Comparator inputs to eliminate jitter and noise. This capacitor value should be: $C = ½\,C_T$, where C_T is the timing capacitor. Refer to Capacitor C4 in the **Application Information** section.

C7 HICCUP CAPACITOR SELECTION

The hiccup capacitor controls two time periods; the ON time duration of 10% duty cycle mode, and the OFF-time duration before re-try. The ON:OFF-time ratios will always be 1:10 due to the current sources which charge (10I) and discharge (I) the hiccup capacitor. Select C_{HICCUP} by using:

Duration of reduced D operation = 100ms/µF

USING THE LX1660/61 DEVICES

C7 HICCUP CAPACITOR SELECTION (continued)

The resulting time is the duration allowed for the 10% duty cycle drive to be applied to the bottom switch (the top switch is OFF during current limit). The OFF-time will be fixed at ten times (10x) this number, and determines the time interval the supply remains completely OFF until re-try. If the short has been removed, the supply will resume normal operation. No power cycling is necessary to reset the VRM module after a current limit event.

As an example, if a 0.1µF hiccup capacitor is chosen, the bottom switch drive will pulse at (approximately) a 10% duty cycle for 10mA, when current limit is reached. It will then shut OFF for 100ms, at which time a re-try cycle is attempted, which will result in either normal operation or another 10% duty cycle burst.

FET SELECTION

To insure reliable operation, the operating junction temperature of the FET switches must be kept below certain limits. The Intel specification states that 115°C maximum junction temperature should be maintained with an ambient of 50°C. This is achieved by properly derating the part, and by adequate heat sinking. One of the most critical parameters for FET selection is the $R_{DS(ON)}$ resistance. This parameter directly contributes to the power dissipation of the FET devices, and thus impacts heat sink design, mechanical layout, and reliability. In general, the larger the current handling capability of the FET, the lower the $R_{DS(ON)}$ will be, since more die area is available.

TABLE 4 - FET Selection Guide

This table gives selection of suitable FETs from International Rectifier.

Device	$R_{DS(ON)}$ @ 10V (mΩ)	I_D @ T_C = 100°C	Max. Break-down Voltage
IRL3803	6	83	30
IRL22203N	7	71	30
IRL3103	14	40	30
IRL3102	13	56	20
IRL3303	26	24	30
IRL2703	40	17	30

All devices in TO-220 package. For surface mount devices (TO-263 / D²-Pak), add 'S' to part number, e.g. IRL3103S.

The recommended solution is to use IRL3102 for the high side and IRL3303 for the low side FET, for the best combination of cost and performance. Alternative FET's from any manufacturer could be used, provided they meet the same criteria for $R_{DS(ON)}$.

Heat Dissipated In Upper MOSFET

The heat dissipated in the top MOSFET will be:

$$P_D = (I^2 * R_{DS(ON)} * Duty\ Cycle) + (0.5 * I * V_{IN} * t_{SW} * f_S)$$

where t_{SW} is switching transition line for body diode (~100ns) and f_S is the switching frequency.

FET SELECTION (continued)

For the IRL3102 (13mΩ $R_{DS(ON)}$), converting 5V to 2.8V at 14A will result in typical heat dissipation of 1.48W.

Synchronous Rectification – Lower MOSFET

The lower pass element can be either a MOSFET or a Schottky diode. The use of a MOSFET (synchronous rectification) will result in higher efficiency, but at higher cost than using a Schottky diode (non-synchronous).

Power dissipated in the bottom MOSFET will be:

$$P_D = I^2 * R_{DS(ON)} * [1 - Duty\ Cycle] = 2.24W$$

[IRL3303 or 1.12W for the IRL3102]

Non-Synchronous Operation - Schottky Diode

A typical Schottky diode, with a forward drop of 0.6V will dissipate 0.6 * 14 * [1 – 2.8/5] = 3.7W (compared to the 1.1 to 2.2W dissipated by a MOSFET under the same conditions). This power loss becomes much more significant at lower duty cycles – synchronous rectification is recommended especially when a 12V-power input is used. The use of a dual Schottky diode in a single TO-220 package (e.g. the MBR2535) helps improve thermal dissipation.

MOSFET GATE BIAS

The power MOSFETs can be biased by one of two methods: charge pump or 12V supply connected to V_{C1}.

1) **Charge Pump (Bootstrap)**
When 12V is supplied to the drain of the MOSFET, as in Figure 5 (option), the gate drive needs to be higher than 12V in order to turn the MOSFET on. Capacitor C20 and diodes D1 & D2 are used as a charge pump voltage doubling circuit to raise the voltage of V_{C1} so that the TDRV pin always provides a high enough voltage to turn on Q1. The 12V supply must always be connected to V_{CC} to provide power for the IC itself, as well as gate drive for the bottom MOSFET.

2) **12V Supply**
When 5V is supplied to the drain of Q1, a 12V supply should be connected to both V_{CC} and V_{C1}.

CURRENT SHARE APPLICATION

Synchronous rectifier stages should not be paralleled unless they are locked in at the same frequency, or undesirable current sourcing/sinking could occur. If synchronization is not practical, the next best alternative is to disable the synchronous (bottom) switch. This is easily accomplished with the LX1660/61 by pulling the SYNCEN pin HIGH. In most applications, a 5 to 6% reduction in efficiency will result when the synchronous driver is disabled. A Schottky diode of the proper voltage and current ratings should be installed across the inactive FET to conduct the inductor current.

USING THE LX1660/61 DEVICES

USING THE LX1660/1661 IN PROGRAMMABLE APPLICATIONS

The LX1660/61 device may be used in conjunction with the **LX1670** Programmable Reference to implement a high-performance, digitally-controlled switched-mode power supply suitable for Pentium Pro Processors and other advanced microprocessor-based designs. The LX1670 incorporates a 5-bit equivalent DAC, which can be programmed by the microprocessor's Voltage Identification Code (VID). The LX1670 then commands the LX1660/61 to provide the required output voltage. System protection functions such as over voltage, SCR drive, and power-good detection are embedded within the LX1670 device. See Figure 5.

PROGRAMMING THE OUTPUT VOLTAGE

Select the voltage divider R14 and R15 values as shown in the table below, using 1% metal film resistors:

TABLE 5

Desired Converter V_{OUT}	R14 Value	R15 Value
2.8	806Ω	2kΩ
2.9	909Ω	2kΩ
3.0	1.0kΩ	2kΩ
3.1	1.10kΩ	2kΩ
3.2	1.21kΩ	2kΩ
3.3	1.30kΩ	2kΩ
3.4	1.40kΩ	2kΩ
3.5	1.50kΩ	2kΩ

If other V_{OUT} values are needed, the divider values may be calculated as follows:

$$V_{OUT} = V_{REF} (1 + R14/R15)$$

where V_{REF} = 2.0V. Note that resistor R4 is part of a filter element, and does not enter into the calculations.

Please refer to the **Application Information** schematic for the reference designators and part locations.

LAYOUT GUIDELINES - THERMAL DESIGN

A great deal of time and effort were spent optimizing the thermal design of the demo boards. Any user who intends to implement an embedded motherboard would be well advised to carefully read and follow these guidelines. If the FET switches have been carefully selected, external heatsinking is generally not required. However, this means that copper trace on the PC board must now be used. This is a potential trouble spot; as much copper area as possible must be dedicated to heatsinking the FET switches, and the diode as well if a non-synchronous solution is used.

In our VRM module, heatsink area was taken from internal ground and V_{CC} planes which were actually split and connected with VIAS to the power device tabs. The TO-220 and TO-263 cases are well suited for this application, and are the preferred packages. Remember to remove any conformal coating from all exposed PC traces which are involved in heatsinking.

LAYOUT GUIDELINES - THERMAL DESIGN (continued)

General Notes

As always, be sure to provide local capacitive de-coupling close to the chip. Be sure use ground plane construction for all high-frequency work. Use low ESR capacitors where justified, but be alert for damping and ringing problems. High-frequency designs demand careful routing and layout, and may require several iterations to achieve desired performance levels.

Power Traces

To reduce power losses due to ohmic resistance, careful consideration should be given to the layout of traces that carry high currents. The main paths to consider are:

- Input power from 5V supply to drain of top MOSFET.
- Trace between top MOSFET and lower MOSFET or Schottky diode.
- Trace between lower MOSFET or Schottky diode and ground.
- Trace between source of top MOSFET and inductor, sense resistor and load.

All of these traces should be made as wide and thick as possible, in order to minimize resistance and hence power losses. It is also recommended that, whenever possible, the ground, input and output power signals should be on separate planes (PCB layers). See Figure 10 – bold traces are power traces.

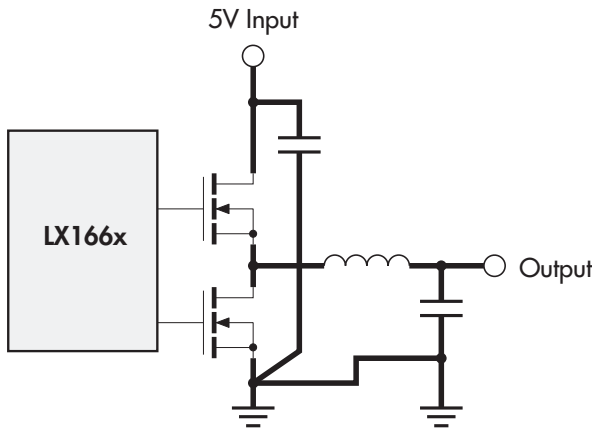


FIGURE 10 — Power Traces

USING THE LX1660/61 DEVICES

C9 Input De-coupling (V_{cc}) Capacitor

Ensure that this 1µF capacitor is placed as close to the IC as possible to minimize the effects of noise on the device.

Layout Assistance

Please contact Linfinity's Applications Engineers for assistance with any layout or component selection issues. A Gerber file with layout for the most popular devices is available upon request.

Evaluation boards are also available upon request. Please check Linfinity's web site for further application notes.

RELATED DEVICES

LX1662/1663
Single-Chip Programmable PWM Controller w/ 5-Bit DAC

LX1664/1665
Dual Output PWM for µProcessor Applications

LX1668
Triple Output PWM for µProcessor Applications

LX1553
PWM for 5V - 3.3V Conversion

LX1670
Programmable Reference & Voltage Monitor