DATA SHEET

TZA3005H
SDH/SONET STM1/OC3 and STM4/OC12 transceiver

Product specification
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Philips
Semiconductors

PHILIPS

SDH/SONET STM1/OC3 and STM4/OC12 transceiver

TZA3005H

FEATURES

- Supports STM1/OC3 (155.52 Mbits/s) and STM4/OC12 (622.08 Mbits/s)
- Supports reference clock frequencies of 19.44, 38.88, 51.84 and 77.76 MHz
- Meets Bellcore, ANSI and ITU-T specifications
- Meets ITU jitter specification typically to a factor of 2.5
- Integral high-frequency PLL for clock generation
- Interface to TTL logic
- Low jitter PECL (Positive Emitter Coupled Logic) interface
- 4 or 8-bit STM1/OC3 TTL data path
- 4 or 8-bit STM4/OC12 TTL data path
- No external filter components required
- QFP64 package
- Diagnostic and line loopback modes
- Lock detect
- LOS (Loss of Signal) input
- Low power (0.9 W typical)
- Selectable frame detection and byte realignment
- Loop timing
- Forward and reverse clocking
- Squelched clock operation
- Self-biased PECL inputs to support AC coupling.

APPLICATIONS

- SDH/SONET modules
- SDH/SONET-based transmission systems
- SDH/SONET test equipment
- ATM (Asynchronous Transfer Mode) over SDH/SONET
- Add drop multiplexers
- Broadband cross-connects
- Section repeaters
- Fibre optic test equipment
- Fibre optic terminators.

GENERAL DESCRIPTION

The TZA3005H SDH/SONET transceiver chip is a fully integrated serialization/deserialization STM1/OC3 (155.52 Mbits/s) and STM4/OC12 (622.08 Mbits/s) interface device. It performs all necessary serial-to-parallel and parallel-to-serial functions in accordance with SDH/SONET transmission standards. It is suitable for SONET-based applications and can be used in conjunction with the data and clock recovery unit (TZA3004), optical front-end (TZA3023 with TZA3034/44) and a laser driver (TZA3001). A typical network application is shown in Fig.10.

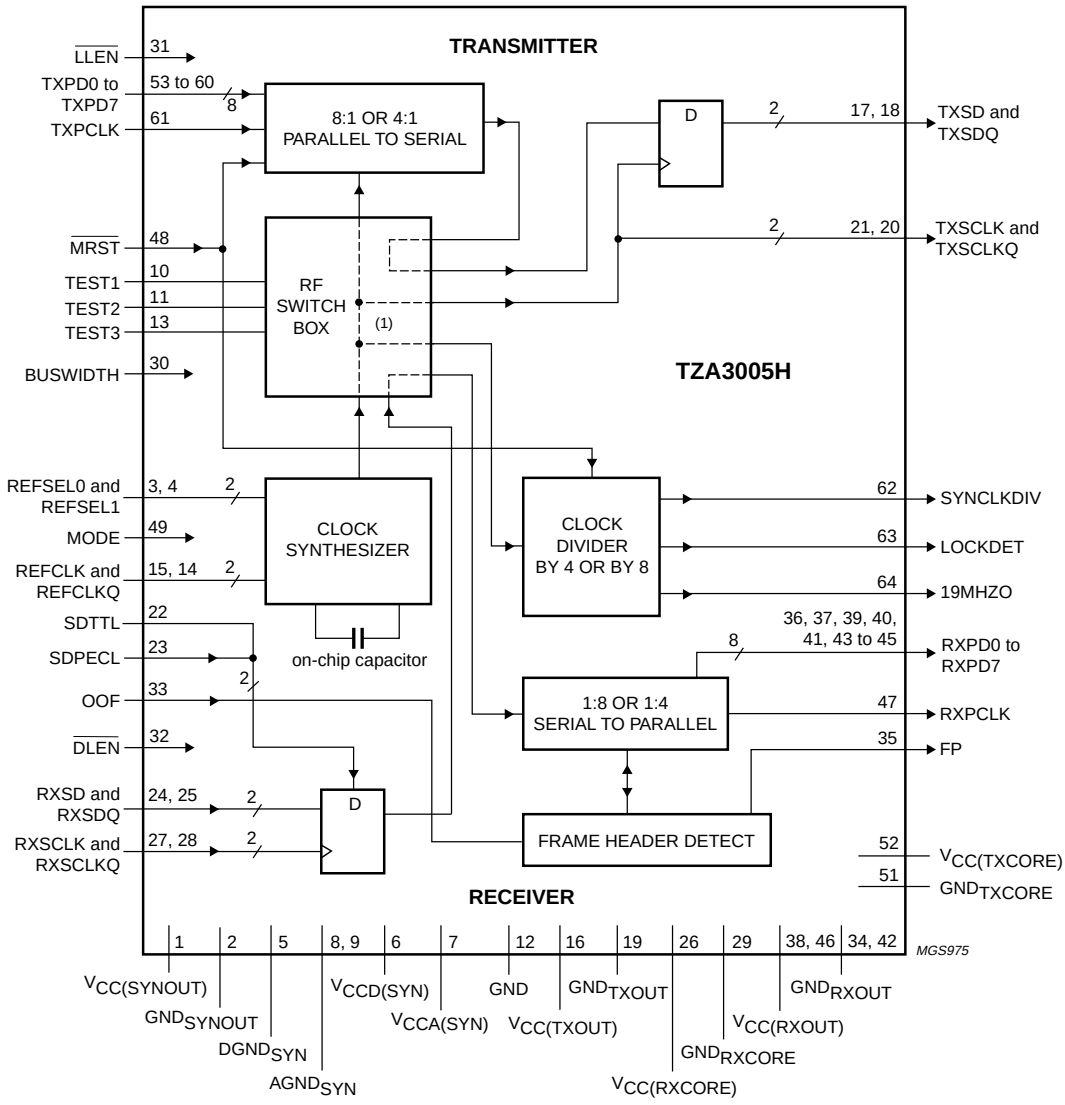
A high-frequency phase-locked loop is used for on-chip clock synthesis, which allows a slower external transmit reference clock to be used. A reference clock of 19.44, 38.88, 51.84 or 77.76 MHz can be used to support existing system clocking schemes. The TZA3005H also performs SDH/SONET frame detection.

The low jitter PECL interface ensures that Bellcore, ANSI, and ITU-T bit-error rate requirements are satisfied. The TZA3005H is supplied in a compact QFP64 package.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA3005H	QFP64	plastic quad flat package; 64 leads (lead length 1.6 mm); body $14 \times 14 \times 2.7$ mm	SOT393-1

BLOCK DIAGRAM



(1) Dashed lines represent normal operation mode.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	TYPE[1]	DESCRIPTION
$V_{CC(SYNOUT)}$	1	S	supply voltage (synthesizer output)
GND_{SYNOUT}	2	G	ground (synthesizer output)
REFSEL0	3	I	reference clock select input 0
REFSEL1	4	I	reference clock select input 1
$DGND_{SYN}$	5	G	digital ground (synthesizer)
$V_{CCD(SYN)}$	6	S	digital supply voltage (synthesizer)
$V_{CCA(SYN)}$	7	S	analog supply voltage (synthesizer)
$AGND_{SYN}$	8	G	analog ground (synthesizer)
$AGND_{SYN}$	9	G	analog ground (synthesizer)
TEST1	10	I	test and control input
TEST2	11	I	test and control input
GND	12	G	ground
TEST3	13	I	test and control input
REFCLKQ	14	I	inverted reference clock input
REFCLK	15	I	reference clock input
$V_{CC(TXOUT)}$	16	S	supply voltage (transmitter output)
TXSD	17	O	serial data output
TXSDQ	18	O	inverted serial data output
GND_{TXOUT}	19	G	ground (transmitter output)
TXSCLKQ	20	O	inverted serial clock output
TXSCLK	21	O	serial clock output
SDTTL	22	I	TTL signal detect input
SDPECL	23	I	PECL signal detect input
RXSD	24	I	serial data input
RXSDQ	25	I	inverted serial data input
$V_{CC(RXCORE)}$	26	S	supply voltage (receiver core)
RXSCLK	27	I	serial clock input
RXSCLKQ	28	I	inverted serial clock input
GND_{RXCORE}	29	G	ground (receiver core)
BUSWIDTH	30	I	4/8 bus width select input
$\overline{LLEN}$	31	I	line loopback enable input (active LOW)
$\overline{DLEN}$	32	I	diagnostic loopback enable input (active LOW)
OOF	33	I	out-of-frame enable input
GND_{RXOUT}	34	G	ground (receiver output)
FP	35	O	frame pulse output
RXPD0	36	O	parallel data output 0
RXPD1	37	O	parallel data output 1
$V_{CC(RXOUT)}$	38	S	supply voltage (receiver output)
RXPD2	39	O	parallel data output 2
RXPD3	40	O	parallel data output 3

SYMBOL	PIN	TYPE[1]	DESCRIPTION
RXPD4	41	O	parallel data output 4
GND_{RXOUT}	42	G	ground (receiver output)
RXPD5	43	O	parallel data output 5
RXPD6	44	O	parallel data output 6
RXPD7	45	O	parallel data output 7
$V_{CC(RXOUT)}$	46	S	supply voltage (receiver output)
RXPCLK	47	O	receive parallel clock output
$\overline{MRST}$	48	I	master reset (active LOW)
MODE	49	I	serial data rate select STM1/STM4
ALTPIN	50	I	test and control input
GND_{TXCORE}	51	G	ground (transmitter core)
$V_{CC(TXCORE)}$	52	S	supply voltage (transmitter core)
TXPD0	53	I	parallel data input 0
TXPD1	54	I	parallel data input 1
TXPD2	55	I	parallel data input 2
TXPD3	56	I	parallel data input 3
TXPD4	57	I	parallel data input 4
TXPD5	58	I	parallel data input 5
TXPD6	59	I	parallel data input 6
TXPD7	60	I	parallel data input 7
TXPCLK	61	I	transmit parallel clock input
SYNCLKDIV	62	O	transmit byte/nibble clock output (synchronous)
LOCKDET	63	O	lock detect output
19MHZO	64	O	19 MHz reference clock output

Note

1. Pin type abbreviations: O = Output, I = Input, S = Supply, G = Ground.

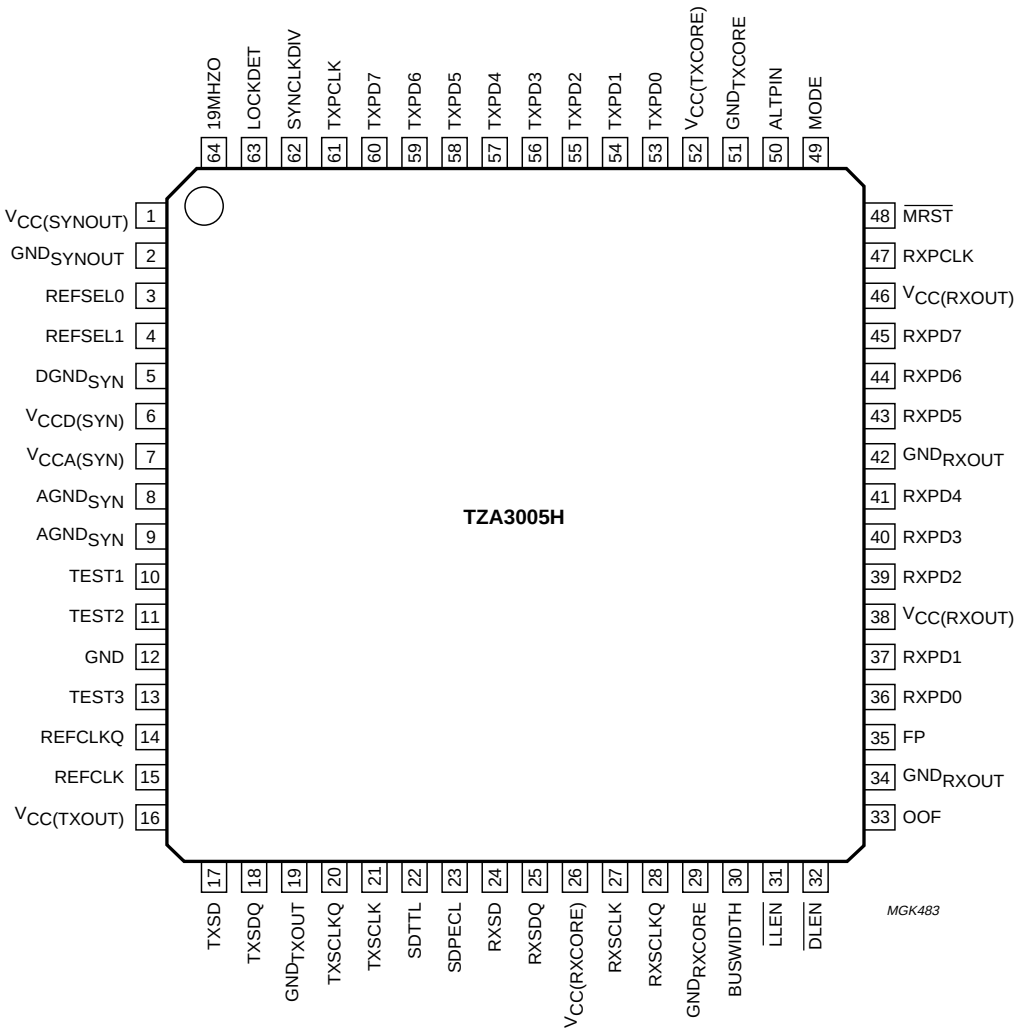


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Introduction

The TZA3005H transceiver implements SDH/SONET serialization/deserialization, transmission and frame detection/recovery functions. The TZA3005H can be used as the front-end for SONET equipment. It handles the serial receive and transmit interface functions including parallel-to-serial and serial-to-parallel conversion and clock generation. A block diagram showing the basic operation of the chip is shown in Fig.1.

The TZA3005H has a transmitter section, a receiver section, and an RF switch box. The sequence of operations is as follows:

- Transmitter operations:
  - 4 or 8-bit parallel input
  - parallel-to-serial conversion
  - serial output.
- Receiver operations:
  - serial input
  - frame detection
  - serial-to-parallel conversion
  - 4 or 8-bit parallel output.

The RF switch box receives serial clock and data signals from the transmitter section, the receiver input buffers and from the clock synthesizer. These signals are routed by multiplexers to the transmitter section, the transmitter output, the receiver and to the clock divider, depending on the status of the control inputs. The switch box also supports a number of test and loop modes.

Transmitter operation

The transmitter section of the TZA3005H converts STM1/OC3 or STM4/OC12 byte-serial input data to a bit-serial output data format. Input data rates of 19.44, 38.88, 77.76 or 155.52 Mbytes/s are converted to an output data rate of either 155.52 or 622.08 Mbits/s. It also provides diagnostic loopback (transmitter to receiver), line loopback (receiver to transmitter) and also loop timing (transmitter clocked by the receiver clock).

An integral frequency synthesizer, comprising a phase-locked loop and a divider, can be used to generate a high-frequency bit clock from an input reference clock frequency of 19.44, 38.88, 51.84 or 77.76 MHz.

CLOCK SYNTHESIZER

The clock synthesizer generates a serial output clock (TXSCLK) which is phase synchronised with the input reference clock (REFCLK). The serial output clock is synthesized from one of four SDH/SONET input reference clock frequencies and can have a frequency of either 155.52 MHz for STM1/OC3 or 622.08 MHz for STM4/OC12 selected by the MODE input (see Table 1).

Table 1 Transmitter output clock (TXSCLK) frequency options

MODE INPUT	TXSCLK FREQUENCY	OPERATING MODE
0	155.52 MHz	STM1/OC3
1	622.08 MHz	STM4/OC12

The frequency of the input reference clock is divided to obtain a frequency of about 19 MHz which is fed to the phase detector in the PLL. The appropriate divisor is selected by control inputs REFSEL0 and REFSEL1 as shown in Table 2.

Table 2 Reference frequency (REFCLK) options

REFSEL1	REFSEL0	REFCLK FREQUENCY
0	0	19.44 MHz
0	1	38.88 MHz
1	0	51.84 MHz
1	1	77.76 MHz

To ensure the TXSCLK frequency is accurate enough to operate in a SONET system, REFCLK must be generated from a differential PECL crystal oscillator having a frequency accuracy better than 4.6 ppm for compliance with *"ITU G.813 (option 1)"*, or 20 ppm for *"ITU G.813 (option 2)"*.

To comply with SONET jitter requirements, the maximum value specified for reference clock signal jitter must be guaranteed over the 12 kHz to 1 MHz bandwidth (see Table 3).

Table 3 ITU reference clock signal (REFCLK) jitter limits

MAXIMUM JITTER OF REFCLK 12 kHz TO 1 MHz	OPERATING MODE
56 ps (RMS)	STM1/OC3
14 ps (RMS)	STM4/OC12

The on-chip PLL contains a phase detector, a loop filter and a VCO. The phase detector compares the phases of the VCO and the divided REFCLK signals. The loop filter converts the phase detector output to a smooth DC voltage which controls the VCO frequency and ensures that it is always 622.08 MHz. In STM1/OC3 mode, the correct output frequency at TXSCLK is obtained by dividing the VCO frequency by 4. The loop filter parameters are optimized for minimal output jitter.

CLOCK DIVIDER

The clock divider generates either a byte rate or a nibble rate version of the serial output clock (TXSCLK) which is output on pin SYNCLKDIV (see Table 4).

Table 4 SYNCLKDIV frequency

MODE INPUT	BUSWIDTH	SYNCLKDIV FREQUENCY	OPERATING MODE
0	0 (nibble)	38.88 MHz	STM1/OC3
0	1 (byte)	19.44 MHz	STM1/OC3
1	0 (nibble)	155.52 MHz	STM4/OC12
1	1 (byte)	77.76 MHz	STM4/OC12

SYNCLKDIV is intended for use as a byte speed clock for upstream multiplexing and overhead processing circuits. Using SYNCLKDIV for upstream circuits ensures a stable frequency and phase relationship is maintained between the data in to and out of the TZA3005H.

For parallel-to-serial data conversion, the parallel input data is transferred from the TXPCLK byte clock timing domain to the internally generated bit clock timing domain. The internally generated bit clock does not have to be phase aligned to the TXPCLK signal but must be synchronized by the master reset ($\overline{\text{MRST}}$) signal.

Receiver operation

The receiver section of the TZA3005H converts STM1/OC3 or STM4/OC12 bit-serial input data to a parallel data output format. In byte mode, input data rates of 155.52 or 622.08 Mbits/s are converted to an output data rate of either 19.44 or 77.76 Mbytes/s. In nibble mode, a 4-bit parallel data stream is generated having a clock frequency of either 38.88 or 155.52 MHz. It also provides diagnostic loopback (transmitter to receiver), line loopback (receiver to transmitter) and squelched clock operation (transmitter clock to receiver).

FRAME AND BYTE BOUNDARY DETECTION

The frame and byte boundary detection circuit searches the incoming data for the correct 48-bit frame pattern which is a sequence of three consecutive A1 bytes of F0 H followed immediately by three consecutive A2 bytes of 28 H. Frame pattern detection is enabled and disabled by the out-of-frame enable input (OOF). Detection is enabled by a rising edge on pin OOF, and remains enabled while the level on pin OOF is HIGH. It is disabled when at least one frame pattern is detected and the level on pin OOF is no longer HIGH. When frame pattern detection is enabled, the frame pattern is used to locate byte and frame boundaries in the incoming data stream (Received Serial Data (RXSD) or looped transmitter data). The serial to parallel converter block uses the located byte boundary to divide the incoming data stream into bytes for output on the parallel output data bus (RXPD0 to RXPD7). When the correct 48-bit frame pattern is detected, the occurrence of the frame boundary is indicated by the Frame Pulse (FP) signal. When frame pattern detection is disabled, the byte boundary is fixed, and only frame patterns which align with the fixed byte boundary produce an output on pin FP.

It is extremely unlikely that random data in an STM1/OC3 or STM4/OC12 data stream will replicate the 48-bit frame pattern. Therefore, the time taken to detect the beginning of the frame should be less than 250 μs (as specified in *"ITU G.783"*) even at extremely high bit error rates.

Once down-stream overhead circuits verify that frame and byte synchronization are correct, OOF can be set LOW to prevent the frame search process synchronizing to a mimic frame pattern.

SERIAL-TO-PARALLEL CONVERTER

The serial-to-parallel converter causes a delay between the first bit of an incoming serial data byte to the start of the parallel output of that byte. The delay depends on the time taken for the internal parallel load timing circuit to synchronize the data byte boundaries to the falling edge of RXPCLK. The timing of RXPCLK is independent of the byte boundaries. RXPCLK is neither truncated nor extended during reframe sequences.

Transceiver pin descriptions

TRANSMITTER INPUT SIGNALS

Parallel data inputs (TXPD0 to TXPD7)

These are TTL data word inputs. The input data is aligned with the TXPCLK parallel input clock. TXPD7 is the most significant bit (corresponding to bit 1 of each PCM word, the first bit transmitted). TXPD0 is the least significant bit (corresponding to bit 8 of each PCM word, the last bit transmitted). Bits TXPD0 to TXPD7 are sampled on the rising edge of TXPCLK. If a 4-bit bus width is selected, TXPD7 is the most significant bit and TXPD4 is the least significant bit. Inputs TXPD0 to TXPD3 are unused.

Parallel clock input (TXPCLK)

This is a TTL input clock signal having a frequency of either 19.44, 38.88, 77.76 or 155.52 MHz and a duty factor of nominally 50%, to which input data bits TXPD0 to TXPD7 are aligned. TXPCLK transfers the input data to a holding register in the parallel-to-serial converter. The rising edge of TXPCLK samples bits TXPD0 to TXPD7. After a master reset, one rising edge of TXPCLK is required to fully initialize the internal data path.

RECEIVER INPUT SIGNALS

Receive serial data (RXSD and RXSDQ)

These are differential PECL serial data inputs, normally connected to an optical receiver module or to the TZA3004 data and clock recovery unit, and clocked by RXSCLK and RXSCLKQ. These inputs can be AC coupled without external biasing.

Receive serial clock (RXSCLK and RXSCLKQ)

These are differential PECL recovered clock signals synchronized to the input data RXSD and RXSDQ. It is used by the receiver as the master clock for framing and deserialization functions. These inputs can be AC coupled without external biasing.

Out-of-frame (OOF)

This is a TTL signal which enables frame pattern detection logic in the TZA3005H. The frame pattern detection logic is enabled by a rising edge on pin OOF, and remains enabled until a frame boundary is detected and OOF goes LOW. OOF is an asynchronous signal with a minimum pulse width of one RXPCLK period (see Fig.3).

Signal detect PECL (SDPECL)

This is a single-ended PECL input with an internal pull-down resistor. This input is driven by an external optical receiver module to indicate a loss of received optical power (LOS). SDPECL is active HIGH when SDTTL is at logic 0 and active LOW when SDTTL is at logic 1or unconnected. When there is a loss of signal, SDPECL is inactive and the bit-serial data on pins RXSD and RXSDQ is internally forced to a constant zero. When SDPECL is active, the bit-serial data on pins RXSD and RXSDQ is processed normally (see Table 5).

Signal detect TTL (SDTTL)

This is a single-ended TTL input with an internal pull-up resistor. This input is driven by an external optical receiver module to indicate a loss of received optical power (LOS). SDTTL is active HIGH when pin SDPECL is logic 0 or unconnected, and active LOW when pin SDPECL is at logic 1. When there is a loss of signal, SDTTL is inactive and the bit-serial data on pins RXSD and RXSDQ is internally forced to a constant zero. When SDTTL is active, the bit-serial data on pins RXSD and RXSDQ is processed normally (see Table 5).

If pin SDTTL instead of pin SDPECL is to be connected to the optical receiver module, connect pin SDPECL to a logic HIGH-level to implement an active-LOW signal detect, or leave pin SDPECL unconnected to implement an active-HIGH signal detect.

Table 5 SDPECL/SDTTL truth table

SDPECL	SDTTL	RXPD OUTPUT DATA
0 or floating	0	0
0 or floating	1 or floating	RXSD input data
1	0	RXSD input data
1	1 or floating	0

COMMON INPUT SIGNALS

Bus width selection (BUSWIDTH)

This is a TTL signal which selects 4-bit or 8-bit operation for the transmit and receive parallel interfaces. BUSWIDTH LOW selects a 4-bit bus width. BUSWIDTH HIGH selects an 8-bit bus width.

Reference clock (REFCLK and REFCLKQ)

These are differential PECL reference clock inputs for the internal bit clock synthesizer.

Diagnostic loopback enable ($\overline{DLEN}$)

This is an active-LOW TTL signal which selects diagnostic loopback. When $\overline{DLEN}$ is HIGH, the TZA3005H receiver uses the primary data (RXSD) and clock (RXSCLK) inputs. When $\overline{DLEN}$ is LOW, the receiver uses the diagnostic loopback clock and the transmitter input data.

Master reset ($\overline{MRST}$)

This is an active LOW TTL signal which initializes the transmitter. SYNCLKDIV is LOW during reset.

Line loopback enable ($\overline{LLEN}$)

This is an active LOW TTL signal which selects line loopback. When $\overline{LLEN}$ is LOW, the TZA3005H routes the data and clock from the receiver inputs RXSD and RXSCLK to the transmitter outputs TXSD and TXSCLK.

Reference select (REFSEL0 and REFSEL1)

These are TTL signals which select the reference clock frequency (see Table 2).

Mode select (MODE)

This TTL signal selects the transmitter serial data rate. MODE LOW selects 155.52 Mbits/s. MODE HIGH selects 622.08 Mbits/s.

Test inputs (ALTPIN, TEST1, TEST2, TEST3)

These are active HIGH TTL signals which control the operating mode and test internal circuits during production testing. For normal operation, these inputs are left unconnected and internal pull-down resistors hold each pin LOW. See Table 7 for more details.

TRANSMITTER OUTPUT SIGNALS

Transmit clock outputs (TXSCLK and TXSCLKQ)

These are differential PECL serial clock signals which can be used to retime TXSD. The clock frequency is either 155.52 MHz or 622.08 MHz depending on the operating mode.

Transmit serial data (TXSD and TXSDQ)

These are differential PECL serial data stream outputs which are normally connected to an optical transmitter module or to the TZA3001 laser driver.

Parallel clock (SYNCLKDIV)

This is a TTL reference clock generated by dividing the internal bit clock by eight, or by four when BUSWIDTH is LOW. It is normally used to coordinate byte-wide transfers between upstream logic and the TZA3005H.

Lock detect (LOCKDET)

This is an active HIGH CMOS signal. When active, it indicates that the transmit PLL is locked to the reference clock input.

19 MHz clock output (19MHZO)

This is a 19 MHz CMOS clock from the clock synthesizer. It can be connected to the reference clock input of an external clock recovery unit, such as the TZA3004.

RECEIVER OUTPUT SIGNALS

Parallel data outputs (RXPD0 to RXPD7)

These outputs comprise a parallel TTL data bus. The parallel output data is aligned with the parallel output clock (RXPCLK). RXPD7 is the most significant bit (corresponding to bit 1 of each PCM word, the first bit received). RXPD0 is the least significant bit (corresponding to bit 8 of each PCM word, the last bit received). RXPD0 to RXPD7 are updated on the falling edge of RXPCLK. When a 4-bit bus width is selected, RXPD7 is the most significant bit and bit 4 is the least significant bit. Outputs RXPD0 to RXPD3 are forced LOW.

Frame pulse (FP)

This is a TTL signal which indicates frame boundaries detected in the incoming data stream on pin RXSD. When frame pattern detection is enabled (see Section “Out-of-frame (OOF)”), FP goes HIGH for one cycle of RXPCLK when a 48-bit sequence matching the frame pattern is detected on inputs RXSD and RXSDQ. When frame pattern detection is disabled, FP goes HIGH only when the incoming data matches the frame pattern and fits exactly within the fixed byte boundary. FP is updated on the falling edge of RXPCLK.

Parallel output clock (RXPCLK)

This is a TTL byte-rate output clock having a frequency of either 19.44, 38.88, 77.76 or 155.52 MHz and a duty factor of nominally 50%, to which the byte-serial output data bits RXPD0 to RXPD7 are aligned. The falling edge of RXPCLK updates the data on pins RXPD0 to RXPD7 and the FP signal.

Other operating modes

Diagnostic loopback

A transmitter-to-receiver loopback mode is available for diagnostic purposes. When $\overline{DLEN}$ is LOW, the differential serial clock and data from the transmitter parallel-to-serial block continue to be routed to transmitter outputs, but are also routed to the receiver serial-to-parallel block instead of the receiver input signals from pins RXSD/RXSDQ and RXSCLK/RXSCLKQ.

Line loopback

A receiver-to-transmitter loopback mode is available for line testing purposes. When $\overline{LLEN}$ is LOW, the receiver input signals (RXSD/RXSDQ and RXSCLK/RXSCLKQ) are routed, after retiming, to the transmitter output buffers. The receiver clock and data are also routed to the serial-to-parallel block.

Loop timing

In loop timing mode, the transmitter section is clocked by the receiver input clock (RXSCLK) instead of by the internal clock synthesizer. SYNCLKDIV is now derived from RXSCLK so that it can be used to clock upstream transmitter logic. Loop timing is enabled by setting pins ALTPIN, TEST1, TEST2 and TEST3 (see Table 6). After activating the loop timing mode, the receiver clock must be synchronized to the transmitter input data (TXPD0 to TXPD7) by activating master reset ($\overline{MRST}$). In loop timing mode, the internal clock synthesizer is still used to generate the 19MHz output clock signal on pin 19MHZO.

Squelched clock operation

Some clock recovery devices force their recovered output clock to zero if a loss of input signal is detected. If this happens, the SDTTL or SDPECL signals are inactive and no clock signal is present at pins RXSCLK and RXSCLKQ.

If no clock signal is present at pins RXSCLK/RXSCLKQ, there is no RXPCLK signal. This may not be suitable for some applications, in which case, the TZA3005H can be set to squelched clock operation by setting pins ALTPIN, TEST1, TEST2 and TEST3 as shown in Table 6.

In squelched clock operation, receiver timing is performed by a part of the internal clock synthesizer which normally only provides transmitter timing. This produces a RXPCLK clock signal when either SDTTL or SDPECL is inactive. If either SDTTL or SDPECL is inactive in squelched clock operation, it is equivalent to normal operation. During a transition from normal operation to squelched clock operation, the RXPCLK clock cycle exhibits a once-only random shortening.

Table 6 shows that the same operating mode can be selected at different settings of the control inputs. If ALTPIN = 0, the STM4 nibble mode is not available, but is used for squelched clock operation. If ALTPIN = 1, all operating modes are available, including STM4 nibble mode.

Table 6 Truth table operating modes

ALTPIN (pin 50)	TEST1 (pin 10)	TEST2 (pin 11)	TEST3 (pin 13)	BUSWIDTH (pin 30)	MODE (pin 49)	SD[1]	$\overline{\text{LLEN}}$ (pin 31)	$\overline{\text{DLEN}}$ (pin 32)	FUNCTIONAL OPERATING MODE
0	X	X	0	X	0	X	1	1	normal operation (STM1 byte/nibble)
0	X	X	0	0	1	0	1	1	squelched clock operation (STM4 byte)
0	X	X	0	0	1	1	1	1	normal operation (STM4 byte)
0	X	X	0	1	1	X	1	1	normal operation (STM4 byte)
0	X	X	1	X	X	X	1	1	loop timing
1	0	0	0	X	X	X	1	1	normal operation
1	0	0	1	X	X	X	1	1	loop timing
1	0	1	0	X	X	0	1	1	squelched clock operation
1	0	1	0	X	X	1	1	1	normal operation
X	X	X	X	X	X	X	X	0	diagnostic loopback
X	X	X	X	X	X	X	0	X	line loopback

Note

1. SD denotes either pin 22 (SDTTL) or pin 23 (SDPECL) (signal present = active = 1; loss of signal = inactive = 0). During a loss of signal, the outputs RXPD0 to RXPD7 are forced to zero (see Table 5).

Receiver frame alignment

Figure 3 shows a typical frame and boundary alignment sequence. Frame and byte boundary detection is enabled on the rising edge of OOF and remains enabled while OOF is HIGH. Byte boundaries are recognized after the third A2 byte is received. FP goes HIGH for one RXPCLK cycle to indicate that this is the first data byte with the correct byte alignment on the output parallel data bus (RXPD0 to RXPD7).

When interfaced with a section terminating device, OOF must remain HIGH for a full frame period after the initial frame pulse (FP). This is to allow the section terminating device to internally verify that frame and byte alignment are correct (see Fig.4). Because at least one frame pattern will have been detected since the rising edge of OOF, boundary detection is disabled when OOF goes LOW.

The frame and byte boundary detection block is activated on the rising edge of OOF, and remains active until a frame pulse (FP) occurs and OOF goes LOW, whichever occurs last. Figure 4 shows a typical OOF timing pattern when the TZA3005H is connected to a down stream section terminating device. OOF stays HIGH for one full frame after the first frame pulse (FP). The frame and byte boundary detection block is active until OOF goes LOW.

Figure 5 shows frame and byte boundary detection activated on the rising edge of OOF, and deactivated by the first frame pulse (FP) after OOF goes LOW.

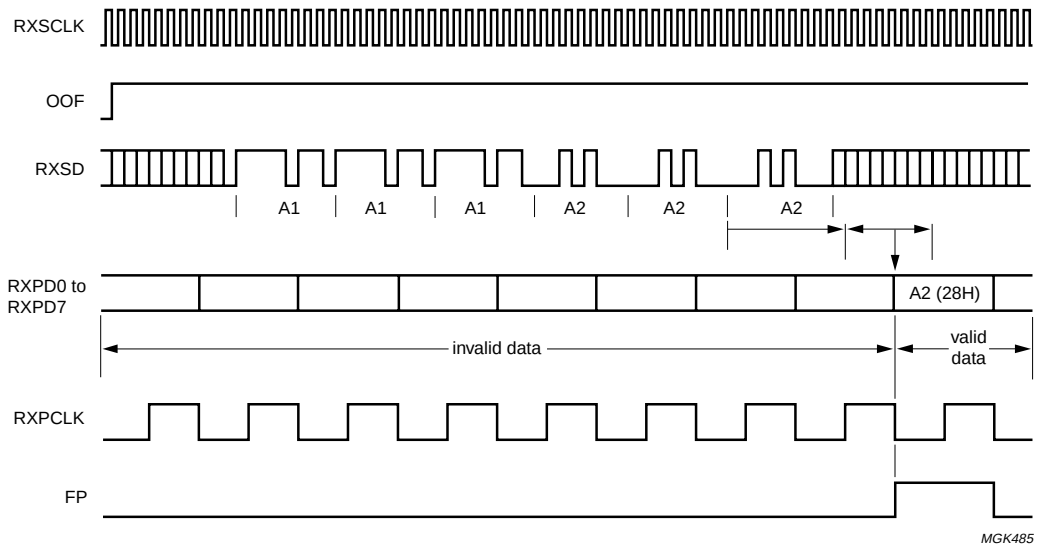


Fig.3 Frame and byte detection.

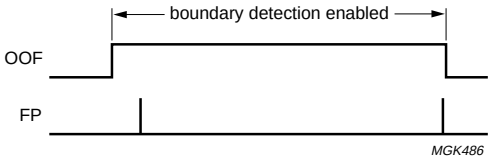


Fig.4 OOF operating time with PM5312 STTX or PM5355 SUNI-622 (see Table 7).

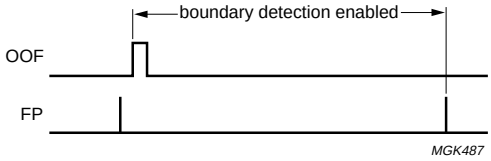


Fig.5 Alternate OOF timing.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–0.5	+6	V
V_n	voltage			
	on any input pin	–0.5	V_{CC} + 0.5	V
	between two differential PECL input pins	–2	+2	V
	on SDPECL input pin	V_{CC} – 3	V_{CC} + 0.5	V
$I_{I(n)}$	current			
	into any TTL output pin	–8	+8	mA
	into any PECL output pin	–50	+1.5	mA
P_{tot}	total power dissipation	–	1.5	W
T_{stg}	storage temperature	–65	+150	°C
$T_{j(bias)}$	junction temperature under bias	–55	+125	°C
$T_{case(bias)}$	case temperature under bias	–55	+100	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However it is good practice to take normal precautions appropriate to handling MOS devices (see *"Handling MOS devices"*).

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
T_{amb}	ambient temperature; note 1	–40	+85
T_j	junction temperature	–40	+125
$R_{th(j-a)}$	thermal resistance from junction to ambient; note 2	55	K/W

Notes

1. For applications with T_{amb} >75 °C, it is advised that the board layout is designed to allow optimum heat transer.
2. $R_{th(j-a)}$ is determined with the IC soldered on a standard single-sided 57 × 57 × 1.6 mm FR4 epoxy PCB with 35 µm thick copper tracks. The measurements are performed in still air. This value will vary depending on the number of board layers, copper sheet thickness and area, and the proximity of surrounding components.

DC CHARACTERISTICS

For typical values, T_{amb} = 25 °C and V_{CC} = 3.3 V; minimum and maximum values are valid over entire T_j and V_{CC} ranges.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
General						
V_{CC}	supply voltage		3.0	3.3	5.5	V
P_{tot}	total power dissipation	outputs open;				
		V_{CC} = 3.47 V	–	0.9	1.4	W
		V_{CC} = 5.5 V	–	–	2.3	W
$I_{CC(tot)}$	total supply current	outputs open;				
		V_{CC} = 3.47 V	–	272	394	mA
		V_{CC} = 5.5 V	–	–	420	mA
TTL inputs						
V_{IH}	HIGH-level input voltage		2	–	V_{CC}	V
V_{IL}	LOW-level input voltage		0	–	0.8	V
I_{IH}	HIGH-level input current	$V_{IH} = V_{CC}$; note 1	–10	–	+10	µA
I_{IL}	LOW-level input current	V_{IL} = 0; note 1	–10	–	+10	µA
R_{pu}	pull-up resistor	note 2	8	10	12	kΩ
R_{pd}	pull-down resistor at pin SDTTL		8	10	12	kΩ
TTL outputs						
V_{OH}	HIGH-level output voltage	I_{OH} = –1 mA; note 3	2.4	–	–	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	–	–	+0.5	V
PECL I/O						
V_{IH}	HIGH-level input voltage	note 4	V_{CC} – 1.2	–	–	V
V_{IL}	LOW-level input voltage		–	–	V_{CC} – 1.6	V
V_{OH}	HIGH-level output voltage	terminated with 50 Ω to V_{CC} – 2.0 V	V_{CC} – 1.1	–	V_{CC} – 0.9	V
V_{OL}	LOW-level output voltage		V_{CC} – 1.9	–	V_{CC} – 1.6	V
$\Delta V_{o(dif)}$	differential output voltage		±600	–	±900	mV
$\Delta V_{i(dif)(sens)}$	differential input sensitivity	PECL inputs are AC coupled	±100	–	–	mV

Notes

1. For input pins REFSEL0, REFSEL1, BUSWIDTH, $\overline{\text{LLEN}}$, $\overline{\text{DLEN}}$, OOF, $\overline{\text{MRST}}$, MODE, TXPDn, TXPCLK.
2. For input pins SDPECL, ALTPIN, TEST1, TEST2, TEST3.
3. Only applies to pin 19MHZO; guaranteed by simulation.
4. The PECL inputs are high impedance. The transmission lines should be terminated externally using an appropriate termination.

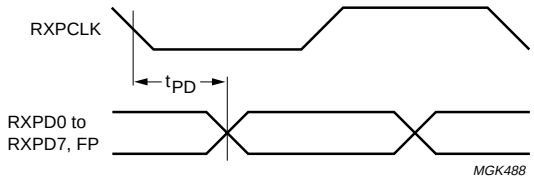
AC CHARACTERISTICS

For typical values, T_{amb} = 25 °C and V_{CC} = 3.3 V; minimum and maximum values are valid over entire T_j and V_{CC} ranges.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
General						
$f_{TXSCLK(nom)}$	nominal TXSCLK frequency	f_{REFCLK} as Table 2;				
		MODE = 0	155.517	155.52	155.523	MHz
		MODE = 1	622.068	622.08	622.092	MHz
J_o	data output jitter	in lock; note 1	–	0.004	0.006	UI (RMS)
$f_{REFCLK(tol)}$	frequency tolerance of REFCLK	meets SONET output frequency specification; note 1	–20	–	+20	ppm
t_r, t_f	rise/fall time PECL outputs	20% to 80%; 50 Ω load to V_{CC} – 2.0 V	–	220	450	ps
Receiver timing (see Figs 6 and 7)						
C_L	TTL output load capacitance		–	–	15	pF
δ_{RXPCLK}	duty factor of RXPCLK	note 2	40	50	60	%
t_{PD}	propagation delay; RXPCLK LOW to RXPDn, FP		–0.5	+1.5	+2.5	ns
t_{su}	set-up time; RXSD/RXSDQ to RXSCLK/RXSCLKQ		400	–	–	ps
t_h	hold time; RXSD/RXSDQ to RXSCLK/RXSCLKQ		400	–	–	ps
Transmitter timing (see Figs 8 and 9)						
δ_{TXSCLK}	duty factor of TXSCLK		40	50	60	%
t_{su}	set-up time; TXPDn to TXPCLK		–0.5	–	–	ns
t_h	hold time; TXPDn to TXPCLK		1.5	–	–	ns
t_{PD}	propagation delay time; TXSCLK LOW to TXSD		–	–	440	ps

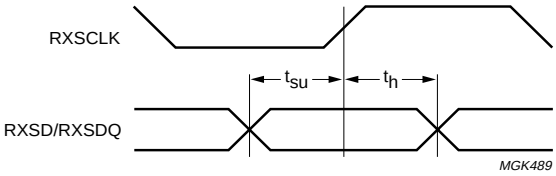
Notes

1. Jitter on pins REFCLK/REFCLKQ complies with Table 3.
2. Minimum value is 35% in STM4 nibble mode.



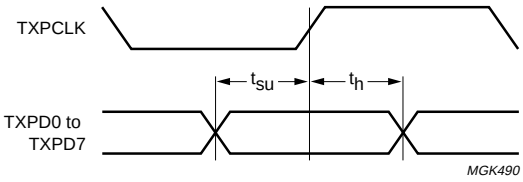
For TTL outputs, t_{PD} is the time (ns) from the 50% point of the reference signal to the 50% point of the output signal.

Fig.6 Receiver output timing.



Timing is measured from the cross-over point of the reference signal to the cross-over point of the input signal.

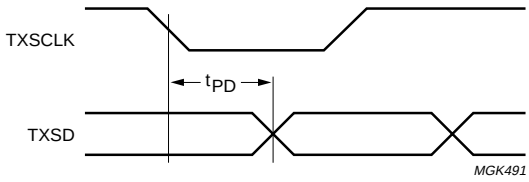
Fig.7 Receiver input timing.



For TTL signals, t_{su} between input data and clock signals is the time (ps) from the 50% point of the data to the 50% point of the clock.

For TTL signals, t_h between input data and clock signals is the time (ps) from the 50% point of the clock to the 50% point of the data.

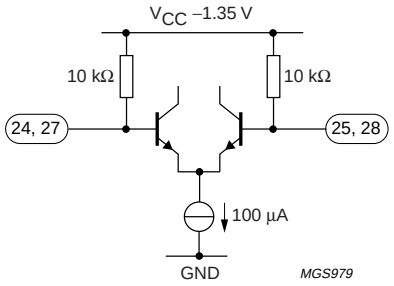
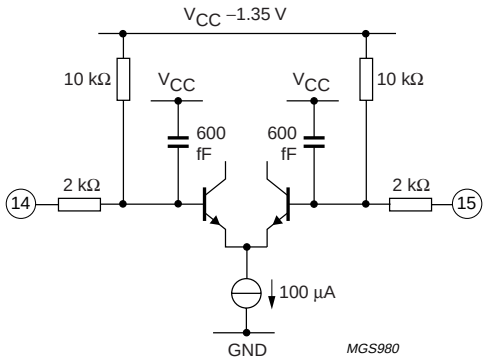
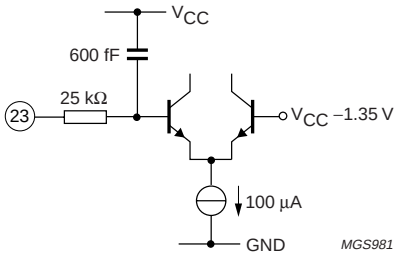
Fig.8 Transmitter input timing.

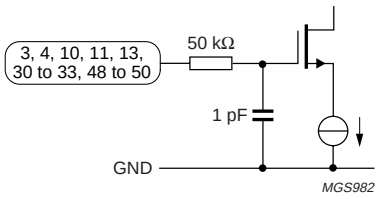
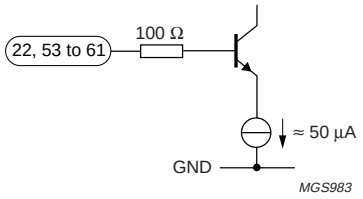
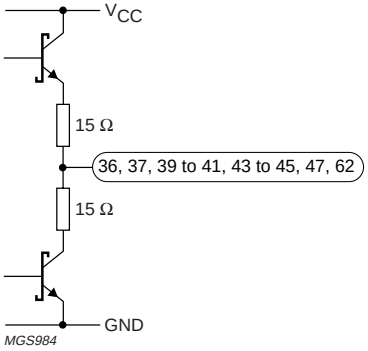


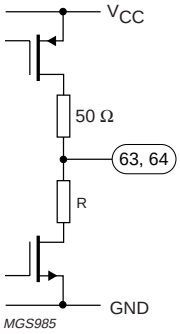
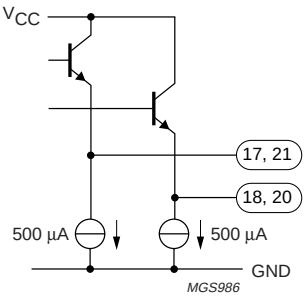
Timing is measured from the cross-over point of the reference signal to the cross-over point of the output signal.

Fig.9 Transmitter output timing.

INTERNAL CIRCUITRY

PIN	SYMBOL AND DESCRIPTION	CHARACTERISTIC	EQUIVALENT CIRCUIT
24	RXSD; serial data input	PECL inputs	
27	RXSCLK; serial clock input		
25	RXSDQ; inverted serial data input		
28	RXSCLKQ; inverted serial clock input		
14	REFCLKQ; inverted reference clock input	PECL inputs	
15	REFCLK; reference clock input		
23	SDPECL; PECL signal detect input	PECL input	

PIN	SYMBOL AND DESCRIPTION	CHARACTERISTIC	EQUIVALENT CIRCUIT
3	REFSEL0; reference clock select input 0	TTL inputs	
4	REFSEL1; reference clock select input 1		
10	TEST1; test and control input		
11	TEST2; test and control input		
13	TEST3; test and control input		
30	BUSWIDTH; 4/8 bus width select input		
31	$\overline{\text{LLEN}}$; line loopback enable input (active LOW)		
32	$\overline{\text{DLEN}}$; diagnostic loopback enable input (active LOW)		
33	OOF; out-of-frame enable input		
48	$\overline{\text{MRST}}$; master reset (active LOW)		
49	MODE; serial data rate select STM1/STM4		
50	ALTPIN; test and control input		
22	SDTTL; TTL signal detect input	TTL inputs	
53	TXPD0; parallel data input 0		
54	TXPD1; parallel data input 1		
55	TXPD2; parallel data input 2		
56	TXPD3; parallel data input 3		
57	TXPD4; parallel data input 4		
58	TXPD5; parallel data input 5		
59	TXPD6; parallel data input 6		
60	TXPD7; parallel data input 7		
61	TXPCLK; transmit parallel clock input		
36	RXPD0; parallel data output 0	TTL outputs	
37	RXPD1; parallel data output 1		
39	RXPD2; parallel data output 2		
40	RXPD3; parallel data output 3		
41	RXPD4; parallel data output 4		
43	RXPD5; parallel data output 5		
44	RXPD6; parallel data output 6		
45	RXPD7; parallel data output 7		
47	RXPCLK; receive parallel clock output		
62	SYNCLKDIV; transmit byte/nibble clock output (synchronous)		

PIN	SYMBOL AND DESCRIPTION	CHARACTERISTIC	EQUIVALENT CIRCUIT
63	LOCKDET; lock detect output; R = 50 Ω	CMOS outputs	
64	19MHZO; 19 MHz reference clock output; R = 20 Ω		
17	TXSD; serial data output	PECL outputs	
18	TXSDQ; inverted serial data output		
20	TXSCLKQ; inverted serial clock output		
21	TXSCLK; serial clock output		

APPLICATION INFORMATION

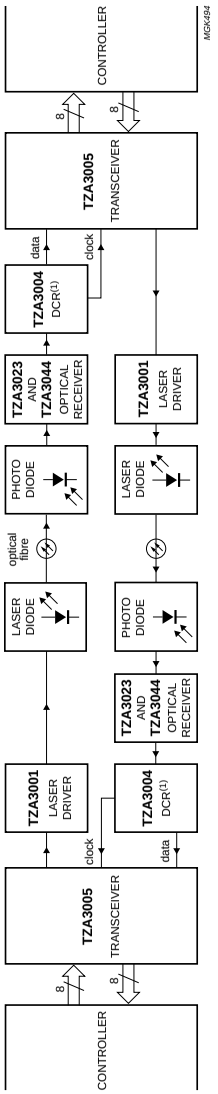


Fig.10 Application diagram.

(1) DCR = Data and Clock Recovery unit.

Forward clocking

It is sometimes necessary to ‘forward clock’ data in an SDH/SONET system. When this is the case, the input parallel data clock (TXPCLK) and the reference clock (REFCLK/REFCLKQ) from which the high speed serial clock is synthesized will both originate from the same clock source. This section explains how to configure the TZA3005H to operate in this mode.

The connections required for forward clocking are shown in Fig.13. There are no timing specifications for the phase relationship between REFCLK and TXPCLK.
The TZA3005H can handle any phase relationship between these two input clocks if they are derived from the same clock source. The TZA3005H internal transmitter logic must be synchronized by asserting a master reset ($\overline{\text{MRST}}$).

Reverse clocking

In many cases, a reverse clocking scheme is used where the upstream logic is clocked by the TZA3005H using SYNCLKDIV (see Fig.14). There is no requirement specification for the propagation delay from SYNCLKDIV to TXPCLK because the TZA3005H can handle any phase relationship between these two signals. The TZA3005H internal transmitter logic must be synchronized by asserting a master reset ($\overline{\text{MRST}}$).

PECL output termination

The PECL outputs have to be terminated with 50 Ω connected to V_{CC} − 2.0 V. If this voltage is not available, a Thevenin termination can be used as shown in Figs 11 and 12.

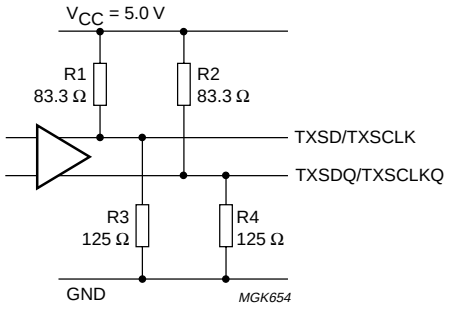


Fig.11 PECL output termination scheme (V_{CC} = 5.0 V).

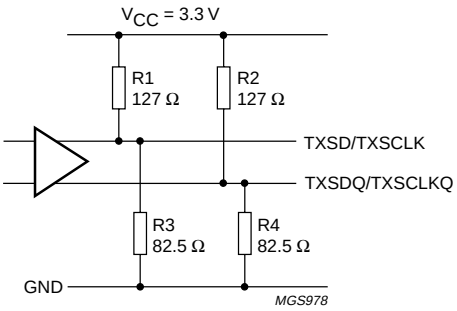


Fig.12 PECL output termination scheme (V_{CC} = 3.3 V).

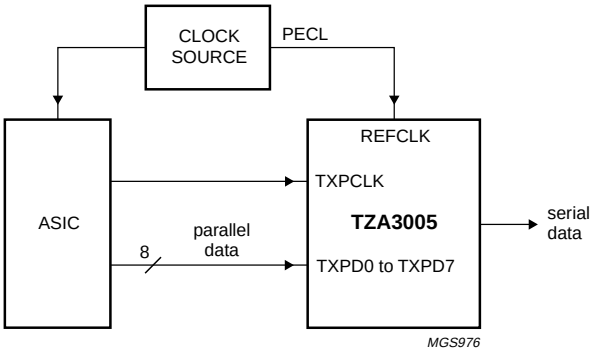


Fig.13 TZA3005H in forward clocking scheme.

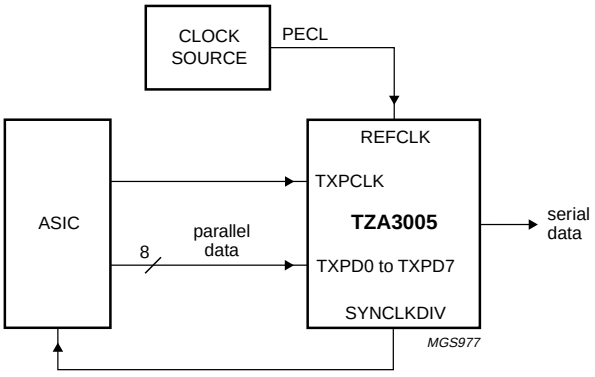


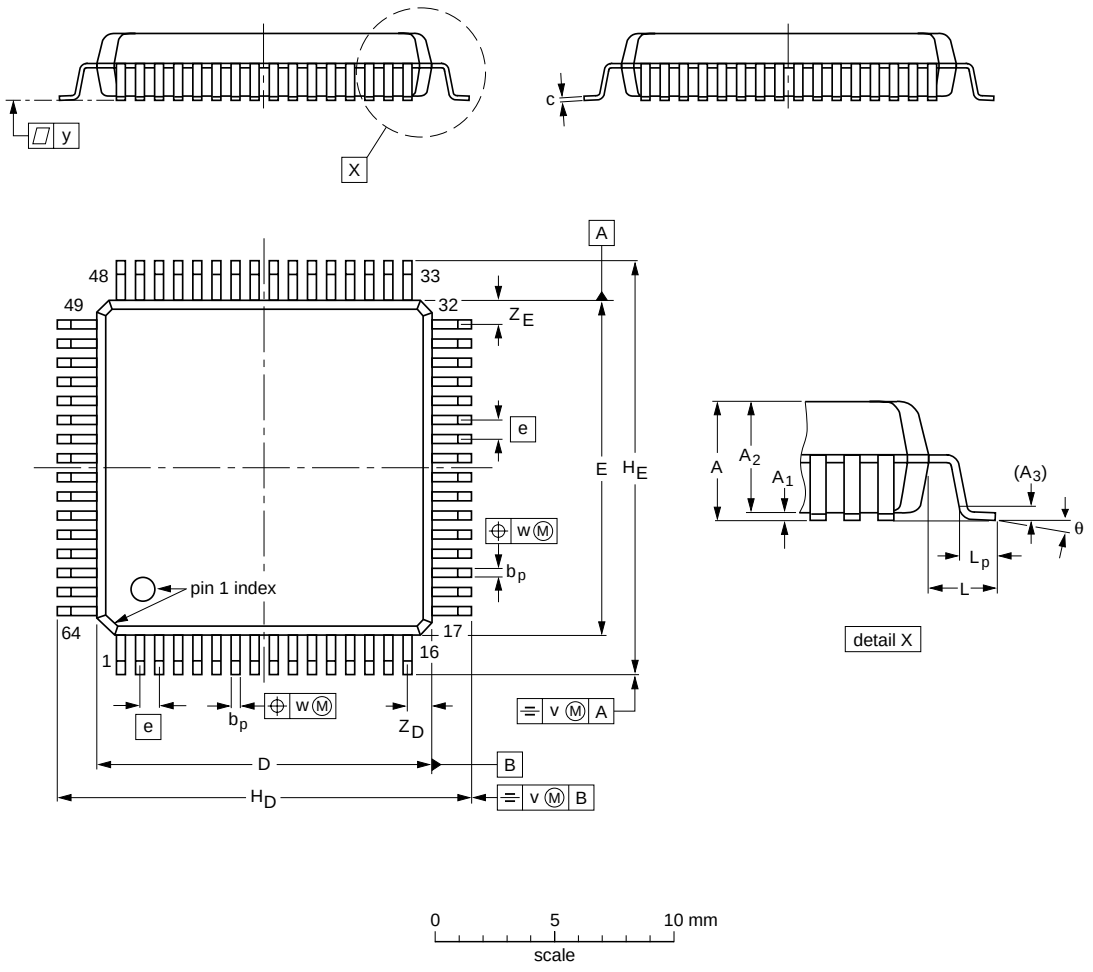
Fig.14 TZA3005H in reverse clocking scheme.

Table 7 Suggested interface devices

MANUFACTURER	TYPE	DATA RATE (Mbits/s)	FUNCTION
Philips	TZA3004	622 or 155	clock recovery
	TZA3031/3001	155/622	laser driver
	TZA3034/3044	155/622	post amplifier
	TZA3033/3023	155/622	transimpedance amplifier
PMC-Sierra	PM5312	155 or 622	transport terminal transceiver
	PM5355	622	Saturn user network interface

PACKAGE OUTLINE

QFP64: plastic quad flat package; 64 leads (lead length 1.6 mm); body 14 x 14 x 2.7 mm **SOT393-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.00	0.25 0.10	2.75 2.55	0.25	0.45 0.30	0.23 0.13	14.1 13.9	14.1 13.9	0.8	17.45 16.95	17.45 16.95	1.60	1.03 0.73	0.16	0.16	0.10	1.2 0.8	1.2 0.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT393-1	134E07	MS-022				~~99-12-27~~ 00-01-19

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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