AN8021L, AN8021SB

AC-DC switching power supply control IC

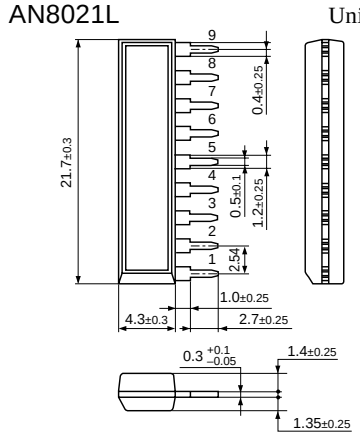
■ Overview

The AN8021L and AN8021SB are ICs which are suitable for controlling the switching power supply using primary side control method.

Those are most suited for a switching power supply of relatively small capacity. Less frequently used functions are removed and only the necessary minimum functions are incorporated, so that they are compact and very easy to use.

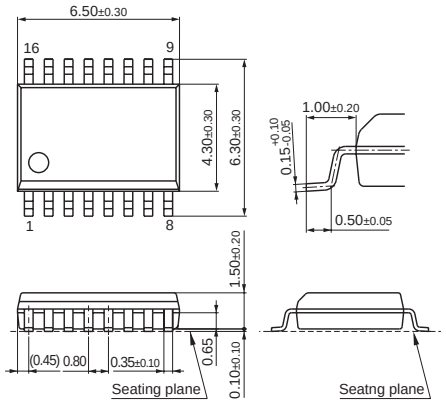
Moreover, the internal settings are incorporated as much as possible, thus cost down can be realized by decreasing the peripheral parts.

AN8021L Unit: mm



SIP009-P-0000D

AN8021SB Unit: mm



SSOP016-P-0225B

■ Features

- It operates at a control frequency up to 700 kHz, realizing the output rise time of 35 ns and the output fall time of 25 ns.
- Pre-start operating current is as small as 70 µA (typical) so that it is possible to use a miniaturized start resistor.
- Output block employs totem pole method.
  The absolute maximum rating of ±1.0 A (peak) allows the direct drive of power MOSFET.
- Built-in pulse-by-pulse overcurrent protection circuit
- Built-in protection circuit against malfunction at low voltage (on/off: 14.2 V/9.2 V)
- Equipped with timer latch function and overvoltage protection circuit.
- Two kinds of packages: 9-pin SIP, 16-pin SOP

■ Applications

- Various power supply equipment

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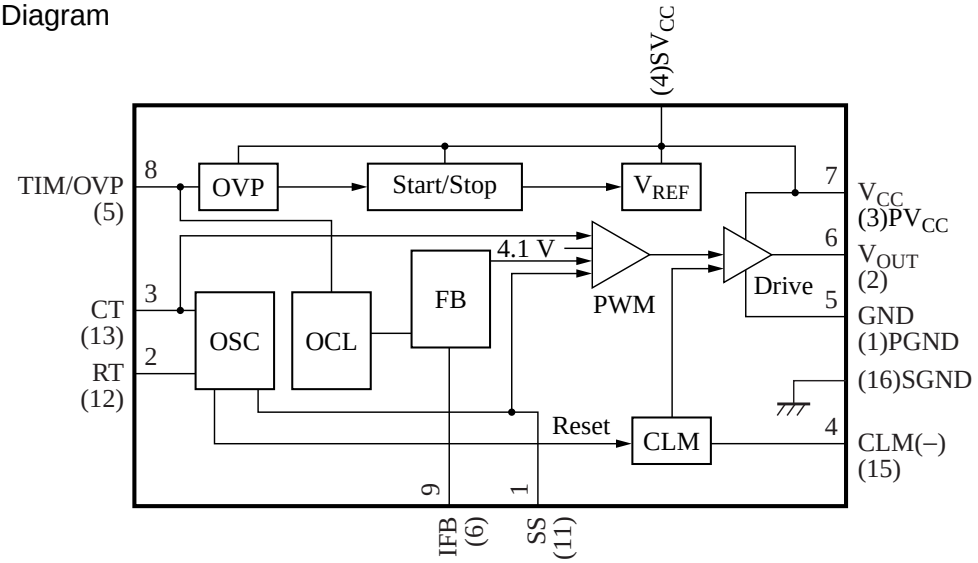
■ Block Diagram



Note) The number in ( ) shows the pin number for the AN8021SB.

■ Pin Descriptions

• AN8021L

Pin No.	Symbol	Description
1	SS	Soft start pin
2	RT	Resistor connection pin that determines charge and discharge current of triangular wave
3	CT	Triangular wave generating capacitor connection pin
4	CLM(–)	Pulse-by-pulse overcurrent protection input pin
5	GND	Grounding pin
6	V_{OUT}	Power MOSFET direct drive pin
7	V_{CC}	Power supply voltage pin
8	TIM/OVP	Pin for overvoltage protection and timer latch (joint use)
9	IFB	Current feedback signal input pin from power-supply-output photocoupler

• AN8021SB

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	PGND	Grounding pin	10	N.C.	N.C.
2	V_{OUT}	Power MOSFET direct drive pin	11	SS	Soft start pin
3	PV_{CC}	Power supply voltage pin	12	RT	Charge and discharge current of triangular wave determining resistance connection pin
4	SV_{CC}	Power supply voltage pin			
5	TIM/OVP	Pin for overvoltage protection and timer latch combined use	13	CT	Triangular wave generating capacitor connection pin
6	IFB	Power supply output photocoupler current feedback signal input pin	14	N.C.	N.C.
7	N.C.	N.C.	15	CLM(–)	Pulse-by-pulse overcurrent protection input pin
8	N.C.	N.C.			
9	N.C.	N.C.	16	SGND	Grounding pin

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■ Absolute Maximum Ratings

Parameter		Symbol	Rating	Unit
Supply voltage		V_{CC}	35	V
OVP terminal allowable application voltage		V_{OVP}	V_{CC}	V
CLM terminal allowable application voltage		V_{CLM}	− 0.3 to +7.0	V
SS terminal allowable application voltage		V_{SS}	− 0.3 to +7.0	V
Constant output current		I_O	±150	mA
Peak output current		I_{OP}	±1 000	mA
IFB terminal allowable application voltage		I_{FB}	−5	mA
Power dissipation	AN8021L	P_D	658	mW
	AN8021SB		340	
Operating ambient temperature *		T_{opr}	−30 to +85	°C
Storage temperature *		T_{stg}	−55 to +150	°C

Note) ∗: Expect for the operating ambient temperature and storage temperature, all ratings are for T_a = 25°C.

■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Timing resistor R_T	R_7	15 to 20	kΩ

■ Electrical Characteristics at T_a = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Start voltage	$V_{CC-START}$		13.0	14.2	15.4	V
Stop voltage	$V_{CC-STOP}$		8.5	9.2	9.9	V
Standby bias current	I_{CC-STB}	V_{CC} = 12 V	50	70	105	µA
Operating bias current	I_{CC-OPR}	V_{CC} = 34 V	6.4	8.0	9.6	mA
OVP operating bias current 1	$I_{CC-OVP1}$	V_{CC} = 20 V	2.4	3.0	3.6	mA
OVP operating bias current 2	$I_{CC-OVP2}$	V_{CC} = 10 V	0.44	0.55	0.66	mA
OVP operating threshold voltage	V_{TH-OVP}	V_{CC} = 18 V	5.4	6.0	6.6	V
OVP release supply voltage	$V_{CC-OVPC}$		7.6	8.4	9.2	V
Timer latch charge current	I_{CH-TIM}	V_{CC} = 18 V, R_T = 19 kΩ	−20	−30	−40	µA
Timer latch start feedback current	I_{FB-TIM}	V_{CC} = 18 V	− 0.37	− 0.5	− 0.63	mA
Soft-start charge current	I_{CH-SS}	V_{CC} = 18 V, R_T = 19 kΩ	−20	−30	−40	µA
Overcurrent protection threshold voltage 1	$V_{TH-CLM1}$	V_{CC} = 18 V	−180	−200	−220	mV
Pre-start low-level output voltage	V_{OL-STB}	V_{CC} = 12 V, I_O = 10 mA	—	0.8	1.8	V
Low-level output voltage	V_{OL}	V_{CC} = 18 V, I_O = 100 mA	—	1.3	1.8	V
High-level output voltage	V_{OH}	V_{CC} = 18 V, I_O = −100 mA	15.0	16.5	—	V
Oscillation frequency 1	f_{OSC1}	V_{CC} = 18 V	175	200	225	kHz
Maximum duty 1	Du_{max1}	V_{CC} = 18 V	62	66	70	%
Feedback current at 0% duty	$I_{FB-Du_{min}}$	V_{CC} = 18 V	−1.1	−1.5	−1.9	mA
Feedback current at maximum duty	$I_{FB-Du_{max}}$	V_{CC} = 18 V	− 0.37	− 0.5	− 0.63	mA

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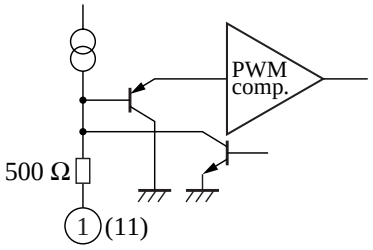
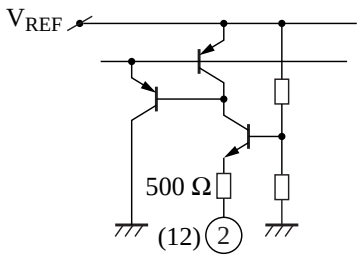
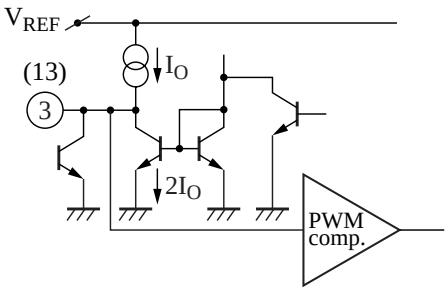
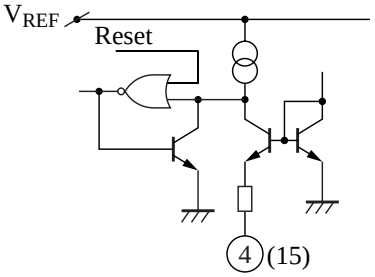
■ Electrical Characteristics at T_a = 25°C (continued)

• Design reference data

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Oscillation frequency 2	f_{OSC2}	T_a = −30°C to +85°C	160	—	240	kHz
Overcurrent protection delay time	$t_{Dry-CLM}$	V_{CC} = 18 V under no load	—	200	—	ns
Output voltage rise time	t_r	V_{CC} = 18 V under no load	—	35	—	ns
Output voltage fall time	t_f	V_{CC} = 18 V under no load	—	25	—	ns

■ Terminal Equivalent Circuits

Pin No.	Equivalent circuit	Description	I/O
1 (11)		SS: Soft start terminal. When V_{CC} is applied, the capacitor connected to this pin is charged, and the output duty is decreased by inputting the capacitor voltage to the PWM.	—
2 (12)		RT: The terminal for connecting a resistor to determine the charge and discharge current of the triangular wave.	—
3 (13)		CT: The terminal for connecting a capacitor to generate the triangular wave.	—
4 (15)		CLM(−): The input terminal for pulse-by-pulse overcurrent protection. It is usually required to attach an external filter.	I
5 (1)(16)	—	GND, (PGND), (SGND): Grounding terminal.	—

Note) The number in ( ) shows the pin number for the AN8021SB.

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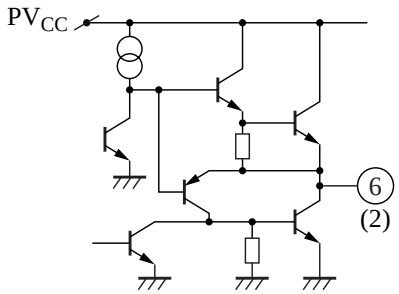
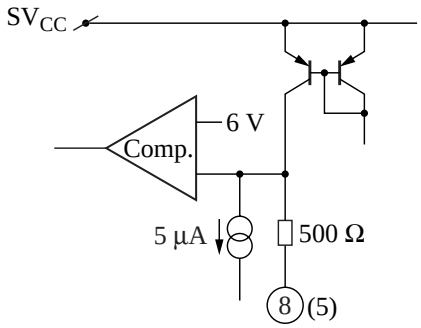
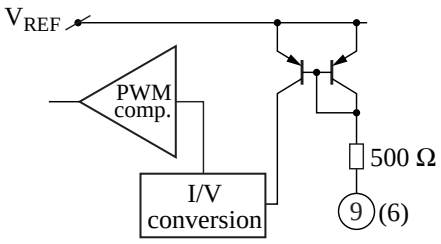
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I/O
6 (2)		V_{OUT}: The terminal for directly driving a power MOSFET.	O
7 (3)(4)	—	V_{CC} , (PV_{CC}), (SV_{CC}): Supply voltage terminal. It monitors the supply voltage and has operating threshold value for start/stop/OVP reset.	—
8 (5)		TIM/OVP: The terminal with double functions such as OVP (overcurrent protection) and timer latch terminal. [OVP] When it receives the overvoltage signal of the power supply output and high is input to the terminal, internal circuit is turned off. At the same time, this condition (latch) is hold. To reset the OVP latch, it is necessary to reduce V_{CC} under the release voltage. [Timer latch] The output voltage drop due to the overcurrent condition of power supply output is detected through the current level for IFB-input. When I_{IFB} becomes less than current of a certain value, charge current flows into the capacitor connected to this terminal. When the capacitor is charged to the threshold voltage of OVP, OVP starts to operate and the IC stays stop.	I
9 (6)		IFB : The terminal into which the current feedback signal is input from the photocoupler of the power supply output.	I

Note) The number in ( ) shows the pin number for the AN8021SB.

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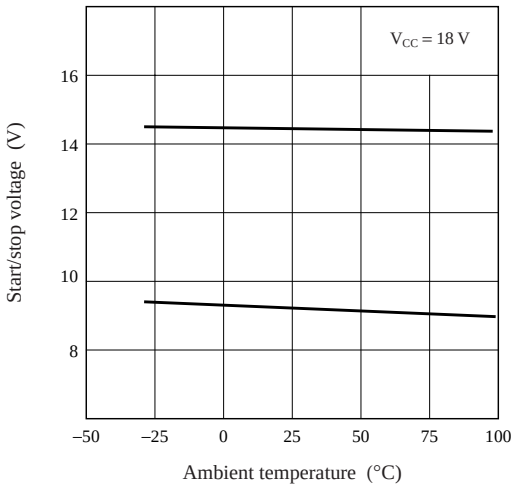
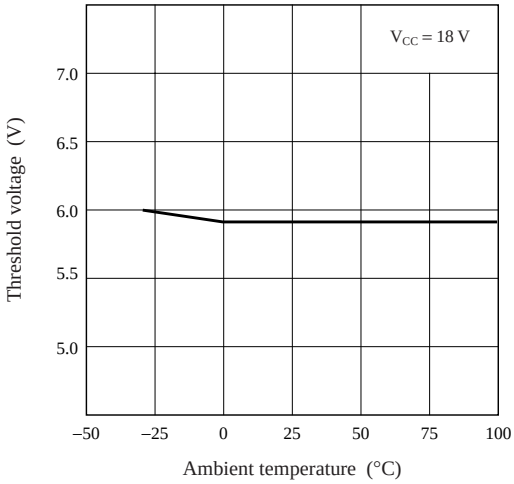
■ Application Notes

[1] Main characteristics [Load: C_L = 3 300 pF, R_L = 20 Ω]

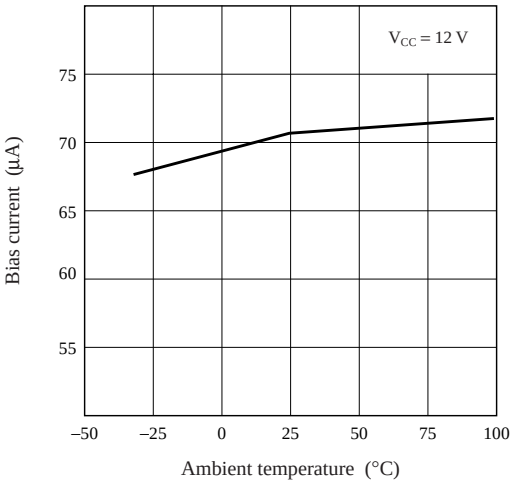
Start/stop voltage characteristics



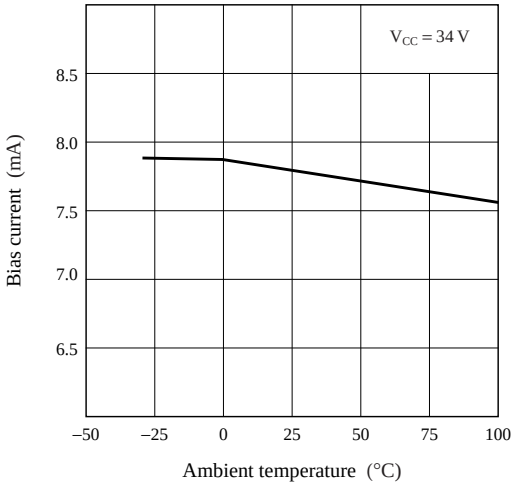
OVP operation threshold voltage characteristics



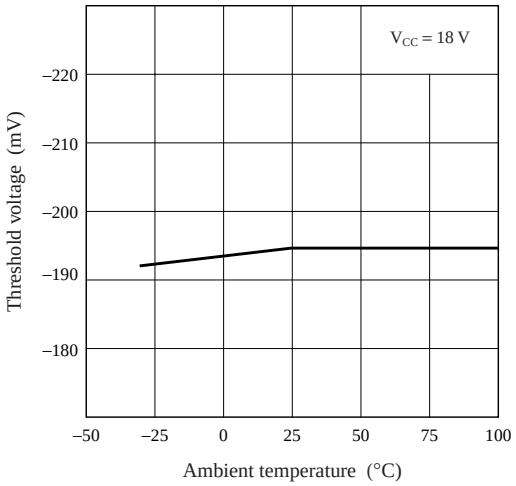
Standby bias current characteristics



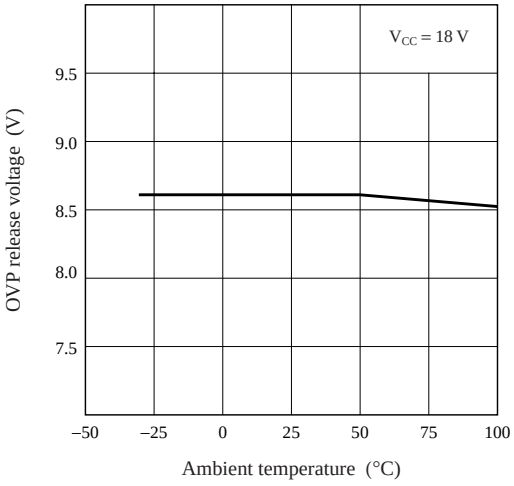
Operating bias current characteristics



Overcurrent protection threshold voltage characteristics



OVP release voltage characteristics



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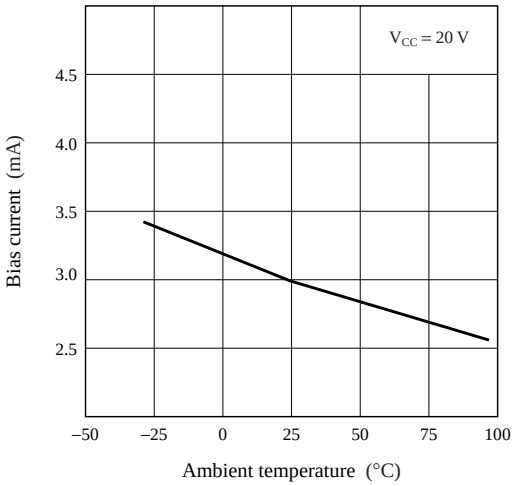
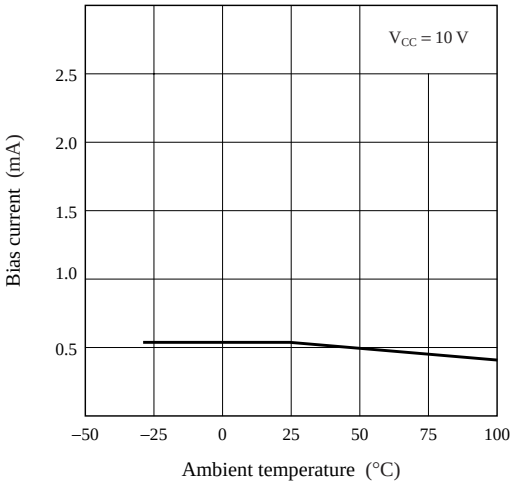
■ Application Notes (continued)

[1] Main characteristics [Load: C_L = 3 300 pF, R_L = 20 Ω] (continued)

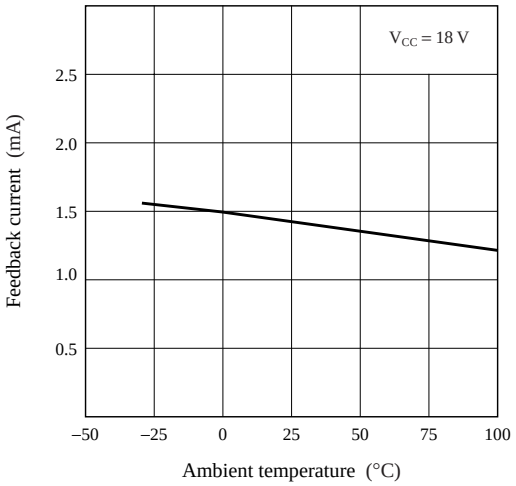
OVP operating bias current characteristics 1



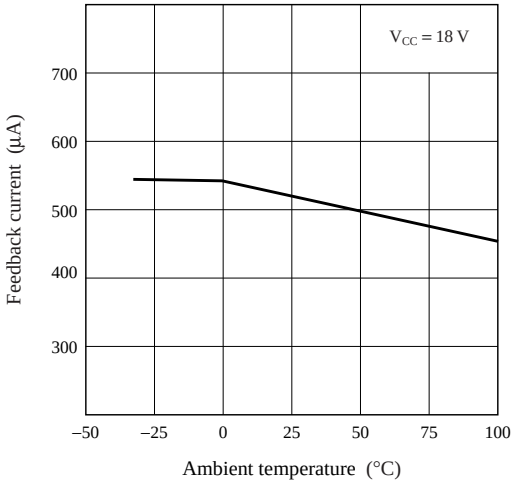
OVP operating bias current characteristics 2



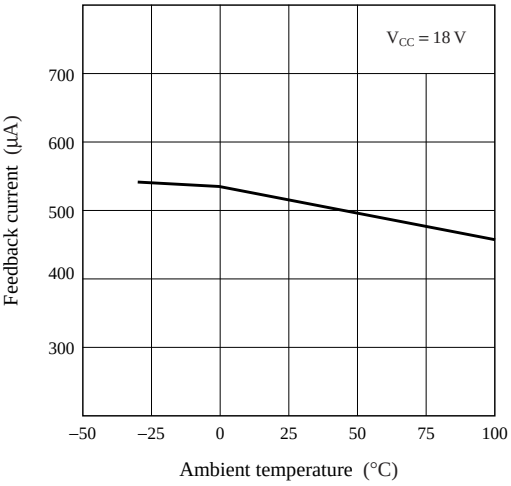
Feedback current at 0% duty characteristics



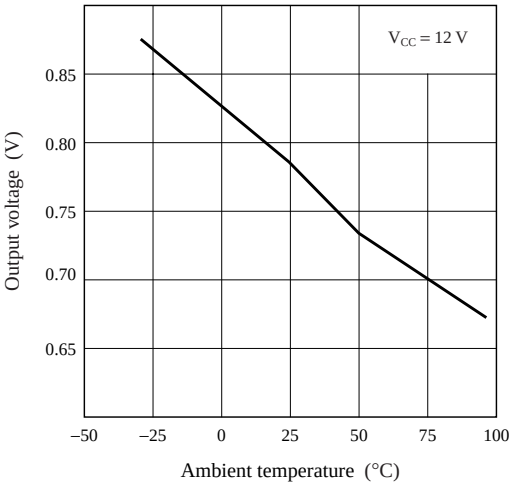
Feedback current at maximum duty characteristics



Timer latch feedback current characteristics



Pre-start low-level output voltage characteristics



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■ Application Notes (continued)

[2] Operation descriptions

1. Start/stop circuit block

- Start mechanism

When AC voltage is applied and the supply voltage reaches the start voltage through the current from the start resistor, the IC starts operation. Then the power MOSFET driving starts. Thereby, bias is generated in the transformer and the supply voltage is given from the bias coil to the IC. (This is point a in figure 1.)

During the period from the time when the start voltage is reached and the voltage is generated in the bias coil to the time when the IC is provided with a sufficient supply voltage, the supply voltage of the IC is supplied by the capacitor (C1) connected to V_{CC} .

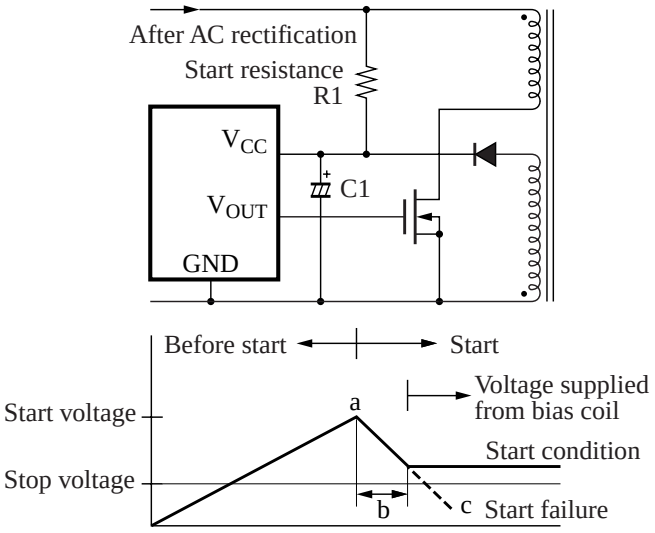

Figure 1

Since the supply voltage continuously decreases during the above period (area b in figure 1), the power supply is not able to start (state c in figure 1), if the stop voltage of the IC is reached before the sufficient supply voltage is supplied from the bias coil.

- Function

The start/stop circuit block is provided with the function to monitor the V_{CC} voltage, and to start the operation of IC when V_{CC} voltage reaches the start voltage (14.2 V typical), and to stop when it decreases under the stop voltage (9.2 V typical). A large voltage difference is set between start and stop (5.0 V typical), so that it is easier to select the start resistor and the capacitor to be connected to V_{CC} .

Note) To start up the IC operation, the startup current which is a pre-start current plus a circuit drive current is necessary. Set the resistance value so as to supply a startup current of 450 µA.

2. Oscillation circuit

The PWM is an abbreviation of pulse width modulation. In this IC, the smaller voltage between the voltage level which is converted from the current input to IFB terminal and dead-time control level which is fixed internally is compared with the internal triangular oscillation level through PWM comparator, and optimal duty is determined, and then it is output via output driving stage.

- Triangular wave oscillation

The triangular waveform oscillation is performed through constant current charge/constant current discharge to/from the external capacitor connected to the CT. The ratio of the charge current to the discharge current is set inside, and the current value is determined by the external resistor connected to the RT terminal.

The RT terminal voltage is determined by the level which is a resistor-divided voltage of the internal reference voltage (which is determined by Zener diode and V_{BE} of NPN transistor, and temperature-compensated). For this reason, the effect of fluctuation with temperature and dispersion is small. By the use of a temperature-compensated external resistor, the effect of the fluctuation with temperature and dispersion on the charge and discharge current value will be reduced further.

Moreover, since the upper/lower voltage level of the triangular wave oscillation is given by the resistor-division of internal reference voltage, the effect of fluctuation with temperature and dispersion has been suppressed.

As described above, the sufficient consideration has been given to the effect of fluctuation with temperature and dispersion in the design of the triangular wave oscillation frequency.

(Reference calculation of oscillation frequency)

$$f_{OSC} = \frac{5}{6 \times C_T \times R_T} \quad [Hz]$$

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■ Application Notes (continued)

[2] Operation descriptions (continued)

3. Overvoltage protection circuit (OVP)

OVP is an abbreviation of Over Voltage Protection. It refers to a self-diagnosis function, which stops the power supply to protect the load when the power supply output generates abnormal voltage higher than the normal output voltage due to failure of the control system or an abnormal voltage applied from the outside (figure 2 and figure 3).

Basically, it is set to monitor the voltage of supply voltage V_{CC} terminal of the IC. Normally, the V_{CC} voltage is supplied from the transformer drive coil. Since this voltage is proportional to the secondary side output voltage, it still operates even when the secondary side output has overvoltage.

1) When the voltage input to the OVP terminal exceeds the threshold voltage (6.0 V typical) as the result of power supply output abnormality, the protective circuit shuts down the internal reference voltage of the IC to stop all of the controls and keeps this stop condition.

2) The OVP is released (reset) under the following conditions:

- Decreasing the supply voltage (V_{CC} < 8.4 V typical: OVP release supply voltage)

The discharge circuit is incorporated so that the electric charge which is charged in the capacitor connected to the OVP terminal can be discharged with the constant current of 5 µA (typical) for the next re-start.

$$V_{th(OUT)} = \frac{\text{Secondary side output voltage under normal operation } V_{OUT}}{V_{CC} \text{ terminal voltage under normal operation}} \times V_7$$

$$V_7 = V_{th(OVP)} + V_Z$$

$V_{th(OUT)}$: Secondary side output overvoltage threshold
$V_{th(OVP)}$: OVP operation threshold
V_Z : Zener voltage (external parts of OVP terminal)

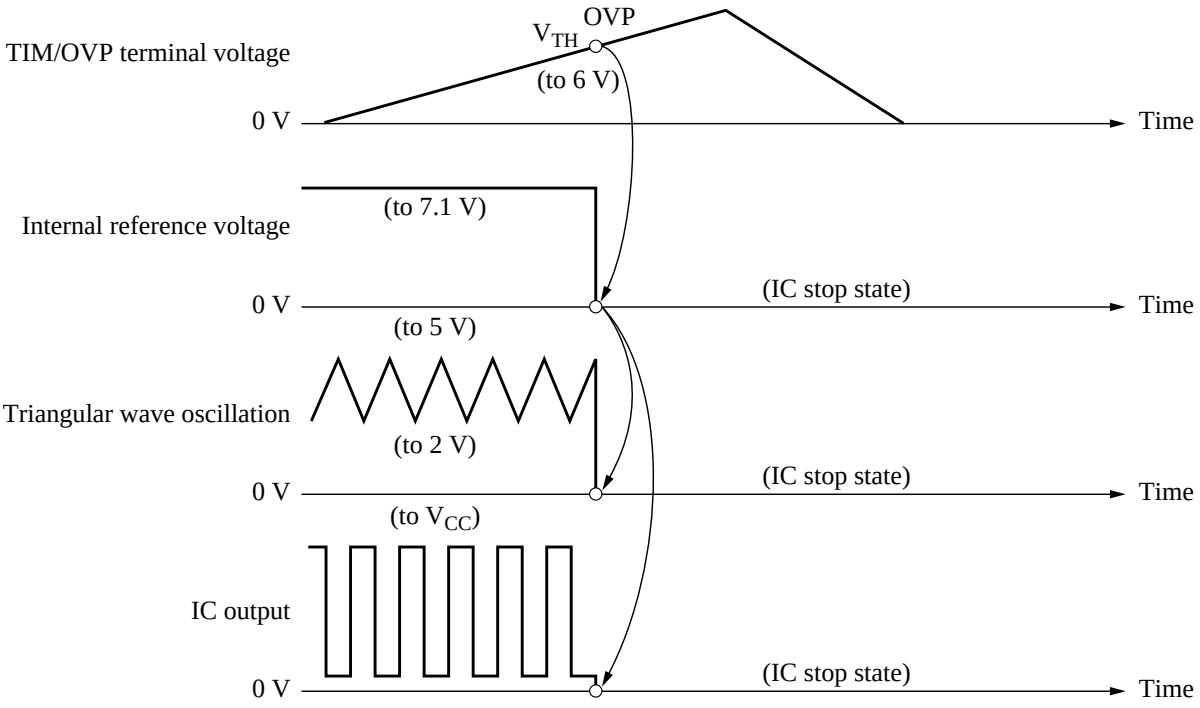

Figure 2. Explanation of OVP operation

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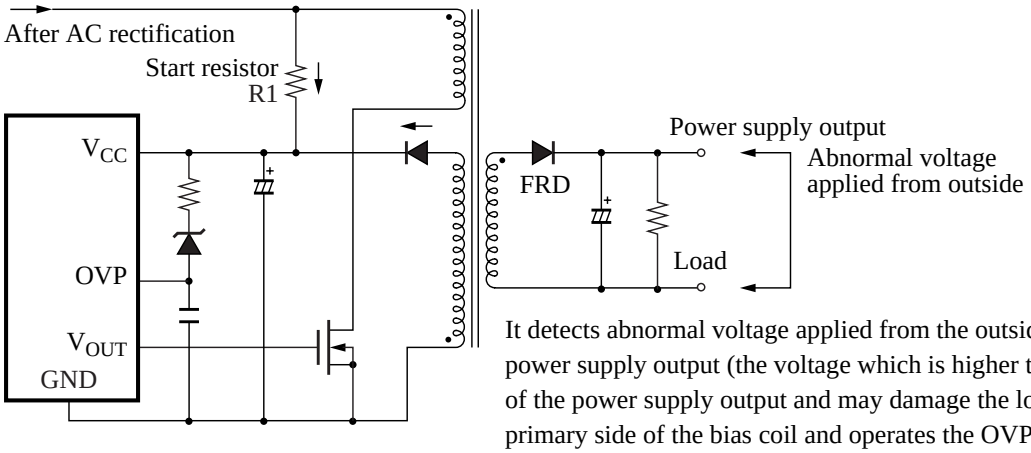
■ Application Notes (continued)

[2] Operation descriptions (continued)

3. Overvoltage protection circuit (OVP) (continued)



It detects abnormal voltage applied from the outside to the power supply output (the voltage which is higher than voltage of the power supply output and may damage the load) by the primary side of the bias coil and operates the OVP.

Figure 3

• Operating supply current characteristics

While the OVP is operating, the decrease of the supply current causes the rise of the supply voltage V_{CC} , and in the worst case, the guaranteed breakdown voltage of the IC (35 V) can be exceeded. In order to prevent the rise of supply voltage, the IC is provided with such characteristics as the supply current rises in the constant resistance mode. This characteristics ensure that the OVP can not be released unless the AC input is cut, if the supply voltage V_{CC} under OVP operation is stabilized over the OVP release supply voltage (which depends on start resistor selection). (Refer to figure 4.)

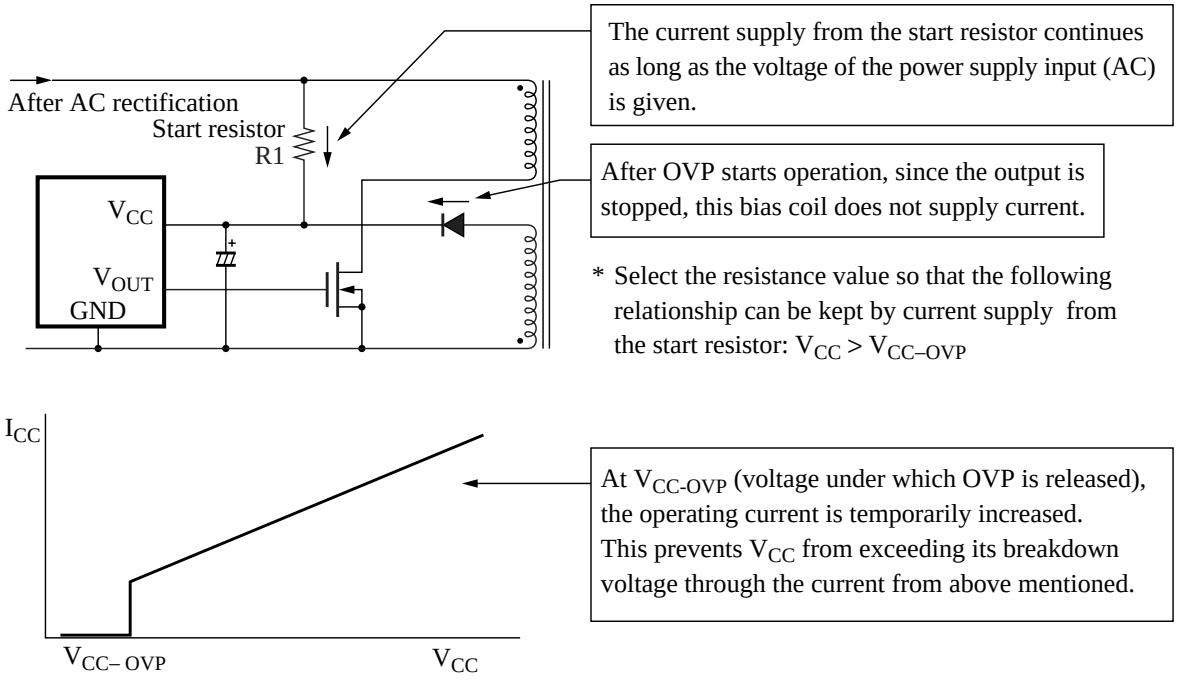


Figure 4

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■ Application Notes (continued)

[2] Operation descriptions (continued)

4. Overcurrent protection circuit (OVP)

The overcurrent of the power supply output is proportional to the value of current flowing in the main switch in the primary side (power MOSFET). Taking advantage of the above fact, by regulating the upper limit of the pulse current flowing in the main switch, the circuit protects the parts which are easily damaged by the overcurrent.

For the current flowing in the main switch, the current detection is achieved by monitoring the voltage in both ends of the low resistance, which is connected between the source of power MOSFET and the power supply GND. When the power MOSFET is turned on and the threshold voltage of CLM (current limit) is detected, the overcurrent protection circuit controls so that current can not flow further by turning off the output to turn off the power MOSFET. The threshold voltage of CLM is approximately –200 mV (typical) under $T_a = 25°C$ with respect to GND of the IC. This control is repeated for each cycle. Once the overcurrent is detected, the off condition is kept during that cycle, and it can not be turned on until the next cycle. The overcurrent detection method described above is called pulse-by-pulse overcurrent detection. (Refer to figure 6.)

The R4, R5 and C3 in figure 5 construct the filter circuit, which functions to remove the noise generated by the parasitic capacitance which is equivalently formed at turning-on of the power MOSFET.

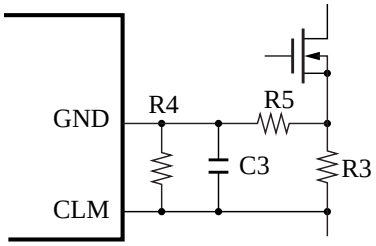

Figure 5

• Notes on the detection level precision

This overcurrent detection level is reflected on the operating current level of the power supply overcurrent protection. Therefore, if this detection level fluctuates with temperature or dispersion, the operating current level of the power supply overcurrent protection also fluctuates. Since such level fluctuation increases the necessity of withstand capability for the parts to be used and in the worst case it means the cause of destruction, the accuracy of detection level is raised as much as possible for these ICs, the AN8021L and AN8021SB.

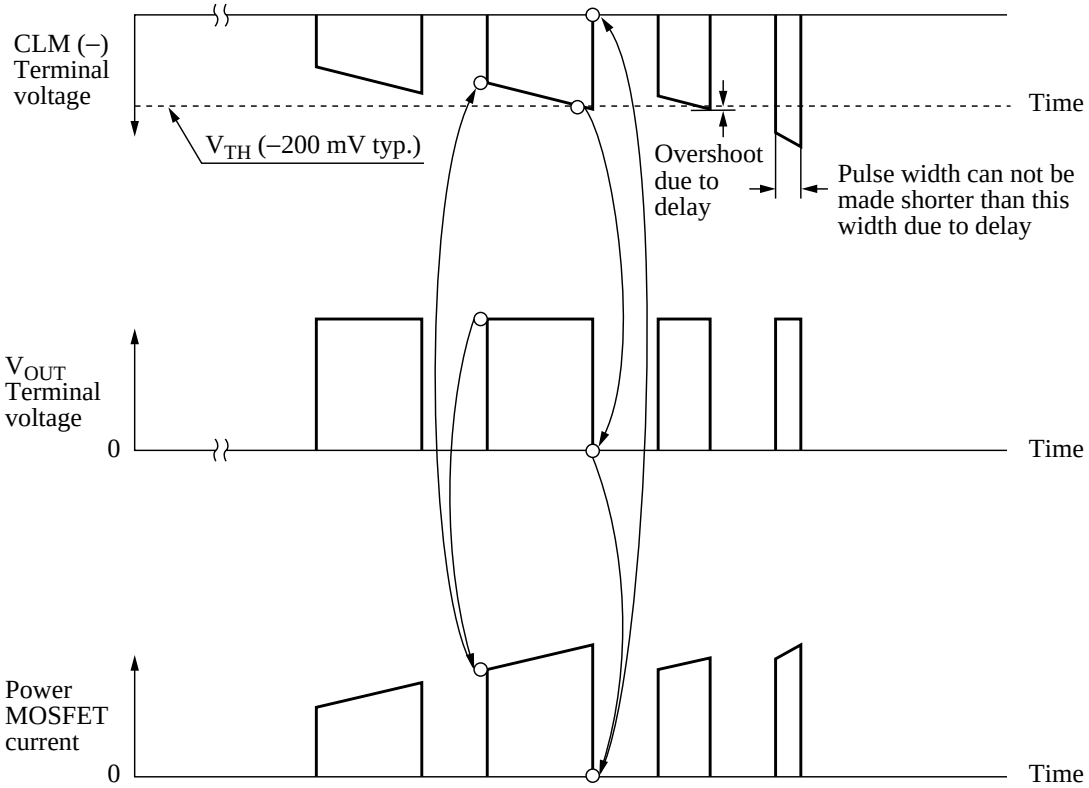

Figure 6. Pulse-by-pulse overcurrent detector operation waveform

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■ Application Notes (continued)

[2] Operation descriptions (continued)

5. Soft start

At start of the power supply, the capacitor connected to the power supply output causes the power supply to rise under overload condition. Under this condition, the power supply output is low. For the normal PWM control, attempt is made to limit the current by the pulse-by-pulse overcurrent protection so that the power supply output can rise at maximum duty. However, pulses can not be made down to zero due to circuit delay. As a result, large current flows in the mains switch (the power MOSFET) or in the diode in the secondary side, and in the worst case these parts are damaged.

For this reason, soft start function in which the power supply output does not rise with maximum duty but rises with gradually widening duty from the minimum one (0%) at the power supply start is adopted.

The use of this function requires more rise time of power supply output. However, it can extend the service life of parts and raise the reliability of the power supply.

The soft start (SS) terminal is connected to the PWM input (hereinafter its voltage is referred to as V_{SS}). In the PWM, three voltages are input; the voltage to which the current feedback level is converted (hereinafter referred to as V_{FB}), the voltage determining the maximum duty (hereinafter referred to as V_{DTC}). This voltage is determined inside the IC), and the triangular wave oscillation voltage (hereinafter referred to as V_{CT}). V_{SS} , V_{FB} and V_{DTC} are input in the non-reverse input (+) of the PWM comparator and V_{CT} is input in the reverse input (–). Among the three signals of the non-reverse input, the lowest one is selected for input to the PWM comparator.

The external capacitor (hereinafter referred to as C_{SS}) is connected to the SS terminal. In the pre-start condition, this capacitor is set to be sufficiently discharged by the transistor inside the IC.

When the supply voltage exceeds the start voltage to start the IC operation, charging is started in the C_{SS} by the constant current source inside the IC. Therefore V_{SS} gradually rises from 0 V.

On the other hand, the V_{FB} has high voltage because the power supply output is low. And, the V_{DTC} is positioned at the medium voltage of the triangular wave oscillation waveform as constant voltage. Therefore, at operation starting, the V_{SS} is input to the PWM comparator as the lowest voltage and is compared with the triangular wave oscillation waveform.

As the result, the output of the IC generates the pulse of duty which gradually becomes large with the rise of V_{SS} from the minimum duty. (Refer to figure 7.)

However, when the V_{SS} exceeds the V_{FB} or V_{DTC} , the duty of the output pulse depends on the V_{FB} or V_{DTC} . The soft start function works only up to that point and after that the normal control comes.

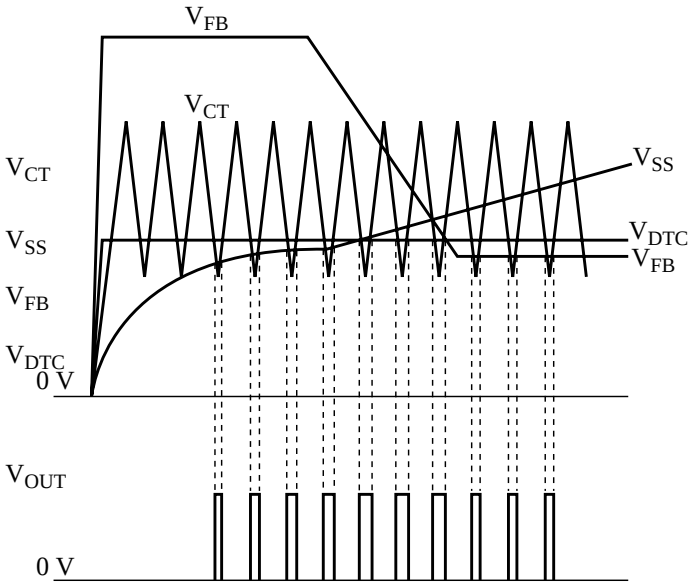

Figure 7. Soft start operation waveform

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■ Application Notes (continued)

[2] Operation descriptions (continued)

6. Timer latch

When the short-circuit or overload of the power supply output continues for a certain period, the pulse-by-pulse overcurrent protection is not sufficient for protection of the transformer, fast recovery diode (FRD), schottky diode in the secondary side and the power MOSFET. For this reason, the timer latch function is employed, which stops the power supply by hitting the OVP, when the overcurrent condition continues for a certain period.

The short-circuit or overload of the power supply output is monitored as the decrease of the power supply output (at this time the pulse-by-pulse overcurrent protector is in the operating condition). The decrease of the power supply output is detected as the decrease of current amount from the current feedback terminal of the normal PWM control. When the decrease amount of this current exceeds a certain value, the comparator inside the IC reverses and the constant current flows to the TIM/OVP terminal.

The external capacitor is connected to the TIM/OVP terminal. Electric charges are accumulated in this capacitor to rise the OVP terminal voltage. When the OVP operating threshold voltage (6 V typical) is reached, the OVP starts operation to stop the IC and keeps this stop condition. (Refer to figure 8.)

• Timer period

The period from the time when an error of the power supply output is detected to the time when the OVP starts operation (hereinafter referred to as timer period) should be longer than the rise time of the power supply. Since at operation start the IC is in the same condition as the overload or output short-circuit condition, if the timer period is shorter, the power supply works latch and can not start.

Therefore, the IC is designed so that the timer period can be set to any desired value with capacitance value of the external capacitor connected to the TIM/OVP terminal. However, particular care should be taken, because too large value of this capacitance may cause the breakdown of the power supply.

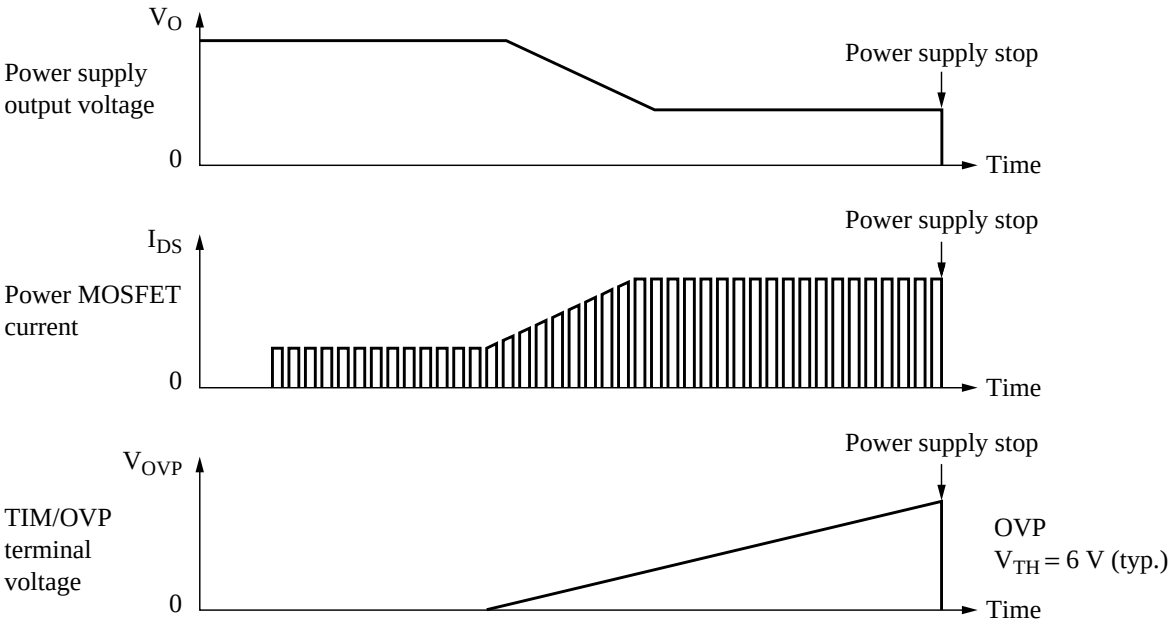

Figure 8. Timer latch basic operation

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■ Application Notes (continued)

[2] Operation descriptions (continued)

7. Output Block

The AN8021L and AN8021SB employ the output circuit using the totem pole (push-pull) method, by which sink/source of current is performed with the NPN transistor as shown in figure 9, in order to drive the power MOSFET at high speed.

The maximum sink/source current is ±0.1 A (DC) and ±1.0 A (peak). Even when the supply voltage V_{CC} is under the stop voltage, the sink function works to ensure that the power MOSFET be turned off.

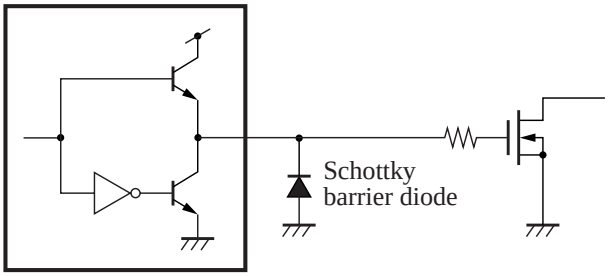


Figure 9

For the current capability, the peak current is major concern, and the particularly large current is not required normally: the power MOSFET which works as load on the output is capacitive load. Therefore, in order to drive it at high speed, the large peak current is required. However, after charge/discharge, particularly large current is not required to keep that condition.

For the AN8021L or AN8021SB, capacitance value of the power MOSFET used is taking into account, and the capability of peak value ±1 A is ensured.

The parasitic LC of the power MOSFET may produce ringing which makes the output pin go under the GND potential. When the decrease of the output pin becomes larger than the voltage drop of diode and its voltage becomes negative, the parasitic diode consisting of the substrate and collector of the output NPN turns on. This phenomenon may cause the malfunction of the device. In such a case, the Schottky barrier diode should be connected between the output and GND.

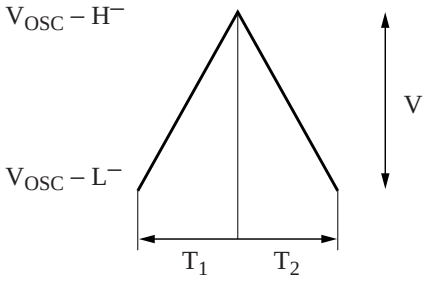
[3] Design reference data

1. Setting the output frequency

The output is controlling the triangular oscillation with PWM control: Triangular oscillation frequency = output frequency

CT (C6) = capacitor terminal for triangular oscillation

RT (C7) = resistor terminal for triangular oscillation



[Reference calculation formula]

$$T_1 = T_2 = \frac{C_6 \cdot V}{2I_{RT}\ (\text{charge/discharge current})}$$

Since the I_{RT} is given by rough calculation of 2.5 V/R_T , and V becomes approximately 3 V, the output frequency is obtained in the following equation:

$$f_{OUT} = \frac{1}{T_1 + T_2} = \frac{I_{RT}}{C_6 \cdot V} = \frac{5}{6 \cdot C_6 \cdot R_7}$$

However, it may deviate a little from the design value due to delay of the internal circuit.

(Reference value)

f_{OUT} = approximately 200 kHz

at C_T (C6) = 220 pF and R_T (R7) = 19 kΩ

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■ Application Notes (continued)

[3] Design reference data (continued)

2. Setting the timer latch period

The timer latch period t, the period from the time when an abnormality of the power supply output is detected to the time when the overvoltage protector is activated, can be set to any desired value by using the external capacitance C_{TIM} (C2) based on the following equation:

TIM/OVP = capacitor terminal for timer latch period setting

[Reference calculation formula]

$$t = \frac{C_2 \cdot V_{TIM}}{I_{TIM}} \text{ [s]}$$

V_{TIM} = 6 V (typ.): Overvoltage protection threshold value
I_{TIM} = timer latch charge current
(Varies depending on R7 value, at R7 = 19 kΩ)
I_{TIM} = 30 µA (typ.)

3. Setting the soft start time

• Soft start charge current

Most of the conventional ICs are charged by using the internal resistor from the internal reference voltage, or by using the constant current source which is determined by the internal resistance. However, the above charging method suffers from problems on dispersion or temperature change and can not ensure the soft start time. For this reason, the AN8021L and AN8021SB use the following method: The soft start charge current is given from the constant current source used in the internal triangular wave oscillation circuit. In addition, the above constant current source is stable with respect to dispersion or fluctuation with temperature because it has the current value which is determined by the external resistor and the terminal voltage given from the resistor-divider of internal reference voltage. However, for this method, particular care should be taken on the application: Since each time the setting of oscillation frequency is changed, the soft start constant should be also changed.

SS (C5) = capacitor terminal for soft start

[Reference calculation formula]

$$t = \frac{C_5 \cdot V_{SS}}{I_{SS}} \text{ [s]}$$

I_{SS} = soft start charging current
(Varies depending on R7 value, at R_T (R7) = 19 kΩ)
I_{SS} = 30 µA (typ.)
V_{SS} = 2.0 V, at duty = 0%
V_{SS} = 4.1 V, at maximum duty

4. Start circuit

The start time from the power-on to the actual start can be set by using the values of R1 and C1. Too long start time makes the power supply to rise slowly.

[Setting the start resistor R1]

1) When the overload shutting-off condition is kept, the shut-off bias current (OVP operating bias current) of the AN8021L and AN8021SB is 550 µA (typical) at V_{CC} = 10 V. Therefore, set the R1 as shown in the following equation :

$$R_1 < \frac{V_{IN} - 10\text{ V}}{550\ \mu\text{A}}$$

2) When automatic reset is desired after the overload shut-off, the standby current of the AN8021L and AN8021SB is 70 µA (typical) at V_{CC} = 12 V. Therefore, set the R1 as shown in the following equation :

$$\frac{V_{IN} - 10\text{ V}}{550\ \mu\text{A}} < R_1 < \frac{V_{IN} - 12\text{ V}}{70\ \mu\text{A}}$$

[Setting the C1]

When the AN8021L or AN8021SB is started, the operating supply current of 7.5 mA is required at V_{CC} = 18 V.

The current should be supplied with the discharge current of the C1 during the period from the soft start time up to the time when the supply current is supplied from the auxiliary bias coil. Therefore set the C1 as shown in the following equation:

$$\frac{(V_{CC(START)} - V_{CC(STOP)}) \cdot C_1}{7.5\text{ mA}} > \text{Soft start time}$$

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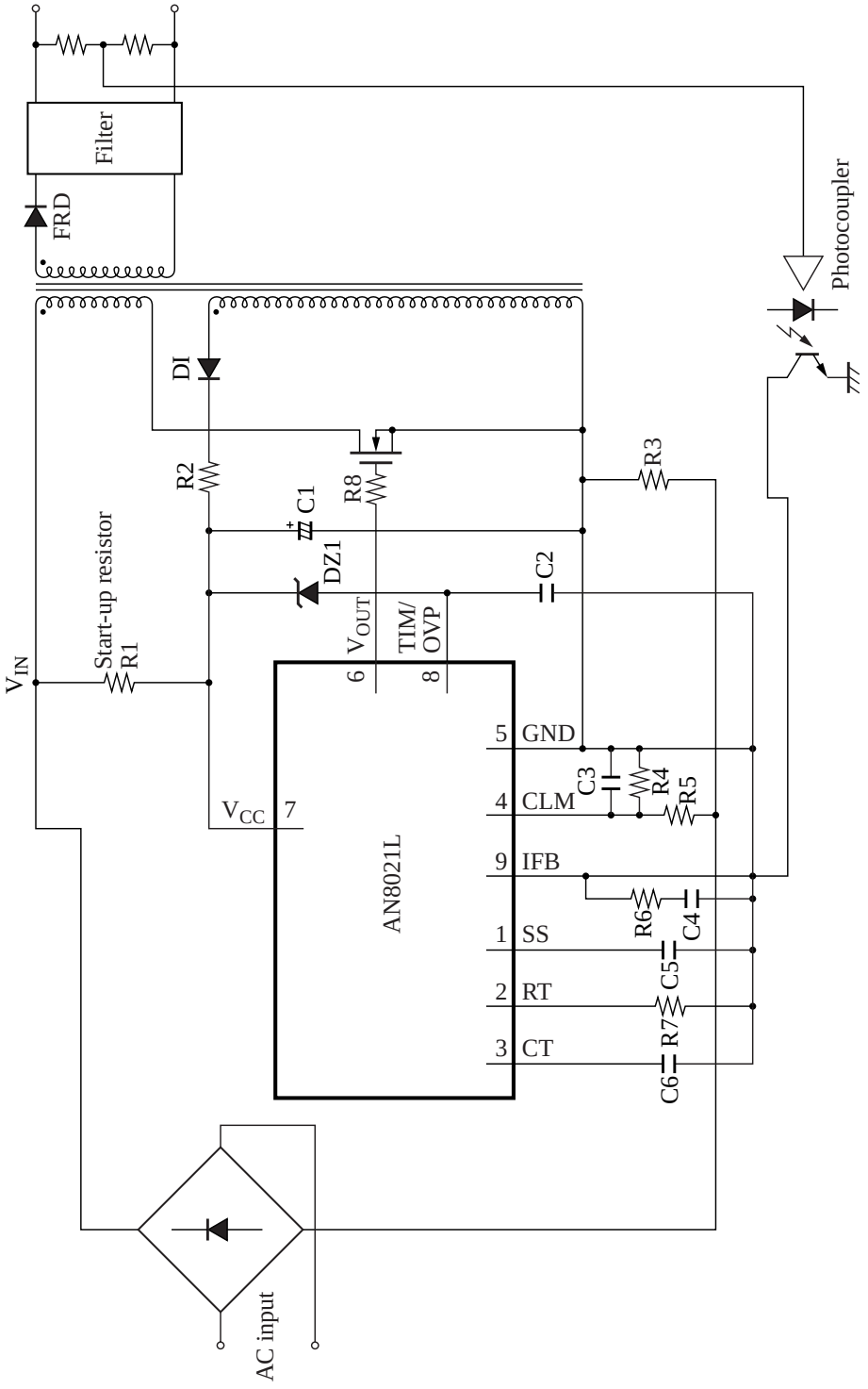
■ Application Circuit Example



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